(V) Preliminary Specifications
( ) Final Specifications

Module	**7”(7”) 1280X800 16:10 Color TFT-LCD with LED Backlight design**
Model Name	B070EW01 V0 (H/W:1A)
Note ( )	***LED Backlight without driving circuit design***

Customer **Date**	**Approved by** **Date**
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Note: This Specification is subject to change without notice.	**NBBU Marketing Division AU Optronics corporation**

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1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
11) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
12) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B070EW01V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 HD, 1,280(H) x800(V) screen without LED backlight driving circuit. All input signals are LVDS interface compatible.

B070EW01 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	177.74			
Active Area	[mm]	150.72 X 94.20			
Pixels H x V		1280x3(RGB) x 800			
Pixel Pitch	[mm]	0.11775x 0.11775			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I_{LED}=22 mA) **(Note: I_{LED} is LED current)**	[cd/m^2]	400 typ. (5 points average)			
Luminance Uniformity		1.25 max (5 points)			
Contrast Ratio		600:1 min / 800:1 (typ)			
Response Time	[ms]	25ms typ			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption **(w/o LED driver)**	[Watt]	2.2 W Max[1] (note1 &2)			
Weight	[Grams]	90g max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	163.90	164.20	164.50
		Width	106.45	106.75	107.05
		Thickness	-	-	5.1
Electrical Interface		1 channel LVDS			

Note[1] Logic Power preliminary estimated value is 0.7W at mosaic pattern & backlight light unit preliminary estimated value power is 1.45W @400nits.

Note2: LED driver on system

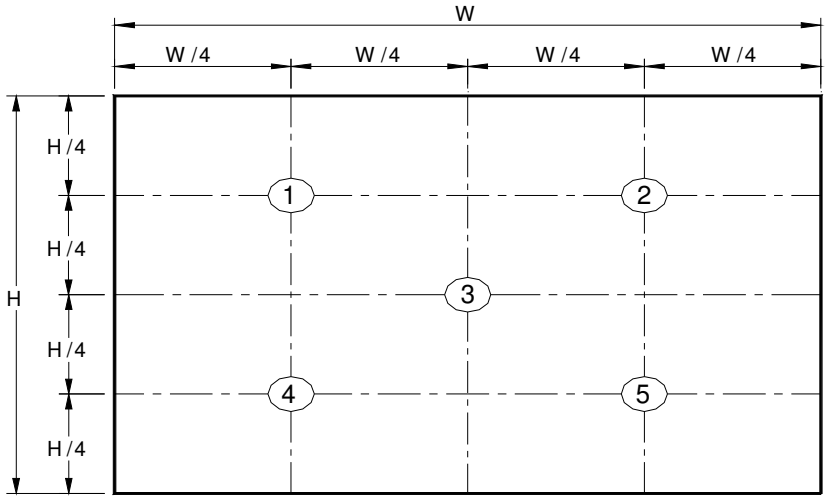
Glass Thickness	[mm]	0.3
Surface Treatment		Glare, Hardness 3H,
Support Color		262K corlors (RGB 6 bits)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

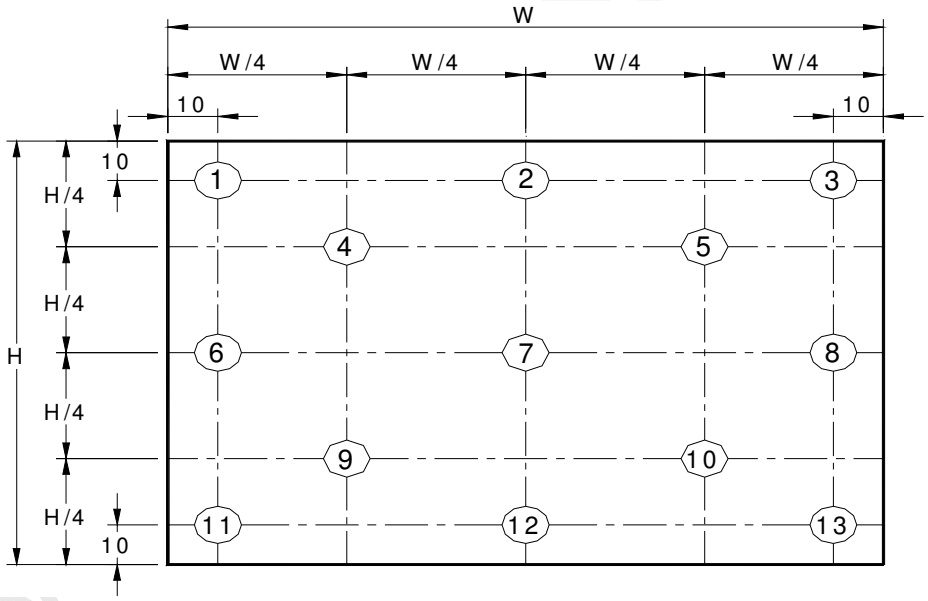
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=22mA			5 points average	340	400	-	cd/m^2	1, 4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	80 80	85 85	- -	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	80 80	85 85	- -		
Luminance Uniformity		δ_{5P}	5 Points			1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points			1.43		2, 3, 4
Contrast Ratio		CR		600	800	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_{RT}	Rising + Falling		25	35	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.562	0.592	0.622		4
		Ry		0.312	0.342	0.372		
	Green	Gx		0.305	0.335	0.365		
		Gy		0.557	0.587	0.617		
	Blue	Bx		0.126	0.156	0.186		
		By		0.088	0.118	0.148		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC (typ)		%		-	50	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

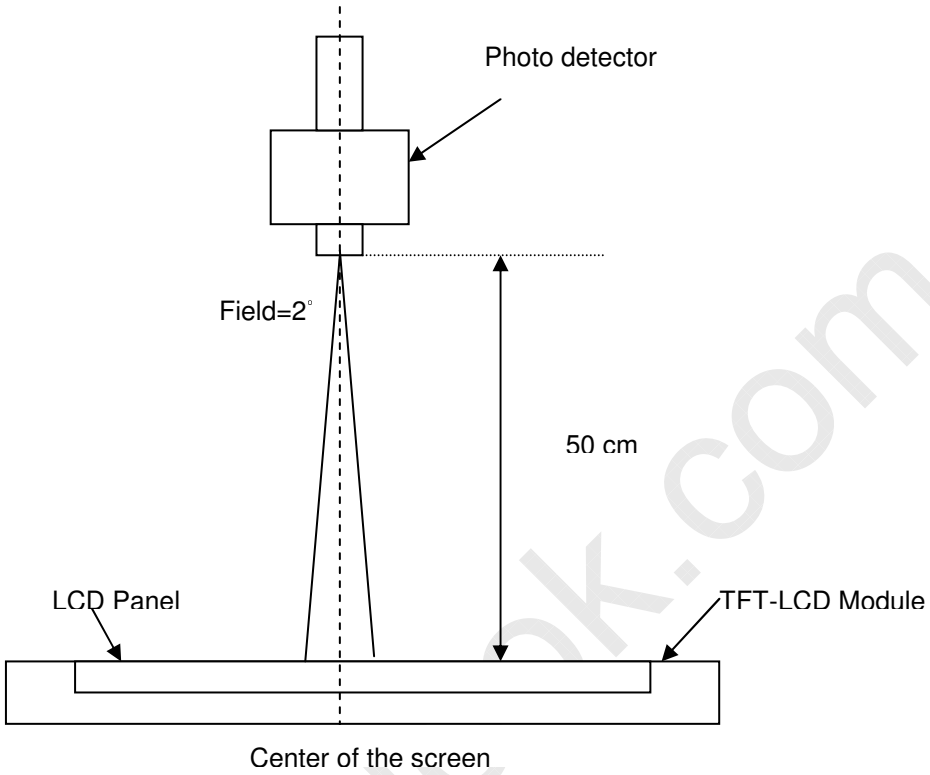
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes

in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

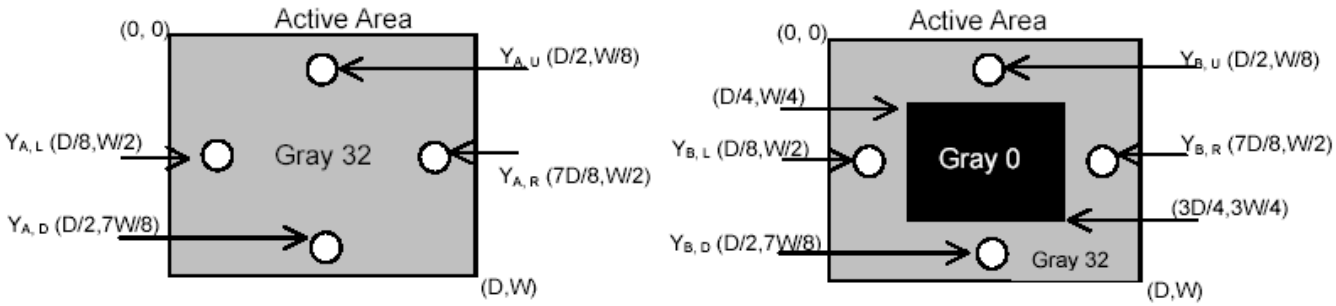
Note 7： Definition of Cross Talk (CT)

$CT = |Y_B - Y_A| / Y_A \times 100\ (\%)$

Where

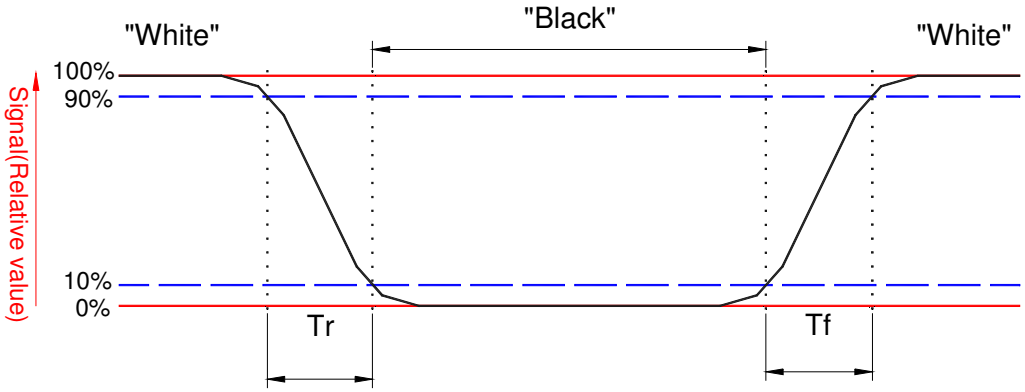
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



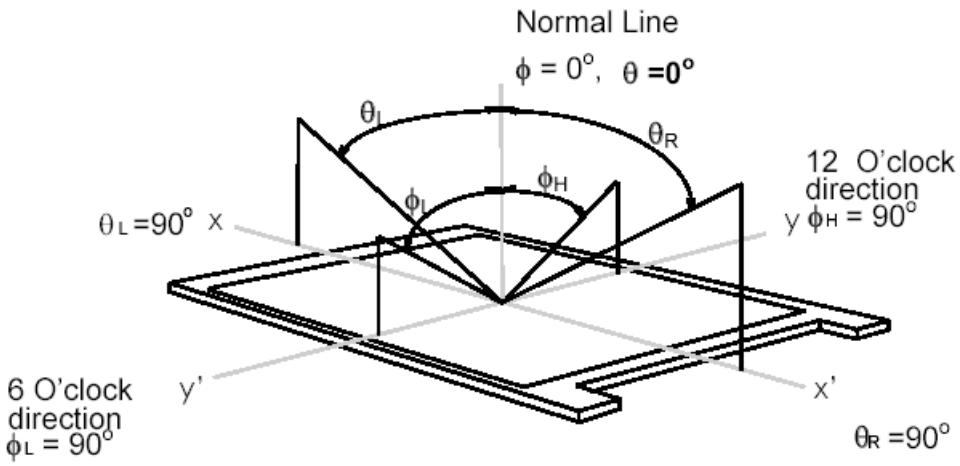
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



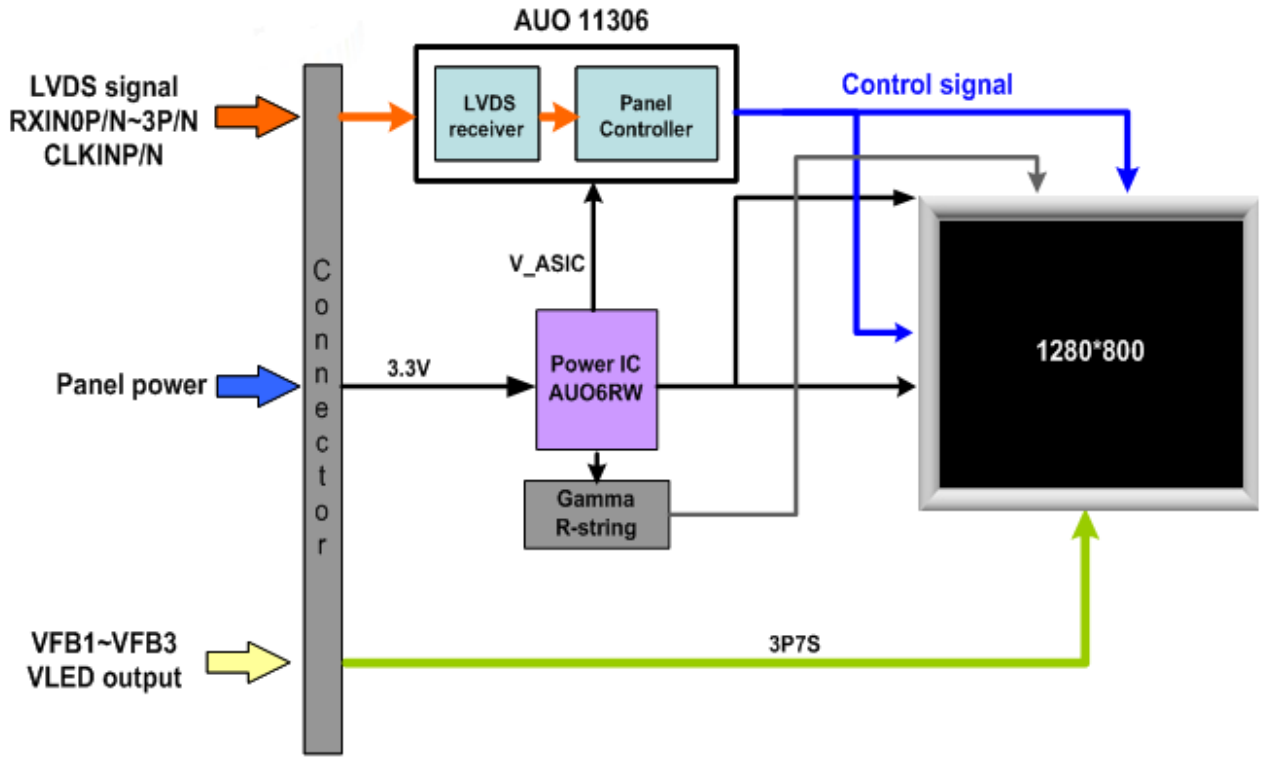
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 7 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Typ	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	3.3	3.6	[Volt]	Note 1,2,3

4.2 Absolute Ratings of Environment

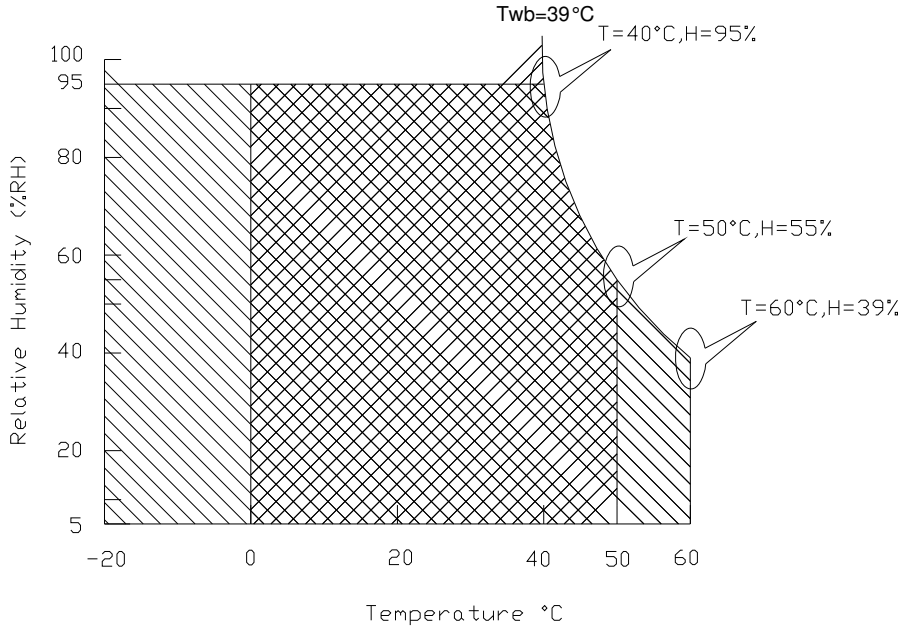
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃) and **mosaic pattern**.

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

The power specifications are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.7	[Watt]	Note 1
IDD	IDD Current	-	-	212	[mA]	Note 1
IRush	Inrush Current	-	-	TBD	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	TBD	[mV] p-p	

Note 1 : Measurement Condition：Mosaic pattern at 3.3V driving voltage. (Pdd=$V_{3.3}$ x $I_{mosaic)}$

Note 2：Measure Condition

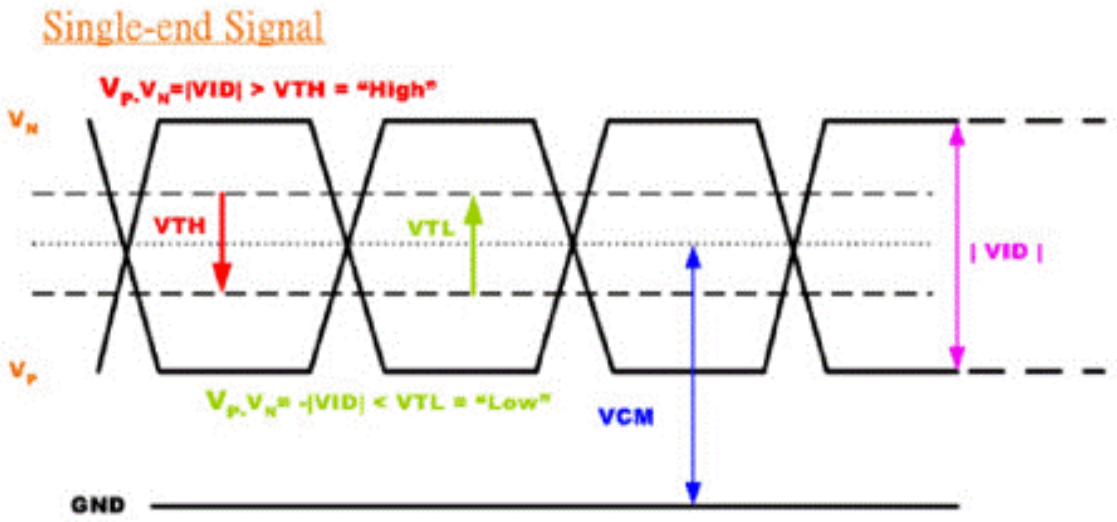
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
V_{tl}	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
V_{ID}	Differential Input Voltage	100	600	[mV]
V_{cm}	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	1.45	[Watt]	(@ 400 nit, Ta=25℃), Vf=3.0 V max Note 1
LED Life-Time	N/A	15000	-	-	Hour	(Ta=25℃), Note 3 I_F=22 mA

Note 1: LED driver on system

Note 2, Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 3: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight output to LCM signal characteristics

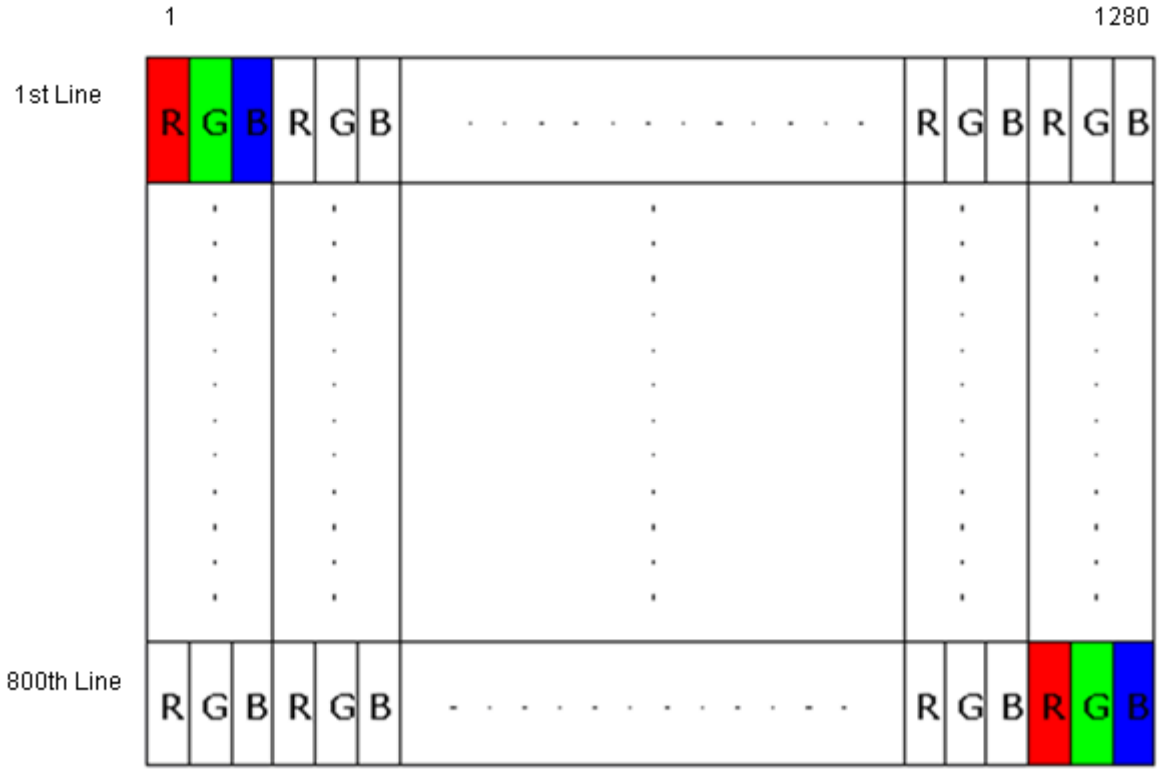
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED Output		20.3V	21 V	[Volt]	Define as Connector Interface (Ta=25℃) Note1
DCR High Level (High Acitve)	DCR_EN		3.3		[Volt]	
DCR Low Level		2.5	-	-	[Volt]	
PWM_SYS to LCM Frequency	PWN_IN	200	-	1k	Hz	
PWM Duty Ratio	Duty	5	--	-	%	

Note1: LED driver on system

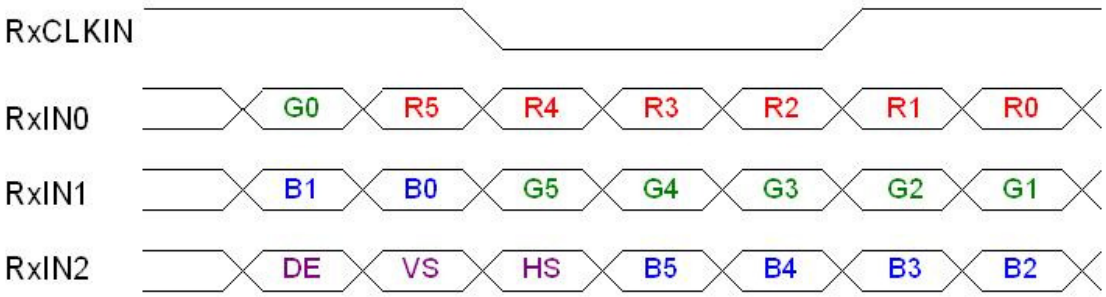
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	STM or compatible
Type / Part Number	STM/MSAK 24025P40
Mating Housing/Part Number	STM/0.5 pitch/40 pin

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN #	Acer Recommend	SIGNAL NAME	DESCRIPTION
1	NC	NC	No connection
2	VDD	VDD	Power Supply +3.3V
3	VDD	VDD	Power Supply +3.3V
4	VDDedid	VDDedid	EDID +3.3V Power
5	NC	NC	AUO Testing
6	CLKedid	CLKedid	EDID Clock Input
7	DATAedid	DATAedid	EDID Data Input
8	RXIN0N	RXIN0N	-LVDS Differential Data INPUT(Odd R0-R5,G0)
9	RXIN0P	RXIN0P	+LVDS Differential Data INPUT(Odd R0-R5,G0)
10	VSS	VSS	Ground
11	RXIN1N	RXIN1N	-LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
12	RXIN1P	RXIN1P	+LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
13	VSS	VSS	Ground
14	RXIN2N	RXIN2N	-LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
15	RXIN2P	RXIN2P	+LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
16	VSS	VSS	Ground
17	CK1INN	CK1INN	-LVDS Differential Clock INPUT
18	CK1INP	CK1INP	+LVDS Differential Clock INPUT

19	GND	GND	Ground
20	NC	NC	
21	NC	NC	
22	GND	GND	Ground
23	NC	NC	No connection
24	NC	NC	No connection
25	GND	GND	Ground
26	NC	NC	No connection
27	NC	NC	No connection
28	NC	NC	No connection
29	NC	NC	No connection
30	NC	NC	No connection
31	VFB1	VFB1	Feedback pin1 (current balance use)
32	VFB2	VFB2	Feedback pin2 (current balance use)
33	VFB3	VFB3	Feedback pin3 (current balance use)
34	NC	NC	No connection
35	NC	NC	No connection
36	NC	NC	No connection
37	Ground (DCR off)	Ground (DCR off)	DCR off
38	VLED Output	VLED Output	LED output voltage
39	VLED Output	VLED Output	LED output voltage
40	VLED Output	VLED Output	LED output voltage

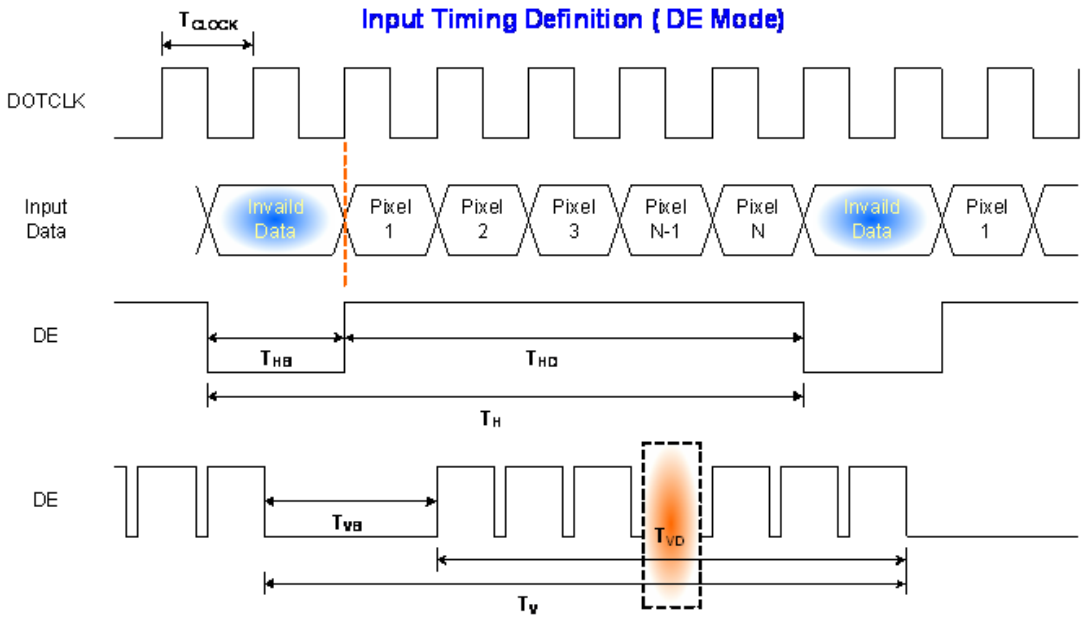
6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

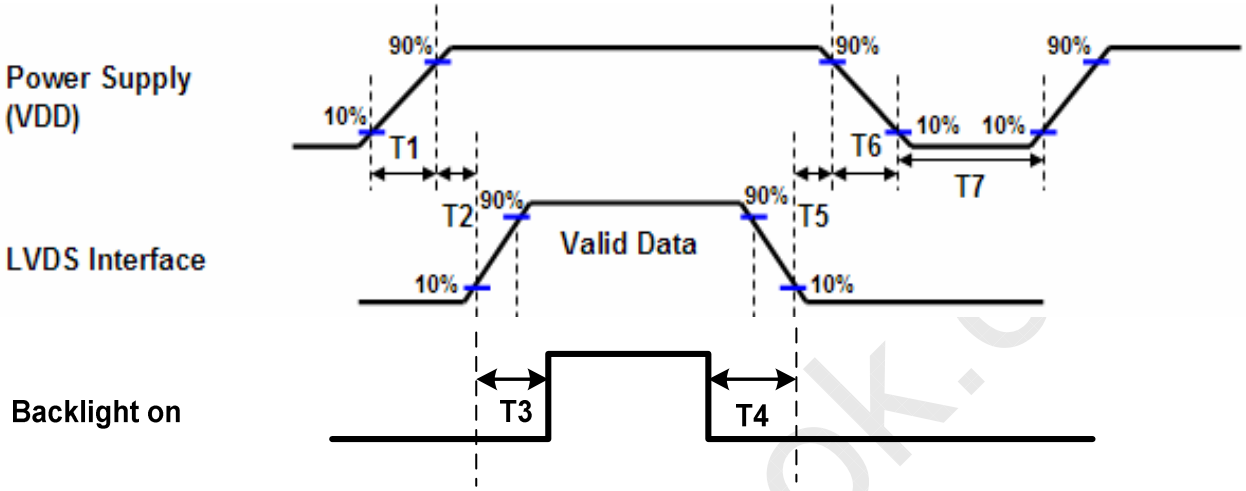
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60		Hz
Clock frequency		1/ T_{Clock}	TBD	69.3	TBD	MHz
Vertical Section	Period	TBD	TBD	814	TBD	T_{Line}
	Active	T_{VD}	800			
	Blanking	T_{VB}	-	14	TBD	
Horizontal Section	Period	T_H	-	1418	TBD	T_{Clock}
	Active	T_{HD}	1280			
	Blanking	T_{HB}	-	138	TBD	

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	0	50	
T3	200	-	
T4	200	-	
T5	0	50	
T6	0	10	
T7	500	-	

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

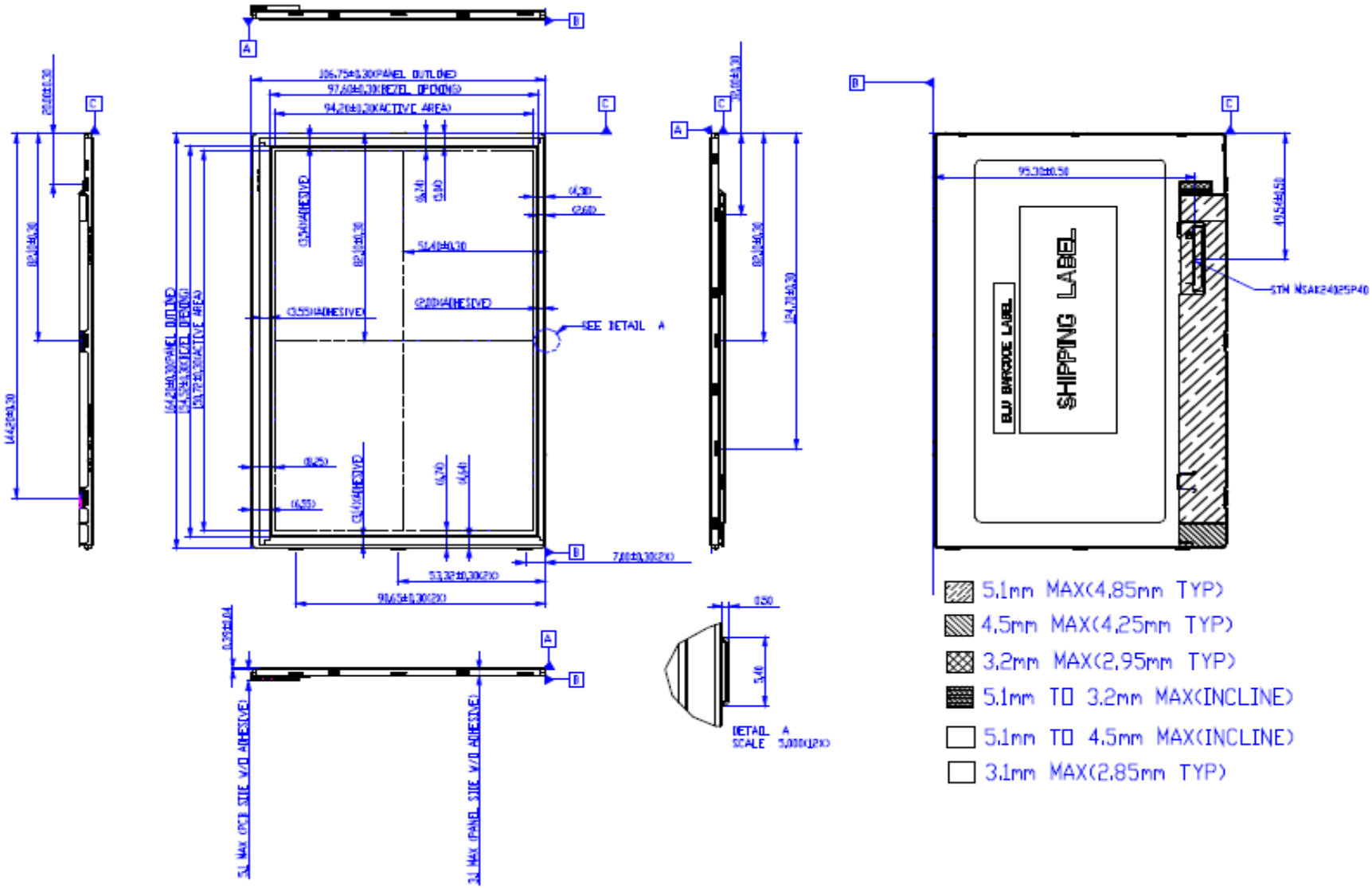
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 300h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

8. Mechanical Characteristics

8.1 LCM Outline Dimension



Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

9. Shipping and Package

9.1 Shipping Label Format

[TBD]

9.2 Carton Package

[TBD]

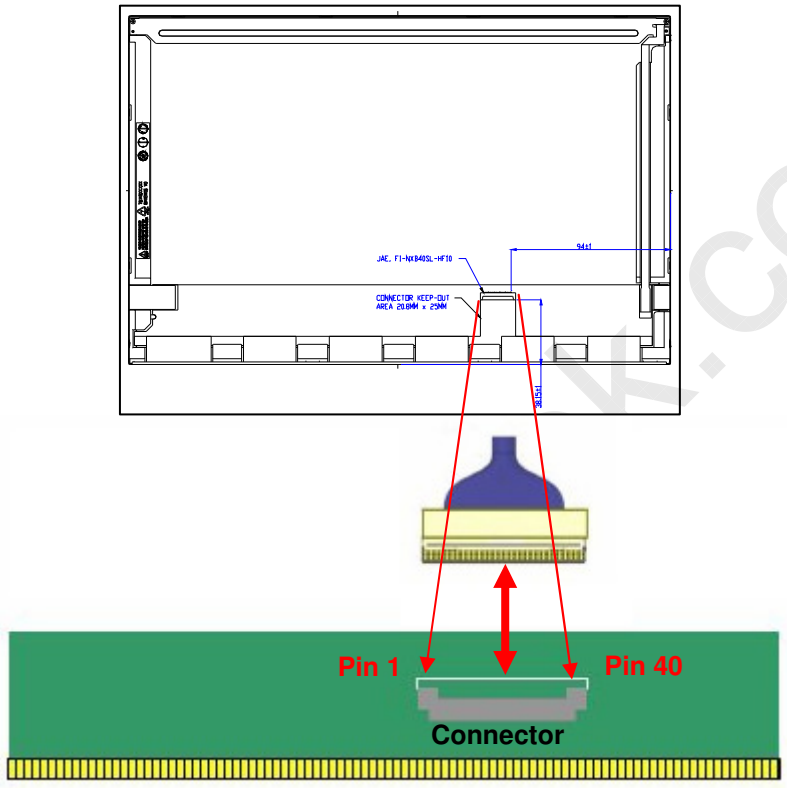
10. Appendix: EDID Description

Address HEX	FUNCTION	Value HEX	Value BIN	Value DEC	Note
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	A4	10100100	164	
0B	hex, LSB first	10	00010000	16	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	24	00100100	36	
11	Year of manufacture	14	00010100	20	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	90	10010000	144	
15	**Max H image size** *(rounded to cm)*	0F	00001111	15	
16	**Max V image size** *(rounded to cm)*	09	00001001	9	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	15	00010101	21	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	85	10000101	133	
1B	Red x **(Upper 8 bits)**	97	10010111	151	
1C	Red y/ highER 8 bits	58	01011000	88	
1D	Green x	53	01010011	83	
1E	Green y	8A	10001010	138	
1F	Blue x	26	00100110	38	
20	Blue y	25	00100101	37	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	

26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	12	00010010	18	
37	Pixel Clock/10000 USB	1B	00011011	27	
38	Horz active **Lower 8bits**	00	00000000	0	
39	Horz blanking **Lower 8bits**	8A	10001010	138	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80	
3B	Vertical Active **Lower 8bits**	20	00100000	32	
3C	Vertical Blanking **Lower 8bits**	0E	00001110	14	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48	
3E	HorzSync. Offset	28	00101000	40	
3F	HorzSync.Width	1C	00011100	28	
40	VertSync.Offset : VertSync.Width	24	00100100	36	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	96	10010110	150	
43	Vertical Image Size **Lower 8bits**	5E	01011110	94	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	00	00000000	0	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	

4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	30	00110000	48	0
73	Manufacture P/N	37	00110111	55	7
74	Manufacture P/N	30	00110000	48	0
75	Manufacture P/N	45	01000101	69	E
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	31	00110001	49	1
79	Manufacture P/N	20	00100000	32	

7A	Manufacture P/N	56	01010110	86	V
7B	Manufacture P/N	30	00110000	48	0
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	20	00100000	32	



Note1: Input signals shall be low or High-impedance state when VDD is off.