Ver 1.3

8-Bit 1GSPS Analog to Digital Converter

Datasheet

Part Number：B08D1000RH

中国航天 CASC
北京微电子技术研究所
Beijing Microelectronics Technology Institute

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2015.9	-	-	
1.1	2016.9	Chapter 5	Modified parameter list	
1.2	2017.9	Appendix	Increased the pin number	
1.3	2018.3	-	Changed the template	

TABLE OF CONTENTS

1. Unique features

- Internal Sample-and-Hold
- Single +1.9V ±0.1V Operation
- Choice of SDR or DDR output clocking
- Interleave Mode for 2X Sampling Rate
- Multiple ADC Synchronization Capability
- Guaranteed No Missing Codes
- Serial Interface for Extended Control
- Fine Adjustment of Input Full-Scale Range and Offset
- Duty Cycle Corrected Sample Clock
- On-chip high speed digital calibration
- Total Ionizing Dose ≥ 100 Krad(Si)
- SEL threshold ≥ 75 MeV cm^2/mg

2. General Description

The B08D1000RH is a radiation hardened, dual, low power, high performance, CMOS analog-to-digital converter that digitizes signals to 8 bits resolution at sampling rates up to 1.2 GSPS. Consuming a typical 1.6 Watts at 1 GSPS from a single 1.9 Volt supply, this device is guaranteed to have no missing codes over the full operating temperature range. The innovative design of the internal sample-and-hold amplifier and the self-calibration scheme enable a very flat response of all dynamic performance. B08D1000RH has Extended Control Mode enable user change the operational parameters for high performance.

3. Block Diagram

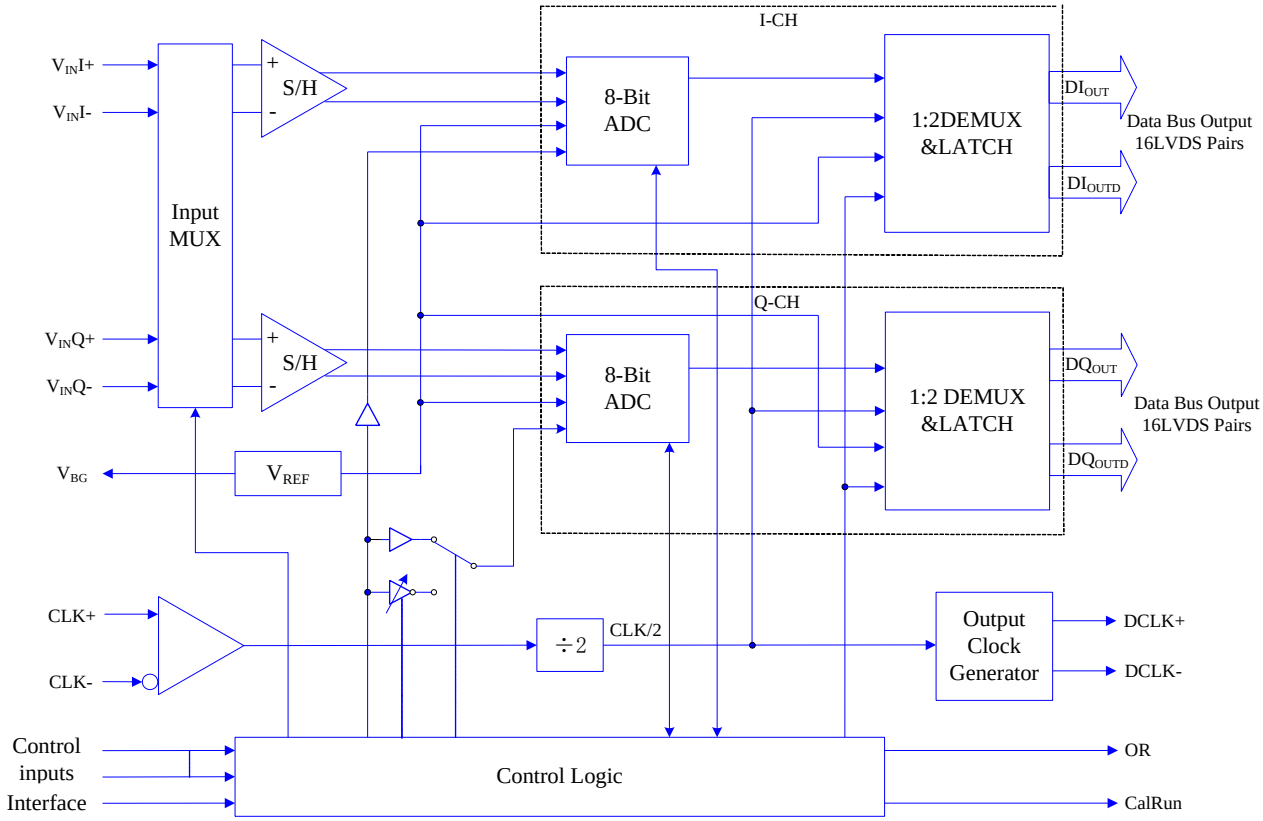


Figure1. Block Diagram

4. Pin Description

The B08D1000RH is packaged in a 128-pin ceramic quad leaded package (CQFP128). The pins description are shown in Figure 2, Table1 and Table2.

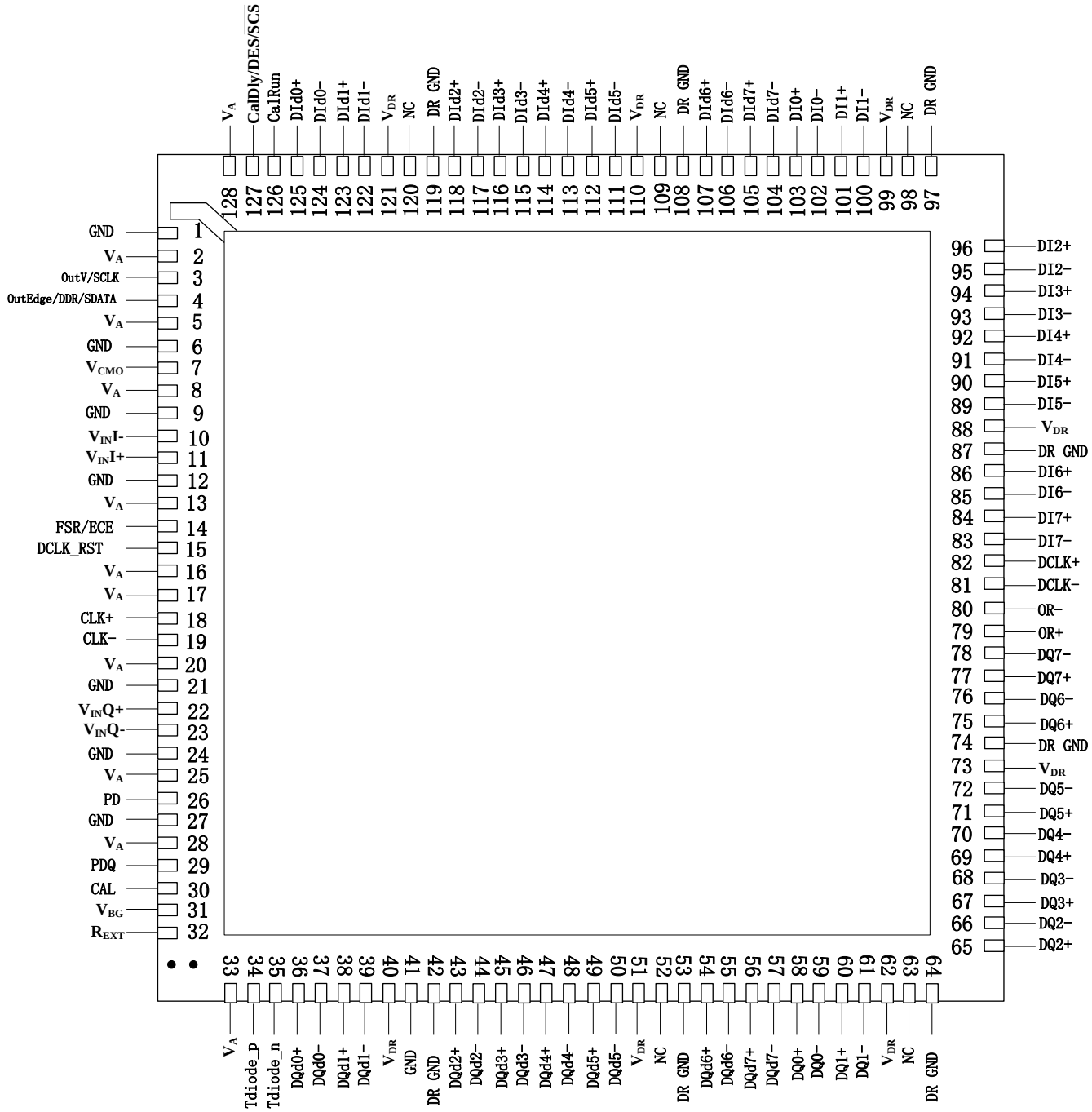


Figure2. Pin configuration

Table1 pin configuration

Pin	Symbol	Property	Pin	Symbol	Property
1	GND	GND	**33**	V_A	VDD
2	V_A	VDD	**34**	Tdiode_p	OUT
3	OutV/SCLK	IN	**35**	Tdiode_n	OUT
4	OutEdge/ DDR/SDATA	IN	**36**	DQd0+	OUT
5	V_A	VDD	**37**	DQd0-	OUT
6	GND	GND	**38**	DQd1+	OUT
7	V_{CMO}	IN	**39**	DQd1-	OUT
8	V_A	VDD	**40**	V_{DR}	VDD
9	GND	GND	**41**	GND	GND
10	V_{IN}I-	IN	**42**	DR GND	GND
11	V_{IN}I+	IN	**43**	DQd2+	OUT
12	GND	GND	**44**	DQd2-	OUT
13	V_A	VDD	**45**	DQd3+	OUT
14	FSR/ECE	IN	**46**	DQd3-	OUT
15	DCLK_RST	IN	**47**	DQd4+	OUT
16	V_A	VDD	**48**	DQd4-	OUT
17	V_A	VDD	**49**	DQd5+	OUT
18	CLK+	IN	**50**	DQd5-	OUT
19	CLK-	IN	**51**	V_{DR}	VDD
20	V_A	VDD	**52**	NC	FLAOTING
21	GND	GND	**53**	DR GND	GND
22	V_{IN}Q+	IN	**54**	DQd6+	OUT
23	V_{IN}Q-	IN	**55**	DQd6-	OUT
24	GND	GND	**56**	DQd7+	OUT
25	V_A	VDD	**57**	DQd7-	OUT
26	PD	IN	**58**	DQ0+	OUT
27	GND	GND	**59**	DQ0-	OUT
28	V_A	VDD	**60**	DQ1+	OUT
29	PDQ	IN	**61**	DQ1-	OUT
30	CAL	IN	**62**	V_{DR}	VDD
31	V_{BG}	OUT	**63**	NC	FLOATING
32	R_{EXT}	IN	**64**	DR GND	GND

Table1 (continued)

Pin	Symbol	Property	Pin	Symbol	Property
65	DQ2+	OUT	**97**	DR GND	GND
66	DQ2-	OUT	**98**	NC	FLOATING
67	DQ3+	OUT	**99**	V_{DR}	VDD
68	DQ3-	OUT	**100**	DI1-	OUT
69	DQ4+	OUT	**101**	DI1+	OUT
70	DQ4-	OUT	**102**	DI0-	OUT
71	DQ5+	OUT	**103**	DI0+	OUT
72	DQ5-	OUT	**104**	DId7-	OUT
73	V_{DR}	VDD	**105**	DId7+	OUT
74	DR GND	GND	**106**	DId6-	OUT
75	DQ6+	OUT	**107**	DId6+	OUT
76	DQ6-	OUT	**108**	DR GND	GND
77	DQ7+	OUT	**109**	NC	FLOATING
78	DQ7-	OUT	**110**	V_{DR}	VDD
79	OR+	OUT	**111**	DId5-	OUT
80	OR-	OUT	**112**	DId5+	OUT
81	DCLK-	OUT	**113**	DId4-	OUT
82	DCLK+	OUT	**114**	DId4+	OUT
83	DI7-	OUT	**115**	DId3-	OUT
84	DI7+	OUT	**116**	DId3+	OUT
85	DI6-	OUT	**117**	DId2-	OUT
86	DI6+	OUT	**118**	DId2+	OUT
87	DR GND	GND	**119**	DR GND	GND
88	V_{DR}	VDD	**120**	NC	FLOATING
89	DI5-	OUT	**121**	V_{DR}	VDD
90	DI5+	OUT	**122**	DId1-	OUT
91	DI4-	OUT	**123**	DId1+	OUT
92	DI4+	OUT	**124**	DId0-	OUT
93	DI3-	OUT	**125**	DId0+	OUT
94	DI3+	OUT	**126**	CalRun	OUT
95	DI2-	OUT	**127**	CalDly/DES/ $\overline{SCS}$	IN
96	DI2+	OUT	**128**	V_A	VDD

Table2 Pin Description

Pin Symbol	Description
OutV / SCLK	Output Voltage Amplitude and Serial Interface Clock. Tie this pin high for normal differential DCLK and data amplitude. Ground this pin for a reduced differential output amplitude and reduced power consumption. When the extended control mode is enabled, this pin functions as the SCLK input which clocks in the serial data.
OutEdge / DDR / SDATA	DCLK Edge Select, Double Data Rate Enable and Serial Data Input. This input sets the output edge of DCLK+ at which the output data transitions. When this pin is floating or connected to 1/2 the supply voltage, DDR clocking is enabled. When the extended control mode is enabled, this pin functions as the SDATA input.
DCLK_RST	DCLK Reset. A positive pulse on this pin is used to reset and synchronize the DCLK outs of multiple converters.
PD，PDQ	Power Down Pins. A logic high on the PD pin puts the entire device into the Power Down Mode. A logic high on the PDQ pin puts only the "Q" ADC into the Power Down mode.
CAL	Calibration Cycle Initiate. A minimum t_{CAL_L} input clock cycles logic low followed by a minimum of t_{CAL_H} input clock cycles high on this pin initiates the self calibration sequence.
FSR/ECE	Full Scale Range Select and Extended Control Enable. In non-extended control mode, a logic low on this pin sets the full-scale differential input range to a reduced V_{IN} input level. A logic high on this pin sets the full-scale differential input range to a higher V_{IN} input level. See Converter Electrical Characteristics. To enable the extended control mode, whereby the serial interface and control registers are employed, allow this pin to float or connect it to a voltage equal to $V_A/2$.
CalDly/ DES / $\overline{SCS}$	Calibration Delay, Dual Edge Sampling and Serial Interface Chip Select. With a logic high or low on pin 14, this pin functions as Calibration Delay and sets the number of input clock cycles after power up before calibration begins. With pin 14 floating, this pin acts as the enable pin for the serial interface input and the CalDly value becomes "0" (short delay with no provision for a long power-up calibration delay). When this pin is floating or connected to a voltage equal to $V_A/2$, DES (Dual Edge Sampling) mode is selected where the "I" input is sampled at twice the input clock rate and the "Q" input is ignored.
CLK+ CLK-	LVDS Clock input pins for the ADC. The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on the falling edge of CLK+.

Table2 (continued)

Pin Symbol	Description
$V_{IN}I+$,$V_{IN}I-$, $V_{IN}Q+$,$V_{IN}Q-$	Analog signal inputs to the ADC. The differential full-scale input range of this input is programmable using the FSR pin in normal mode and the Input Full-Scale Voltage Adjust register in the extended control mode. Refer to the V_{IN} specification in the Converter Electrical Characteristics for the full-scale input range in the normal mode.
V_{CMO}	Common Mode Voltage. The voltage output at this pin is required to be the common mode input voltage at $V_{IN}+$ and $V_{IN}-$ when d.c. coupling is used. This pin should be grounded when a.c. coupling is used at the analog inputs. This pin is capable of sourcing or sinking 100μA.
V_{BG}	Bandgap output voltage capable of 100μA source/sink.
CalRun	Calibration Running indication. This pin is at a logic high when calibration is running.
R_{EXT}	External bias resistor connection. Nominal value is 3.3k-Ohms (±0.1%) to ground.
DCLK+ DCLK-	Differential Clock outputs used to latch the output data. Delayed and non-delayed data outputs are supplied synchronous to this signal. This signal is at 1/2 the input clock rate in SDR mode and at 1/4 the input clock rate in the DDR mode. The DCLK outputs are not active during a calibration cycle, therefore this is not recommended as a system clock.
DI7− / DQ7− DI7+ / DQ7+ DI6− / DQ6− DI6+ / DQ6+ DI5− / DQ5− DI5+ / DQ5+ DI4− / DQ4− DI4+ / DQ4+ DI3− / DQ3− DI3+ / DQ3+ DI2− / DQ2− DI2+ / DQ2+ DI1− / DQ1− DI1+ / DQ1+ DI0− / DQ0− DI0+ / DQ0+	I and Q channel LVDS Data Outputs that are not delayed in the output demultiplexer. Compared with the DId and DQd outputs, these outputs represent the later time samples. These outputs should always be terminated with a 100Ω differential resistor.

Table2 (continued)

Pin Symbol	Description
DId7− / DQd7− DId7+ / DQd7+ DId6− / DQd6− DId6+ / DQd6+ DId5− / DQd5− DId5+ / DQd5+ DId4− / DQd4− DId4+ / DQd4+ DId3− / DQd3− DId3+ / DQd3+ DId2− / DQd2− DId2+ / DQd2+ DId1− / DQd1− DId1+ / DQd1+ DId0− / DQd0− DId0+ / DQd0+	I and Q channel LVDS Data Outputs that are delayed by one CLK cycle in the output demultiplexer. Compared with the DI/DQ outputs, these outputs represent the earlier time sample. These outputs should always be terminated with a 100Ω differential resistor.
OR+ OR-	Out Of Range output. A differential high at these pins indicates that the differential input is out of range (outside the range $\pm V_{IN}/2$ as programmed by the FSR pin in non-extended control mode or the Input Full-Scale Voltage Adjust register setting in the extended control mode).
Tdiode_P Tdiode_N	Temperature Diode Positive (Anode) and Negative (Cathode) for die temperature measurements.
V_A	Analog power supply pins. Bypass these pins to ground.
V_{DR}	Output Driver power supply pins. Bypass these pins to DR GND.
GND	Ground return for V_A.
DR GND	Ground return for V_{DR}.
NC	No Connection. Make no connection to these pins.

5. Electrical Characteristic

The following specifications apply after calibration for V_A = V_{DR} = +1.9V, OutV = 1.9V, V_{IN} FSR (a.c. coupled) = differential 800mV_{P-P}, Differential, a.c. coupled Sine Wave Input Clock, f_{CLK} = 1 GHz at 0.6V_{P-P} with 50% duty cycle, V_{BG} = Floating,

Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}.** All other limits -55℃ ≤ T_A ≤ +125 ℃, unless otherwise noted.

Table3 Electrical Characteristic

Symbol	Parameter	Considerations（note 1,2,3）	Typical	Limits	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
Integral Non-Linearity (Best fit)	INL	DC Coupled, 1MHz Sine Wave Over ranged	±0.3	**±3**	LSB(max)
Differential Non-Linearity	DNL	DC Coupled, 1MHz Sine Wave Over ranged	±0.15	**±1**	LSB(max)
Resolution with No Missing Codes				**8**	Bits
Offset Error	V_{OFF}		-0.45	**-2**	LSB(min)
				+2	LSB(max)
Positive Full-Scale Error	PFSE	note4	-0.6	**±27**	mV(max)
Negative Full-Scale Error	NFSE	note4	-1.31	**±27**	mV(max)
Out of Range Output Code (In addition to OR Output high)		(V_{IN+})-(V_{IN-})> + Full Scale		**255**	
		(V_{IN+})-(V_{IN-})< − Full Scale		**0**	
NORMAL MODE (Non DES) DYNAMIC CONVERTER CHARACTERISTICS					
Full Power Bandwidth	FPBW	Normal Mode(non DES)	1.6		GHz
Gain Flatness		d.c. to 500 MHz	±0.5		dBFS
		d.c. to 1 GHz	±1.0		dBFS
Effective Number of Bits	ENOB	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	7.4	**6.8**	Bits
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	7.0		
Signal-to-Noise Plus Distortion Ratio	SINAD	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	46.3	**42.5**	dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	43.9		
Signal-to-Noise Ratio	SNR	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	46.9	**43**	dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	44.1		

Symbol	Parameter	Considerations（note 1,2,3）	Typical	Limits	Units (Limits)
Total Harmonic Distortion	THD	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	-55.1	**-46**	dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	-47.5		
Spurious-Free dynamic Range	SFDR	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	55.4	**47**	dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	47.5		
INTERLEAVE MODE (DES Pin 127=Float) - DYNAMIC CONVERTER CHARACTERISTICS					
Full Power Bandwidth	FPBW (DES)	Dual Edge Sampling Mode	800		MHz
Effective Number of Bits	ENOB	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	7.3	**6.6**	Bits
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	6.8		
Signal-to-Noise Plus Distortion Ratio	SINAD	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	46.1	**41**	dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	42.5		
Signal-to-Noise Ratio	SNR	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	46.5	**41.5**	dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	43.5		
Total Harmonic Distortion	THD	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	-56.0	**-45**	dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	-49.5		
Spurious-Free dynamic Range	SFDR	f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	57.1	**46**	dB
		f_{IN} = 248 MHz, V_{IN} = FSR − 0.5dB	47.9		
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
Full Scale Analog Differential Input Range	V_{IN}	Pin 14 is low	600	**530**	mV_{P-P}(min)
				670	mV_{P-P}(max)
		Pin 14 is high	800	**720**	mV_{P-P} (min)
				880	mV_{P-P}(max)
Analog Input Common Mode Voltage	V_{CMI}		V_{CMO}	**V_{CMO-}50**	mV_{P-P} (min)
				V_{CMO+}50	mV_{P-P}(max)
Differential Input Resistance	R_{IN}		100	**94**	Ω (min)
				106	Ω (max)

Symbol	Parameter	Considerations（note 1,2,3）	Typical	Limits	Units (Limits)
ANALOG OUTPUT CHARACTERISTICS					
Common Mode Output Voltage	V_{CMO}		1.26	**0.95**	V(min)
				1.45	V(max)
Bandgap Reference Output Voltage	V_{BG}	I_{BG} = ±100 μA	1.26	**1.15**	V(min)
				1.38	V(max)
CLOCK INPUT CHARACTERISTICS					
Differential Clock Input Level	V_{ID}	Sine Wave Clock	0.6	**0.4**	V_{P-P}(min)
				2.0	V_{P-P}(max)
		Square Wave Clock	0.6	**0.4**	V_{P-P}(min)
				2.0	V_{P-P}(max)
DIGITAL CONTROL PIN CHARACTERISTICS					
Logic High Input	V_{IH}			**0.85×V_A**	V(min)
Logic Low Input	V_{IL}			**0.15×V_A**	V(max)
DIGITAL OUTPUT CHARACTERISTICS					
LVDS Differential Output Voltage	V_{OD}	Measured differentially, OutV = V_A, V_{BG}=floating(note5)	710	**400**	mV_{P-P} (min)
				920	mV_{P-P}(max)
		Measured differentially, OutV = GND, V_{BG}=floating(note5)	510	**280**	mV_{P-P} (min)
				720	mV_{P-P}(max)
Output Offset Voltage	V_{OS}	V_{BG}=Floating	800		mV
		V_{BG}=V_A	1200		mV
POWER SUPPLY CHARACTERISTICS					
Analog Supply Current	I_A	PD = PDQ = Low	660	**980**	mA(max)
		PD = Low, PDQ = High	430	**640**	
Output Driver Supply Current	I_{DR}	PD = PDQ = Low	200	**345**	mA(max)
		PD = Low, PDQ = High	110	**200**	
Power Consumption	P_D	PD = PDQ = Low	1.6	**2.5**	W(max)
		PD = Low, PDQ = High	1.0	**1.6**	
AC ELECTRICAL CHARACTERISTICS					
Reset Pulse Width	t_{RPW}	(Note 6)		**4**	Clock Cycles(min)
Reset Setup Time	t_{RS}	(Note 6)	150		ps
Reset Hold Time	t_{RH}	(Note 6)	250		ps
Differential Low to High Transition Time	t_{LHT}	10% to 90%, C_L=2.5pF	250		ps

Symbol	Parameter	Considerations（note 1,2,3）	Typical	Limits	Units (Limits)
Differential High to Low Transition Time	t_{HLT}	10% to 90%, C_L=2.5pF	250		ps
Serial Clock Low Time				**6**	ns(min)
Serial Clock High Time				**6**	ns(min)
Calibration Cycle Time	t_{CAL}		1.4×10^5		Clock Cycles
CAL Pin Low Time	t_{CAL_L}	(Note 6)	80	**640**	Clock Cycles(min)
CAL Pin High Time	t_{CAL_H}	(Note 6)	80	**640**	Clock Cycles(min)
Calibration delay determined by pin 127	t_{CalDly}	CalDly = Low (Note 6)		$\mathbf{2^{25}}$	Clock Cycles(min)
		CalDly = High (Note 6)		$\mathbf{2^{31}}$	Clock Cycles (max)
Max Input Clock Frequency	$f_{CLK(max)}$	Normal Mode (DES or non-DES)	1.2	**1.0**	GHz(min)
Minimum Input Clock Frequency	$f_{CLK(min)}$	Normal Mode(non-DES)	200	-	MHz(min)
Minimum Input Clock Frequency	$f_{CLK(min)}$	Normal Mode(DES)	500	-	MHz(min)
Input Clock Duty Cycle		200MHz≤Input Clock Frequency≤1GHz (Normal Mode)	50	**20**	%(min)
				80	%(max)
Input Clock Duty Cycle		500MHz≤Input Clock Frequency≤1GHz (DES Mode)	50	**20**	%(min)
				80	%(max)
DCLK Duty Cycle			50	**45**	%(min)
				55	%(max)
Sampling Delay	t_{AD}	Input CLK transition to Acquisition of Data	1.3		ns
Aperture Jitter	t_{AJ}		0.4		ps rms

Symbol	Parameter	Considerations（note 1,2,3）		Typical	Limits	Units (Limits)
Input Clock to Data Output Delay	t_{OD}	50% of Input Clock transition to 50% of Data transition		3.1		ns
Pipeline Delay (Latency)		DI Outputs			**13**	Input Clock Cycles
		DId Outputs			**14**	
		DQ Outputs	Normal Mode		**13**	
			DES Mode		**13.5**	
		DQD Outputs	Normal Mode		**14**	
			DES Mode		**14.5**	
Serial Clock Frequency	f_{SCLK}	(Note 6)		67		MHz
Data to Serial Clock Setup Time	t_{SSU}	(Note 6)		2.5		ns(min)
Data to Serial Clock Hold Time	t_{SSH}	(Note 6)		1		ns(min)
Input Clock Low Time	t_{CL}	(Note 6)		500	**200**	ps(min)
Input Clock High Time	t_{CH}	(Note 6)		500	**200**	ps(min)
DCLK to Data Output Skew	t_{OSK}	50% of DCLK transition to 50% of Data transition, SDR Mode and DDR Mode(Note 6)		±50		ps(max)
Data to DCLK Set-Up Time	t_{SU}	DDR Mode, 90 ºDCLK (Note 6)		750		ps
Data to DCLK Hold Time	t_H	DDR Mode, 90 ºDCLK (Note 6)		890		ps

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no guarantee of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The analog inputs are protected by current limit resistor and current limit diode, Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device.

Note 3: To guarantee accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.

Note4: Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of

Full-Scale Error and Reference Voltage Error.

Note5: Tying V_{BG} to the supply rail will increase the output offset voltage (V_{OS}) by 330mV (typical), as shown in the V_{OS} specification above. Tying V_{BG} to the supply rail will also affect the differential LVDS output voltage (V_{OD}), causing it to increase by 40mV (typical).

Note6: This parameter is guaranteed by design and is not tested in production.

6. Transfer Characteristic and Timing Diagrams

6.1 Transfer Characteristic

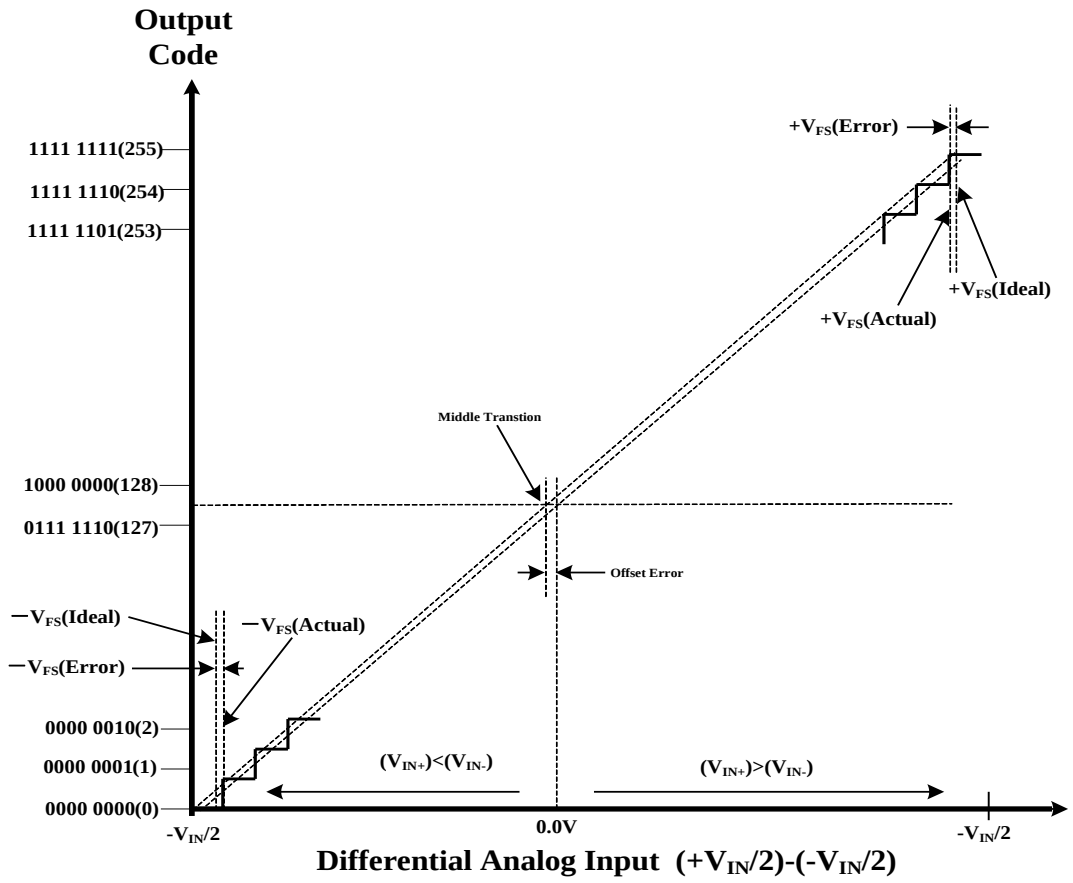


Figure3. Input / Output Transfer Characteristic

6.2 Timing Diagrams

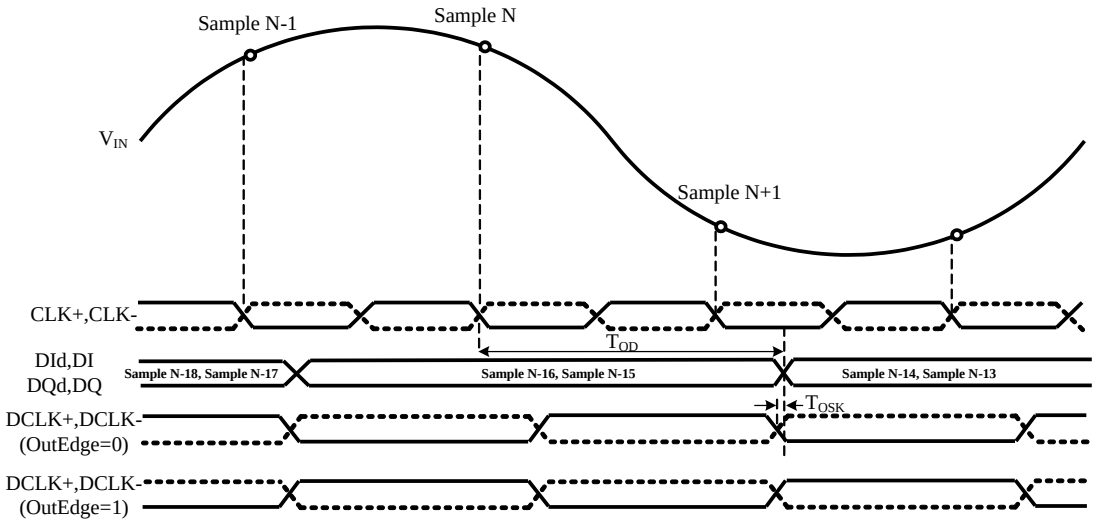


Figure4. B08D1000RH Timing — SDR Clocking

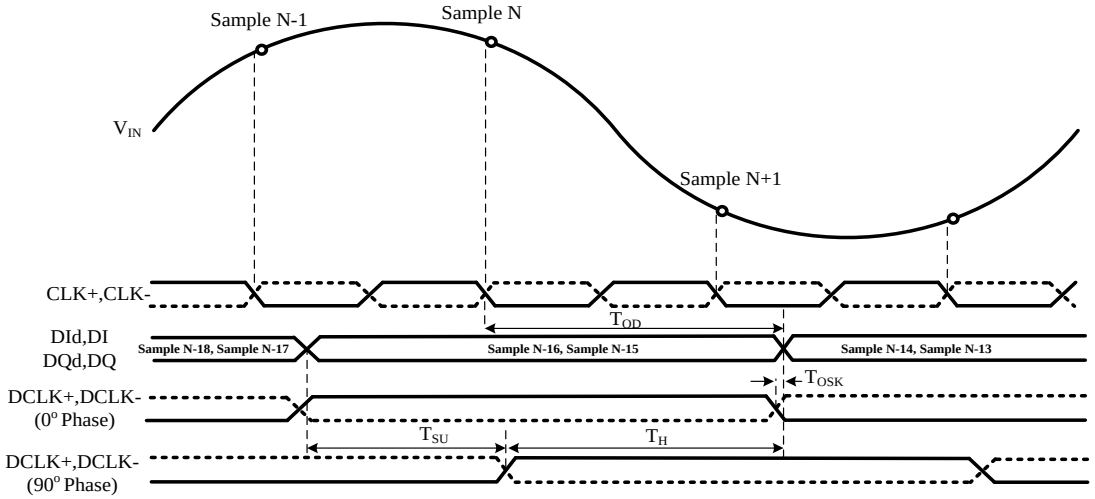


Figure5. B08D1000RH Timing — DDR Clocking

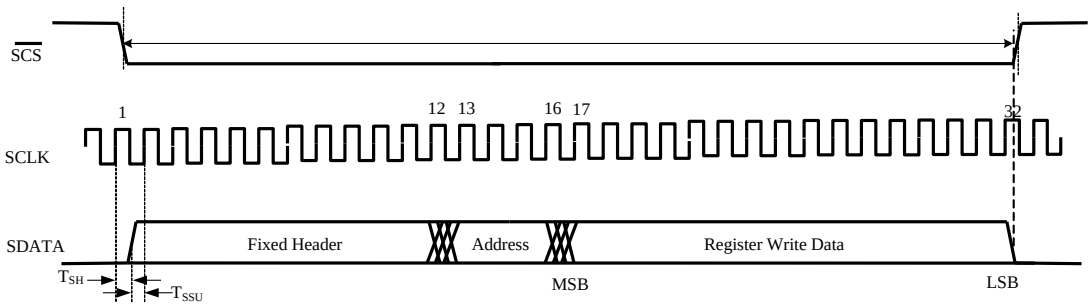


Figure6. Serial Interface Timing

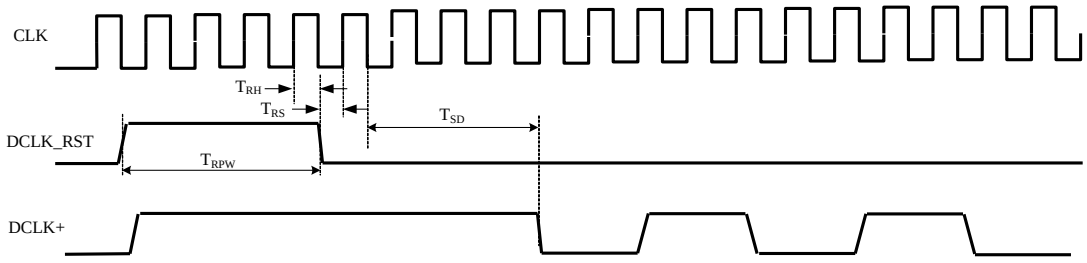


Figure7. Clock Reset Timing in DDR Mode

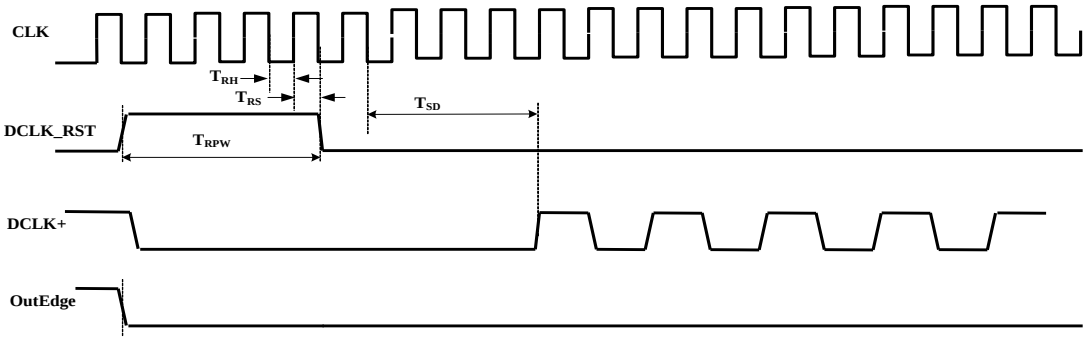


Figure8. Clock Reset Timing in SDR Mode with OUTEDGE Low

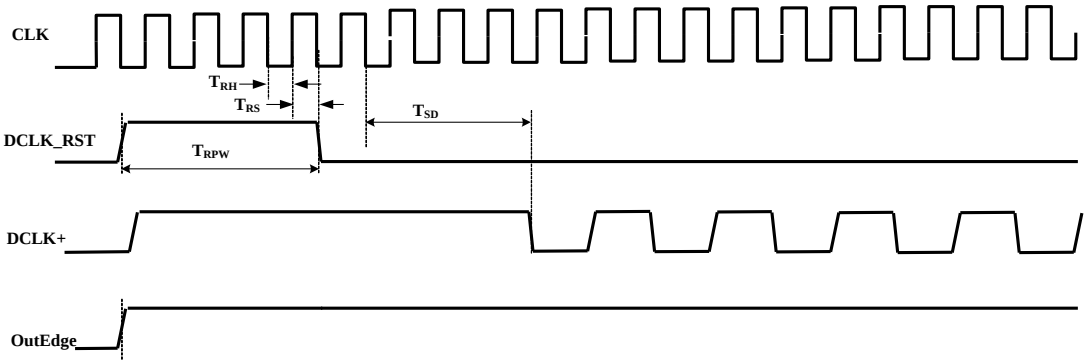


Figure9. Clock Reset Timing in SDR Mode with OUTEDGE High

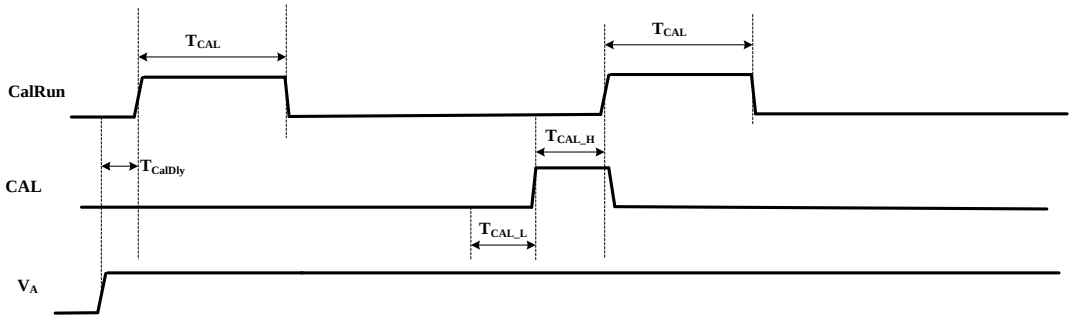


Figure10. Self Calibration and On-Command Calibration Timing

7. Function Description

The B08D1000RH is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in the Applications Information Section.

While it is generally poor practice to allow an active pin to float, pins 4, 14 and 127 of the B08D1000RH are designed to be left floating without jeopardy. In all discussions throughout this data sheet, whenever a function is called by allowing a control pin to float, connecting that pin to a potential of one half the V_A supply voltage will have the same effect as allowing it to float.

7.1 Overview

The B08D1000RH uses a calibrated folding and interpolating architecture that achieves 7.5 effective bits. The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 200 MSPS to 1.2 GSPS, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at either the "I" or "Q" input will cause the OR (Out of Range) output to be activated. This single OR output indicates when the output code from one or both of the channels is below negative full scale or above positive full scale.

Each of the two converters has a 1:2 demultiplexer that feeds two LVDS output buses. The data on these buses provide an output word rate on each bus at half the ADC sampling rate and must be interleaved by the user to provide output words at the full conversion rate.

The output levels may be selected to be normal or reduced. Using reduced levels saves power but could result in erroneous data capture of some or all of the bits, especially at higher sample rates and in marginally designed systems.

7.1.1 Self-Calibration

A self-calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the 100Ω analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command. Running the self calibration is an important part of this chip's functionality and is required in order to obtain adequate performance. In addition to the requirement to be run at power-up, self calibration must be re-run whenever the sense of the FSR pin is changed. For best performance, we recommend that self calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly, according to the system design performance specifications. See 8.4.2 On-Command Calibration for more information. Calibration cannot be initiated or run while the device is in the power-down mode. See 7.1.7 Power Down for information on the interaction between Power Down and Calibration.

During the calibration process, the input termination resistor is trimmed to a value that is equal to R_{EXT} / 33. This external resistor is located between pin 32 and ground. R_{EXT} must be 3300 Ω ±0.1%. With this value, the input termination resistor is trimmed to be 100 Ω. Because R_{EXT} is also used to set the proper current for the Track and Hold amplifier, for the preamplifiers and for the comparators, other values of R_{EXT} should not be used.

In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least t_{CAL_L} clock cycles, then hold it high for at least another t_{CAL_H} clock cycles as defined in the Converter Electrical Characteristics. The time taken by the calibration procedure is specified as t_{CAL} in Converter Electrical Characteristics. Holding the CAL pin high upon power up will prevent the calibration process from running until the CAL pin experiences the above-mentioned t_{CAL_L} clock cycles followed by t_{CAL_H} clock cycles.

CalDly (pin 127) is used to select one of two delay times after the application of power to the start of calibration. This calibration delay time is dependent on the setting of the CalDly pin and is specified as t_{CalDly} in the Converter Electrical Characteristics. These delay values allow the power supply to come up and stabilize

before calibration takes place. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

Calibration Operation Notes:：

During the calibration cycle, the OR output may be active as a result of the calibration algorithm. All data on the output pins and the OR output are invalid during the calibration cycle.

During the power-up calibration and during the on-command calibration, all clocks are halted on chip, including internal clocks and DCLK, while the input termination resistor is trimmed to a value that is equal to R_{EXT} / 33. This is to reduce noise during the input resistor calibration portion of the calibration cycle. See 8.4.2 Self Calibration for information on maintaining DCLK operation during on-command calibration.

This external resistor is located between pin 32 and ground. R_{EXT} must be 3300Ω ± 0.1%. With this value, the input termination resistor is trimmed to be 100Ω. Because R_{EXT} is also used to set the proper current for the Track and Hold amplifier, for the preamplifiers and for the comparators, other values of R_{EXT} should not be used.

The CalRun output is high whenever the calibration procedure is running. This is true whether the calibration is done at power-up or on-command.

7.1.2 Acquiring the Input

Data is acquired at the falling edge of CLK+ (pin 18) and the digital equivalent of that data is available at the digital outputs 13 input clock cycles later for the DI and DQ output buses and 14 input clock cycles later for the DId and DQd output buses. There is an additional internal delay called t_{OD} before the data is available at the outputs. See the Timing Diagram. The B08D1000RH will convert as long as the input clock signal is present. The fully differential comparator design and the innovative design of the sample-and-hold amplifier, together with self calibration, enables a very flat SINAD/ENOB response beyond 1.0 GHz. The B08D1000RH output data signaling is LVDS and the output format is offset binary.

7.1.3 Control Modes

Much of the user control can be accomplished with several control pins that are provided. Examples include initiation of the calibration cycle, power down mode and full scale range setting. However, the B08D1000RH also provides an Extended

Control mode whereby a serial interface is used to access register-based control of several advanced features. The Extended Control mode is not intended to be enabled and disabled dynamically. Rather, the user is expected to employ either the normal control mode or the Extended Control mode at all times. When the device is in the Extended Control mode, pin-based control of several features is replaced with register based control and those pin-based controls are disabled. These pins are OutV (pin 3), OutEdge/DDR (pin 4), FSR (pin 14) and CalDly/DES (pin 127). See 7.2 NORMAL/ EXTENDED CONTROL for details on the Extended Control mode.

7.1.4 The Analog Inputs

The B08D1000RH must be driven with a differential input signal. Operation with a single-ended signal is not recommended. It is important that the inputs either be a.c. coupled to the inputs with the V_{CMO} pin grounded, or d.c. coupled with the V_{CMO} pin left floating. An input common mode voltage equal to the V_{CMO} output must be provided when d.c. coupling is used.

Two full-scale range settings are provided with pin 14 (FSR). The input full-scale range is programmable in the normal mode by setting a level on pin 14 (FSR) as defined in by the specification V_{IN} in the Converter Electrical Characteristics. The full-scale range setting operates equally on both ADCs.

7.1.5 Clocking

The B08D1000RH must be driven with an a.c. coupled, differential clock signal. Section 8.3 describes the use of the clock input pins. A differential LVDS output clock is available for use in latching the ADC output data into whatever device is used to receive the data.

The B08D1000RH offers two options for input and output clocking. These options include a choice of Dual Edge Sampling (DES) or "interleaved mode" where the B08D1000RH performs as a single device converting at twice the input clock rate, a choice of which DCLK edge the output data transitions on, and a choice of Single Data Rate (SDR) or Double Data Rate (DDR) outputs.

The B08D1000RH also has the option to use a duty cycle corrected clock receiver as part of the input clock circuit. This feature is enabled by default and provides improved ADC clocking especially in the Dual-Edge Sampling mode (DES). This circuitry allows the ADC to be clocked with a signal source having a duty cycle ratio of 80/20 % (worst case) for both the normal and the Dual Edge Sampling modes.

Dual-Edge Sampling

The DES mode allows one of the B08D1000RH's inputs (I or Q Channel) to be sampled by both ADCs. One ADC samples the input on the positive edge of the input clock and the other ADC samples the same input on the other edge of the input clock. A single input is thus sampled twice per input clock cycle, resulting in an overall sample rate of twice the input clock frequency, or 2 GSPS with a 1 GHz input clock.

In this mode the outputs are interleaved such that the data is effectively demultiplexed 1:4. Since the sample rate is doubled, each of the 4 output buses have a 500 MSPS output rate with a 1 GHz input clock. All data is available in parallel. The four bytes of parallel data that are output with each clock is in the following sampling order, from the earliest to the latest: DQd, DId, DQ, DI. Table4 indicates what the outputs represent for the various sampling possibilities.

The B08D1000RH also includes an automatic clock phase background calibration feature which can be used in DES mode to automatically and continuously adjust the clock phase of the I and Q channel. This feature removes the need to adjust the clock phase setting manually and provides optimal Dual-Edge Sampling ENOB performance.

IMPORTANT NOTE:

The background calibration feature in DES mode does not replace the requirement for On-Command Calibration which should be run before entering DES mode, or if a large swing in ambient temperature is experienced by the device.

Table4 Input Channel Samples Produced at Data Outputs

Data Outputs (Always sourced with respect to fall of DCLK)	Normal Sampling Mode	Dual-Edge Sampling Mode (DES)	
		I-Channel Selected	Q-Channel Selected *
DI	"I" Input Sampled with Fall of CLK 13 cycles earlier.	"I" Input Sampled with Fall of CLK 13 cycles earlier.	"Q" Input Sampled with Fall of CLK 13 cycles earlier.
DId	"I" Input Sampled with Fall of CLK 14 cycles earlier.	"I" Input Sampled with Fall of CLK 14 cycles earlier.	"Q" Input Sampled with Fall of CLK 14 cycles earlier.
DQ	"Q" Input Sampled with Fall of CLK 13 cycles earlier.	"I" Input Sampled with Rise of CLK 13.5 cycles earlier.	"Q" Input Sampled with Rise of CLK 13.5 cycles earlier.
DQd	"Q" Input Sampled with Fall of CLK 14 cycles after being sampled.	"I" Input Sampled with Rise of CLK 14.5 cycles earlier.	"Q" Input Sampled with Rise of CLK 14.5 cycles earlier.

* Note: In DES + normal mode, only the I Channel is sampled. In DES + extended control

mode, I or Q channel can be sampled.

OutEdge Setting

To help ease data capture in the SDR mode, the output data may be caused to transition on either the positive or the negative edge of the output data clock (DCLK). This is chosen with the OutEdge input (pin 4). A high on the OutEdge input pin causes the output data to transition on the rising edge of DCLK, while grounding this input causes the output to transition on the falling edge of DCLK.

Double Data Rate

A choice of single data rate (SDR) or double data rate (DDR) output is offered. With single data rate the output clock (DCLK) frequency is the same as the data rate of the two output buses. With double data rate the DCLK frequency is half the data rate and data is sent to the outputs on both edges of DCLK. DDR clocking is enabled in non-Extended Control mode by allowing pin 4 to float.

7.1.6 The LVDS Outputs

The data outputs, the Out Of Range (OR) and DCLK, are LVDS. Output current sources provide 3 mA of output current to a differential 100 Ohm load when the OutV input (pin 14) is high or 2.2 mA when the OutV input is low. For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low, which results in lower power consumption. If the LVDS lines are long and/or the system in which the B08D1000RH is used is noisy, it may be necessary to tie the OutV pin high.

The LVDS data output have a typical common mode voltage of 800mV when the V_{BG} pin is unconnected and floating. This common mode voltage can be increased to 1.2V by tying the V_{BG} pin to V_A if a higher common mode is required.

IMPORTANT NOTE:

Tying the V_{BG} pin to V_A will also increase the differential LVDS output voltage by up to 40mV.

7.1.7 Power Down

The B08D1000RH is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode. In this power down mode the data output pins (positive and negative) are put into a high impedance state and the devices power consumption is reduced to a minimal level. The DCLK+/- and OR +/- are not tri-stated, they are weakly pulled down to ground internally. Therefore when both I and Q are powered down the DCLK +/- and OR +/- should not be

terminated to a DC voltage.

A high on the PDQ pin will power down the "Q" channel and leave the "I" channel active. There is no provision to power down the "I" channel independently of the "Q" channel. Upon return to normal operation, the pipeline will contain meaningless information.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state. Calibration will function with the "Q" channel powered down, but that channel will not be calibrated if PDQ is high. If the "Q" channel is subsequently to be used, it is necessary to perform a calibration after PDQ is brought low.

7.2 Normal/Extended Control

The B08D1000RH may be operated in one of two modes. In the simpler standard control mode, the user affects available configuration and control of the device through several control pins. The "extended control mode" provides additional configuration and control options through a serial interface and a set of 8 registers. The two control modes are selected with pin 14 (FSR/ECE: Extended Control Enable). The choice of control modes is required to be a fixed selection and is not intended to be switched dynamically while the device is operational. Table 5 shows how several of the device features are affected by the control mode chosen.

Table5 Features and modes

Feature	Normal Control Mode	Extended Control Mode
SDR or DDR Clocking	DDR Clocking selected with pin 4 floating. SDR clocking selected when pin 4 is not floating.	Selected with nDE in the Configuration Register (1h; bit-10). When the device is in DDR mode, address 1h, bit-8 must be set to 0b.
DDR Clock Phase	Not Selectable (0 °Phase Only)	Selected with DCP bit in the Configuration Register (1h; bit-11).
SDR Data transitions with rising or falling DCLK edge	SDR Data transitions with rising edge of DCLK+ when pin 4 is high and on falling edge when low.	Selected with OE in the Configuration Register (1h; bit-8).
LVDS output level	Normal differential data and DCLK amplitude selected when	Selected with the OV in the Configuration Register (1h; bit-9).

	pin 3 is high and reduced amplitude selected when low.	
Power-On Calibration Delay	Short delay selected when pin 127 is low and longer delay selected when high.	Short delay only.
Full-Scale Range	Selected with pin 14. Selected range applies to both channels.	Up to 512 step adjustments over a nominal range. Selected using the Input Full-Scale Adjust register (3h; bits-7 to 15).
Input Offset Adjust	Not possible	512 steps of adjustment using the Input Offset register (2h; bits-7 to 15).
Dual Edge Sampling Selection	Enabled with pin 127	Enabled through DES Enable Register.
Dual Edge Sampling Input Channel Selection	Only I-Channel Input can be used.	Either I- or Q-Channel input may be sampled by both ADCs.
DES Sampling Clock Adjustment	The Clock Phase is adjusted Automatically.	Automatic Clock Phase control can be selected by setting bit 14 in the DES Enable register (Dh). The clock phase can also be adjusted manually through the Coarse & Fine registers (Eh and Fh).

The default state of the Extended Control Mode is set upon power-on reset (internally performed by the device) and is shown in Table 6.

Table6 Extended Control Mode Operation (Pin 14 Floating)

Feature	**Extended Control Mode Default State**
SDR or DDR Clocking	DDR Clocking
DDR Clock Phase	Data changes with DCLK edge (0 °phase)
LVDS Output Amplitude	Normal amplitude (710 mV_{P-P})
Calibration Delay	Short Delay
Full-Scale Range	700 mV nominal for both channels
Input Offset Adjust	No adjustment for either channel
DES Dual Edge Sampling (DES)	Not enabled

7.3 The Serial Interface

The 3-pin serial interface is enabled only when the device is in the Extended Control mode. The pins of this interface are Serial Clock (SCLK), Serial Data (SDATA) and Serial Interface Chip Select ($\overline{SCS}$) Eight write only registers are accessible through this serial interface.

$\overline{SCS}$：This signal should be asserted low while accessing a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK：Serial data input is accepted with the rising edge of this signal. There is no minimum frequency requirement for SCLK.

SDATA：Each register access requires a specific 32-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. See the Timing Diagram.

Each Register access consists of 32 bits, as shown in Figure 6 of the Timing Diagrams. The fixed header pattern is 0000 0000 0001 (eleven zeros followed by a 1). The loading sequence is such that a "0" is loaded first. These 12 bits form the header. The next 4 bits are the address of the register that is to be written to and the last 16 bits are the data written to the addressed register. The addresses of the various registers are indicated in Table 7.

Refer to the Register Description (Section 7.4) for information on the data to be written to the registers.

Subsequent register accesses may be performed immediately, starting with the 33rd SCLK. This means that the $\overline{SCS}$ input does not have to be de-asserted and asserted again between register addresses. It is possible, although not recommended, to keep the $\overline{SCS}$ input permanently enabled (at a logic low) when using extended control.

IMPORTANT NOTE: The Serial Interface should not be used when calibrating the ADC. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time.

Table7 Register Addresses

4-Bit Address		Register Addressed
Binary	Hex	
0000	0h	×
0001	1h	Configuration
0010	2h	"I" Ch Offset
0011	3h	"I" Ch Full-Scale Voltage Adjust
0100	4h	×
0101	5h	×
0110	6h	×
0111	7h	×

1000	8h	×
1001	9h	×
1010	Ah	"Q" Ch Offset
1011	Bh	"Q" Ch Full-Scale Voltage Adjust
1100	Ch	×
1101	Dh	DES Enable
1110	Eh	DES Coarse Adjust
1110	Fh	DES Fine Adjust

7.4 Register Description

Eight write-only registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Normal Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit.

Configuration Register

Addr：1h（0001b） W only（0xB2FF）

D15	D14	D13	D12	D11	D10	D9	D8
1	0	1	DCS	DCP	nDE	OV	OE

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 Must be set to 1b

Bit 14 Must be set to 0b

Bit 13 Must be set to 1b

Bit 12 DCS: Duty Cycle Stabilizer. When this bit is set to 1b, a duty cycle stabilization circuit is applied to the clock input. When this bit is set to 0b the stabilization circuit is disabled.

POR State: 1b

Bit 11 DCP: DDR Clock Phase. This bit only has an effect in the DDR mode. When this bit is set to 0b, the DCLK edges are time-aligned with the data bus edges ("0 ° Phase"). When this bit is set to 1b, the DCLK edges are placed in the middle of the data bit-cells ("90 ° Phase"), using the one-half speed DCLK shown in *Figure 5* as the phase reference.

POR State: 0b

Bit 10 nDE: DDR Enable. When this bit is set to 0b, data bus clocking follows the DDR (Dual Data Rate) mode whereby a data word is output with each rising and falling edge of DCLK. When this bit is set to a 1b, data bus clocking follows the SDR (single data rate) mode whereby each data word is output with either the rising or falling edge of DCLK ,

as determined by the OutEdge bit.

POR State: 0b

Bit 9 OV: Output Voltage. This bit determines the LVDS outputs' voltage amplitude and has the same function as the OutV pin that is used in the normal control mode. When this bit is set to 1b, the standard output amplitude of 710mV$_{P-P}$ is used. When this bit is set to 0b, the reduced output amplitude of 510mV$_{P-P}$ is used.

POR State: 1b

Bit 8 OE: Output Edge. This bit selects the DCLK edge with which the data words transition in the SDR mode and has the same effect as the OutEdge pin in the normal control mode. When this bit is 1, the data outputs change with the rising edge of DCLK+. When this bit is 0, the data output change with the falling edge of DCLK+.

POR State: 0b

Bits 7:0 Must be set to 1b.

I-Channel Offset

Addr：2h（0010b） W only（0x007F）

D15	D14	D13	D12	D11	D10	D9	D8
（MSB）	Offset Value						（LSB）

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8 Offset Value. The input offset of the I-Channel ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides 0.176 mV of offset.

POR State: 0000 0000 b

Bit 7 Sign bit. 0b gives positive offset, 1b gives negative offset.

POR State: 0b

Bit 6:0 Must be set to 1b

I-Channel Full-Scale Voltage Adjust

Addr：3h（0011b） W only（0x807F）

D15	D14	D13	D12	D11	D10	D9	D8
（MSB）	Adjust Value						

D7	D6	D5	D4	D3	D2	D1	D0
（LSB）	1	1	1	1	1	1	1

Bit 15:7 Full Scale Voltage Adjust Value. The input fullscale voltage or gain of the I-Channel ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV$_{P-P}$ differential value.

0000 0000 0 560mV$_{P-P}$

1000 0000 0 Default Value 700mV$_{P-P}$

1111 1111 1 840mV$_{P-P}$

For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.

POR State: 1000 0000 0b (no adjustment)

Bit 6:0 Must be set to 1b

Q-Channel Offset

Addr: Ah（1010b） W only（0x007F）

D15	D14	D13	D12	D11	D10	D9	D8
（MSB）			Offset Value				（LSB）

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8 Offset Value. The input offset of the Q-Channel ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides about 0.176 mV of offset.

POR State: 0000 0000 b

Bit 7 Sign bit. 0b gives positive offset, 1b gives negative offset.

POR State: 0b

Bit 6:0 Must be set to 1b

Q-Channel Full-Scale Voltage Adjust

Addr: Bh（1011b） W only（0x807F）

D15	D14	D13	D12	D11	D10	D9	D8
（MSB）			Adjust Value				

D7	D6	D5	D4	D3	D2	D1	D0
（LSB）	1	1	1	1	1	1	1

Bit 15:7 Full Scale Voltage Adjust Value. The input full scale voltage or gain of the I-Channel ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV$_{P-P}$ differential value.

0000 0000 0 560mV$_{P-P}$

1000 0000 0 Default Value 700mV$_{P-P}$

1111 1111 1 840mV$_{P-P}$

For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.

POR State: 1000 0000 0b (no adjustment)

Bit 6:0 Must be set to 1b

DES Enable

Addr: Dh（1101b） W only（0x3FFF）

D15	D14	D13	D12	D11	D10	D9	D8
DEN	ACP	1	1	1	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 DES Enable. Setting this bit to 1b enables the Dual Edge Sampling mode. In this mode the ADCs in this device are used to sample and convert the same analog input in a time interleaved manner, accomplishing a sampling rate of twice the input clock rate. When this bit is set to 0b, the device operates in the normal dual channel mode.

POR State: 0b

Bit 14 Automatic Clock Phase Control. (ACP) Setting this bit to 1b enables the Automatic Clock Phase Control. In this mode the DES Coarse and Fine manual controls are disabled. A phase detection circuit continually adjusts the I and Q sampling edges to be 180 degrees out of phase. When this bit is set to 0b, the sample (input) clock delay between the I and Q channels is set manually using the DES Coarse and Fine Adjust registers. (See 8.4.5 Dual Edge Sampling for important application information) Using the ACP Control option is recommended over the manual DES settings.

POR State: 0b

DES Coarse Adjust

Addr: Eh（1110b） W only（0x07FF）

D15	D14	D13	D12	D11	D10	D9	D8
IS	ADS	CAM			1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15 Input Select. When this bit is set to 0b the "I" input is operated upon by both ADCs. When this bit is set to 1b the "Q" input is operated on by both ADCs.

POR State: 0b

Bit 14 Adjust Direction Select. When this bit is set to 0b, the programmed delays are applied to the "I" channel sample clock while the "Q" channel sample clock remains fixed. When this bit is set to 1b, the programmed delays are applied to the "Q" channel sample clock while the "I" channel sample clock remains fixed.

POR State: 0b

Bit 13:11 Coarse Adjust Magnitude. Each code value in this field delays either the "I" channel or the "Q" channel sample clock (as determined by the ADS bit) by approximately 20 picoseconds. A value of 000b in this field causes zero adjustment.

POR State: 000b

Bit 10:0 Must be set to 1b.

DES Fine Adjust

Addr：Fh（1111b） W only（0x007F）

D15	D14	D13	D12	D11	D10	D9	D8
（MSB）	FAM						

D7	D6	D5	D4	D3	D2	D1	D0
（LSB）	1	1	1	1	1	1	1

Bit 15:7 Fine Adjust Magnitude. Each code value in this field delays either the "I" channel or the "Q" channel sample clock (as determined by the ADS bit of the DES Coarse Adjust Register) by approximately 0.1 ps. A value of 0000 0000 0b in this field causes zero adjustment. Note that the amount of adjustment achieved with each code will vary with the device conditions as well as with the Coarse Adjustment value chosen.

POR State: 0000 0000 0b

Bit 6:0 Must be set to 1b.

7.4.1 Note Regarding Extended Mode Offset Correction

When using the I or Q channel Offset Adjust registers, the following information should be noted. For offset values of +0000 0000 and -0000 0000, the actual offset is not the same. By changing only the sign bit in this case, an offset step in the digital output code of about 1/10th of an LSB is experienced. This is shown more clearly in the figure below.

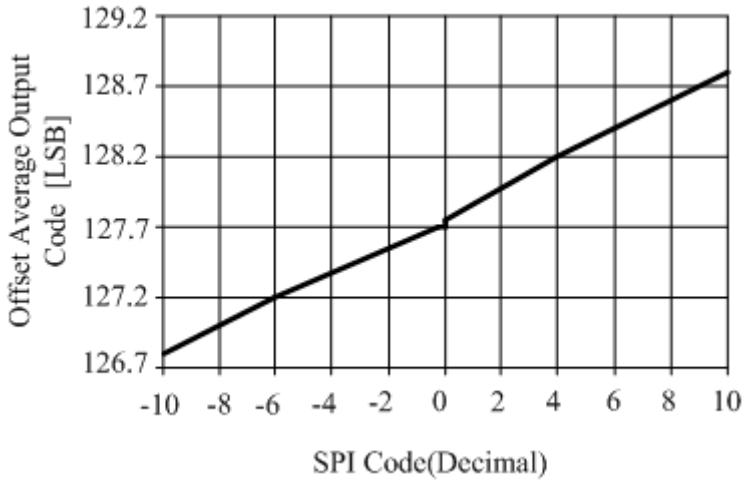


Figure11. Extended Mode Offset Behavior

IMPORTANT NOTE: The Serial Interface are not recommended to be used when the ADC is used in aerospace applications or environments.

7.5 Multiple ADC Synchronization

The B08D1000RH has the capability to precisely reset its sampling clock input to DCLK output relationship as determined by the user-supplied DCLK_RST pulse. This allows multiple ADCs in a system to have their DCLK (and data) outputs transition at the same time with respect to the shared CLK input that all the ADCs use for sampling.

The DCLK_RST signal must observe some timing requirements that are shown in Figure 7, Figure 8 and Figure 9 of the Timing Diagrams. The DCLK_RST pulse must be of a minimum width and its desertion edge must observe setup and hold times with respect to the CLK input rising edge. These times are specified in the AC Converter Electrical Characteristics.

The DCLK_RST signal can be asserted asynchronous to the input clock. If DCLK_RST is asserted, the DCLK output is held in a designated state. The state in which DCLK is held during the reset period is determined by the mode of operation (SDR/DDR) and the setting of the Output Edge configuration pin or bit. (Refer to Figure 7, Figure 8 and Figure 9 for the DCLK reset state conditions). Therefore, depending upon when the DCLK_RST signal is asserted, there may be a narrow pulse on the DCLK line during this reset event. When the DCLK_RST signal is de-asserted in synchronization with the CLK rising edge, the next CLK falling edge synchronizes the DCLK output with those of other B08D1000RHs in the system. The DCLK output is enabled again after a constant delay (relative to the input clock frequency) which is equal to the CLK input to DCLK output delay (t_{SD}). The device always exhibits this

delay characteristic in normal operation.

The DCLK-RST pin should NOT be brought high while the calibration process is running (while CalRun is high). Doing so could cause a digital glitch in the digital circuitry, resulting in corruption and invalidation of the calibration.

7.6 Radiation Hardened Performance

a） Total Ionizing Dose ≥ 100 Krad(Si)

b） SEL threshold ≥ 75 MeV·cm^2/mg

8. Application Information

8.1 The Reference Voltage

The voltage reference for the B08D1000RH is derived from a 1.254V bandgap reference, a buffered version of which is made available at pin 31, V_{BG}, for user convenience.

This output has an output current capability of ±100 μA and should be buffered if more current than this is required.

Differential input signals up to the chosen full-scale level will be digitized to 8 bits. Signal excursions beyond the full-scale range will be clipped at the output. These large signal excursions will also activate the OR output for the time that the signal is out of range. See 8.2.2 Out Of Range (OR) Indication.

One extra feature of the V_{BG} pin is that it can be used to raise the common mode voltage level of the LVDS outputs. The output offset voltage (V_{OS}) is typically 800 mV when the V_{BG} pin is used as an output or left unconnected. To raise the LVDS offset voltage to a typical value of 1200 mV the V_{BG} pin can be connected directly to the supply rails.

8.2 The Analog Input

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. In the normal mode, the full-scale input range is selected using the FSR pin as specified in the Converter Electrical Characteristics. In the Extended Control mode, the full-scale input range is selected by programming the Full-Scale Voltage Adjust register through the Serial Interface. For best performance when adjusting the input full-scale range in the Extended Control, refer to 7.4. for guidelines on limiting the amount of adjustment. Table 8 gives the input to output relationship with the FSR pin high and the normal (non-extended) mode is used. With

the FSR pin grounded, the millivolt values in Table 8 are reduced to 75% of the values indicated. In the Enhanced Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

Table8 DIFFERENTIAL INPUT TO OUTPUT RELATIONSHIP

(Non-Extended Control Mode, FSR High)

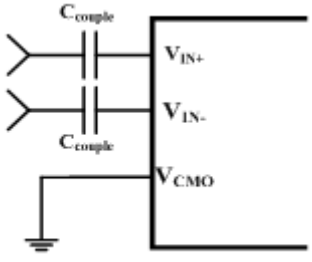
V_{IN}+	V_{IN}-	Output Code
V_{CM}-200mV	V_{CM}+200mV	0000 0000
V_{CM}-100mV	V_{CM}+100mV	0100 0000
V_{CM}	V_{CM}	0111 1111/1000 0000
V_{CM}+100mV	V_{CM}-100mV	1100 0000
V_{CM}+200mV	V_{CM}-200mV	1111 1111

The buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

Note that a precise d.c. common mode voltage must be present at the ADC inputs. This common mode voltage, V_{CMO}, is provided on-chip when a.c. input coupling is used and the input signal is a.c. coupled to the ADC.

When the inputs are a.c. coupled, the V_{CMO} output must be grounded, as shown in Figure 12. This causes the on-chip V_{CMO} voltage to be connected to the inputs through on-chip 50k-Ohm resistors.

IMPORTANT NOTE: An Analog input channel that is not used (e.g. in DES Mode) should be left floating when the inputs are a.c. coupled. Do not connect an unused analog input to ground. When the d.c. coupled mode is used, a common mode voltage must be provided at the differential inputs. This common mode voltage should track the V_{CMO} output pin. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change.



B08D1000RH

Figure12. Differential Input Drive

IMPORTANT NOTE: An analog input channel that is not used (e.g. in DES Mode) should be tied to the V_{CMO} voltage when the inputs are d.c. coupled. Do not connect unused analog inputs to ground.

Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}.

Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog inputs remain within 50 mV of V_{CMO}.

If d.c. coupling is used, it is best to servo the input common mode voltage, using the V_{CMO} pin, to maintain optimum performance. An example of this type of circuit is shown in Figure 13.

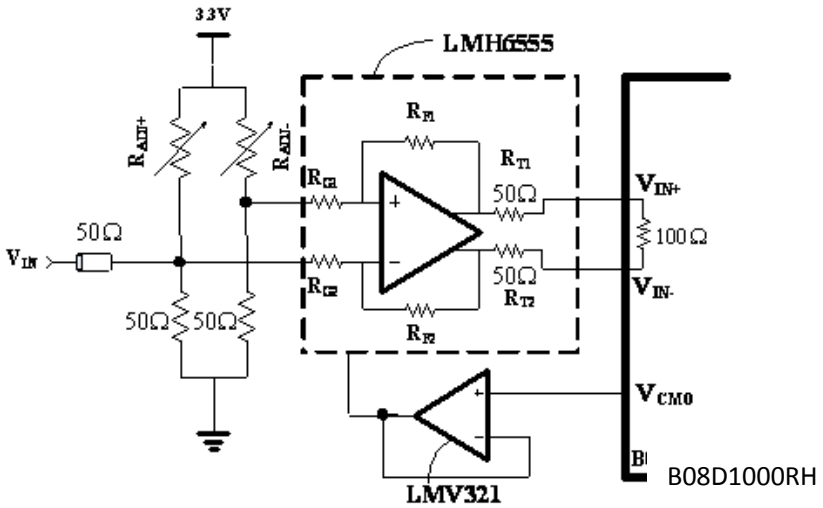


Figure13. Example of Servoing the Analog Input with V_{CMO}

IMPORTANT NOTE: Be sure that the current drawn from the V_{CMO} output does not exceed 100 μA.The Input impedance in the d.c. coupled mode (V_{CMO} pin not grounded) consists of a precision 100Ω resistor between $V_{IN}+$ and $V_{IN}-$ and a capacitance from each of these inputs to ground. In the a.c. coupled mode the input appears the same except there is also a resistor of 50K between each analog input pin and the V_{CMO} potential.

8.2.1 Handling Single-Ended Input Signals

There is no provision for the B08D1000RH to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC. The easiest way to accomplish single-ended to differential signal conversion is with an appropriate balun-connected

transformer, as shown in Figure 14.

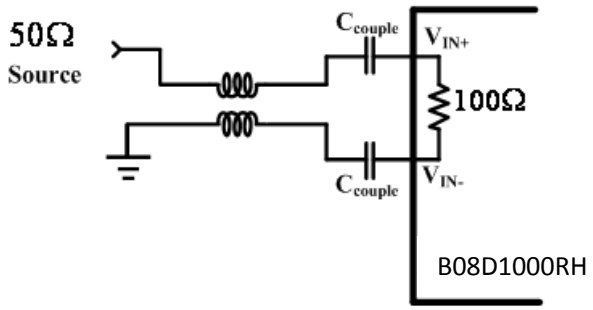


Figure14. Single-Ended to Differential Signal Conversion Using a Balun

a.c. Coupled Input

The 100 Ohm external resistor placed across the output terminals of the balun in parallel with the B08D1000RH's on-chip 100 Ohm resistor makes a 50 Ohms differential impedance at the balun output. Or, 25 Ohms to virtual ground at each of the balun output terminals.

8.2.2 Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is activated such that OR+ goes high and OR- goes low. This output is active as long as accurate data on either or both of the buses would be outside the range of 00h to FFh.

8.2.3 Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the B08D1000RH is derived from an internal band-gap reference. The FSR pin controls the effective reference voltage of the B08D1000RH such that the differential full-scale input range at the analog inputs is a normal amplitude with the FSR pin high, or a reduced amplitude with FSR pin low as defined by the specification V_{IN} in the Converter Electrical Characteristics. Best SNR is obtained with FSR high, but better distortion and SFDR are obtained with the FSR pin low.

8.3 The Clock Inputs

The B08D1000RH has differential LVDS clock inputs, CLK+ and CLK-, which must be driven with an a.c. coupled, differential clock signal. Although the B08D1000RH is tested and its performance is guaranteed with a differential 1.0 GHz clock, it typically will function well with input clock frequencies indicated in the Converter Electrical Characteristics. The clock inputs are internally terminated and biased. The input clock signal must be capacitively coupled to the clock pins as indicated in Figure 15.

Operation up to the sample rates indicated in the Converter Electrical Characteristics is typically possible if the maximum ambient temperatures indicated are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Important also for reliability is proper thermal management.

The differential input clock line pair should have a characteristic impedance of 100Ω and (when using a balun), be terminated at the clock source in that (100Ω) characteristic impedance. The input clock line should be as short and as direct as possible. The B08D1000RH clock input is internally terminated with an untrimmed 100Ω resistor.

Insufficient input clock levels will result in poor dynamic performance. Excessively high input clock levels could cause a change in the analog input offset voltage. To avoid these problems, keep the input clock level within the range specified in the Converter Electrical Characteristics.

High speed, high performance ADCs such as the B08D1000RH, require a very stable input clock signal with minimum phase noise or jitter.

Input clock amplitudes above those specified in the Converter Electrical Characteristics may result in increased input offset voltage. This would cause the converter to produce an output code other than the expected 127/128 when both input pins are at the same potential.

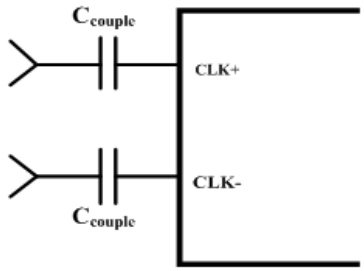


Figure15. Differential (LVDS) Input Clock Connection

8.4 Control Pins

Six control pins (without the use of the serial interface) provide a wide range of possibilities in the operation of the B08D1000RH and facilitate its use. These control pins provide Full-Scale Input Range setting, Self Calibration, Calibration Delay, Output Edge Synchronization choice, LVDS Output Level choice and a Power Down

feature.

8.4.1 Full-Scale Input Range Setting

The input full-scale range can be selected with the FSR control input (pin 14) in the normal mode of operation. The is specified as V_{IN} in the Converter Electrical Characteristics. In the extended control mode, the input full-scale range may be programmed using the Full-Scale Adjust Voltage register. See8.2 THE ANALOG INPUT for more information.

8.4.2 Self Calibration

The B08D1000RH self-calibration must be run to achieve specified performance. The calibration procedure is run upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is an input clock present upon power up or if the clock begins some time after application of power. The CalRun output indicator is high while a calibration is in progress. Note that DCLK outputs are not active during a calibration cycle, therefore it is not recommended as a system clock.

Power-On Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is determined by the setting of CalDly, The calibration process will be not be performed if the CAL pin is high at power up. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The B08D1000RH will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired.

The internal power-on calibration circuitry comes up in an unknown logic state. If the input clock is not running at power up and the power on calibration circuitry is active, it will hold the analog circuitry in power down and the power consumption will typically be less than 200 mW. The power consumption will be normal after the clock starts.

On-Command Calibration

On-command calibration may be run at any time in NORMAL (non-DES) mode only. Do not run a calibration while operating the ADC in Auto DES Mode.

If the ADC is operating in Auto DES mode and a calibration cycle is required then the controlling application should bring the ADC into normal (non DES) mode before an On Command calibration is initiated. Once calibration has completed, the ADC can be put back into Auto DES mode.

To initiate an on-command calibration, bring the CAL pin high for a minimum of t_{CAL_H} input clock cycles after it has been low for a minimum of t_{CAL_L} input clock cycles. Holding the

CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of t_{CAL_L} input clock cycles, then brought high for a minimum of another t_{CAL_H} input clock cycles. The calibration cycle will begin t_{CAL_H} input clock cycles after the CAL pin is thus brought high. The CalRun signal should be monitored to determine when the calibration cycle has completed.

The minimum t_{CAL_H} and t_{CAL_L} input clock cycle sequences are required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in Section 7.1.1 for best performance, a self calibration should be performed 20 seconds or more after power up and repeated when the operating temperature changes significantly, according to the particular system performance requirements. ENOB drops slightly with increasing junction temperature, and a self calibration eliminates the change. In the first example, (see Figure 16) a sample clock of 1GSPS is used to capture a full-scale 749MHz signal at the I-channel input as

the junction temperature (T_J) is increased from 65℃ to 125℃ with no intermediate calibration cycles. The vertical line at 125℃ is the result of an on-command calibration cycle that essentially eliminates the drop in ENOB. Of course, calibration cycles can be run more often, at smaller intervals of temperature change, if system design specifications require it. In the second example, (see Figure 16) the test method is the same and the I-channel input signal is 249MHz. The variation in ENOB vs. T_J has a smaller range then the previous example, and is again removed by an on-command calibration cycle at the maximum test temperature.

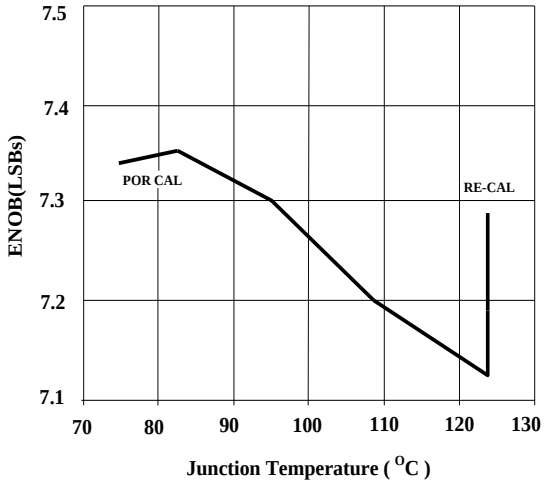


Figure16. ENOB vs. Junction Temperature, 749 MHz Input

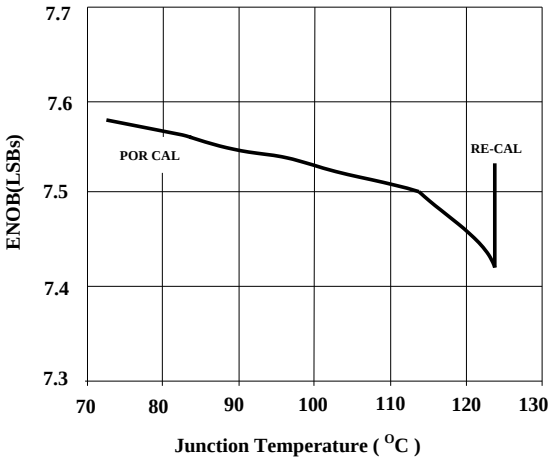


Figure17. ENOB vs. Junction Temperature, 249 MHz Input

Calibration Delay

The CalDly input (pin 127) is used to select one of two delay times after the application of power to the start of calibration. The calibration delay values allow the power supply to come up and stabilize before calibration takes place. With no delay or insufficient delay, calibration would begin before the power supply is stabilized at its operating value and result in non-optimal calibration coefficients. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply. Note that the calibration delay selection is not possible in the Extended Control mode and the short delay time is used.

8.4.3 Output Edge Synchronization

DCLK signals are available to help latch the converter output data into external circuitry. The output data can be synchronized with either edge of these DCLK signals. That is, the output data transition can be set to occur with either the rising edge or the falling edge of the DCLK signal, so that either edge of that DCLK signal can be used to latch the output data into the receiving circuit.

When OutEdge (pin 4) is high, the output data is synchronized with (changes with) the rising edge of the DCLK+ (pin 82). When OutEdge is low, the output data is synchronized with the falling edge of DCLK+.

At the very high speeds of which the B08D1000RH is capable, slight differences in the lengths of the DCLK and data lines can mean the difference between successful and erroneous data capture. The OutEdge pin is used to capture data on the DCLK

edge that best suits the application circuit and layout.

8.4.4 LVDS Output Level Control

The output level can be set to one of two levels with OutV (pin3). The strength of the output drivers is greater with OutV high. With OutV low there is less power consumption in the output drivers, but the lower output level means decreased noise immunity.

For short LVDS lines and low noise systems, satisfactory performance may be realized with the OutV input low. If the LVDS lines are long and/or the system in which the B08D1000RH is used is noisy, it may be necessary to tie the OutV pin high.

8.4.5 Dual Edge Sampling

The Dual Edge Sampling (DES) feature causes one of the two input pairs to be routed to both ADCs. The other input pair is deactivated. One of the ADCs samples the input signal on one input clock edge (duty cycle corrected), the other samples the input signal on the other input clock edge (duty cycle corrected). The result is a 1:4 demultiplexed output with a sample rate that is twice the input clock frequency.

To use this feature in the non-enhanced control mode, allow pin 127 to float and the signal at the "I" channel input will be sampled by both converters. The Calibration Delay will then only be a short delay. In the enhanced control mode, either input may be used for dual edge sampling. See 7.1.5 Dual-Edge Sampling.

IMPORTANT NOTES :

1) For the Extended Control Mode - When using the Automatic Clock Phase Control feature in dual edge sampling mode, it is important that the automatic phase control is disabled (set bit 14 of DES Enable register Dh to 0) before the ADC is powered up. Not doing so may cause the device not to wake up from the power down state.

2) For the Non-Extended Control Mode - When the B08D1000RH is powered up and DES mode is required, ensure that pin 127 (CalDly/DES/$\overline{\text{SCS}}$) is initially pulled low during or after the power up sequence. The pin can then be allowed to float or be tied to V_A / 2 to enter the DES mode. This will ensure that the part enters the DES mode correctly.

3) The automatic phase control should also be disabled if the input clock is interrupted or stopped for any reason. This is also the case if a large abrupt change in

the clock frequency occurs.

4) If a calibration of the ADC is required in Auto DES mode, the device must be returned to the Normal Mode of operation before performing a calibration cycle. Once the Calibration has been completed, the device can be returned to the Auto DES mode and operation can resume.

8.4.6 Power Down Feature

The Power Down pins (PD and PDQ) allow the B08D1000RH to be entirely powered down (PD) or the "Q" channel to be powered down and the "I" channel to remain active. See 7.1.7 Power Down for details on the power down feature.

The digital data (+/-) output pins are put into a high impedance state when the PD pin for the respective channel is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

8.5 The Digital Outputs

The B08D1000RH demultiplexes the output data of each of the two ADCs on the die onto two LVDS output buses (total of four buses, two for each ADC). For each of the two converters,

the results of successive conversions started on the odd falling edges of the CLK+ pin are available on one of the two LVDS buses, while the results of conversions started on the even falling edges of the CLK+ pin are available on the other LVDS bus. This means that, the word rate at each LVDS bus is 1/2 the B08D1000RH input clock rate and the two buses must be multiplexed to obtain the entire 1 GSPS conversion result.

Since the minimum recommended input clock rate for this device is 200 MSPS (normal non DES mode), the effective rate can be reduced to as low as 100 MSPS by using the results available on just one of the two LVDS buses and a 200 MHz input clock, decimating the 200 MSPS data by two.

There is one LVDS output clock pair (DCLK+/-) available for use to latch the LVDS outputs on all buses. Whether the data is sent at the rising or falling edge of DCLK is determined by the sense of the OutEdge pin, as described in Section8.4.3.

DDR (Double Data Rate) clocking can also be used.

In this mode a word of data is presented with each edge of DCLK, reducing the DCLK frequency to 1/4 the input clock frequency. See the Timing Diagram section for details.

The OutV pin is used to set the LVDS differential output levels. See 8.4.4 LVDS Output Level Control.

The output format is Offset Binary. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}− will produce an output code of all ones, a full-scale input level with V_{IN}− positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}− are equal, the output code will vary between codes 127 and 128.

8.6 Power Considerations

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins. A 0.1 µF capacitor should be placed as close as possible to each V_A pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the JW Miller FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the B08D1000RH should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a system where a lot of digital power is being consumed should not be used to supply power to the B08D1000RH. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

8.6.1 Supply Voltage

The B08D1000RH is specified to operate with a supply voltage of 1.9V±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than

does the voltage at the B08D1000RH power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the B08D1000RH. The circuit of Figure 17 will provide supply overshoot protection.

Many linear regulators will produce output spiking at power-on unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the B08D1000RH, unless a minimum load is provided for the supply. The 100Ω resistor at the regulator output provides a minimum output current during power-up to ensure there is no turn-on spiking.

In the circuit of Figure 18, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V. If a 3.3V supply is used, an LM1086 linear regulator is recommended.

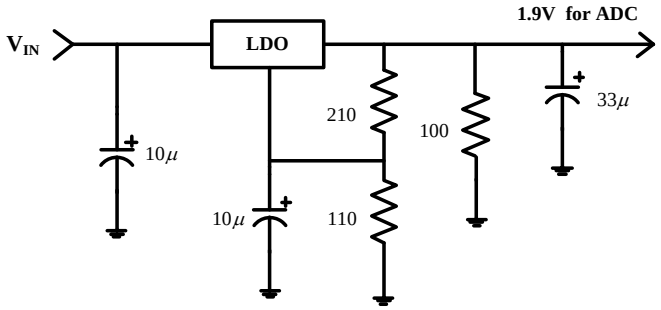


Figure18. Non-Spiking Power Supply

The output drivers should have a supply voltage, V_{DR} that is within the range specified in the Operating Ratings table. This voltage should not exceed the VA supply voltage.

If the power is applied to the device without an input clock signal present, the current drawn by the device might be below 200 mA. This is because the B08D1000RH gets reset through clocked logic and its initial state is unknown. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less than 100 mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the input clock is established.

8.6.2 Thermal Management

As a convenience to the user, the B08D1000RH incorporates a thermal diode to aid in temperature measurement. However, this diode has not been characterized and has

no information to provide regarding its characteristics. Hence, no information is available as to the temperature accuracy attainable when using this diode.

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB.

8.7 Layout And Grouding

Proper grounding and proper routing of all signals are essential to ensure accurate conversion. A single ground plane should be used, instead of splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry. High power digital components should not be located on or near any linear component or power supply trace or plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC, causing excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90 ℃to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines should be isolated from ALL other lines, analog and digital. The generally accepted 90 ° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a straight signal path.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the B08D1000RH. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the analog ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

8.8 Dynamic Performance

The B08D1000RH is a.c. tested and its dynamic performance is guaranteed. To

meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in Section 8.3.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the input clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

This is because this path from the die to ground is a lower impedance than offered by the package pins.

8.9 Using The Serial Interface

The B08D1000RH may be operated in the non-extended control (non-Serial Interface) mode or in the extended control mode. Table 9 and Table 10 describe the functions of pins 3, 4, 14 and 127 in the non-extended control mode and the extended control mode, respectively.

Non-Extended Control Mode Operation

Non-extended control mode operation means that the Serial Interface is not active and all controllable functions are controlled with various pin settings. That is, the full-scale range, single-ended or differential input, the power on calibration delay, the output voltage and the input coupling (a.c. or d.c.). The non-extended control mode is used by setting pin 14 high or low, as opposed to letting it float. Table 9 indicates the pin functions in the non-extended control mode.

Table9 Non-Extended Control Mode Operation(Pin 14 High or Low)

Pin	Low	High	Floating
3	Reduced V_{OD}	Normal V_{OD}	n/a
4	OutEdge=Neg	OutEdge=Pos	DDR
127	CalDly Short	CalDly Long	n/a
14	Reduced V_{IN}	Normal V_{IN}	Extended Control Mode

Pin 3 can be either high or low in the non-extended control mode. Pin 14 must not be left floating to select this mode. See7.2 NORMAL/EXTENDED CONTROL for more information. Pin 4 can be high or low or can be left floating in the non-extended control mode. In the non-extended control mode, pin 4 high or low defines the edge at which the output data transitions. See 8.4.3 Output Edge Synchronization for more information. If this pin is floating, the output clock (DCLK) is a DDR (Double Data Rate) clock (see 7.1.5 Double Data Rate) and the output edge synchronization is

irrelevant since data is clocked out on both DCLK edges. Pin 127 in the non-extended control mode sets the calibration delay. Pin 127 is not designed to remain floating.

Table10 Extended Control Mode Operation

Pin	Function
3	SCLK(Serial Clock)
4	SDATA(Serial Data)
127	$\overline{SCS}$（Serial Interface Chip Select）

8.10 Common Application Pitfalls

Driving the inputs (analog or digital) beyond the power supply rails.

For device reliability, no input should go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot. Care should be taken not to overdrive the inputs of the B08D1000RH. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode.

As discussed in sections 7.1.4 and 8.2, the Input common mode voltage must remain within 50 mV of the V_{CMO} output , which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is more than 50 mV from V_{CMO} .

Using an inadequate amplifier to drive the analog input.

Use care when choosing a high frequency amplifier to drive the B08D1000RH as many high speed amplifiers will have higher distortion than will the B08D1000RH, resulting in overall system performance degradation.

Driving the V_{BG} pin to change the reference voltage.

As mentioned in Section 8.1, the reference voltage is intended to be fixed to provide one of two different full-scale values (600 mV_{P-P} and 800 mV_{P-P}). Over driving this pin will not change the full scale value, but can be used to change the LVDS common mode voltage from 0.8V to 1.2V by tying the V_{BG} pin to V_A.

Driving the clock input with an excessively high level signal.

The ADC input clock level should not exceed the level described in the Operating Ratings Table or the input offset could change.

Inadequate input clock levels.

As described in Section 8.3, insufficient input clock levels can result in poor performance. Excessive input clock levels could result in the introduction of an input offset.

Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace.

This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

9. Storage Condition

The warehouse environment of B08D1000RH should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

Table 11. The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

10. Applications

10.1 Applications Field

- Direct RF Down Conversion
- High-speed Radars
- Digital Oscilloscopes
- Satellite Set-top boxes
- Communications Systems
- Test Instrumentation

10.2 Typical Application

The device is available in a CQFP package with 128 leads. To guarantee fine characteristics of the device, some pins of 2，5，8，13，16，17，20，25，28，33，128 should be connected to the analog power supply V_A, some pins of 1，6，9，

12，21，24，27, 41 should be connected to the analog ground GND, some pins of 40，51，62，73，88，99，110，121 should be connected to the drive power supply V_{DR}, some pins of 42，53，64，74，87，97，108，119 should be connected to the drive ground DR GND. The differential resistors of 100Ω are connected between the data output+ and data output-. To monitor the reference current of the device, a resistor of 3.3k is used. Simultaneously, the Low-Dropout-Regulator which provides stable power supply and enough drive capability and 0.1uF capacitance linked between the power supply and ground are applied to decrease the power supply fluctuation.

There are lots of configurations in this device, so it can work flexibly. Table 12 shows how several of the device features are affected by the configuration of pins and the figure 19 as follows illustrates the typically application and the peripheral circuit in details.

Table 12 the pin configuration operation

Configuration	Conditions	Features
Normal Mode(pin14(FSR/ECE) is not floating)		
Pin3(OutV/SCLK)	(OutV)=V_A	Large voltage range output
	(OutV)=GND	Small voltage range output
Pin4(OutEdge/DDR/SDATA)	(OutEdge)=V_A	Output data are present in the rising edge of the “DCLK”
	(OutEdge)=GND	Output data are present in the falling edge of the “DCLK”.
Pin14(FSR/ECE)	(FSR/ECE)=V_A	Large amplitude input
	(FSR/ECE)=GND	Small amplitude intput
Extended Control Mode(pin14(FSR/ECE) is floating)		
Pin3(OutV/SCLK))	Square Wave Clock	Serial data input is accepted at the rising edge of this input.
Pin4(OutEdge/DDR/SDATA)	-	Each register access requires a specific 32-bit pattern at this input.
Pin14(FSR/ECE)	Pin14 is floating	The extended control mode is selected when this pin is floating.

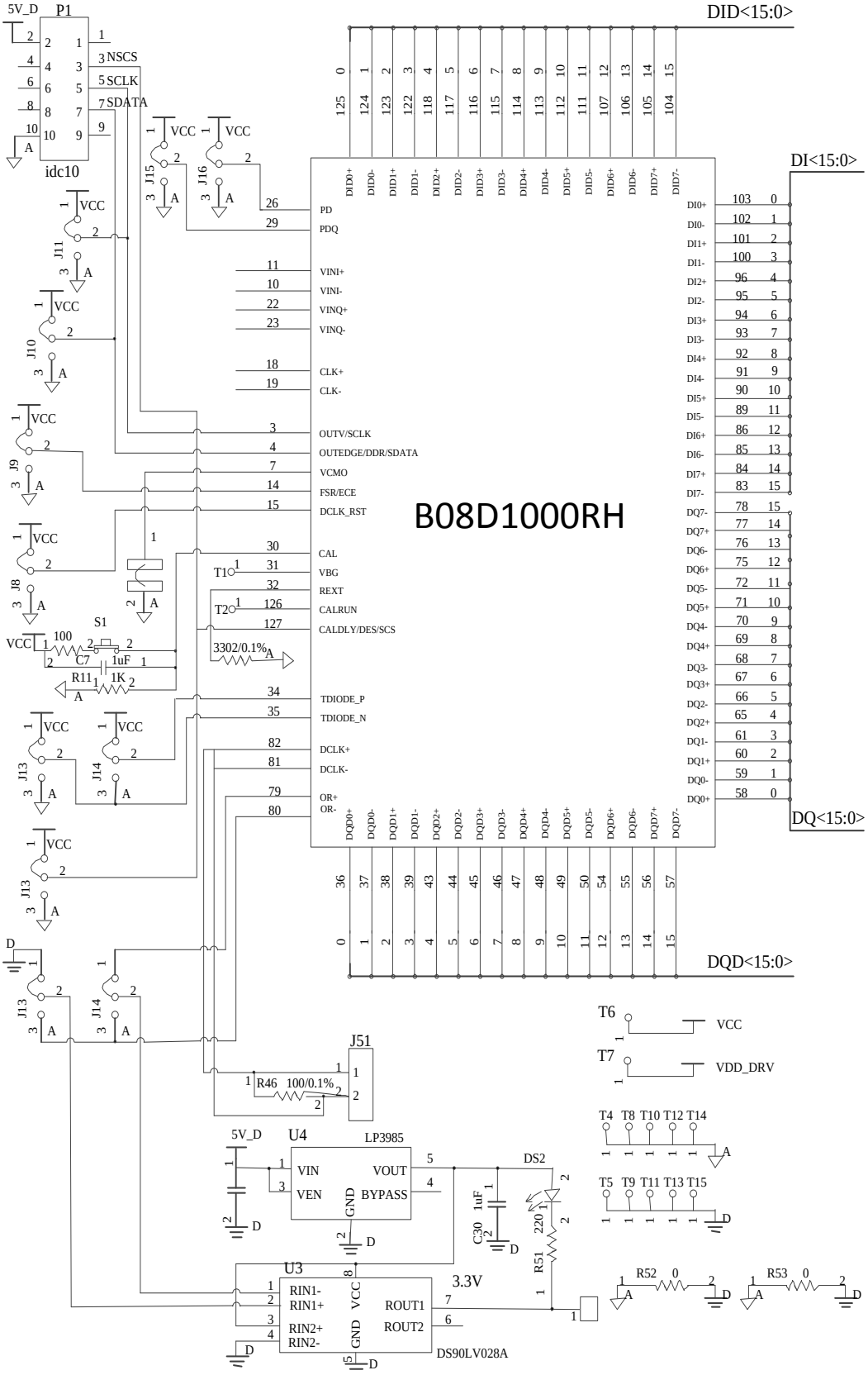


Figure19. The typically application and the peripheral circuit (a)

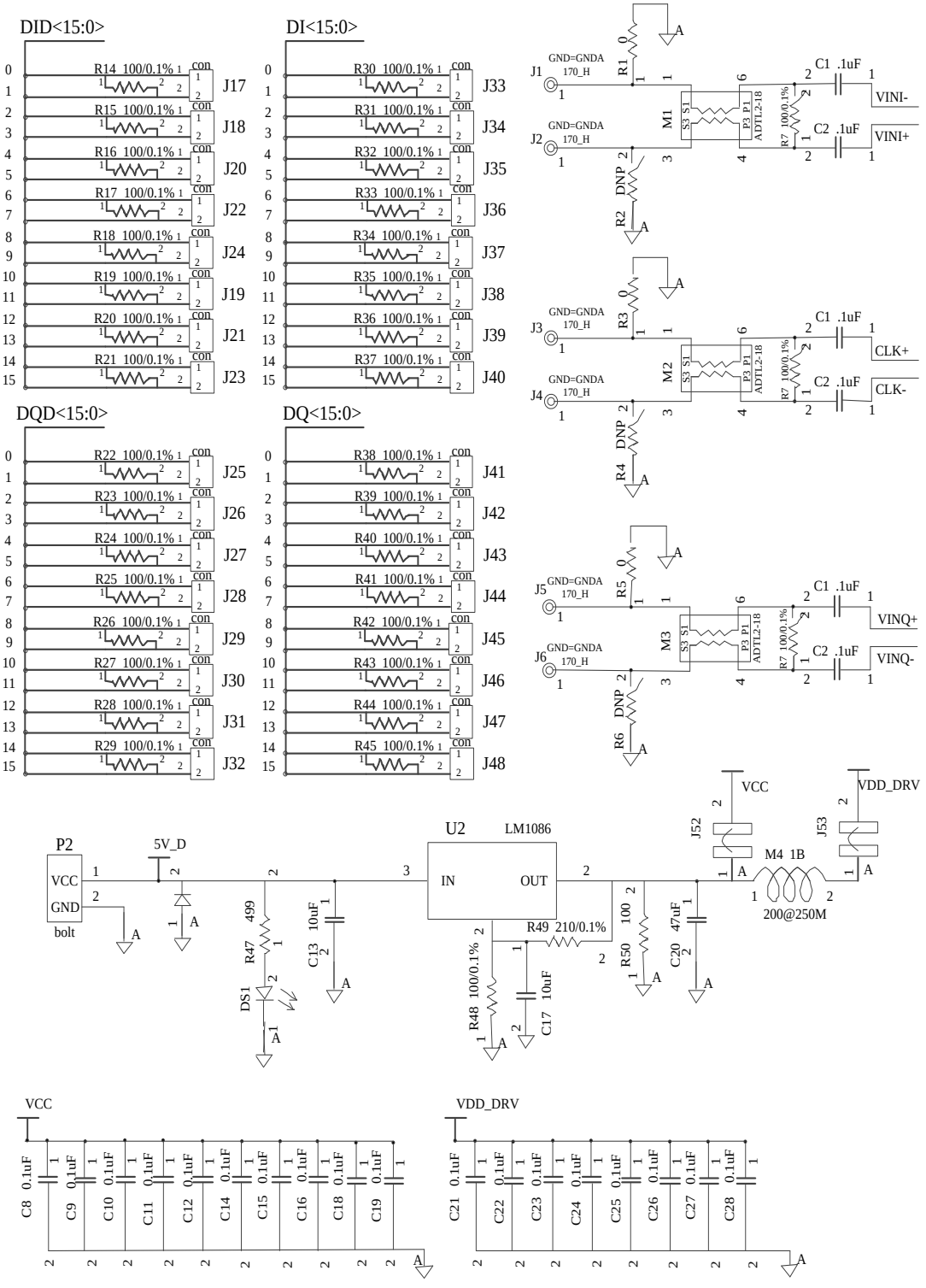
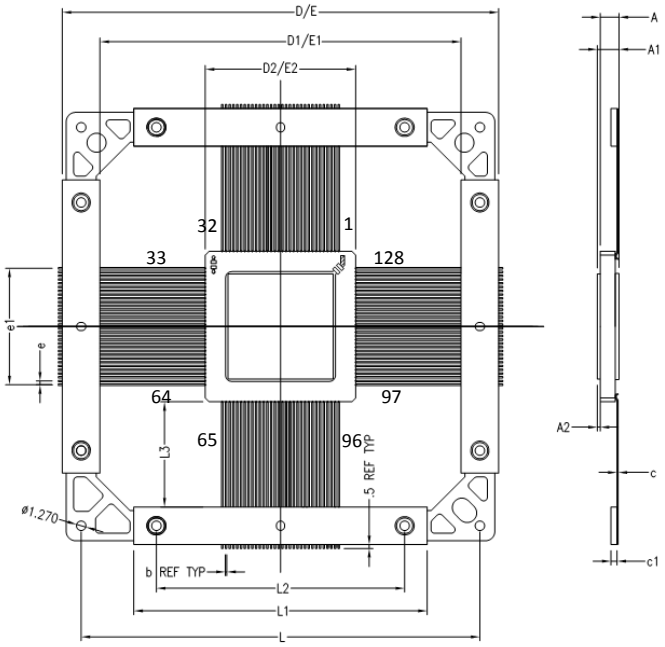


Figure19. The typically application and the peripheral circuit (b)

11. Package Outline Dimension

B08D1000RH's package style is CQFP128, its physical size is shown in figure20.



Symbol	Value (mm)		
	Minimum	Type	Maximum
A	2.30	—	2.70
A1	2.70	—	3.10
A2	—	0.38	—
b	0.15	—	0.25
c	0.10	—	0.20
c1	—	0.80	—
D/E	57.65	—	58.35
D1/E1	47.75	—	48.75
D2/E2	19.80	—	20.20
e	0.45	—	0.55
e1	15.30	—	15.70
L	52.79	—	53.21
L1	38.61	—	39.39
L2	32.70	—	33.30
L3	13.80	—	14.20

Figure20. Physical size

Service & Supply

Address：No.2.Siyingmen N.Rd.Donggaodi, Fengtai District, Beijing, PRC

Department：Department of international cooperation

Telephone：010-67968115-8334

Fax：010-68757706

Zip code：100076