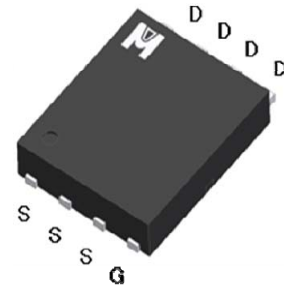
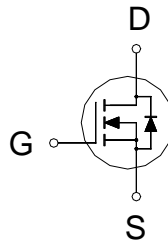




N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV <sub>DSS</sub>	30V
R <sub>DS(on)</sub> (MAX.)	9mΩ
I <sub>D</sub>	50A



UIS, R<sub>g</sub> 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	50	A
	T <sub>C</sub> = 100 °C		35	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	140	
Avalanche Current		I <sub>AS</sub>	37.5	
Avalanche Energy	L = 0.1mH, I <sub>D</sub> =37.5A, R <sub>G</sub> =25Ω	E <sub>AS</sub>	70	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	E <sub>AR</sub>	15	
Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	50	W
	T <sub>C</sub> = 100 °C		20	
Operating Junction & Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

100% UIS testing in condition of V<sub>D</sub>=15V, L=0.1mH, V<sub>G</sub>=10V, I<sub>L</sub>=25A, Rated V<sub>DS</sub>=30V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R <sub>θJC</sub>		2.5	°C / W
Junction-to-Ambient <sup>3</sup>	R <sub>θJA</sub>		50	

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%

<sup>3</sup>50°C / W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.7	3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V			1	μA
		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C			25	
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	50			A
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A		7.5	9	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 15A		11	13.5	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 20A		20		S
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz		828		pF
Output Capacitance	C <sub>oss</sub>			196		
Reverse Transfer Capacitance	C <sub>rss</sub>			174		
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 15mV, V <sub>DS</sub> = 0V, f = 1MHz		1.7		Ω
Total Gate Charge <sup>1,2</sup>	Q <sub>g</sub> (V <sub>GS</sub> =10V)	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 25A		17.6		nC
	Q <sub>g</sub> (V <sub>GS</sub> =4.5V)			12.5		
Gate-Source Charge <sup>1,2</sup>	Q <sub>gs</sub>			2.8		
Gate-Drain Charge <sup>1,2</sup>	Q <sub>gd</sub>			7.4		
Turn-On Delay Time <sup>1,2</sup>	t <sub>d(on)</sub>		V <sub>DS</sub> = 15V, I <sub>D</sub> = 20A, V <sub>GS</sub> = 10V, R <sub>GS</sub> = 2.7Ω		8	
Rise Time <sup>1,2</sup>	t <sub>r</sub>			18		
Turn-Off Delay Time <sup>1,2</sup>	t <sub>d(off)</sub>			20		
Fall Time <sup>1,2</sup>	t <sub>f</sub>			3		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T<sub>C</sub> = 25 °C)</b>						
Continuous Current	I <sub>S</sub>				50	A
Pulsed Current <sup>3</sup>	I <sub>SM</sub>				140	
Forward Voltage <sup>1</sup>	V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0V			1.3	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = I <sub>S</sub> , dI <sub>F</sub> /dt = 100A / μS		22		nS
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>			180		A
Reverse Recovery Charge	Q <sub>rr</sub>			12		nC

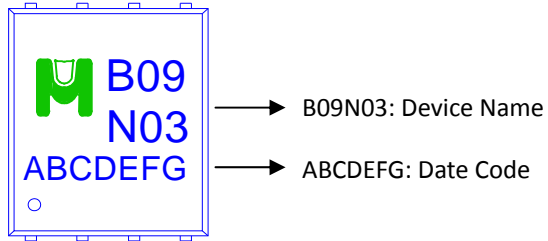
<sup>1</sup>Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Pulse width limited by maximum junction temperature.

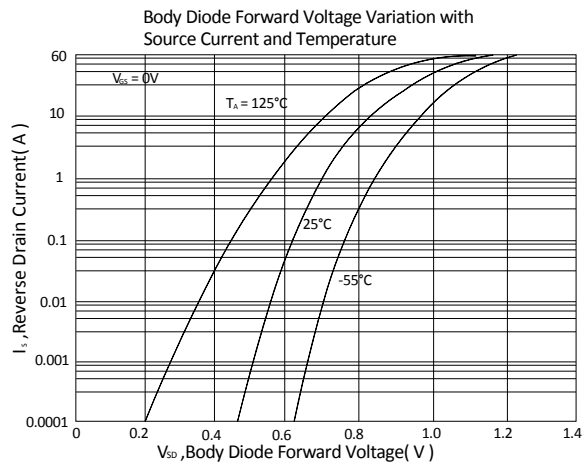
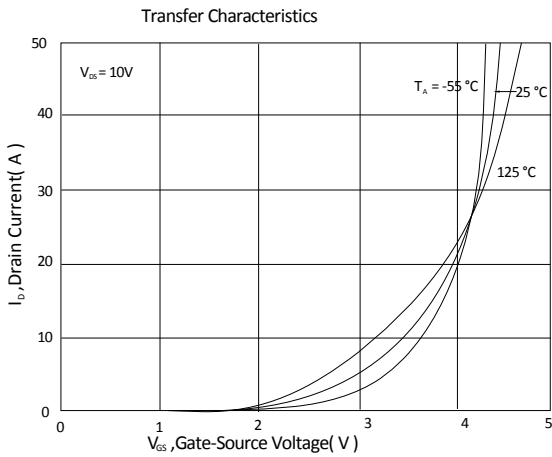
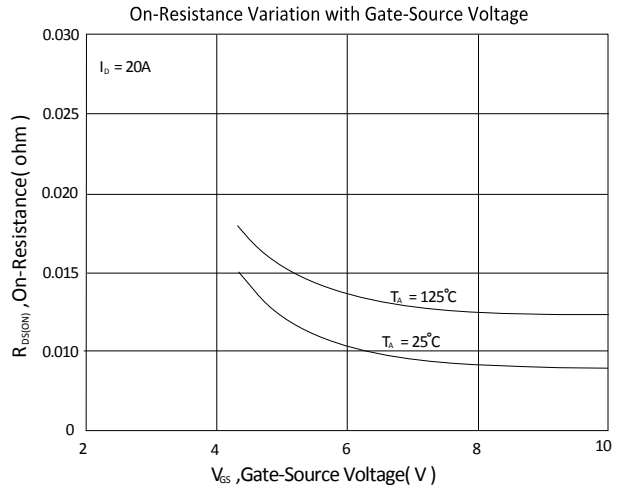
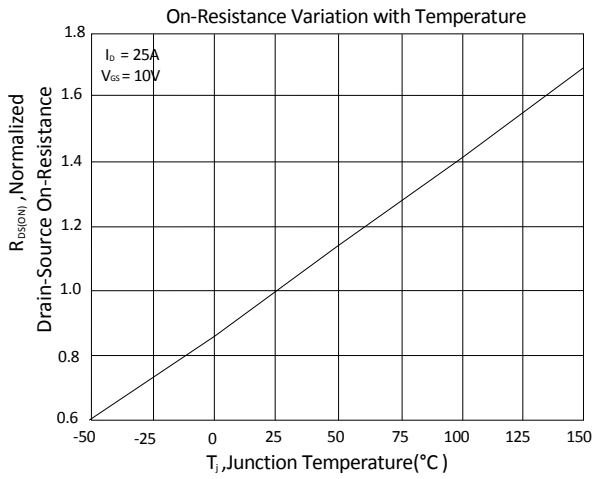
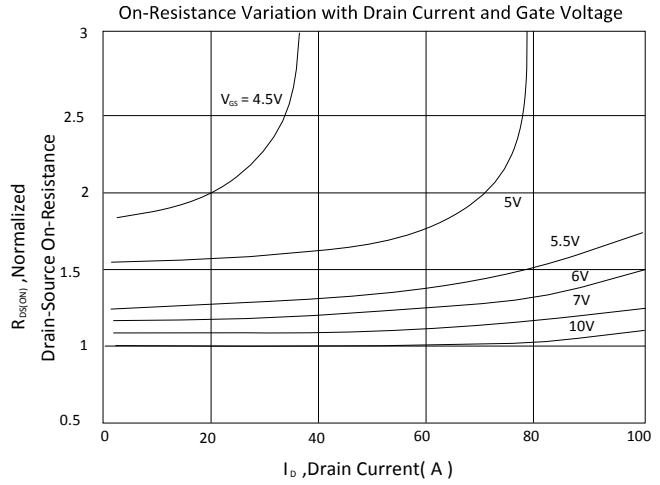
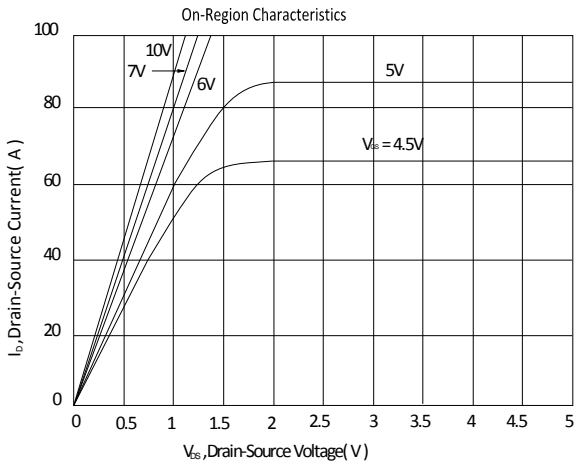
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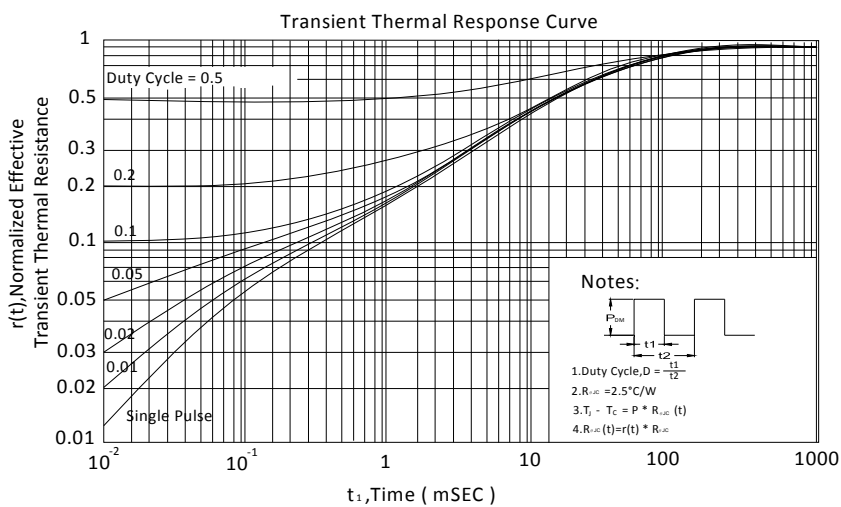
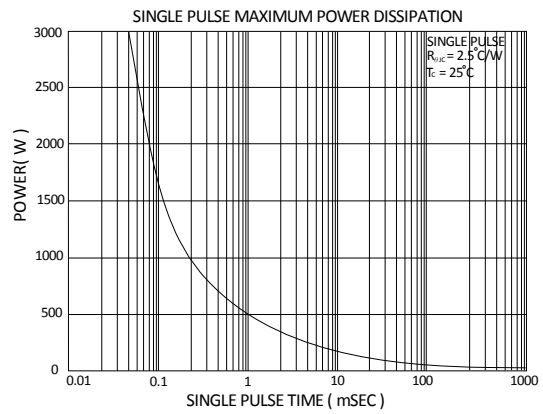
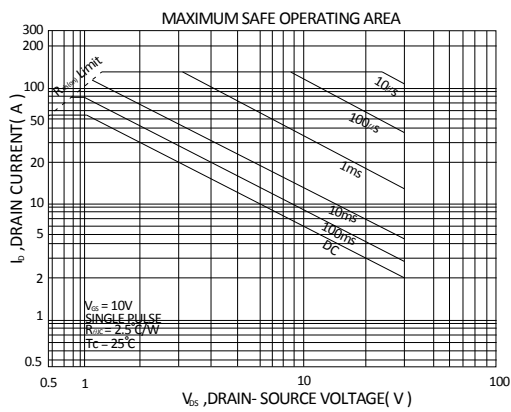
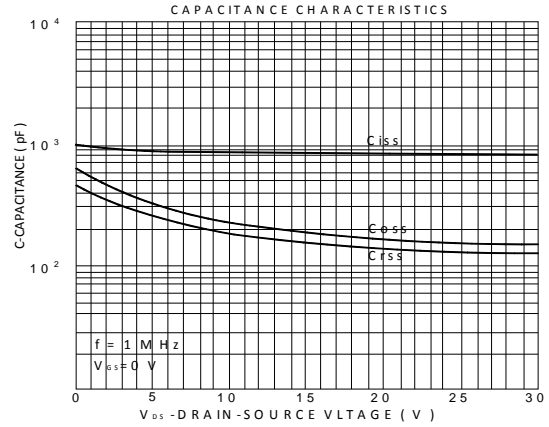
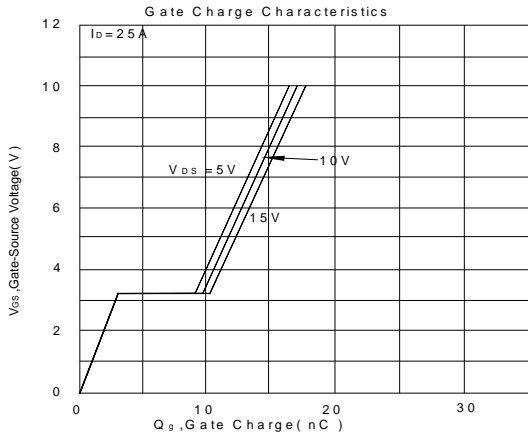
Device Name: EMB09N03H for EDFN 5 x 6





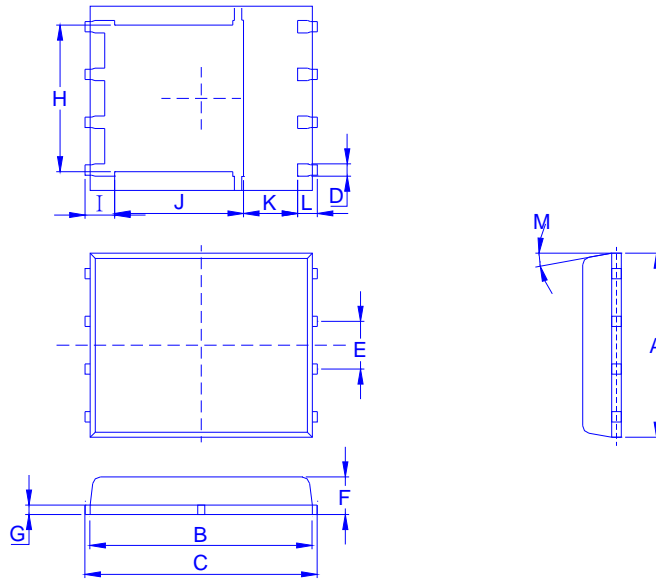
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

