B120 Data Sheet

(Bridge120)

DAT0018C

(Date: 10/28/99)

Genesis Microchip Inc.

165 Commerce Valley Dr. West, Thornhill, ON Canada L3T 7V8 Tel: (905) 889-5400 Fax: (905) 889-0035

1871 Landings Drive, Mountain View, CA, USA 94043 Tel: (650) 428-4277 Fax (650) 428-4288

www.genesis-microchip.com / info@genesis-microchip.on.ca

Revision History:

- March 1998 (First publication)
- August 1998 (General Update)
- October 1998 (Corrections)
- June 1999 (New Format)
- July 1999 (Added Related Documents)
- October 1999 (Incorporated Modified Electronical Characteristics for revision B and C)

Related Documents

- Bridge API Reference Manual Ver.1.00
- DAT-1018
- DSR-0018
- SED-0701
- SED-0700
- SED-0737

Table of Contents

1. General Description.

1.1 Summary

Liquid Crystal Displays have advanced to the point of being comparable with CRT monitors in color capabilities, size, and resolution. In many applications, remote flat panel displays are more desirable than CRTs. However supporting the multi-sync feature of the CRT monitor on the fixed-resolution flat panel display imposes a technical challenge. The B120 chip developed by Paradise Electronics, Inc., a subsidiary of Genesis Microchip Inc., provides a flat-panel-monitor solution that is compatible with today's CRT standards.

1.1 Features

Single Chip Solution without External Frame Buffer

The B120 is a highly integrated single chip interface controller for flat panel monitors. Featuring three integrated 8 bit ADC's (analog-to-digital converters), Clock Generator, Image Processor, and Panel Controller, the chip allows monitor vendors to deliver multi-sync. flat-panel-monitors supporting up to 16.8 million colors and 1280 x 1024 resolutions. Besides the high level of integration, B120 requires no external frame buffer and therefore provides a simplified and cost-effective solution.

CRT interface

- Converts analog RGB signals up to 16.8 million colors
- Sync format support for IBM compatible PCs, Apple Macintosh, NEC PC98, and various Unix workstations. Hsync/Vsync and Csync supported.
- Supports DPMS for monitor power management.

Works with any Graphics Controller

- No special BIOS or software driver required.

TFT Panel Support

- Supports a wide variety of active matrix TFT panels either one or two pixel(s) per clock mode up to SXGA panel resolution.
- Supports all panel interface types (Sync. only, Display Enable only, and Composite) at 4/6/8 bits per pixel up to 16.8 million colors.
- Spatial dithering increases number of colors.
- Programmable slew rate minimizes EMI.

Horizontal and Vertical up-scale engine

- Incoming CRT display resolutions, regardless of their aspect ratios, are expanded to fill the entire flat panel. This full-screen display capability significantly increases image size on the panel and maintains the CRT-like "look and feel."

Independent RGB Offset/Gain and Gamma RAM

- Allows end users to adjust contrast, brightness, color balance, black/white level, and gamma correction.

Host Microcontroller Interface

- Allows the host microcontroller interrupt-driven control of flat panel monitor through robust API (applications programming interface) calls.

OSD Support

- Supports an external OSD controller chip allowing the monitor vendor to maintain a familiar user interface.
- Built-in OSD (On Screen Display) controller with integrated 128-character font ROM.

Built-in High Speed Clock Recovery Circuit

- Generates clocks for the on-chip ADC and TFT pixel clock.

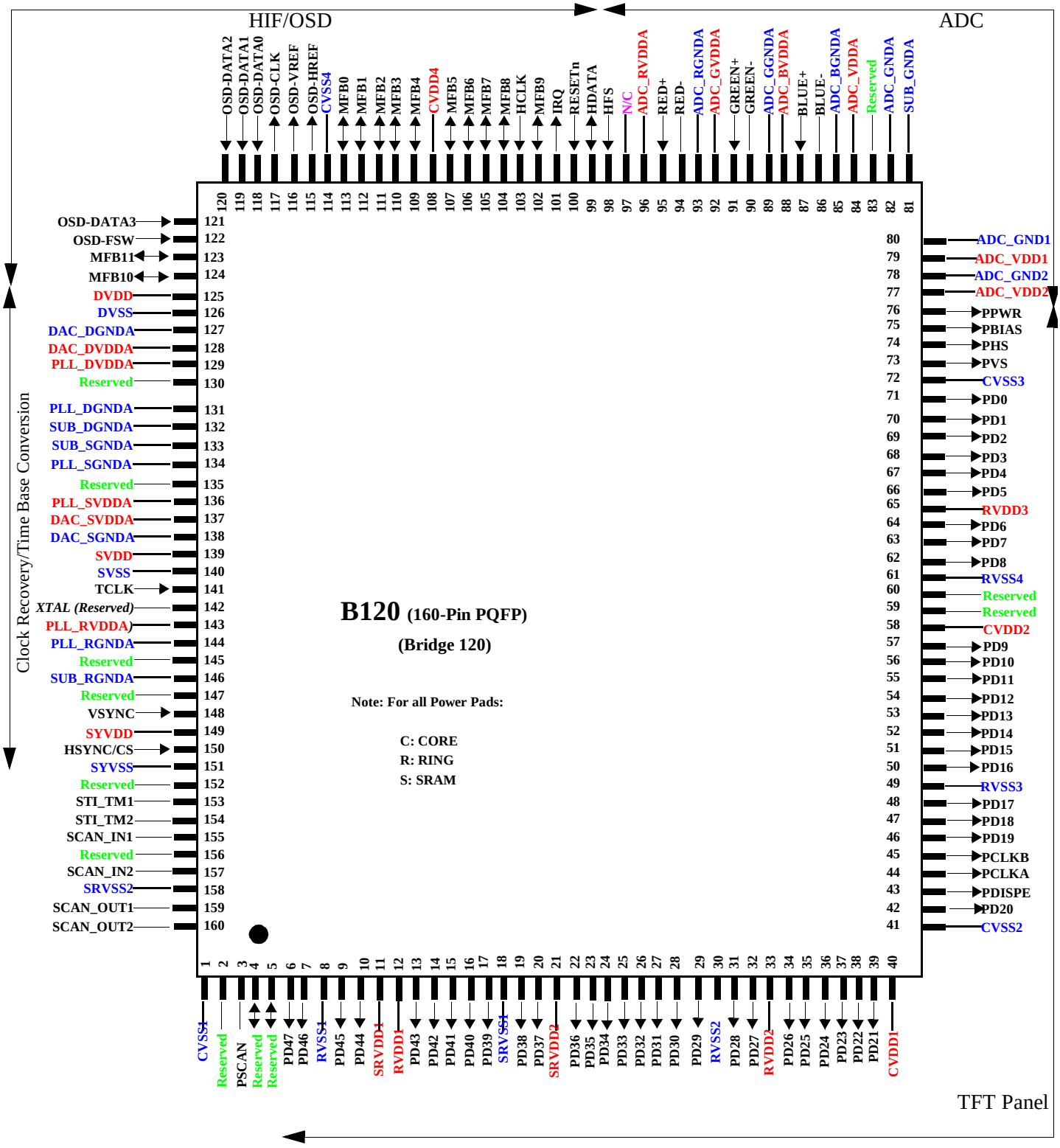
Advanced Test and Reliability Features

- Full Scan Logic for extremely high fault coverage
- Automated PCB assembly testing.

Compact 160 pin PQFP

- Standard, compact QFP package, along with the high level of integration, saves PCB space.

1.3 Pin Diagram



1.4 Pin Description (160-pin PQFP)

Table 1.4.1 Pin Description of the B120

Analog-to-Digital Converter				
Pin	**Name**	**In / Out**	**Drive Current (@10pF)**	**Description**
77	ADC_VDD2			Digital power for ADC encoding logic. Must be bypassed with 0.1 uF capacitor to pin 78 (ADC_GND2)
78	ADC_GND2			Digital GND for ADC encoding logic. Must be directly connected to the digital system ground plane.
79	ADC_VDD1			Digital power for ADC clocking circuit. Must be bypassed with 0.1 uF capacitor to pin 80 (ACD_GND1)
80	ADC_GND1			Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
81	SUB_GNDA			Dedicated pin for substrate guard ring that protects the ADC reference system. Must be directly connected to the analog system ground plane.
82	ADC_GNDA			Analog ground for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be directly connected to analog system ground plane.
84	ADC_VDDA			Analog power for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be bypassed with 0.1 uF capacitor to pin 82 (ADC_GNDA).
83	Reserved			For internal testing purpose only. Do not connect.
85	ADC_BGNDA			Analog ground for the blue channel. Must be directly connected to the analog system ground plane.
88	ADC_BVDDA			Analog power for the blue channel. Must be bypassed with 0.1 uF capacitor to pin 85 (BGNDA).
86	BLUE-	In		Negative analog input for the Blue channel.
87	BLUE+	In		Positive analog input for the Blue channel.
89	ADC_GGNDA			Analog ground for the green channel . Must be directly connected to the analog system ground plane.
92	ADC_GVDDA			Analog power for the green channe. Must be bypassed with 0.1 uF capacitor to pin 89 (ADC_GGNDA).
90	GREEN-	In		Negative analog input for the Green channel.
91	GREEN+	In		Positive analog input for the Green channel.
93	ADC_RGNDA			Analog ground for the red channel. Must be directly connected to the analog system ground plane.
96	ADC_RVDDA			Analog power for the red channel. Must be bypassed with 0.1 uF capacitor to pin 93 (ADC_RGNDA).
94	RED-	In		Negative analog input for the Red channel.
95	RED+	In		Positive analog input for the Red channel.

Host Interface (HIF) / External On-Screen Display				
Pin	**Name**	**In / Out**	**Drive Current (@10pF)**	**Description**
98	HFS	in		Host Frame Sync. Frames the packet on the serial channel.
103	HCLK	in		Clock signal input for the 3-wire serial communication.
99	HDATA	in/out	8 mA	Data signal for the 3-wire serial communication
100	RESETn	in		Resets the B120 chip to a known state when low.
101	IRQ	out	4 mA	Interrupt request output
115	OSD-HREF	out	4 mA	HSYNC output for an external OSD controller chip.
116	OSD-VREF	out	4 mA	VSYNC output for an external OSD controller chip.
117	OSD-Clk	out	4 mA	Clock output for an external OSD controller chip.
118	OSD-Data0	in		Data input 0 from an external OSD controller.
119	OSD-Data1	in		Data input 1 from an external OSD controller.
120	OSD-Data2	in		Data input 2 from an external OSD controller.
121	OSD-Data3	in		Data input 3 from an external OSD controller.
122	OSD-FSW	in		External OSD window display enable. Displays data from external OSD controller when high.
123	MFB11	in/out	8 mA	Multi-Function Bus 11. One of twelve multi-function signals MFB[11:0].
124	MFB10	in/out	8 mA	Multi-Function Bus 10. One of twelve multi-function signals MFB[11:0].
102	MFB9	in/out	8 mA	Multi-Function Bus 9. One of twelve multi-function signals MFB[11:0].
104	MFB8	in/out	8 mA	Multi-Function Bus 8. One of twelve multi-function signals MFB[11:0].
105	MFB7	in/out	8 mA	Multi-Function Bus 7. One of twelve multi-function signals MFB[11:0].
106	MFB6	in/out	8 mA	Multi-Function Bus 6. One of twelve multi-function signals MFB[11:0].
107	MFB5	in/out	8 mA	Multi-Function Bus 5. One of twelve multi-function signals MFB[11:0].
109	MFB4	in/out	8 mA	Multi-Function Bus 4. One of twelve multi-function signals MFB[11:0].
110	MFB3	in/out	8 mA	Multi-Function Bus 3. One of twelve multi-function signals MFB[11:0].
111	MFB2	in/out	8 mA	Multi-Function Bus 2. One of twelve multi-function signals MFB[11:0].
112	MFB1	in/out	8 mA	Multi-Function Bus 1. One of twelve multi-function signals MFB[11:0].
113	MFB0	in/out	8 mA	Multi-Function Bus 0. One of twelve multi-function signals MFB[11:0].

Clock Recovery / Time Base Conversion				
Pin	**Name**	**In / Out**	**Drive Current (@10pF)**	**Description**
125	DVDD			Digital power for Destination DDS (direct digital synthesizer). Must be bypassed with a 0.1 uF capacitor to digital ground plane.
127	DAC_DGNDA			Analog ground for Destination DDS DAC. Must be directly connected to the analog system ground plane.
128	DAC_DVDDA			Analog power for Destination DDS DAC. Must be bypassed with a 0.1 uF capacitor to pin 127 (DAC_DGNDA)
129	PLL_DVDDA			Analog power for the Destination DDS PLL. Must be bypassed with a 0.1 uF capacitor to pin 131 (PLL_DGNDA)
130	Reserved			For testing purposes only. Do not connect.
131	PLL_DGNDA			Analog ground for the Destination DDS PLL. Must be directly connected to the analog system ground plane.
132	SUB_DGNDA			Dedicated pin for the substrate guard ring that protects the Destination DDS. Must be directly connected to the analog system ground plane.
133	SUB_SGNDA			Dedicated pin for the substrate guard ring that protects the Source DDS. Must be directly connected to the analog system ground plane.
134	PLL_SGNDA			Analog ground for the Source DDS PLL. Must be directly connected to the analog system ground.
135	Reserved			For testing purposes only. Do not connect.
136	PLL_SVDDA			Analog power for the Source DDS PLL. Must be bypassed with a 0.1 uF capacitor to pin 134 (PLL_SGNDA)
137	DAC_SVDDA			Analog power for the Source DDS DAC. Must be bypassed with a 0.1 uF capacitor to pin 138 (DAC_SGNDA)
138	DAC_SGNDA			Analog ground for the Source DDS DAC. Must be directly connected to the analog system ground.
139	SVDD			Digital power for the Source DDS. Must be bypassed with a 0.1 uF capacitor to digital ground plane.
141	TCLK	In		Reference clock (TCLK) input from the 50 Mhz crystal oscillator.
142	XTAL	Out		Not used. This pin must be connected to pin 144 (PLL_RGNDA)
143	PLL_RVDDA			Analog power for the Reference DDS PLL. Must be bypassed with a 0.1 uF capacitor to pin 144 (PLL_RGNDA)
144	PLL_RGNDA			Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
145	Reserved			For testing purposes only. Do not connect.
146	SUB_RGNDA			Dedicated pin for the substrate guard ring that protects the Reference DDS. Must be directly connected to the analog system ground plane.
148	VSYNC	In		CRT Vsync input. TTL Schmitt trigger input.
150	HSYNC/ CSYNC	In		CRT Hsync or CRT composite sync input. TTL Schmitt trigger input.

Drive current of the panel output pins are programmable.

TFT Panel Interface				
Pin	**Name**	**In / Out**	**Drive Current (@10pF)**	**Description**
6	PD47	out	2 mA ~ 20 mA	Panel data output 47
7	PD46	out	2 mA ~ 20 mA	Panel data output 46
9	PD45	out	2 mA ~ 20 mA	Panel data output 45
10	PD44	out	2 mA ~ 20 mA	Panel data output 44
13	PD43	out	2 mA ~ 20 mA	Panel data output 43
14	PD42	out	2 mA ~ 20 mA	Panel data output 42
15	PD41	out	2 mA ~ 20 mA	Panel data output 41
16	PD40	out	2 mA ~ 20 mA	Panel data output 40
17	PD39	out	2 mA ~ 20 mA	Panel data output 39
19	PD38	out	2 mA ~ 20 mA	Panel data output 38
20	PD37	out	2 mA ~ 20 mA	Panel data output 37
22	PD36	out	2 mA ~ 20 mA	Panel data output 36
23	PD35	out	2 mA ~ 20 mA	Panel data output 35
24	PD34	out	2 mA ~ 20 mA	Panel data output 34
25	PD33	out	2 mA ~ 20 mA	Panel data output 33
26	PD32	out	2 mA ~ 20 mA	Panel data output 32
27	PD31	out	2 mA ~ 20 mA	Panel data output 31
28	PD30	out	2 mA ~ 20 mA	Panel data output 30
29	PD29	out	2 mA ~ 20 mA	Panel data output 29
31	PD28	out	2 mA ~ 20 mA	Panel data output 28
32	PD27	out	2 mA ~ 20 mA	Panel data output 27
34	PD26	out	2 mA ~ 20 mA	Panel data output 26
35	PD25	out	2 mA ~ 20 mA	Panel data output 25
36	PD24	out	2 mA ~ 20 mA	Panel data output 24
37	PD23	out	2 mA ~ 20 mA	Panel data output 23
38	PD22	out	2 mA ~ 20 mA	Panel data output 22
39	PD21	out	2 mA ~ 20 mA	Panel data output 21
42	PD20	out	2 mA ~ 20 mA	Panel data output 20
46	PD19	out	2 mA ~ 20 mA	Panel data output 19
47	PD18	out	2 mA ~ 20 mA	Panel data output 18
48	PD17	out	2 mA ~ 20 mA	Panel data output 17
50	PD16	out	2 mA ~ 20 mA	Panel data output 16
51	PD15	out	2 mA ~ 20 mA	Panel data output 15
52	PD14	out	2 mA ~ 20 mA	Panel data output 14
53	PD13	out	2 mA ~ 20 mA	Panel data output 13
54	PD12	out	2 mA ~ 20 mA	Panel data output 12
55	PD11	out	2 mA ~ 20 mA	Panel data output 11
56	PD10	out	2 mA ~ 20 mA	Panel data output 10
57	PD9	out	2 mA ~ 20 mA	Panel data output 9
62	PD8	out	2 mA ~ 20 mA	Panel data output 8
63	PD7	out	2 mA ~ 20 mA	Panel data output 7

64	PD6	out	2 mA ~ 20 mA	Panel data output 6
66	PD5	out	2 mA ~ 20 mA	Panel data output 5
67	PD4	out	2 mA ~ 20 mA	Panel data output 4
68	PD3	out	2 mA ~ 20 mA	Panel data output 3
69	PD2	out	2 mA ~ 20 mA	Panel data output 2
70	PD1	out	2 mA ~ 20 mA	Panel data output 1
71	PD0	out	2 mA ~ 20 mA	Panel data output 0
43	PDispE	out	2 mA ~ 20 mA	This output provides a panel display enable signal that is active when flat panel data is valid.
74	PHS	out	2 mA ~ 20 mA	This output provides the panel line clock signal.
73	PVS	out	2 mA ~ 20 mA	This output provides the frame start signal.
44	PCLKA	out	2 mA ~ 20 mA	This output is used to drive the flat panel shift clock.
45	PCLKB	out	2 mA ~ 20 mA	Same as PCLKA above. The polarity and the phase of this signal is independently programmable.
75	Pbias	out	8 mA	This output is used to turn on / off the panel bias power or controls back-light.
76	Ppwr	out	8 mA	This output is used to control the power to a flat panel.

Test Pins				
Pin#	Name	In/Out	Drive Current	Description
3	PSCAN	In		Enable automatic PCB assembly test. When this input is pulled high, the automatic PCB assembly test mode is entered. An internal pull-down resistor drives this input low for normal operation.
155	SCAN_IN1	In		Scan input 1 used for automatic PCB assembly testing.
157	SCAN_IN2	In		Scan input 2 used for automatic PCB assembly testing.
159	SCAN_OUT1	Out		Scan output 1 used for automatic PCB assembly testing.
160	SCAN_OUT2	Out		Scan output 2 used for automatic PCB assembly testing.
153	Reserved			
154	Reserved			

Digital VDD / VSS for the Core Circuitry, Host Interface, and Panel/Memory Interface	
Pins	Description
65, 40, 33, 12	PVDD4 ~ PVDD1 for Panel / memory interface. Connect to +3.3V. Needs to be the same voltage as the CVDD's.
149, 108, 58, 21, 11	CVDD6-5, CVDD3-1 for core circuitry. Connect to +3.3V. Needs to be the save voltage as the PVDD's.
158, 151, 140, 126, 114, 72, 61, 49, 41, 30, 18, 8, 1	Digital grounds for core circuitry and panel / memory interface.

1.5 System-level Block Diagrams

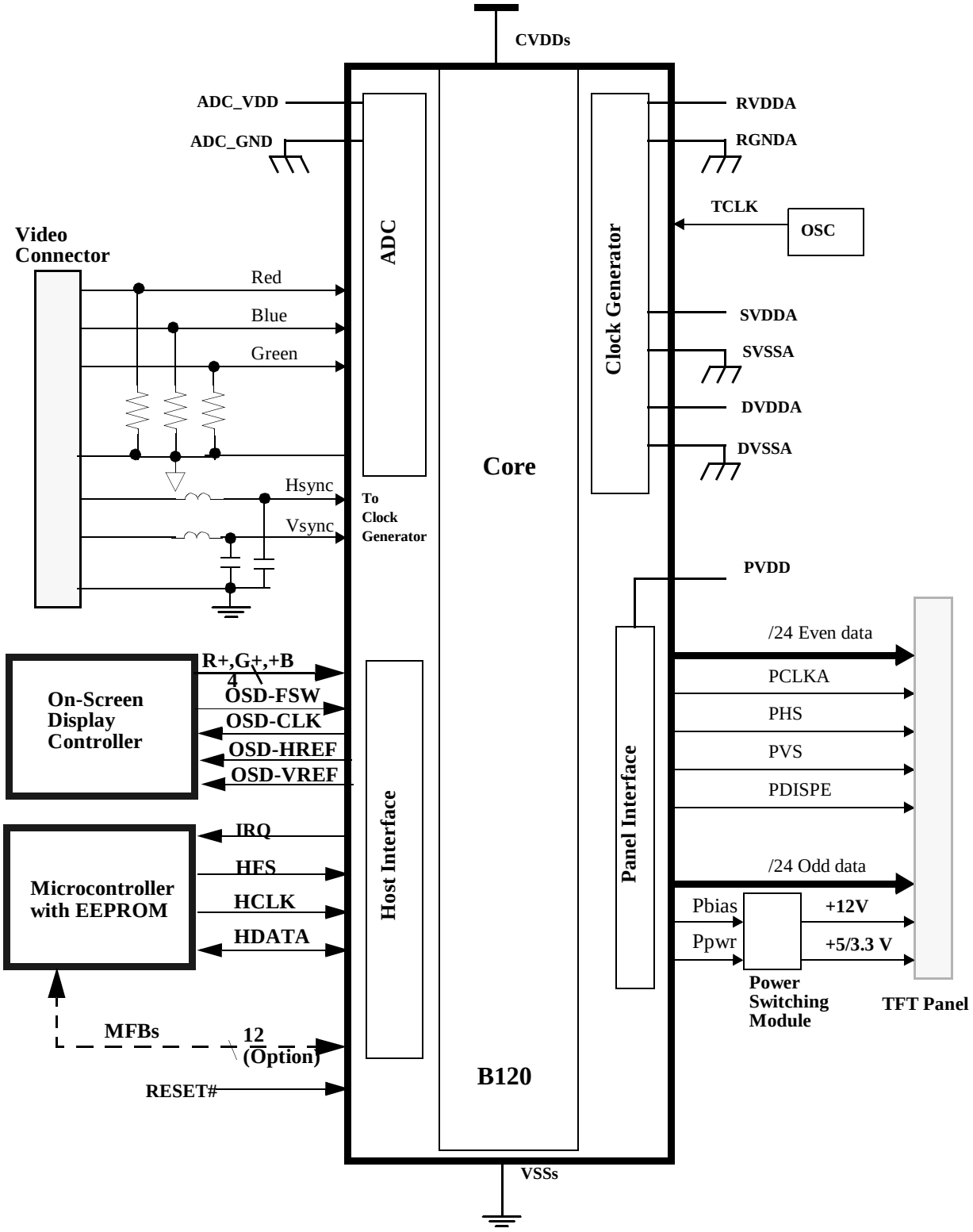


Figure 1.5.1 Typical Stand-alone configuration with External OSD Controller

2. Architectural Description

2.1 Overall Architecture

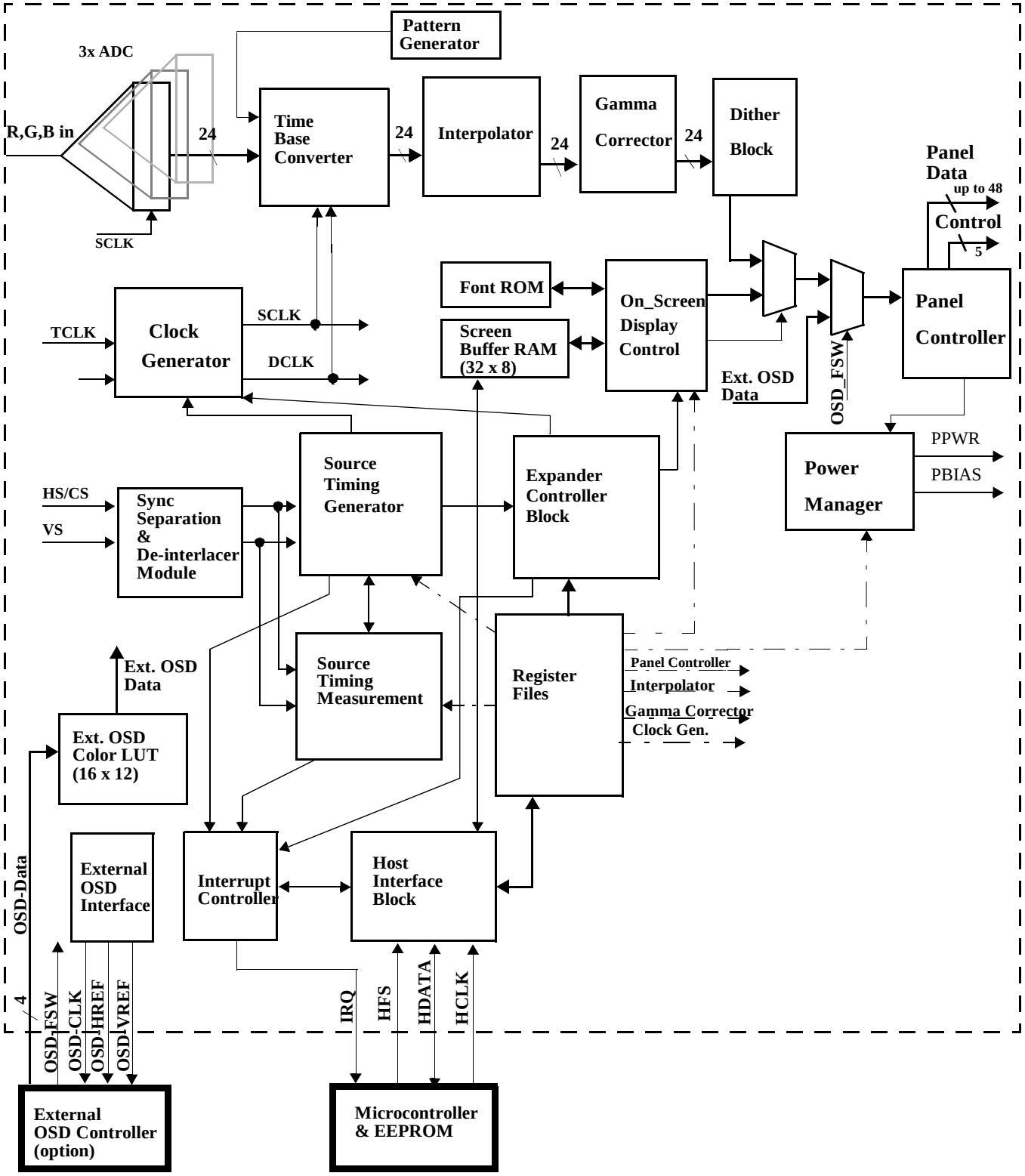


Figure 2.1.1 B120 Block Diagram

Figure 2.1.1 on the previous page is the overall block diagram of the B120 chip.

For the following discussion, refer to Figure 2.1.2 Flow of Source Video Signal

Initialization Upon Power-up

The microcontroller has timing parameters of a panel and various display modes stored in the EPROM/EEPROM.

The panel type and the other configuration options are read during initialization. The panel type and configuration will determine the capabilities of the destination display device (or a TFT LCD panel) which will be used to build the Device Descriptor. The specifications of the panel type selected are read from a serial EEPROM.

The supported video mode table is also read from the serial EEPROM. Timing information in each entry of the mode table will be used to define the Mode Descriptor.

Source Timing Measurement

When it receives the active CRT signal (R, G, B, and Sync. signals), the Source Timing Measurement unit starts measuring the horizontal and vertical timing of the incoming signal using the Sync. signals and the TCLKi as reference. Horizontal measurement occurs by measuring a minimum and maximum value for each parameter to account for TCLKi sampling granularity. Vertical parameters are measured in terms of horizontal lines. Minimum and maximum measurements are not needed in this case. Once the input timing is measured by the hardware, the Source Timing Descriptor is created and used to make several decision under program control.

Stand-Alone Mode

If the source timing is invalid due to one of the sync signals missing or being out of range, the firmware puts the chip in a stand-alone mode. The timing characteristics of the source are ignored in Stand-Alone mode. The panel will be driven at the maximum allowable specifications as defined in the Device Descriptor. Also, instead of using the source video data, the internal static test patterns will be displayed on the panel.

The B120 will remain in Stand-Alone mode until a valid source timing measurement is obtained or a DPMS state is entered under program control.

Determining the Source Display Mode

If the Source Timing Descriptor contains valid timing, it is compared to the modes listed in the mode table by the micro-controller. The micro-controller will select the mode that most closely matches the measured timing. If an exact match occurs, all previously adjusted screen position and size settings will be restored. If an exact match does not occur, user input from a front panel keypad on the monitor will adjust the screen position and size. These settings will be saved in the serial EEPROM so that when the same video mode timing is acquired again in the future, no additional front panel keypad entry will be required.

Generating Source Timing

Information from the Mode Descriptor, Device Descriptor, and Source Timing Descriptor are used to create a Source Descriptor. The B120 will re-generate the source video timing based on this information. From this, the video source display size, position and ADC sampling clock are determined. They are used by the ADC unit to digitize the incoming analog video data.

If the source display size is smaller than the panel size, the B120 will expand the source data to full-panel resolution. Interpolation may be performed to improve the display quality of the expanded image. This operation occurs without the use of external memory. As a result, the frame rate of the panel will always be the same as the frame rate of the source video.

.

Table 2.1.1 B120 Status in Various Source Display Mode / LCD Type Conditions

Condition	Result
Input source resolution is smaller than destination panel size. **For example, source pixel rate is 50-MHz SVGA and panel size is XGA.**	**Input source data is displayed on the panel. Called Normal Mode.** **Time base conversion occurs and the source is expanded and interpolated to fill the entire panel. Called Expansion operation in Normal Mode.** **Destination (Panel) will have a higher pixel rate than the source. However, the destination and the source will have the same vertical refresh rate(72 Hz).**
Input source resolution is same as destination panel size. **For example, source pixel rate is 75-MHz XGA and panel size is XGA**	**Input source data is displayed on the panel. Called Normal Mode.** **Since input resolution equals output resolution, no Expansion is required. Called Native operation in Normal Mode.** **Destination pixel rate and frame rate will be the same as source.**
Input source resolution larger than destination panel size. **For example, source pixel rate is 65 MHz XGA and panel size is SVGA.**	**The firmware will either turn off the panel or display a static pattern from the on-chip pattern generator of the B120 chip.** **The former is called Sleep Mode and the latter is Stand-alone Mode.**

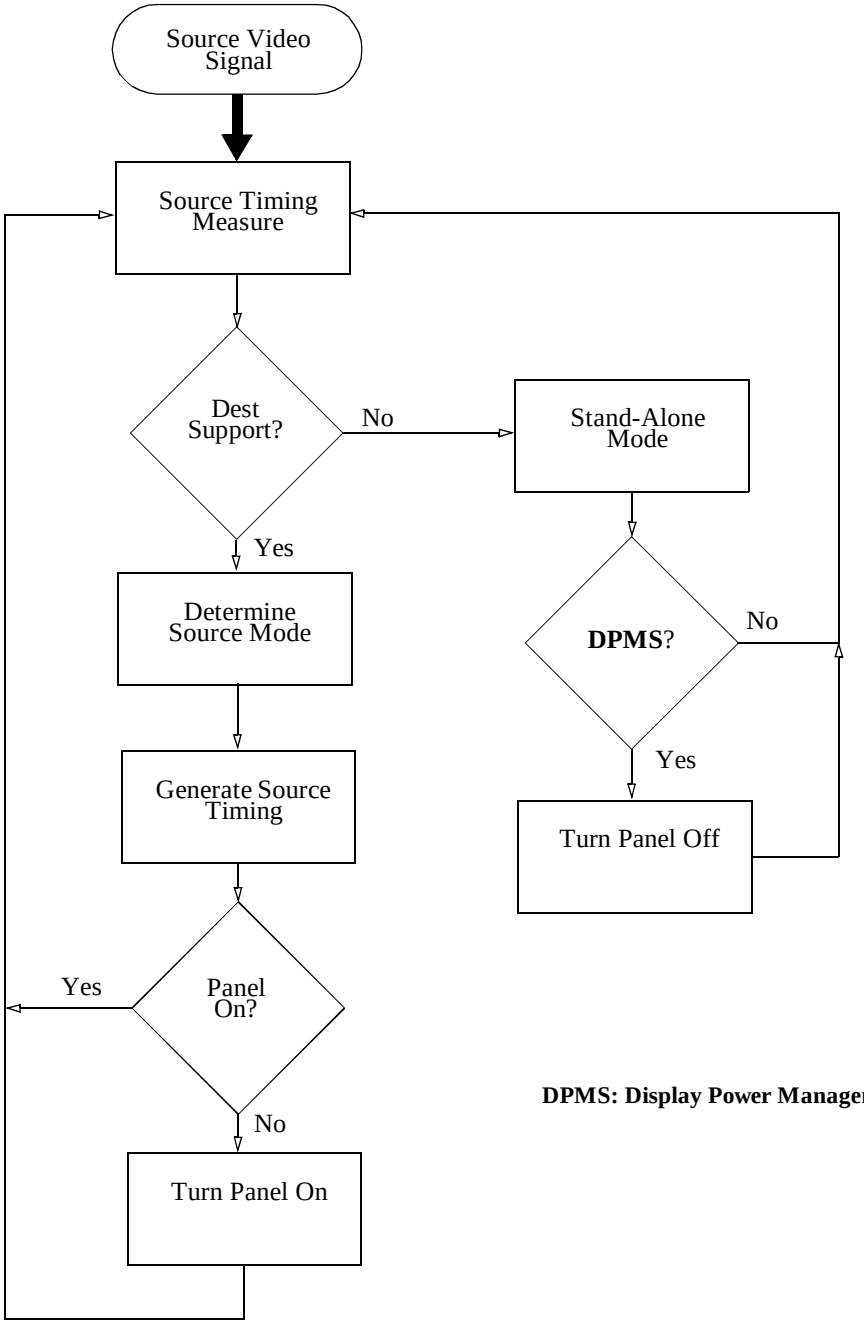
Image Processing

The B120 contains three independent lookup tables for gamma correction which are programmable through the host interface port. In addition, panel data dithering is available to support panels with data width less than 8 bits per pixel.

Programming the B120

Implementations using the B120 will rely on an Application Programming Interface(API) to program the B120. The API is a library of routines that will perform all the low level register and bit manipulations providing a layer of abstraction so that applications written for one family of Paradise products will be easily supported on others. In addition, each descriptor (Mode, Source timing, Device, Source and Destination) be created with a single call.

Refer to the API reference manual for more details.



DPMS: Display Power Management Signaling

Figure 2.1.2 B120 Control Flow Chart

2.2 CRT Interface

2.2.1 Pin Connection

The CRT signals are to be connected to the B120 chip as shown in Table 2.2.1 and Table 2.2.2.

Table 2.2.1 Pin Connection for CRT Connector with HSync/Vsync

B120 Pin Name (Pin Number)	CRT Signal Name	Polarity
Red+(#95)	Red	
Red- (#94)	N/A (Tie to Analog GND for Red on the board)	
Green+ (#91)	Green	
Green- (+90)	N/A (Tie to Analog GND for Green on the board)	
Blue+ (#87)	Blue	
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)	
HSYNC/CS (#150)	Horizontal Sync	Programmable
VSYNC (#148)	Vertical Sync	Programmable

Table 2.2.2 Pin Connection for CRT Connector with Composite Sync

B120 Pin Name (Pin Number)	CRT Signal Name
Red+ (#95)	Red
Red- (#94)	N/A (Tie to Analog GND for Red on the board)
Green+ (#91)	Green
Green- (#90)	N/A (Tie to Analog GND for Green on the board)
Blue+ (#87)	Blue
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)
HSYNC/CS (#150)	Composite Sync (TTL, no sync during vertical sync period)

2.2.2 Analog-to-Digital Converters

The B120 chip has three ADC's (analog-to-digital converters), one for each color (red, green, and blue). The characteristics of the ADC's is summarized in Table 2.2.3.

Table 2.2.3 ADC Characteristics

	MIN	TYP	MAX	NOTE
RGB Track & Hold Amplifiers				
Band Width User Controlled bw<3:2>= 11 bw<3:2>= 10 bw<3:2>= 01 bw<3:2>= 00		 160 MHz 100 MHz 85 MHz 60 MHz		
Settling Time to 1/2 %		8.5 ns		Full Scale Input = 0.75V, BW=160MHz (*)
Full Scale Adjust Range @ R,G,B Inputs	0.45 V		0.95 V	
Full Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output (**)
Zero Scale Adjust Range				Guaranteed to remove all Internal Offsets
Zero Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output
ADC + RGB Track & Hold Amplifiers				
Sampling Frequency (fs)	20 MHz		110 MHz	
DNL			+/- 0.9 LSB	fs = 80 MHz, Guranteed no Missing Codes
INL		+/- 1.5 LSB		fs = 80 MHz
Channel to Channel Matching		+/- 0.5 LSB		
Effective Number of Bits (ENOB)		7 Bits		fin = 1 MHz, fs = 80 MHz Vin= -1 db below full scale = 0.75V
Power Dissipation		400 mW		fs = 110 MHz, Vdd = 3.3V
Shut Down Current			100uA	

(*) Guaranteed by design (**) Independent of full scale R,G,B input

NOTE 1: When the sampling frequency is 120 MHz.

The ADC of the B120 uses a differential input. The built-in pre-amplifier converts single ended RGB inputs from a video source into differential signal pairs, Red+/Red-, Green+/Green-, and Blue+/Blue-. (On the B120-based printed circuit board, Red-/Green-/Blue- pins must be tied to analog ground plane.) The 0V input is converted to -1V differential signal while the full-scale voltage (0.6V ~ 0.9V) is converted to +1V. The zero-level (or the black level) and the full-scale (or the white level) of each color can be adjusted independently.

The offset is adjusted in 16 / 256 steps (4-bit value for Rev AA silicon, 8 bits for Rev BB) in the following manner:

Supply black input to the Red+/Green+/Blue+ pins of the B120 chip. If this 0V input is not converted to -1V, then offset adjustment is needed. When the voltage is lower than -1V, then the underflow bit of the B120 gets set. In this case, add a positive offset till this underflow condition is eliminated. In the meantime, when the voltage is equal to or higher than -1V, the underflow bit does not get set. In this condition, reduce the offset till underflow occurs. Then increase the offset value by one.

As far as the full-scale, it can be adjusted in 16 / 512 steps (4-bit value for Rev AA silicon, 9 bits for Rev BB) as follows:

Supply white input to the Red+/Green+/Blue+ pins of the B120 chip. If this full-scale input is not converted to +1V, In this case, increase the gain value till the overflow condition is eliminated. In the meantime, when the voltage is equal to or higher than +1V, the overflow bit does not get set. In this condition, reduce the gain till overflow occurs. Then increase the gain value by one.

2.2.3 Sync. Signal Support

The type (HSync/VSync vs. Composite Sync) and the polarity of the sync signals are automatically detected by the B120 chip. The monitor application program requests this information using API calls and uses the information for source image timing determination as described in Section 2.1. The change in Sync. signal (polarity and timing) is also to be detected by the B120 chip and is communicated to the monitor application program via an interrupt.

The only type of composite sync. supported by the B120 chip is TTL composite sync. that has no composite sync. pulse during the vertical sync period.

2.2.4 Display Mode Support

The B120 can support standard VGA/VESA/Macintosh display modes shown in Table 2.2.4 depending on an LCD panel specification. By default, all data input is expanded to full-panel-screen resolution.

Note that the display mode support is dependent on the specification of the TFT LCD panel used in a given flat-panel monitor as explained in Table 2.2.5 and Table 2.2.6. As long as the conditions in Table 2.2.5 and Table 2.2.6 are met, the B120 can support higher (or lower) vertical/horizontal/pixel frequencies than those values shown in Table 2.2.4.

Table 2.2.4 Display Mode Table on an SXGA TFT LCD Panel

Resolution	Pixel Frequency (MHz)	Horizontal Frequency (kHz)	Vertical Frequency (Hz)	Standard
360 x 400	14	31.25	70	VGA
720 x 400	28	31.25	70	VGA
320 x 200	12.5	31.25	70	VGA
640 x 200	25	31.25	70	VGA
640 x 350	25	31.25	70	VGA
640 x 480	25	37.5	60	VGA/VESA
	30.24	35.00	67.00	Macintosh
	31.5	37.9	72	VESA
	31.5	37.5	75	VESA
800 x 600	36.0	35.2	56	VESA
	40.0	37.9	60	VESA
	50.0	48.1	72	VESA
	49.5	46.7	75	VESA
832 x 624	57.29	49.80	74.60	Macintosh
1024 x 768	65.0	48.4	60	VESA
	75.0	56.5	70	VESA
	78.8	60.0	75	VESA
	80.00	60.24	75.00	Macintosh
1152 x 864	80.00	54.35	60	VESA
	94.2	64.00	70	VESA
	108.00	67.50	75.0	VESA
1280 x 1024	110.0	60.31	60	VESA

As stated earlier, the display mode support depends on the specification of the panel. The parameters that affect the display-mode support are listed in Table 2.2.5 and Table 2.2.6.

Table 2.2.5 LCD Parameter Requirements for Display Mode Support (1)

The following table is applicable when a display mode resolution is smaller than a panel resolution,

LCD Parameter	Requirement
Max. panel clock (pixel clock) frequency	Must be higher than the pixel-clock frequency of a given display mode.
Min. hor. total (in pixels) x Min. pixel clock cycle	Must be shorter than the horizontal period (1/Hor. Freq.) of a given display mode.
Min./max. vertical total (in lines)	Min./max. vertical total must cover the value calculated from the following equation: Displayed vertical size on LCD x source vertical total / source vertical size where source vertical total and source vertical size are vertical total and vertical display size of a given display mode.
Horizontal/vertical display sizes	The vertical display size must be bigger than that of a given display mode.

Table 2.2.6 LCD Parameter Requirements for Display Mode Support (2)

The following table is applicable when a display mode resolution is the same as the panel resolution.

LCD Parameter	Requirement
Max. panel clock (pixel clock) frequency	Must be higher than the pixel-clock frequency of a given display mode.
Min. and max. horizontal total (in pixels)	The min./max. horizontal total must cover the horizontal total of a given display mode.
Min. and max. vertical total (in lines)	The min./max. vertical total must cover the vertical total of a given display mode.

As far as the color depth is concerned, refer to Table 2.2.7 below and Figure 2.1.1 on page 12.

Table 2.2.7 Color Depth

Signal	Color Depth
Data Input to ADC	Up to 8 bits/color
ADC output Time Base Converter	8 bits/color
Interpolator output	8 bits/color
Gamma (LUT) output to Dither Block	8 bits/color
Panel interface output	Panel color depth dependent *1

NOTE 1: When data color depth is deeper than panel color depth, dithering may be enabled (programming option).

2.3 Panel Interface

The B120 chip interfaces directly with all of today's commonly used active matrix flat panels with 640x480, 800x600, 1024x768 and 1280x1024 resolutions. The resolution and the aspect ratio are NOT limited to specific values.

2.3.1 Pin Connection

The pin connection between various types of LCD panels and the B120 is listed in Table 2.3.1.

Table 2.3.1 Panel Pin Connection (E:Even (first pixel), O:Odd (second pixel))

B120 Pin Name	Pin No.	TFT (one pixel/clock) 8 bit	6 bit	4 bit	TFT (two pixel/clock) 8 bit	6 bit
PD35	23				OB7	OB5
PD34	24				OB6	OB4
PD33	25				OB5	OB3
PD32	26				OB4	OB2
PD31	27				OB3	OB1
PD30	28				OB2	OB0
PD29	29				OG7	OG5
PD28	31				OG6	OG4
PD27	32				OG5	OG3
PD26	34				OG4	OG2
PD25	35				OG3	OG1
PD24	36				OG2	OG0
PD23	37				OR7	OR5
PD22	38				OR6	OR4
PD21	39				OR5	OR3
PD20	42				OR4	OR2
PD19	46				OR3	OR1
PD18	47				OR2	OR0
PD17	48	B7	B5	B3	EB7	EB5
PD16	50	B6	B4	B2	EB6	EB4
PD15	51	B5	B3	B1	EB5	EB3
PD14	52	B4	B2	B0	EB4	EB2
PD13	53	B3	B1		EB3	EB1
PD12	54	B2	B0		EB2	EB0
PD11	55	G7	G5	G3	EG7	EG5
PD10	56	G6	G4	G2	EG6	EG4
PD9	57	G5	G3	G1	EG5	EG3
PD8	62	G4	G2	G0	EG4	EG2
PD7	63	G3	G1		EG3	EG1
PD6	64	G2	G0		EG2	EG0
PD5	66	R7	R5	R3	ER7	ER5
PD4	67	R6	R4	R2	ER6	ER4
PD3	68	R5	R3	R1	ER5	ER3
PD2	69	R4	R2	R0	ER4	ER2
PD1	70	R3	R1		ER3	ER1
PD0	72	R2	R0		ER2	ER0

Table 2.3.1 Panel Pin Connection (E:Even (first pixel), O:Odd (second pixel))

B120 Pin Name	Pin No.	TFT (one pixel/clock) 8 bit	6 bit	4 bit	TFT (two pixel/clock) 8 bit	6 bit
PDispE	43	PDE	PDE	PDE	PDE	PDE
PHsync	74	PHs	PHs	PHs	PHs	PHs
PVsync	73	PVs	PVs	PVs	PVs	PVs
PCLKA	44	CLK	CLK	CLK	CLKA	CLKA
PCLKB	45				(CLKB)	(CLKB)
PD47	6				OB1	
PD46	7				OB0	
PD45	9				OG1	
PD44	10				OG0	
PD43	13				OR1	
PD42	14				OR0	
PD41	15	B1			EB1	
PD40	16	B0			EB0	
PD39	17	G1			EG1	
PD38	19	G0			EG0	
PD37	20	R1			ER1	
PD36	22	R0			ER0	
Pbias	75	switched BLVDD (+12V)				
Ppower	76	switched PVDD (+5V)				

If the color depth of the data is larger than the panel color depth, dithering operation may be enabled. This dithering operation is also an API programming option.

2.3.2 TFT Panel Interface Timing Specification

The TFT panel interface timing parameters of the B120 chip are listed in the table below. Refer to three timing diagrams of Figure 2.3.1 and Figure 2.3.2 for the timing parameter definition.

Table 2.3.2 B120 TFT Panel Interface Timing

(numbers in [ ] are for two pixels/clock mode)

Signal Name			min	typical	max	unit *1
PVS	period	t1	0		2048	lines
				16.67	-	ms
	frequency			60	-	Hz
	front porch	t2	0		2048	lines
	back porch	t3	0		2048	lines
	pulse width	t4	0		2048	lines
	PDispE	t5	0	panel height	2048	lines
	Disp. start from VS	t6	0		2048	lines
	PVS set up to PHS	t18	1		2048	pclk
	PVS hold from PHS	t19	1		2048	pclk
PHS	period	t7	0		2048 [1024]	pclk
	front porch	t8	0		2048	pclk
	back porch	t9	0		2048	pclk
	pulse width	t10	0		2048	pclk
	PDispE	t11	0	panel width	2048 [1024]	pclk
	Disp. start from HS	t12	0		2048	pclk
PclkA, PclkB *4	Frequency	t13			120 [60]	MHz
	Clock (H) *2	t14	DCLK/2 - 3 [DCLK - 3]		DCLK/2 - 2 [DCLK - 2]	ns
	Clock (L) *2	t15	DCLK/2 - 3 [DCLK - 3]		DCLK/2 - 2 [DCLK - 2]	ns
	type		-	one pels/clock [two pels/clock[	-	
Data	set up *3	t16	DCLK/2 - 5 [(DCLK - 5]		DCLK/2 - 2 [DCLK - 2]	ns
	hold *3	t17	DCLK/2 - 5 [(DCLK - 5]		DCLK/2 - 2 [DCLK - 2]	ns
	width		3 bits	18bits [36 bits]	24bits [48bits]	bits/pixel

NOTES

***1:The pclk is the panel shift clock.**

***2: The DCLK stands for Destination Clock (DCLK) period. is equal to:**

- pclk period. in one pixel/clock mode,

- twice the pclk period in two pixels/clock mode.

The drive current of the panel interface signals is programmable as shown in Table 1.4.1 on page 6. The drive current is to be programmed through the API upon the chip initialization. Output current is programmable from 2 mA to 20 mA in increments of 2 mA. Drive strength should be programmed to match the load presented by the cable and input of the panel. Values shown are based on a loading of 20 pF and a drive strength of 8 mA.

***3: The same setup/hold time spec. to the pclk also applies to the PHS and the PDispE signals. The setup time (t16) and the hold time (t17) listed in this table are for the case in which no clock-to-data skew is added: The PVS/PHS/ PDispE/PData signals are asserted on the rising edge of the Pclk.**

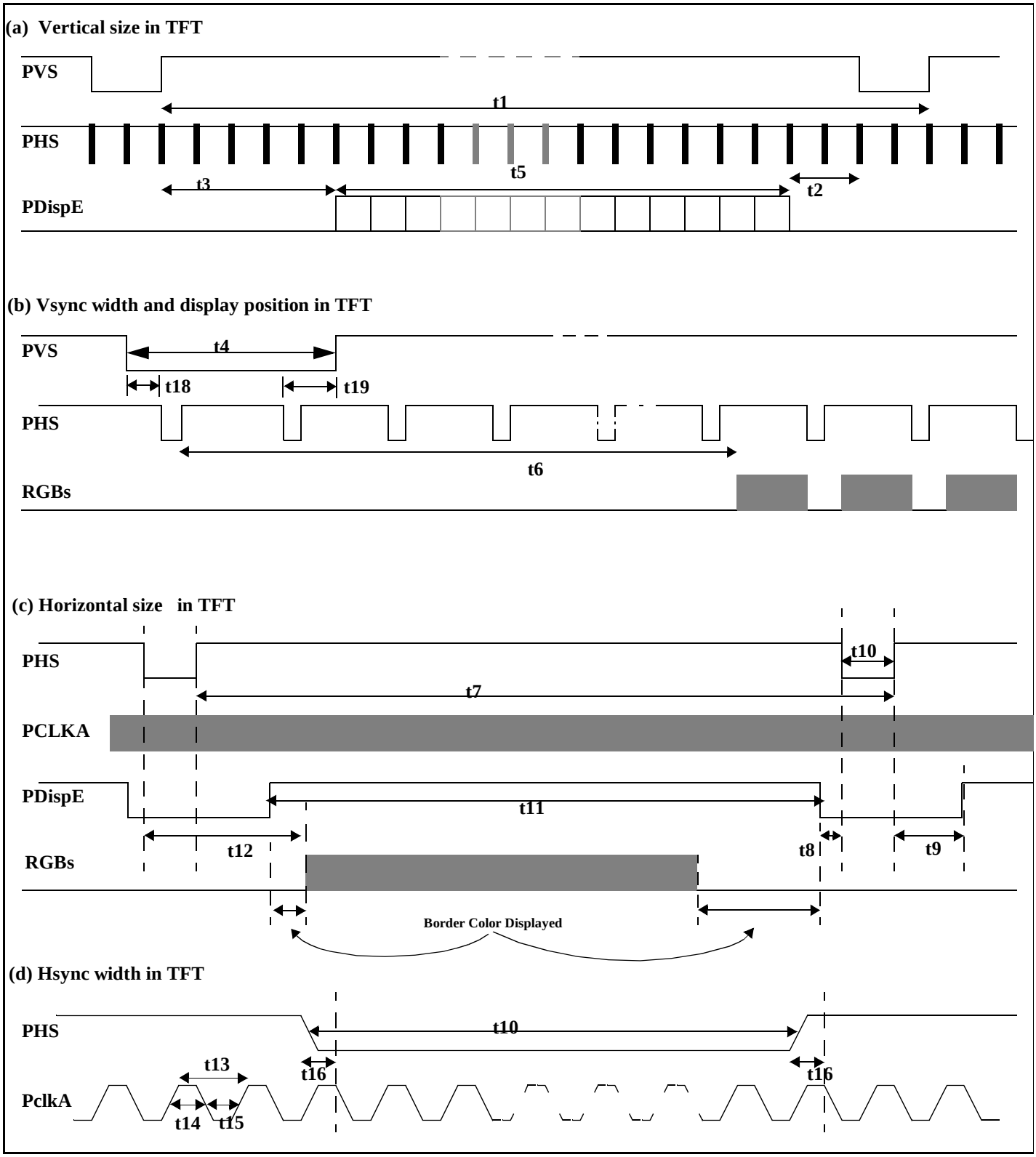
Note that the polarity of the Pclk and its skew are programmable. Clock to Data skew can be adjusted in sixteen 800-ps increments. In combination with the Pclk polarity inversion, the clock-to-data phase can be adjusted in total of 31 steps.

***4: The polarity of the PclkA and the PclkB are independently programmable.**

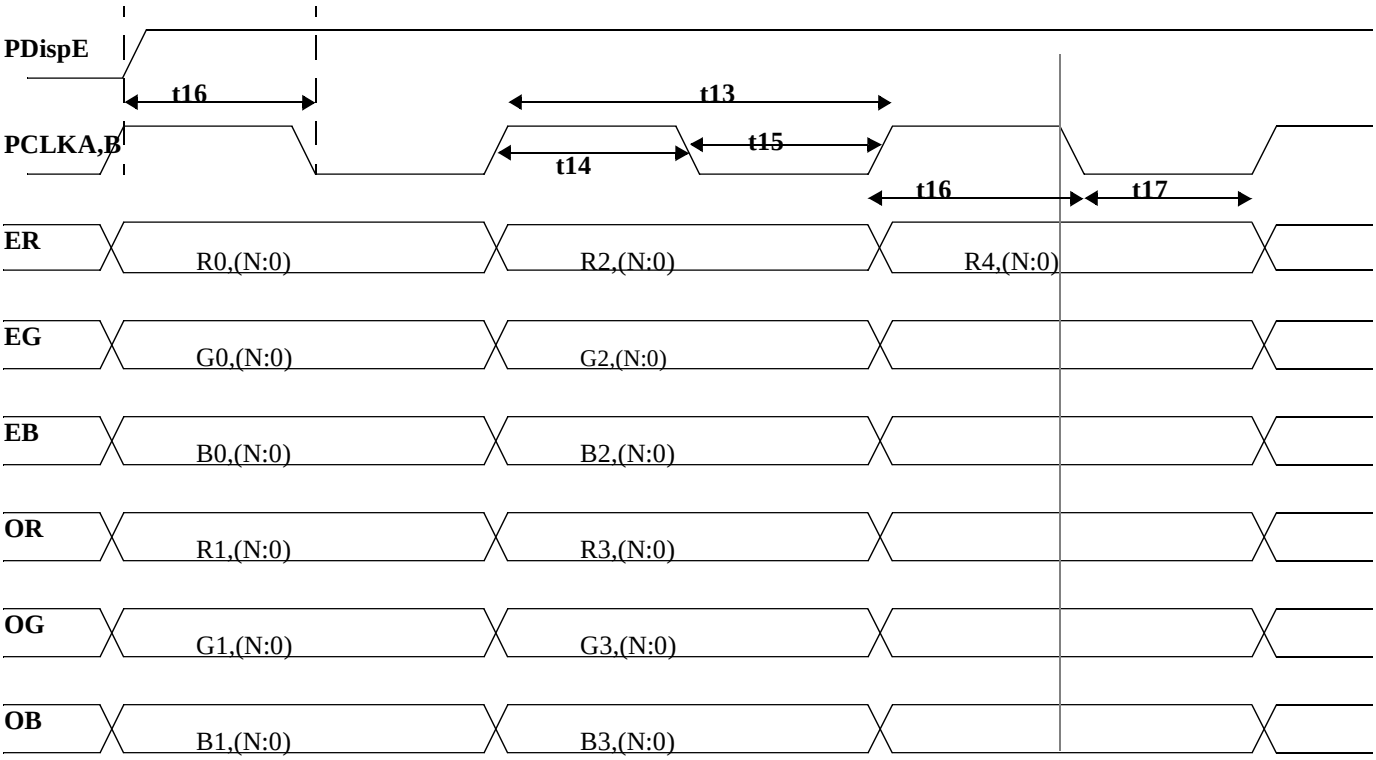
***5: The microcontroller must have all the timing parameters of the panel used for the monitor. The parameters are to be stored in a non-volatile memory. As can be seen from this table, the wide range of timing programmability of the B120 panel interface makes it possible to support various kinds of panels known today:**

One pixel/clock and two pixels/clock; DE-only type, Sync-only type, and composite type; up to 8 bits/color.

Figure 2.3.1 Timing Diagrams of the TFT Panel Interface (one pixel per clock)



(a) Two pixel per clock mode in TFT



(b) One pixel per clock mode in TFT

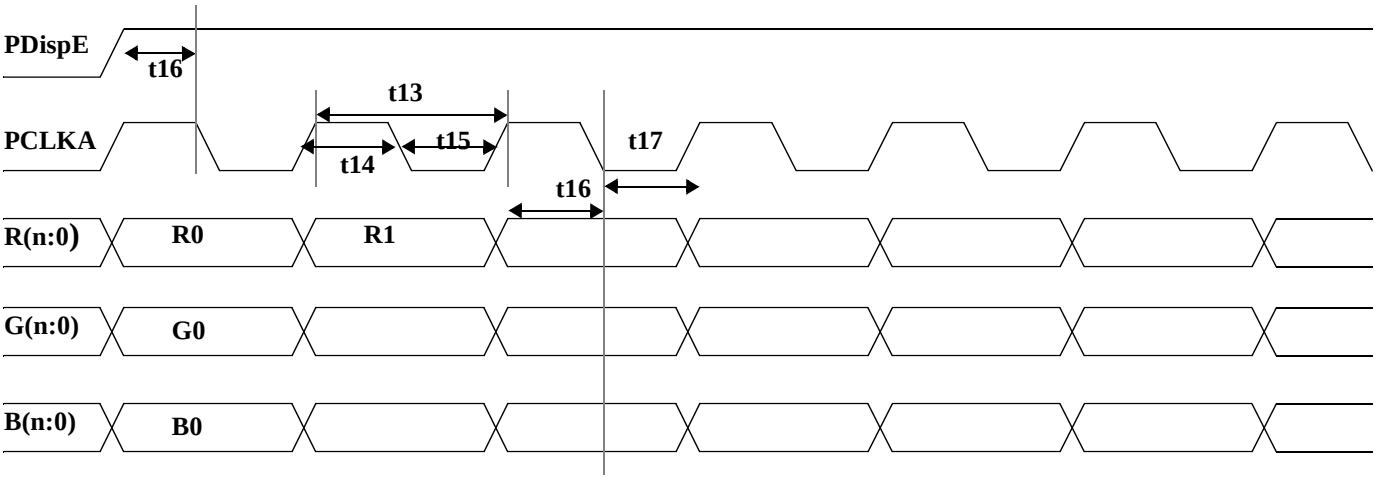


Figure 2.3.2 Data latch timing of the TFT Panel Interface

2.3.3 Power Manager

LCD panels require logic power, panel bias power, and control signals to be sequenced in a specific order. Otherwise, a severe damage may occur and disable the panel permanently.The B120 has a built-in power sequencer, the Power Manager that prevents this kind of damage.

The Power Manager controls the power up/down sequences for LCD panels within the four states described below. Also see the timing diagram, Figure 2.3.3.

State 0 (Power Down)

The Pbias signal and the Ppower signal are low (inactive). The panel controls and data are forced low. This is the final state in power down sequence. PM is kept in state 0 until the panel is enabled.

State 1 (Power On)

Intermediate step 1. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is forced low (inactive).

State 2 (Panel Drive Enabled)

Intermediate step 2. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is active.

State 3 (Panel Fully Active)

Final step in power up sequence with Ppower and Pbias high (active), and the panel interface active. PM is kept in this state until the panel is disabled. The panel can be disabled through either an API call under program control or automatically by the B120 to prevent damage to the panel.

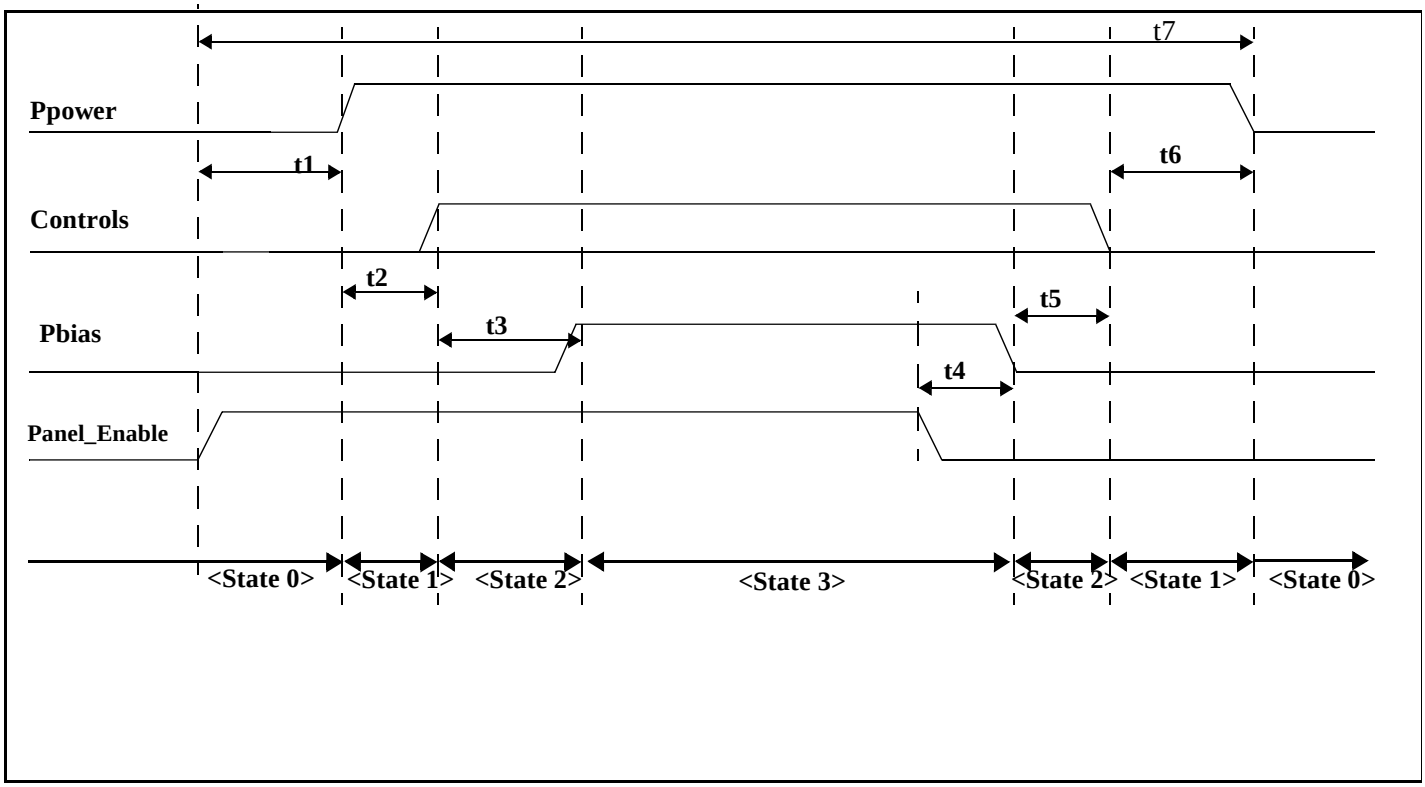


Figure 2.3.3 Panel Power Sequence

All of the six timing parameters (t1 ~ t6) in Figure 2.3.3 are independently programmable from one step to eight steps in length utilizing the API call from the monitor application program.

One-step length is in the range of 511 * X * (TCLKi cycle) or (TCLKi cycle) * 32193 * X where X is any positive integer value equal to or smaller than 256. TCLKi is the reference clock to the gmB120 chip and ranges from 20 MHz to 50 MHz in frequency. This programmability provides enough flexibility to meet a wide range of power sequencing requirements by various panels.

Table 2.3.3 Panel Power Sequence Timing Definition

Timing Symbol	Description
t1	From Power_Enable to Ppower active
t2	Ppower active to all control signals active
t3	All control signals active to Pbias active
t4	From panel on to Pbias inactive
t5	From Pbias inactive to control signals inactive
t6	From control signals inactive to Ppower inactive.
t7	Panel power on/off cycle. The minimum value is the sum of t1 ~ t6.

As is the case with other panel timing parameters, the microcontroller must have the power-sequencing parameters of the panel stored in the EEPROM.

2.3.4 Panel Interface Drive Strength

As mentioned previously, the B120 has programmable output pads for the TFT panel interface. Three groups of panel interface pads (panel clock, data, and control) have independent control and are programmed using API calls. See the API reference manual for details.

Table 2.3.4 Panel Interface Pad Drive Strength

Value (4 bits)	Drive Strength in mA
0	Outputs are in tri-state condition
1	2 mA
2	4 mA
3, 4	6 mA
5, 8	8 mA
6, 9	10 mA
7, 10	12 mA
11, 12	14 mA
13	16 mA
14	18 mA
15	20 mA

2.4 Host Interface

2.4.1 Pin Connection

The host microcontroller of the B120 consists of three signal for serial communication and one IRQ (interrupt request signal). In addition, the B120 has a reset pin that sets the chip to a known state when the pin is pulled low. Those signals are listed in Table 2.4.1.

Table 2.4.1 Five Signals of the B120 Host Interface

Signal Name (Pin Number)	Description
HFS (#98)	**Host Frame Sync. that enables the serial communication when driven high by the microcontroller. The B120 chip has an internal pull-down resistor on chip. Thus, the default state of this signal is low.**
HCLK (#103)	**Serial clock driven by the microcontroller in the write operation. May be connected to an external pull-up resistor.**
HDATA (#99)	**Serial data driven:** **- by the microcontroller in the write operation,** **- by the B120 in the read operation.** **May be connected to an external pull-up resistor.**
IRQ (#102)	**IRQ pin driven by the B120 chip. The polarity is programmable.**
RESETn (#100)	**Sets the chip to a known state when pulled low. Must be low for at least 50 ns,**

The B120 chip has an on-chip pull-down resistor in the HFS input pad. No external pull-up is required. The signal stays low until driven high by the microcontroller.

As for the RESETn, this signal must be low for at least 100 ns after the CVDD has become stable (between +3.15V and +3.45V) to reset the chip to a known state.

2.4.2 Serial Communication Protocol

In the serial communication between the microcontroller and the B120, the microcontroller always acts as an initiator while the B120 is always the target. The following timing diagram describes the protocol of the serial channel of the B120 chip.

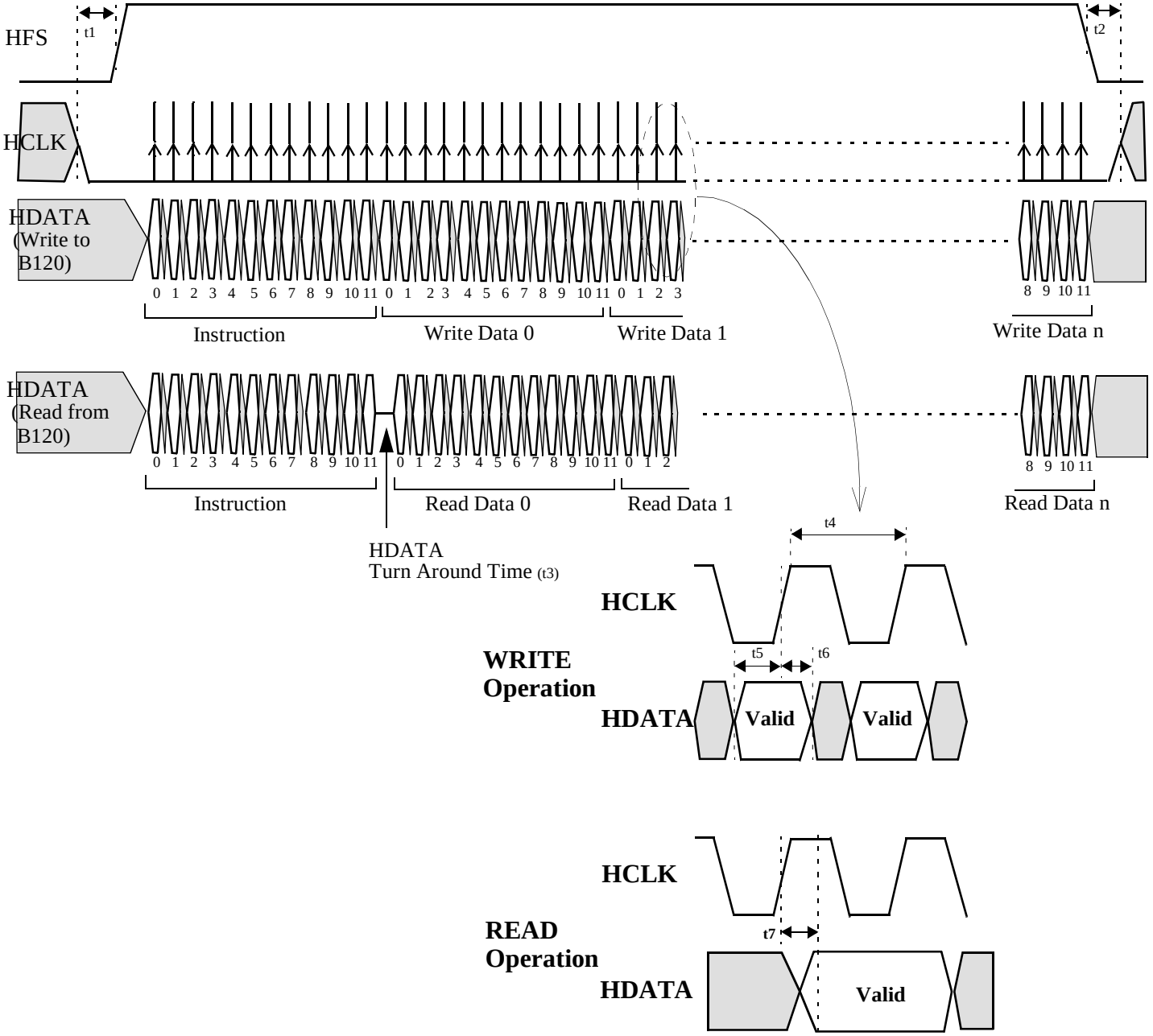


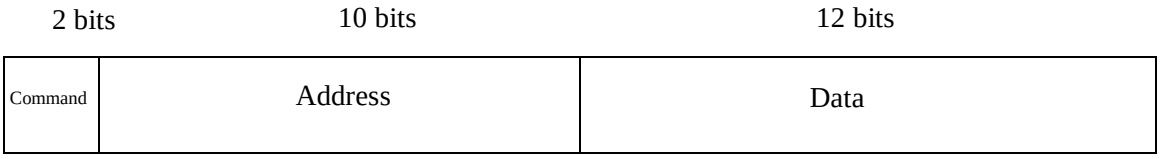
Figure 2.4.1 Timing Diagram of the B120 Serial Communication

Table 2.4.2 summarizes the serial channel specification of the B120. Refer to Figure 2.4.1 for the timing parameter definition.

Table 2.4.2 B120 Serial Channel Specification

Parameter	min.	typ.	max.
Word Size (Instruction and Data)	---	12 bits	---
HCLK low to HFS high (t1)	100 ns		
HFS low to HCLK inactive (t2)	100 ns		
HDATA Write to Read Turnaround Time (t3)	1 HCLK cycle		1 HCLK cycle
HCLK cycle (t4)	100 ns		
Data in setup time (t5)	25 ns		
Data in hold time (t6)	25 ns		
Data out valid (t7)	5 ns		10

In the read operation, the microcontroller (Initiator) issues an instruction lasting 12 HCLKs. After the last bit of the command is transferred to the B120 on the 12th clock, the microcontroller must stop driving data before the next rising edge of HCLK at which point the B120 will start driving data. At the 13th rising edge of HCLK, the B120 will begin driving data.



Command: 00 = Write
01 = Read
1x = Reserved

Figure 2.4.2 Serial Host Interface Data Transfer Format

On the B120 evaluation board, the microcontroller toggles the HCLK and HDATA lines under program control. Paradise Electronics provides API calls to facilitate communication between the microcontroller and the B120. Refer to the API reference manual for details.

2.4.3 Multi-Function Bus (MFB)

As explained earlier in the section, the microcontroller interface of the B120 chip consists of only four pins. The Multi-Function Bus provides additional 12 pins that are used as general purpose input and output (GPIO) pins. Each pin can be independently configured as an input or an output.

The microcontroller can read the status of these pins and determine the state of user interface control buttons connected to them. Refer to the API reference manual for the API calls used with the MFB pins.

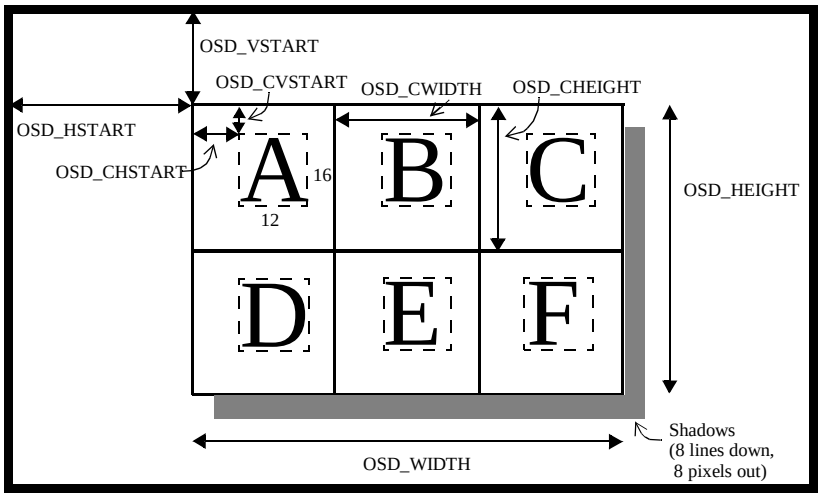
2.5 OSD (On-Screen Display) Control

The B120 chip has a built-in OSD (On-Screen Display) controller with an integrated font ROM. The chip also supports an external OSD controller for monitor vendors to maintain a familiar user interface.

2.5.1 On-Chip OSD

The B120's on-chip OSD controller, a font-based graphics controller, can display character cells at 32 locations on a screen. Each of the 32 screen locations has eight bits of data: six bits for character code and 2 bits for attribute. Each location can occupy up to 64 pixels by 64 scanlines. These screen locations altogether form an OSD window.

The OSD window is not affected by the expansion operation. The size will stay the same whether the source input data is expanded or not.



OSD_HSTART = OSD Window Horizontal Start Position

OSD_VSTART = OSD Window Vertical Start Position

OSD_CHSTART = OSD Character Horizontal Start Position

OSD_CVSTART = OSD Character Vertical Start Position

OSD_CWIDTH = OSD Character Width

OSD_CHEIGHT = OSD Character Height

OSD_Width = OSD Window Width

OSD_Height = OSD Window Height

OSD_Width x OSD_Height =< 32
(1 x 32, 2 x 16, 3 x 10, 4 x 8, 5 x 5, 6 x 5, etc.)

Font size = 12 pixels x 16 scanlines

Figure 2.5.1 On-Chip OSD Window Location

Table 2.5.1 Programmability of On-chip OSD Locations

Parameter	Range	Reference Point
OSD Window Horizontal Start Position	0 ~ 1024 pixels	End-of-line pulse (internal signal)
OSD Window Vertical Start Position	0 ~ 1024 scanlines	End-of-frame pulse (internal signal)
OSD Character Horizontal Start Position	0 ~ 64 pixels	Upper-left corner of a screen location
OSD Character Vertical Start Position	0 ~ 64 scanlines	Upper-left corner of a screen location
OSD Character Width	0 ~ 64 pixels	
OSD Character Height	0 ~ 64 pixels	
OSD Window Width	0 ~ 32 characters	
OSD Window Height	0 ~ 32 characters	
OSD Window Width x OSD Window Height	0 ~ 32 character locations (rectangle or square)	
Font Size	12 pixels wide x 16 scanlines high	

All 32 (or up to 32) screen locations are programmed to the same character cell size and the font start position. The character cell size and the font start position are independently programmable in the range of 0 to 63 pixels and/or lines as shown in Figure 2.5.1. Double width mode and/or double height mode is supported and can be selected independently. This programmability allows for proper spacing of symbols in the OSD window without wasting screen memory.

The hot spot (or the upper-left corner) of the OSD window is programmed at one pixel/one line resolution. This hot spot is referenced to End-of-line pulse (horizontal) of the previous line and End-of-frame pulse (vertical) of the previous frame. These two pulses are internal signals. The pulse position in relation to the display position changes depending on data input resolution and refresh rate. The pulse position change will be transparent to a monitor application program. The API call takes this position change into account when placing an OSD window according to the location parameters passed by a monitor application program.

To improve appearance and make it easy to find the OSD window on the screen, user can select optional shadowing (3D like effect). This shadowing feature will set underlying graphics data to half intensity. The size of shadow area is located at the lower and right boundaries of the window. It is 8 pixels wide and 8 lines high.

The built-in font ROM stores 128 fonts. Each font size is 12 pixels wide and 16 scanlines high. The font images are shown on page 34.

Each screen location is associated with one of four attributes. Each attribute is defined by foreground/background transparency flags as shown in Table 2.5.2.

Table 2.5.2 Character (or Screen Location) Attribute

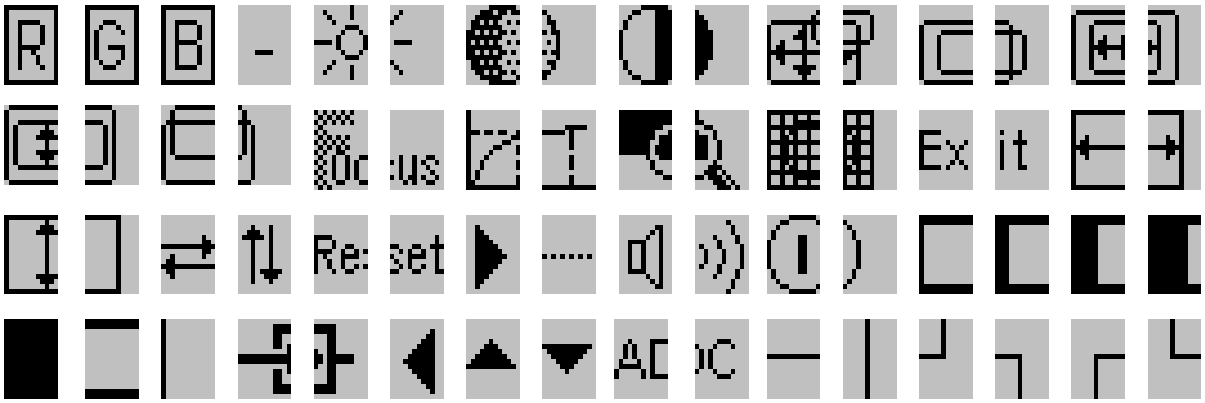
Foreground Transparency	Background Transparency	Visual Effect
0	0	Both the font dots and the background color are displayed.
1	0	The font dots of this screen location is transparent.
0	1	The font dots are displayed with a foreground color and the back ground is transparent.
1	1	This screen location is transparent.

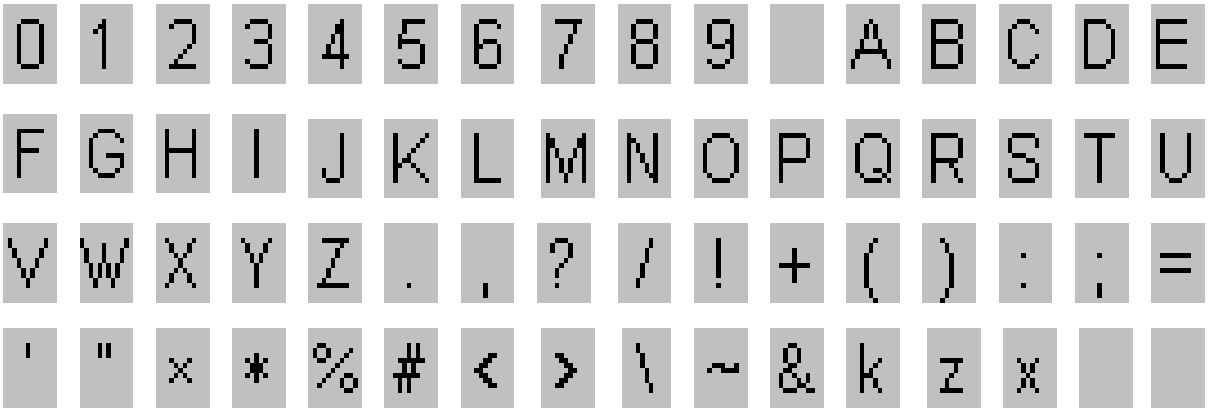
There are four colors available for the foreground and the background.

There is no hardware cursor supported, because character highlighting can be done by changing the corresponding location of attribute.

On-chip OSD as well as external OSD is controlled through the API calls. The external OSD is explained in Section 2.5.3.

2.5.2 Built-in OSD Font





2.5.3 External OSD Support

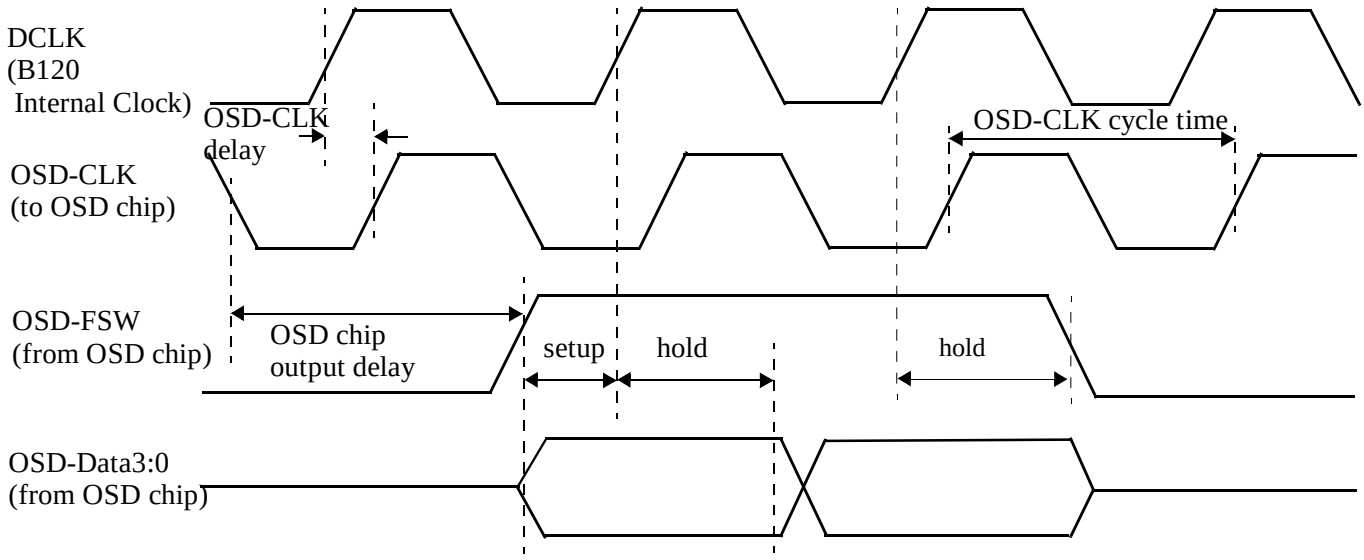
The B120 supports an external OSD controller for monitor vendors who wish to maintain a specific user interface, or the look and the feel. Only those OSD controllers that are developed for a flat-panel monitor application and have a pixel-clock input pin are supported. As is the case with an on-chip OSD, the OSD window size is not affected by the expansion operation.

An external OSD controller is connected to the B120 chip as shown in Table 2.5.3.

Table 2.5.3 Pin Connection Between the B120 and an External OSD controller

B120 Pin Name (Pin#, in/out)	External OSD Controller Pin (in/out)	Polarity	Position
OSD-HREF (#115, output)	HSync (input)	Programmable	Active during horizontal blanking period.
OSD-VREF (#116, output)	VSync (input)	Programmable	Active during vertical blanking period.
OSD-CLK (#117, output)	Pixel Clock (input)		
OSD-FSW (#122, input)	OSD Window Indicator (output)	Programmable	Horizontal: M OSD-CLK cycles after the HREF for N pixels. Vertical: M' HREF pulses after the VREF for N' lines (M, N, M',N' programmed to external OSD chip)
OSD-DATA[3:0] (#118~#121, inputs)	Intensity, R, G, and B (outputs)		

The four-bit data from an external OSD controller becomes one of the 16 entries to the OSD look-up table (LUT), which is 12 bits wide (4 bits/color).



OSD-CLK delay = 3 ns default. Addtional 0 ~ 7 ns delay can be added.

OSD-FSW/OSD-DATA setup/hold time = 1.5 ns min.

OSD-CLK cycle time = DCLK cycle time = 120 MHz max.

Figure 2.5.2 External OSD Interface Data Latch Timing

When the external OSD controller interface is enabled, the data from the OSD LUT is displayed on a TFT panel instead of the ADC output whenever the OSD-FSW signal is active.

The OSD-CLK output to an external OSD controller chip is derived from the DCLK (destination clock) whose clock frequency is the same as the panel clock in frequency (or twice the panel clock frequency on a two-pixels-per-clock panel). The maximum frequency is 120 MHz.

Both the OSD Data and OSD-FSW signals are latched by B120 on the rising edge of the DCLK. To maximize the setup/hold time for the OSD-Data and OSD-FSW signal, delay of up to 6 ns can be added to the OSD-CLK.

Table 2.5.4 External OSD Interface Timing Parameters

Parameter	minimum	typical	maximum
OSD-CLK Frequency			**120 MHz**
OSD-FSW/OSD-DATA setup time	**1.5 ns**		
OSD-FSW/OSD-DATA hold time	**1.5 ns**		
OSD-CLK delay from DCLK		**0 ~ 5.6 ns, programmable in 800-ps increment**	
OSD-HREF delay from DCLK		**0 ~ 12 ns, programmable in 800-ps incremenet**	
OSD-CLK/DCLK ratio		**1/4x, 1/2x, 1x, programmable**	

The external-OSD window position is referenced to the edge of the OSD-HREF and OSD-VREF. The horizontal start position is defined in terms of OSD-CLK pulse counts. The vertical position is defined in terms of OSD-HREF pulse counts. These values must be programmed into an external OSD controller chip.

The trailing edge of OSD-HREF and OSD-VREF are always positioned at the beginning of a display period. Thus, the external OSD window position will stay at the same place regardless of input resolution and refresh rate.

In the meantime, enabling/setting up the external OSD interface and writing to the OSD LUT will be covered by the B120 API calls.

2.6 TCLK Input

The source timing is measured by using the TCLK input as a reference. Also, the reference clock to the on-chip PLL's are derived from the TCLK. Thus, it is crucial to have a jitter-free clock as TCLK.

Table 2.6.1 shows the requirements for the TCLK signal.

Table 2.6.1 TCLK Specification

Frequency	**20 MHz ~ 50 MHz**
Jitter	**250 ps maximum**
Rise Time (10% to 90%)	**5 ns**
Duty Cycle	**40-60**

3. Electrical Characteristics

Table 3.1 Absolute Ratings

Parameter	Min.	Typ.	Max.	Note
PVDD			5.6 volts	
CVDD			5.6 volts	
Vin	Vss - 0.5volt		Vcc + 0.5V	
Operating temperature	0 degreeC		70 degreeC	
Storage temperature	-65 degreeC		150 degreeC	
Maximum power consumption			~2 W	

Table 3.2 DC Electrical Characteristic

Parameter	Min.	Typ.	Max.	Note
PVDD	3.15 volts	3.3 volts	3.47 volts	
CVDD	3.15 volts	3.3 volts	3.47 volts	
Vil (CMOS inputs) Vil (TTL inputs)			0.3 * CVDD 0.8 volts	
Vih (CMOS inputs) Vih (TTL inputs)	0.7 * CVDD 2.0 volts		1.1 * CVDD 5.0+ 0.5 volts	 (1)
Voh	2.4 volts		CVDD	
Vol		0.2 volts	0.4 volts	
input current	-10 uA		10 uA	
PVDD operating supply current	0 mA		20 mA/pad @ 10pF	(2)
CVDD operating supply current	0 mA		500 mA	(3)

NOTE 1:
5V-Tolerent TTL Input Pads are as follows.

- *CRT Interface: HSYNC (pin #150),VSYNC (#148)*
- *Host Interface: HFS (#98), HCLK (#103), HDATA (#99), RESETN (#100)*
- *MFB[11:0]: MFB11 (#123), MFB10 (#124), MFB9 (#102), MFB8 (#104), MFB7 (#105), MFB6 (#106), MFB5 (#107), MFB4 (#109), MFB3 (#110), MFB2 (#111), MFB1 (#112), MFB0 (#113)*
- *OSD Interface: OSD_DATA3 (#121), OSD_DATA2 (#120), OSD_DATA1 (#119), OSD_DATA0 (#118), OSD_FSW (#122)*

Non-5V-Tolerant TTL Input Pad is:

- *TCLK (#141)*

NOTE 2:
When the panel interface is disabled, the supply current is 0 mA. The drive current of each pad can be programmed in the range of 2 mA to 20 mA (@capacitive loading = 10 pF) .

NOTE 3:
When all circuits are powered down and TCLK is stopped, the CVDD supply current becomes 0 mA.

4. Package Dimension

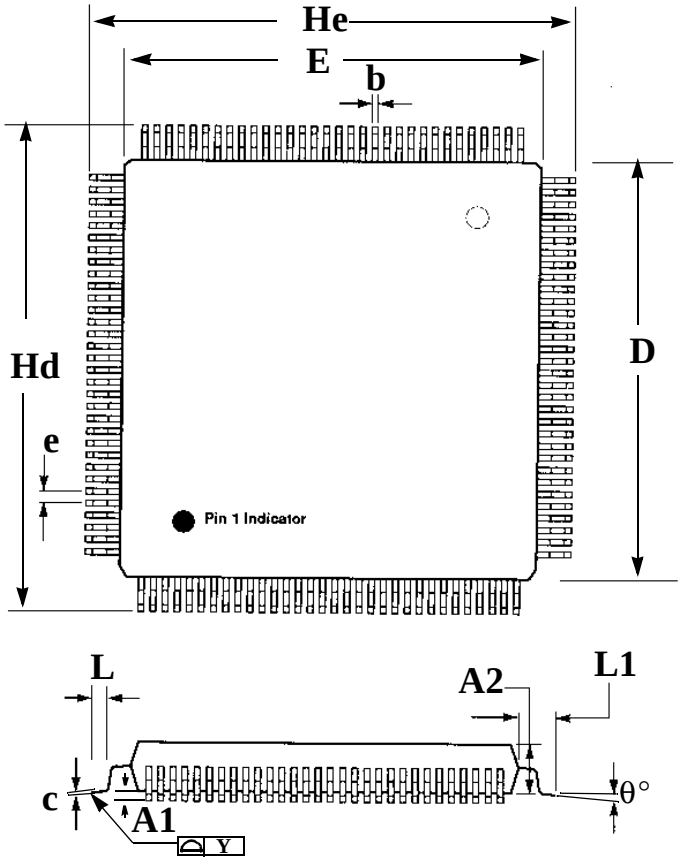


Table 4.1 Package Dimension

Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A1	0.05	0.25	0.50	0.002	0.010	0.020
A2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.65			0.026	
Hd	30.95	31.20	31.45	1.218	1.228	1.238
He	30.95	31.20	31.45	1.218	1.228	1.238
L	0.65	0.80	0.95	0.025	0.031	0.037
L1		1.60			0.063	
Y			0.08			0.003
θ°	0		7	0		7

APPENDIX: List of Tables and Figures