Ver 1.2

12-Bit 8-Channel 1MSPS Analog to Digital Converter

Datasheet

Part Number：B128S102RH

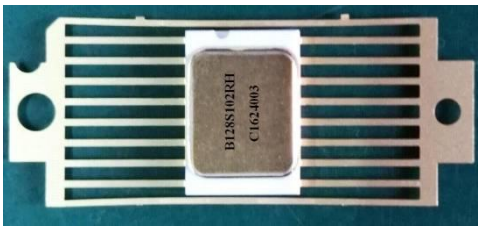
中国航天 CASC
北京微电子技术研究所
Beijing Microelectronics Technology Institute

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2017.1	-	-	
1.1	2017.9	Chapter 7	Modified parameter list	
1.2	2018.3	-	Changed the template	

TABLE OF CONTENTS

1. Unique features



- 12-Bit-Resolution A/D Converter
- 8 Analog Input Channels
- Sample rate 50k to 1MSPS
- Independent Analog and Digital Supplies
- Integral Non-Linearity INL: -2.0 LSB ~+2.0 LSB
- Differential Non-Linearity DNL: -0.9 LSB ~+1.9LSB
- Signal-to-Noise Ratio SNR（f_{IN}=40.2kHz）: ≥67dB
- Effective Number of Bits ENOB（f_{IN}=40.2kHz）: ≥11Bits
- Power Consumption：≤20mW
- Offset Error（Supply Voltage=3V）：-2.5 LSB ~ +2.5LSB
- Full Scale Error：-2.0 LSB ~+2.0LSB
- Conversion (Hold) time $t_{CONVERT}$：≤13 CLK cycles
- Total Ionizing Dose ≥ 100 Krad(Si)
- The Single Event Latch-up robust ability≥75MeV•cm^2/mg
- Packaged in 16-Lead Ceramic FP

2. Description

The B128S102RH is 12-bit，8-channel switched capacitor, anti- nuclear radio harms successive approximation, analog to digital converters. The input clock frequency can be high to 16MHz, the highest sample rate is 1MSPS. The transfer mode is serial input, which can reduce the I/O interface quantity of the processor 51, and can get high level resolution.

3. Functional block diagram

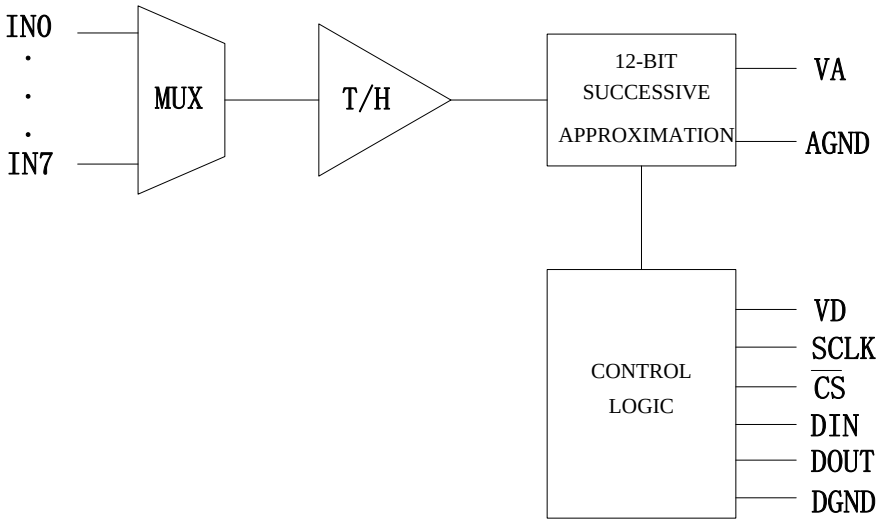


Figure 3-1. Functional block diagram

4. Pin configuration

The pins description of device are shown in figure 4-1.

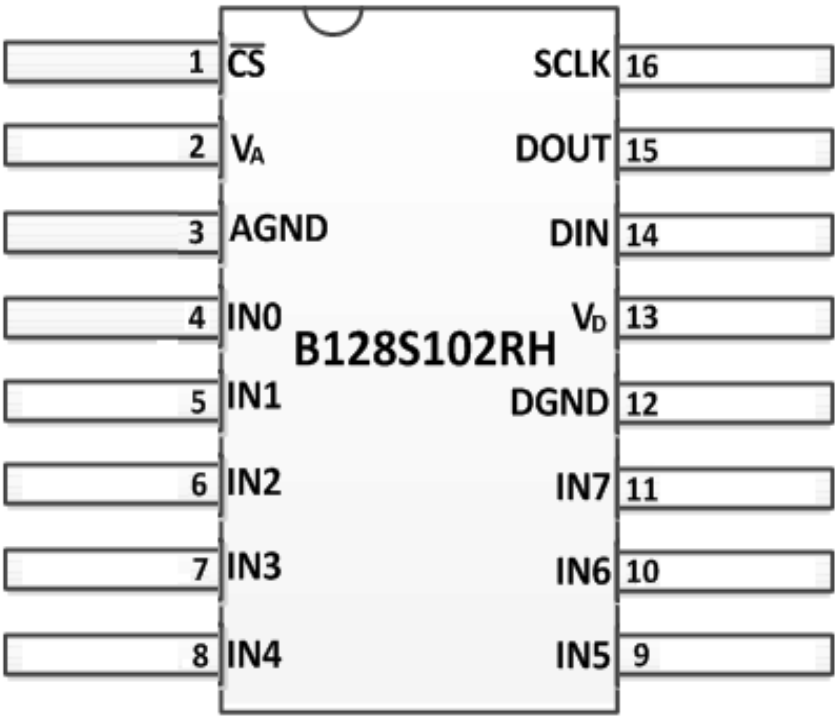


Figure 4-1. Pin description

5. Pin definition

Table 5-1. The pin configuration

No	name	I/O	description
ANALOG I/O			
4-11	IN0-IN7	I	Analog inputs, These signals can range from 0 V to $V_{A.}$
DIGITAL I/O			
16	SCLK	I	Digital clock input. The specified performance range of frequencies for this input is 0.8 MHz to 16 MHz. This clock directly controls the conversion and readout processes.
15	DOUT	O	Digital data output. The output samples are clocked out of this pin on the falling edges of the SCLK pin.
14	DIN	I	Digital data input. The Control Register is loaded through this pin on rising edges of the SCLK pin.
1	/CS	I	Chip select. On the falling edge of CS, a conversion process begins. Conversions continue as long as CS is held low.
POWER SUPPLY			
2	V_A	IO	Positive analog supply pin. This voltage is also used as the reference voltage. This pin should be connected to a quiet 2.7 V to 5.25 V source and bypassed to GND with 1-µF and 0.1-µF monolithic ceramic capacitors located within 1 cm of the power pin.
13	V_D	IO	Positive digital supply pin. This pin should be connected to a 2.7 V to V_A supply, and bypassed to GND with a 0.1-µF monolithic ceramic capacitor located within 1 cm of the power pin.
3	AGND	IO	The ground return for the analog supply and signals.
12	DGND	IO	The ground return for the digital supply and signals.

6. Device description

6.1 Principles of Operation

Simplified schematics of the Chip in both track and hold operation are shown in Figure 6-1 and Figure 6-2 respectively. In Figure 6-1, the Chip is in track mode: switch SW1 connects the sampling capacitor to one of eight analog input channels through the multiplexer, and SW2 balances the comparator inputs. The Chip is in this state for the first three SCLK cycles after CS is brought low.

Figure 6-2 shows the Chip in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the

comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge to or from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The Chip is in this state for the last thirteen SCLK cycles after /CS is brought low.

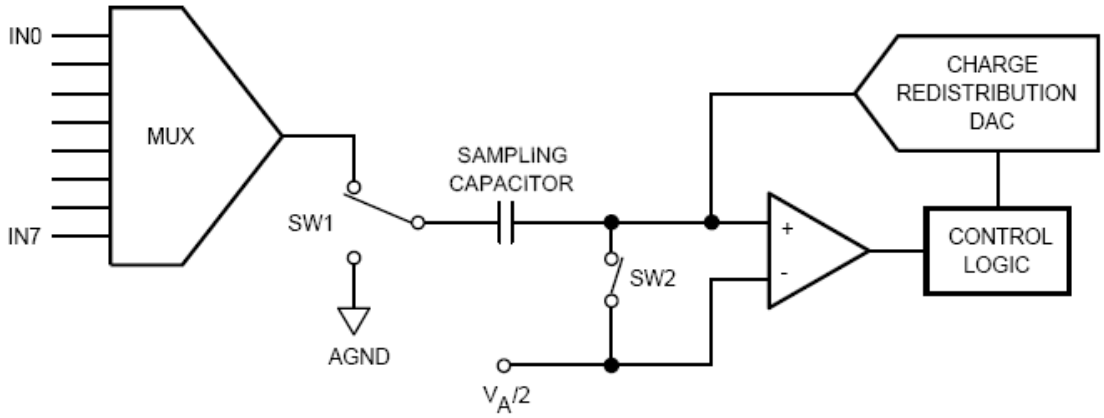


Figure6-1 B128S102RH in Track Mode

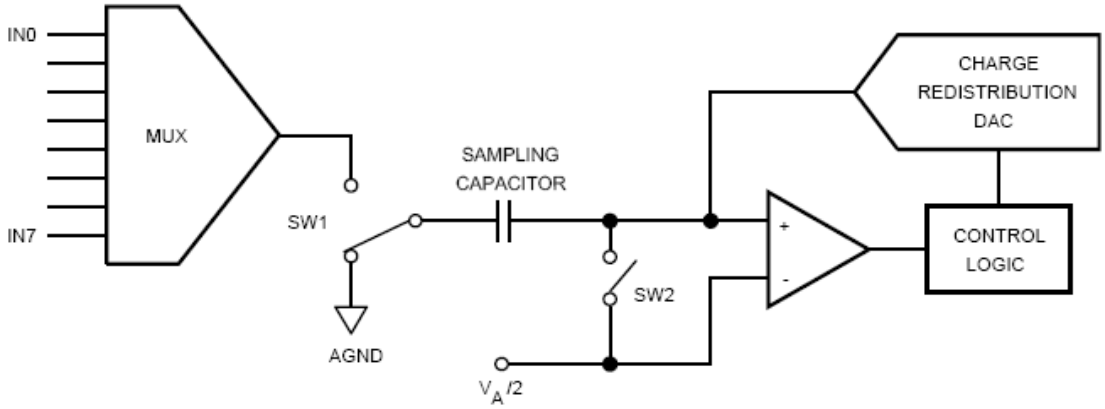


Figure 6-2 B128S102RH in Hold Mode

Programming timing diagram

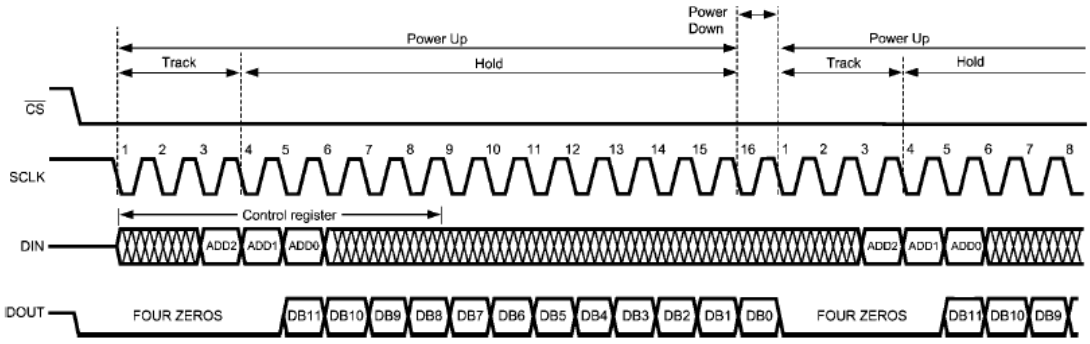


Figure 6-3 Operational Timing Diagram

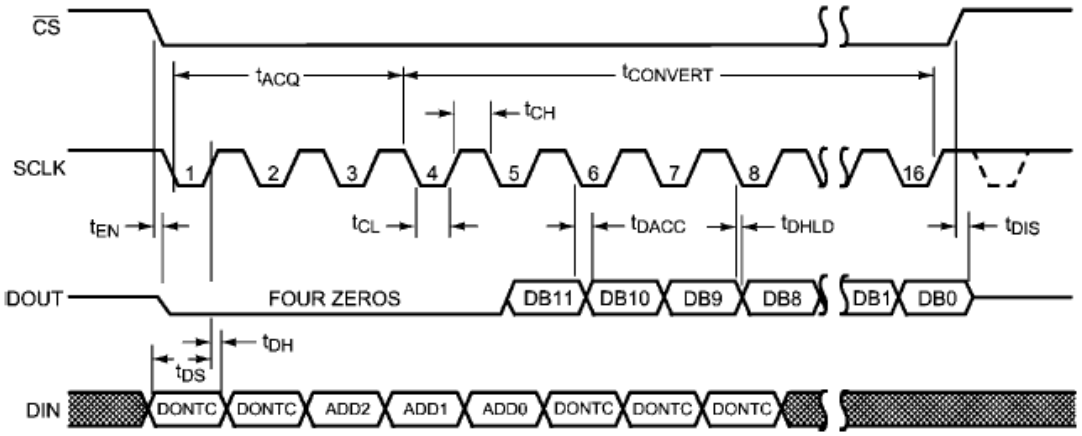


Figure6-4 Serial Timing Diagram

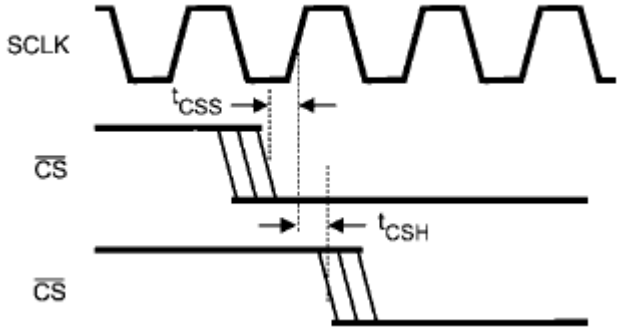


Figure6-5 SCLK and CS Timing Parameters

An operational timing diagram and a serial interface timing diagram for the Chip are shown in Figure6-3 to Figure6-5. CS, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data to be written to the Chip's Control Register is placed on DIN, the serial data input pin. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of CS and ends on the rising edge of CS. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC's DOUT pin is in a high impedance state when CS is high and is active when CS is low. Thus, CS acts as an output enable. Similarly, SCLK is internally gated off when CS is brought high.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out. SCLK falling edges 1 through 4 clock out leading zeros while falling edges 5 through 16 clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC will re-enter

the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK and re-enter the hold/convert mode on the N×16+4th falling edge of SCLK. "N" is an integer value.

The Chip enters track mode under three different conditions. In Figure6-3, CS goes low with SCLK high and the ADC enters track mode on the first falling edge of SCLK. In the second condition, CS goes low with SCLK low. Under this condition, the ADC automatically enters track mode and the falling edge of CS is seen as the first falling edge of SCLK. In the third condition, CS and SCLK go low simultaneously and the ADC enters track mode. While there is no timing restriction with respect to the falling edges of CS and SCLK, see Figure 6-5 for setup and hold time requirements for the falling edge of CS with respect to the rising edge of SCLK.

During each conversion, data is clocked into a control register through the DIN pin on the first 8 rising edges of SCLK after the fall of CS. The control register is loaded with data indicating the input channel to be converted on the subsequent conversion (see Table 6-1, Table6-2, and Table6-3).

Although the Chip is able to acquire the input signal to full resolution in the first conversion immediately following power-up, the first conversion result after power-up will be that of a randomly selected channel. Therefore, the user needs to incorporate a dummy conversion to set the required channel that will be used on the subsequent conversion.

Table 6-1 Control Register Bits

BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DONTC	DONTC	ADD2	ADD1	ADD0	DONTC	DONTC	DONTC

Table 6-2 Control Register Bit Descriptions

BIT	SYMBOL	DESCRIPTION
7、6、2、1、0	DONTC	Don't care. The values of these bits do not affect the device.
5	ADD2	These three bits determine which input channel will sampled and converted at the next conversion cycle. The mapping between codes and channels is shown in Table6-3
4	ADD1	
3	ADD0	

Table 6-3 Input Channel Selection

ADD2	ADD1	ADD0	INPUT CHANNEL
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5

1	1	0	IN6
1	1	1	IN7

Transfer Function characters

The output format of the chip is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the chip is VA / 4096. The ideal transfer characteristic is shown in Figure. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of VA / 8192. Other code transitions occur at steps of one LSB.

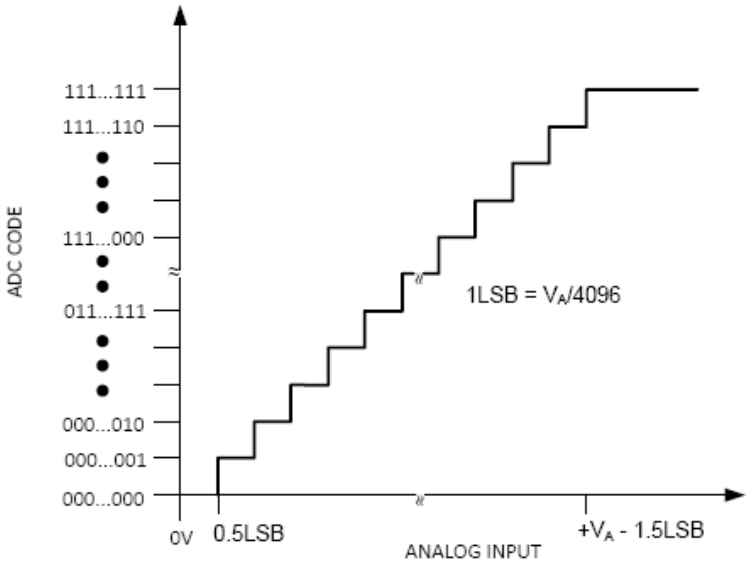


Figure6-6 Ideal Transfer Characteristic

Analog Inputs

An equivalent circuit for one of the input channels of the Chip is shown in Figure. Diodes D1 and D2 provide ESD protection for the analog inputs. The operating range for the analog inputs is 0 V to V_A. Going beyond this range will cause the ESD diodes to conduct and result in erratic operation. The capacitor C1 has a typical value of 3pF and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track/hold switch and is typically 500 Ω. Capacitor C2 is the Chip sampling capacitor, and is typically 30 pF. The Chip will deliver best performance when driven by a low-impedance source (less than 100 Ω). This is especially important when using the Chip to sample dynamic signals. Also important when sampling dynamic signals is a band-pass or low-pass filter which reduces harmonics and noise in the input. These filters are often referred to as anti-aliasing filters.

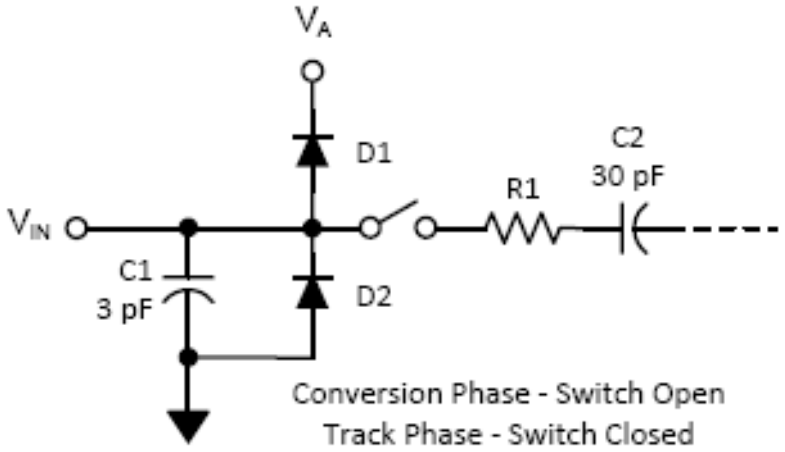


Figure6-7 Equivalent Input Circuit

Digital Inputs and Outputs

The digital inputs of the chip (SCLK, /CS, and DIN) have an operating range of 0 V to V_A. The digital output (DOUT) operating range is controlled by V_D. The output high voltage is V_D – 0.5 V (minimum) while the output low voltage is 0.4 V (maximum).

Power Supply Recommendations

There are three major power supply concerns with this product: power supply sequencing, power management, and the effect of digital supply noise on the analog supply.

Power Supply Sequence

The Device is a dual-supply device. The two supply pins share ESD resources, so care must be exercised to ensure that the power is applied in the correct sequence. To avoid turning on the ESD diodes, the digital supply (V_D) cannot exceed the analog supply (V_A) by more than 300 mV, during a conversion cycle. Therefore, V_A must ramp up before or concurrently with V_D.

Power Management

The Device is fully powered-up whenever /CS is low and fully powered-down whenever /CS is high, with one exception. If operating in continuous conversion mode, the Device automatically enters power-down mode between SCLK's 16th falling edge of a conversion and SCLK's 1st falling edge of the subsequent conversion.

In continuous conversion mode, the Device can perform multiple conversions back to back. Each conversion requires 16 SCLK cycles and the Device will

perform conversions continuously as long as /CS is held low. Continuous mode offers maximum throughput.

In burst mode, the user may trade off throughput for power consumption by performing fewer conversions per unit time. This means spending more time in power-down mode and less time in normal mode. By utilizing this technique, the user can achieve very low sample rates while still utilizing an SCLK frequency within the electrical specifications. The Power Consumption versus SCLK curve in the *Typical Characteristics* shows the typical power consumption of the Device. To calculate the power consumption (P_C), simply multiply the fraction of time spent in the normal mode (t_N) by the normal mode power consumption (P_N), and add the fraction of time spent in shutdown mode (t_S) multiplied by the shutdown mode power consumption (P_S) as shown in the Equation.

$$P_C = \frac{t_N}{t_N + t_S} \times P_N + \frac{t_S}{t_N + t_S} \times P_S$$

Power Supply Noise Considerations

The charging of any output load capacitance requires current from the digital supply, V_D. The current pulses required from the supply to charge the output capacitance will cause voltage variations on the digital supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, if the analog and digital supplies are tied directly together, the noise on the digital supply will be coupled directly into the analog supply, causing greater performance degradation than would noise on the digital supply alone. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low will dump current into the die substrate, which is resistive. Load discharge currents will cause "ground bounce" noise in the substrate that will degrade noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater the noise coupled into the analog channel.

The first solution to keeping digital noise out of the analog supply is to decouple the analog and digital supplies from each other or use separate supplies for them. To keep noise out of the digital supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100-Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This will limit the charge and discharge current of the output capacitance and improve

noise performance. Because the series resistor and the load capacitance form a low frequency pole, verify signal integrity once the series resistor has been added.

6.2 Application information

The Chip is a low-power, eight-channel 12-bit ADC with ensured performance specifications from 50 kSPS to 1 MSPS. A typical application is shown in Figure. The split analog and digital supply pins are both powered in this example by LP2950 low-dropout voltage regulator. The analog supply is bypassed with a capacitor network located close to the chip. The digital supply is separated from the analog supply by an isolation resistor and bypassed with additional capacitors. The chip uses the analog supply (V_A) as its reference voltage, so it is very important that V_A be kept as clean as possible. Due to the low power requirements of the chip, it is also possible to use a precision reference as a power supply.

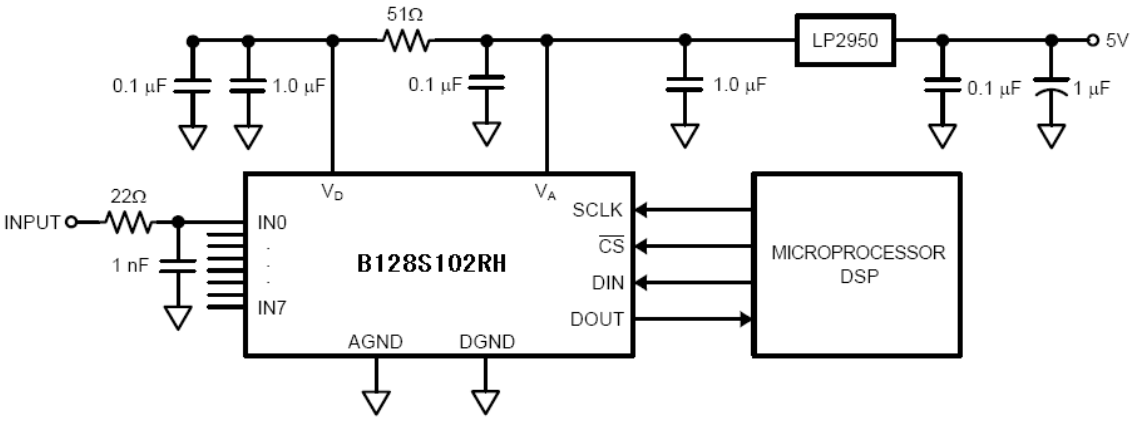


Figure6-8 Typical application diagram

6.3 Storage Condition

The warehouse environment of B128S102RH should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

6.4 Absolute Maximum Ratings

1)Analog Power Voltage（V_A）……-0.3V～6.5V

2)Digital Power Voltage（V_D）……-0.3V～V_A+0.3V

3) Any Pin to GND Voltage: ……-0.3V～V_A+0.3V

4) Any Pin input Current: ……±10mA

5)Power Dissipation（PD）:……1.18W（T_A=25℃，θ_{JA}=127℃/W）

6) Lead Temperature(10 sec)（T_h） ……260℃（10s）

7) Junction Temperature（T_J） ……175℃

8) Storage Temperature (T_{STG})：……-65℃~+ 150℃

9) Thermal Resistance（$R_{th\ (jc)}$） …… 18℃/W

6.5 Recommended Operating conditions

1)Analog Power Voltage（V_A）……..+2.7V～+5.25V

2)Digital Power Voltage（V_D）……..+2.7V～V_A

3) Analog Input Voltage : ……0V～V_A

4)Digital Input Voltage: ……..0V～V_A

5)Clock Frequency: ……0.8MHz～16MHz

6)Input Clock Duty Circle: ……40%~60%

7) Work temperature（T_A）：……-55℃～+125℃

6.6 Radiation hardened performance

a） Total Ionizing Dose：≥100K Rad(Si)

b） The Single Event Latch-up threshold：≥75MeV cm^2/mg

7. Electrical characteristics

Table7-1 Electrical characteristics

Parameter	Symbol	Condition Unless otherwise specified, f_{SCLK}=0.8MHz~16MHz f_{SAMPLE}=50kSPS~1MSPS -55℃≤T_A≤125℃	B128S102RH Min	 Min	Units
Integral Non-LInearity	*INL*	V_A= V_D=+3.0V	-2.0	+2.0	LSB
		V_A= V_D=+5.0V	-2.0	+2.0	
Differential Non-Linearity	*DNL*	V_A= V_D=+3.0V	-0.9	1.9	LSB
		V_A= V_D=+5.0V	-0.9	1.9	
Offset Error	V_{OFF}	V_A= V_D=+3.0V	-2.5	+2.5	LSB
		V_A= V_D=+5.0V	-4.0	+4.0	
Offset Error Match	*OEM*	V_A= V_D=+3.0V	-1.5	+1.5	LSB
		V_A= V_D=+5.0V	-1.5	+1.5	
Full Scale Error	*FSE*	V_A= V_D=+3.0V	-2.0	+2.0	LSB
		V_A= V_D=+5.0V	-2.0	+2.0	
Full Scale Error Match	*FSEM*	V_A= V_D=+3.0V	-1.5	+1.5	LSB
		V_A= V_D=+5.0V	-1.5	+1.5	
Signal-to-Noise Plus Distortion Ratio	*SINAD*	V_A= V_D=+3.0V， f_{IN}=40.2kHz，-0.02dBFS	66	--	dB
		V_A= V_D=+5.0V， f_{IN}=40.2kHz，-0.02dBFS	66	--	
Signal-to-Noise Ratio	*SNR*	V_A= V_D=+3.0V， f_{IN}=40.2kHz，-0.02dBFS	67	--	dB
		V_A= V_D=+5.0V， f_{IN}=40.2kHz，-0.02dBFS	67	--	
Total Harmonic Distortion	*THD*	V_A= V_D=+3.0V， f_{IN}=40.2kHz，-0.02dBFS	--	-74	dB
		V_A= V_D=+5.0V， f_{IN}=40.2kHz，-0.02dBFS	--	-74	
Spurious-Free Dynamic Range	*SFDR*	V_A= V_D=+3.0V， f_{IN}=40.2kHz，-0.02dBFS	75	--	dB
		V_A= V_D=+5.0V， f_{IN}=40.2kHz，-0.02dBFS	75	--	
Effective Number of Bits	*ENOB*	V_A= V_D=+3.0V， f_{IN}=40.2kHz，-0.02dBFS	11	--	Bits

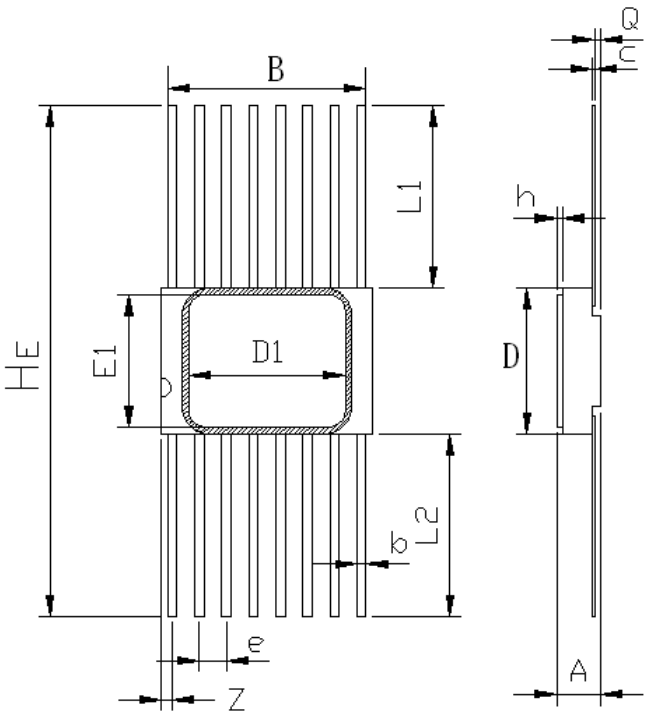
		V_A= V_D=+5.0V， f_{IN}=40.2kHz，-0.02dBFS	11	--	
Intermodulation Distortion, Second Order Terms	*IMD*	V_A= V_D=+3.0V， f_a=19.5kHz，f_b=20.5kHz	--	-78	dB
		V_A= V_D=+5.0V， f_a=19.5kHz，f_b=20.5kHz	--	-78	
Intermodulation Distortion, Third Order Terms		V_A= V_D=+3.0V， f_a=19.5kHz，f_b=20.5kHz	--	-70	
		V_A= V_D=+5.0V， f_a=19.5kHz，f_b=20.5kHz	--	-70	
Channel-to-Channel Isolation	*ISO*	V_A= V_D=+3.0V， f_{IN}=20kHz，-0.02dBFS	65	--	dB
		V_A= V_D=+5.0V， f_{IN}=20kHz，-0.02dBFS	67	--	
Input Range	V_{IN}		0	V_A	V
DC Leakage Current	I_{DCL}		-100	+100	nA
Input High Voltage	V_{IH}	V_A= V_D=+2.7V~+3.6V	2.1	--	V
		V_A= V_D=+4.75V~+5.25V	2.4	--	
Input Low Voltage	V_{IL}	V_A= V_D=+2.7V~+5.25V	--	0.8	V
Input Current	I_{IN}	V_{IN}=0 or V_{IN}= V_D	-100	+100	nA
Digital Input Capacitance	C_{IND}	--	--	4	pF
Output High Voltage	V_{OH}	I_{SOURCE}=200uA， V_A= V_D=+2.7V~+5.25V	V_D-0.5	--	V
Output Low Voltage	V_{OL}	I_{SOURCE}=200uA~1.0mA， V_A= V_D=+2.7V~+5.25V	--	0.4	V
Hi-Impedance Output Leakage Current	I_{OZH}， I_{OZL}	V_A= V_D=+2.7V~+5.25V	--	±1.0	uA
Analog and Digital Supply Voltages	V_A，V_D	V_A≥V_D	2.7		V
				5.25	V
Total Supply Current Normal Mode (CS low)	I_A+I_D	V_A=V_D=+3.6V f_{SAMPLE} =1MSPS ， f_{IN}=40kHz	--	2.0	mA
		V_A=V_D =+5.25V f_{SAMPLE} =1MSPS ， f_{IN}=40kHz	--	4.0	mA
Total Supply Current Shutdown Mode (CS high)		V_A=V_D =+3.6V f_{SCLK}=0kSPS	--	3.0	uA
		V_A=V_D =+5.25V f_{SCLK}=0kSPS	--	4.0	uA
Power Consumption Normal Mode (CS low)	P_C	V_A= V_D=+3.0V f_{SAMPLE} =1MSPS ， f_{IN}=40kHz	--	6.0	mW

		V_A=V_D =+5.0V f_{SAMPLE} =1MSPS， f_{IN}=40kHz	--	20	mW
Power Consumption Shutdown Mode(/CS high)		V_A= V_D=+3.0V f_{SCLK}=0kSPS	--	9	uW
		V_A=V_D =+5.0V f_{SCLK}=0kSPS	--	20	uW
Clock Frequency	f_{SCLK}	V_A=V_D =+2.7V~+5.25V	0.8		MHz
				16	MHz
Sample Rate	f_S	V_A=V_D =+2.7V~+5.25V	50	--	kSPS
			--	1	MSPS
Conversion(Hold)Time	$t_{CONVERT}$	V_A=V_D =+2.7V~+5.25V	--	13	SCLK cycles
Acquisition (Track) Time	t_{ACQ}	V_A=V_D =+2.7V~+5.25V	--	3	SCLK cycles
Throughput Time		Acquisition Time+Conversion Time V_A=V_D =+2.7V~+5.25V	--	16	SCLK cycles
/CS Hold Time after SCLK Rising Edge	t_{CSH}		10	--	ns
/CS Setup Time prior to SCLK Rising Edge	t_{CSS}		10	--	ns
/CS Falling Edge to DOUT enabled	t_{EN}		--	30	ns
DOUT Access Time after SCLK Falling Edge	t_{DACC}		--	27	ns
DOUT Hold Time after SCLK Falling Edge	t_{DHLD}		--	11	ns
DIN Setup Time prior to SCLK Rising Edge	t_{DS}		10	--	ns
DIN Hold Time after SCLK Rising Edge	t_{DH}		10	--	ns
/CS Rising Edge to DOUT high Impedance	t_{DIS}	DOUT falling	--	20	ns
		DOUT Rising	--	20	ns

After Total Ionizing Dose					
Effective Number of Bits	*ENOB*	V_A= V_D=+3.0V，f_{IN}=40.2kHz，-0.02dBFS	10.7		Bits
		V_A= V_D=+5.0V，f_{IN}=40.2kHz，-0.02dBFS	10.7		
Total Supply Current Shutdown Mode (/CS high)	I_A+I_D	V_A=V_D=+2.7V~+3.6V f_{SCLK}=0kSPS		30	uA
		V_A=V_D=+4.75V~+5.25V f_{SCLK}=0kSPS		100	
Hi-Impedance Output Leakage Current	I_{OZH},I_{OZL}	V_A=V_D=+2.7V~+5.25V	-10	+10	uA

8. Package Outline Dimension

The chip is 16 leads FP ceramic package，the chip outline dimension is shown in Figure 9-1.



SIZE SYMBOL	VALUE（unit：mm）		
	MIN	TYP	MAX
A	1.60	——	2.50
B	8.94	——	9.69

b	0.25	——	0.54
c	0.07	——	0.20
D	6.55	——	7.25
e	——	1.27	——
He	20.00	——	25.00
Q	0.13	——	0.90
L1	6.47	——	9.12
L2	6.47	——	9.12
Z	——	——	1.27
D1	——	7.366	——
E1	——	6.223	——
h	0.22	——	0.28

Figure 9-1. the chip outline dimension

Service & Supply

Address：No.2.Siyingmen N.Rd.Donggaodi, Fengtai District, Beijing, PRC

Department：Department of international cooperation

Telephone：010-67968115-8334

Fax：010-68757706

Zip code：100076