(V) Preliminary Specifications
( ) Final Specifications

Module	**14.0" FHD 16:9 Color TFT-LCD Open cell**
Model Name	B140HAN01.4 (H/W:0A)

Customer	**Date**	**Approved by**	**Date**
		Jonken Fan	07/10/2014
Checked & Approved by	**Date**	**Prepared by**	**Date**
		Stany Yeh	07/10/2014
Note: This Specification is subject to change without notice.		**NBBU Marketing Division AU Optronics corporation**	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2014/7/10	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the product.
8) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT LCD Open cell.
9) After installation of the TFT LCD Open cell into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT LCD Open cell even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT LCD Open cell from outside. Otherwise the TFT LCD Open cell may be damaged.
10) Small amount of materials having no flammability grade is used in the TFT LCD Open cell. The TFT LCD Open cell should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
11) Disconnecting power supply before handling TFT LCD Open cell, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT LCD Open cell that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

2. General Description

B140HAN01.4 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD open cell , a driver circuit. The screen format is intended to support the 16:9 FHD, 1920(H) x1080(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP interface compatible.

B140HAN01.4 is designed for a display unit of notebook style personal computer and industrial machine.

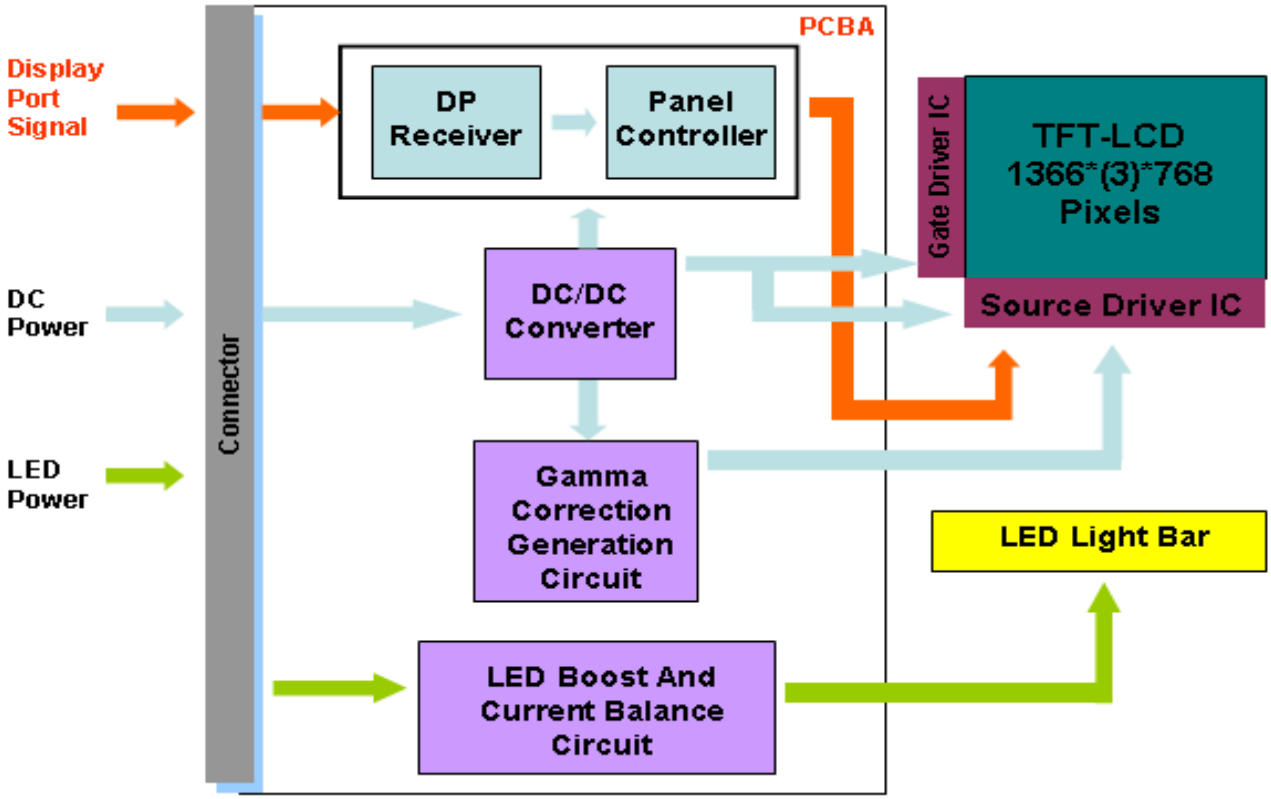
2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	354.69			
Active Area	[mm]	309.14 X 173.89 (typ)			
Pixels H x V		1920x3(RGB) x 1080			
Pixel Pitch	[mm]	0.161X0.161			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
Response Time	[ms]	25			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	1.2 max (Logic power) @ mosaic pattern			
Weight	[Grams]	180 g			
Physical Size Include bracket & PCBA	[mm]		Min.	Typ.	Max.
		Length	317.17	317.37	317.57
		Width	196.94	197.44	197.94
		Thickness		2.44	2.65
Electrical Interface		2 Lane eDP1.2			
Glass Thickness	[mm]	0.5			
Surface Treatment		Anti - Glare, Hardness 3H			
Support Color		6-bit + FRC			
RoHS Compliance		RoHS Compliance			

3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 30 Pin



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

5. Electrical Characteristics

5.1 TFT LCD Open Cell

5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.2	[Watt]	Note 1
IDD	IDD Current	-	-	400	[mA]	Note 1
IRush	Inrush Current	-	-	1500	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Typical Measurement Condition: Mosaic Pattern

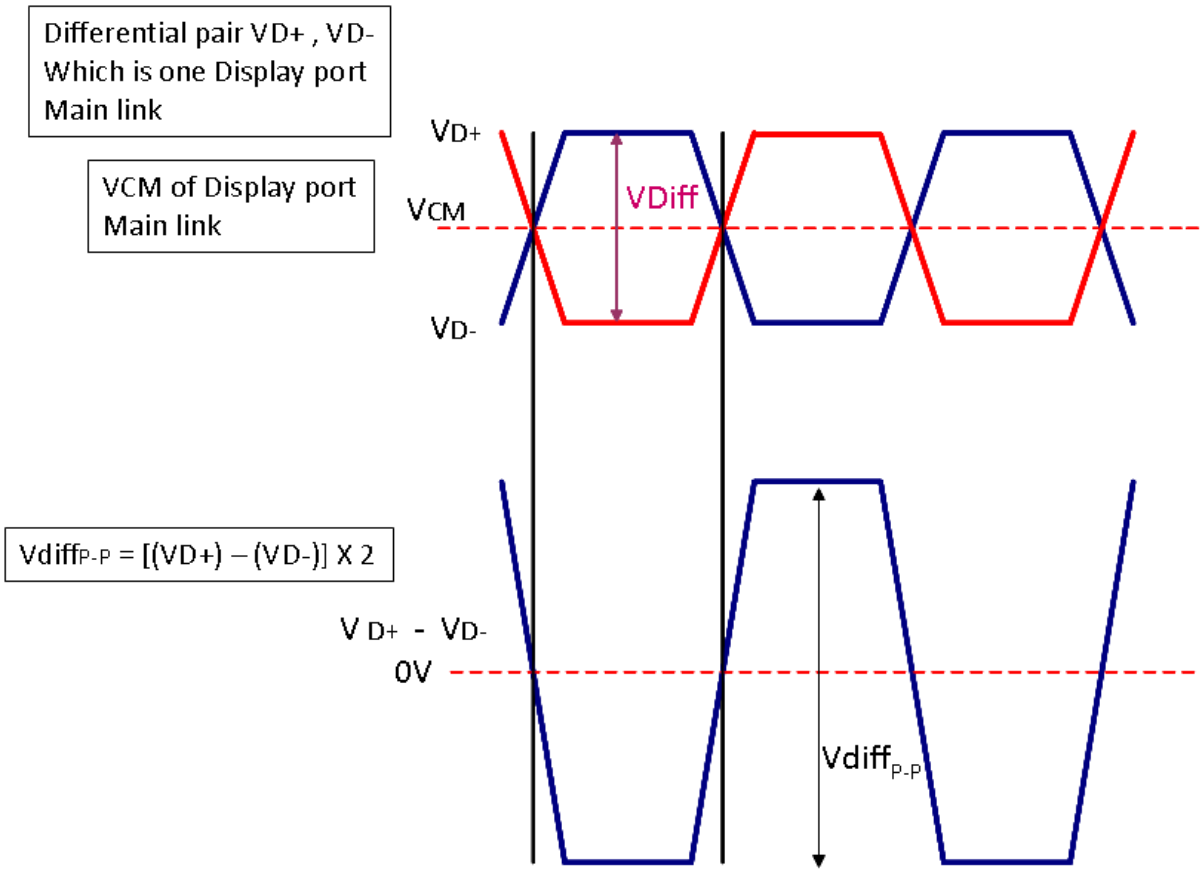
Note 2 : Measure Condition

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

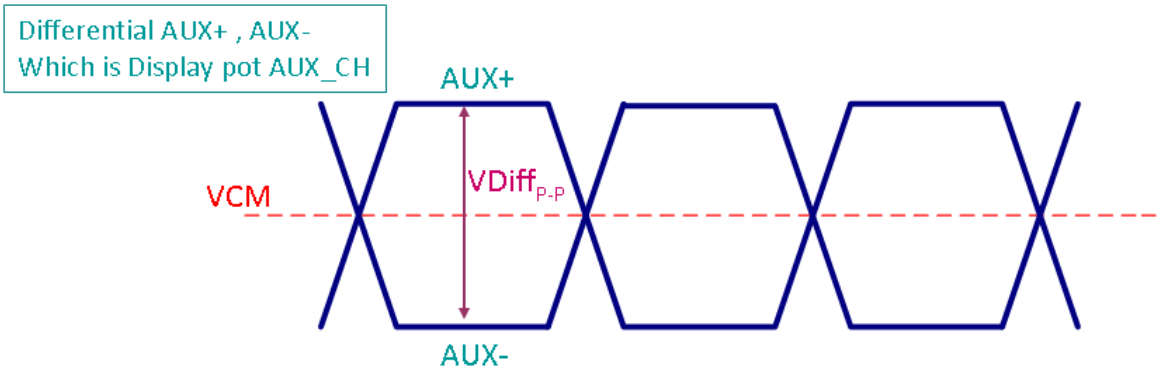
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.3

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard V1.3

Display Port V_{HPD} signal:

Display port V_{HPD}					
		Min	Typ	Max	unit
V_{HPD}	HPD Voltage	2.25		3.6	V

Fallow as VESA display port standard V1.3

5.2 Backlight Unit

5.2.1 Backlight input signal characteristics (Just for reference)

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0 Note2	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	3.3	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	3.3	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

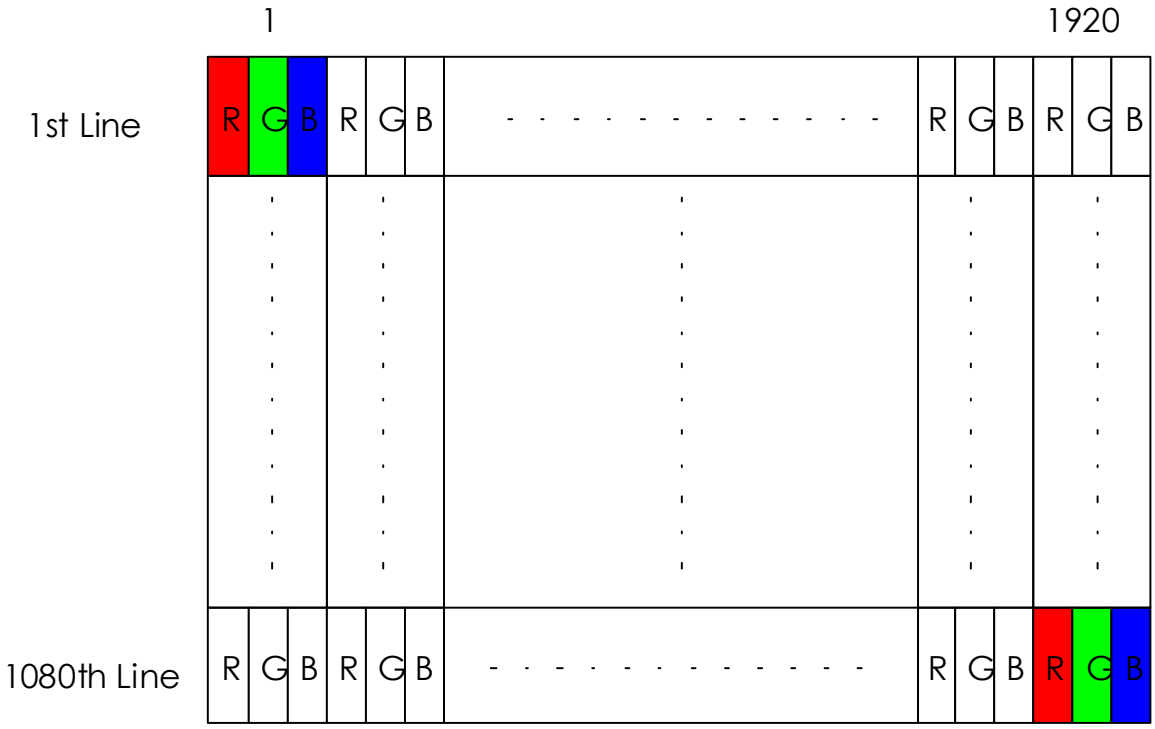
Note 1 : Recommend system pull up/down resistor no bigger than 10kohm

Note 2 : measured in panel VLED at PWM duty ratio 100%

6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Light Bar Connector Description

Light bar connector is capable of accommodating the following signals and will be following components.

Connector Name / Designation	Connector FPC
Manufacturer	STM / Starconn
Type / Part Number	MSK24022P10 / 112G10-000001-A2-R
Mating Housing/Part Number	Flexium/69.14B55.L01

6.2.2 Pin Assignment

Pin	Define	Pin	Define
1	VOUT	6	LB2
2	VOUT	7	LB3
3	VOUT	8	LB4
4	GND	9	LB5
5	LB1	10	LB6

6.2.3 Connector Description

Physical interface is described as for the connector on module.

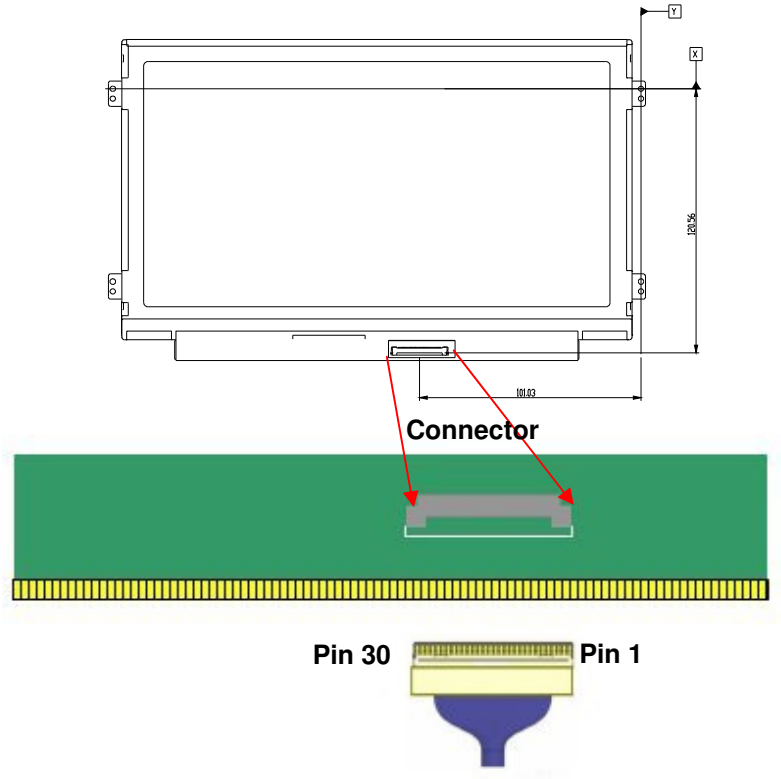
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	**For Signal Connector**
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-030E-12 or compatible
Mating Housing/Part Number	IPEX 20453-030T-11 or compatible

6.2.4 Pin Assignment (2 Lane)

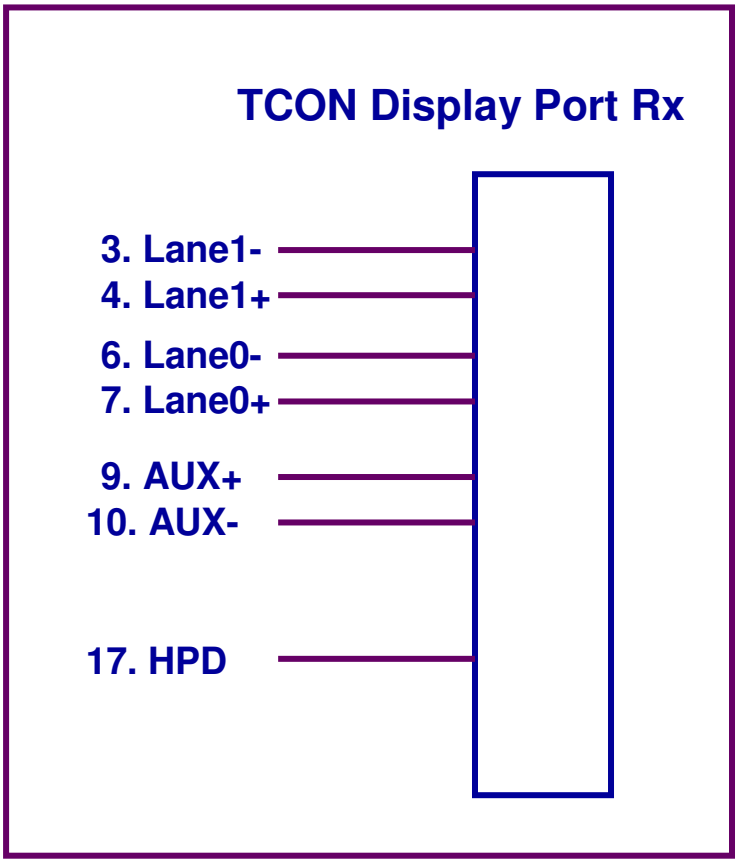
eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	DBC_EN	NC
2	H_GND	High Speed Ground
3	Lane1_N	Complement Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Complement Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Complement Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	BIST	LCD Panel Self Test Enable
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	Hot Plug Detection signal pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	NC	Reverse for AUO TEST only
25	NC	Reverse for AUO TEST only
26	BL_PWR	Backlight power (5.5V~21V)
27	BL_PWR	Backlight power (5.5V~21V)
28	BL_PWR	Backlight power (5.5V~21V)
29	BL_PWR	Backlight power (5.5V~21V)
30	COLOR_EN	NC



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3 Interface Timing

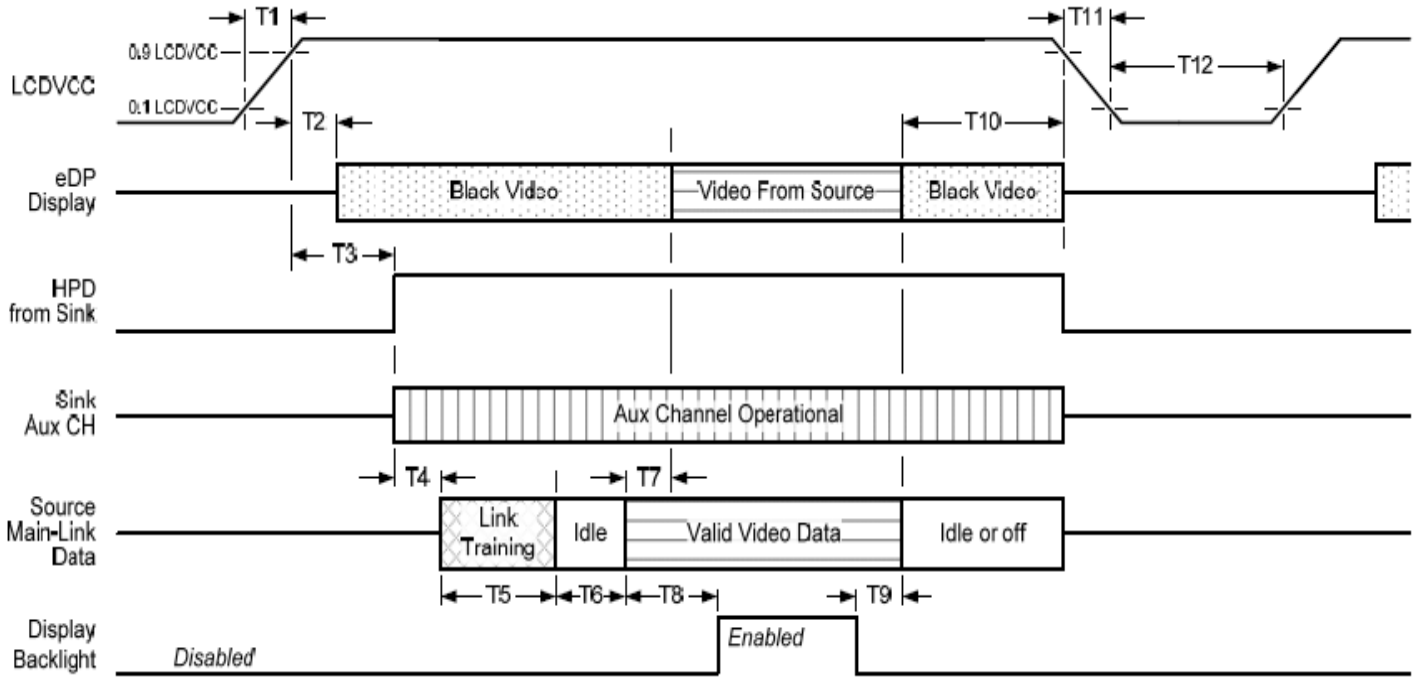
6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

TBD

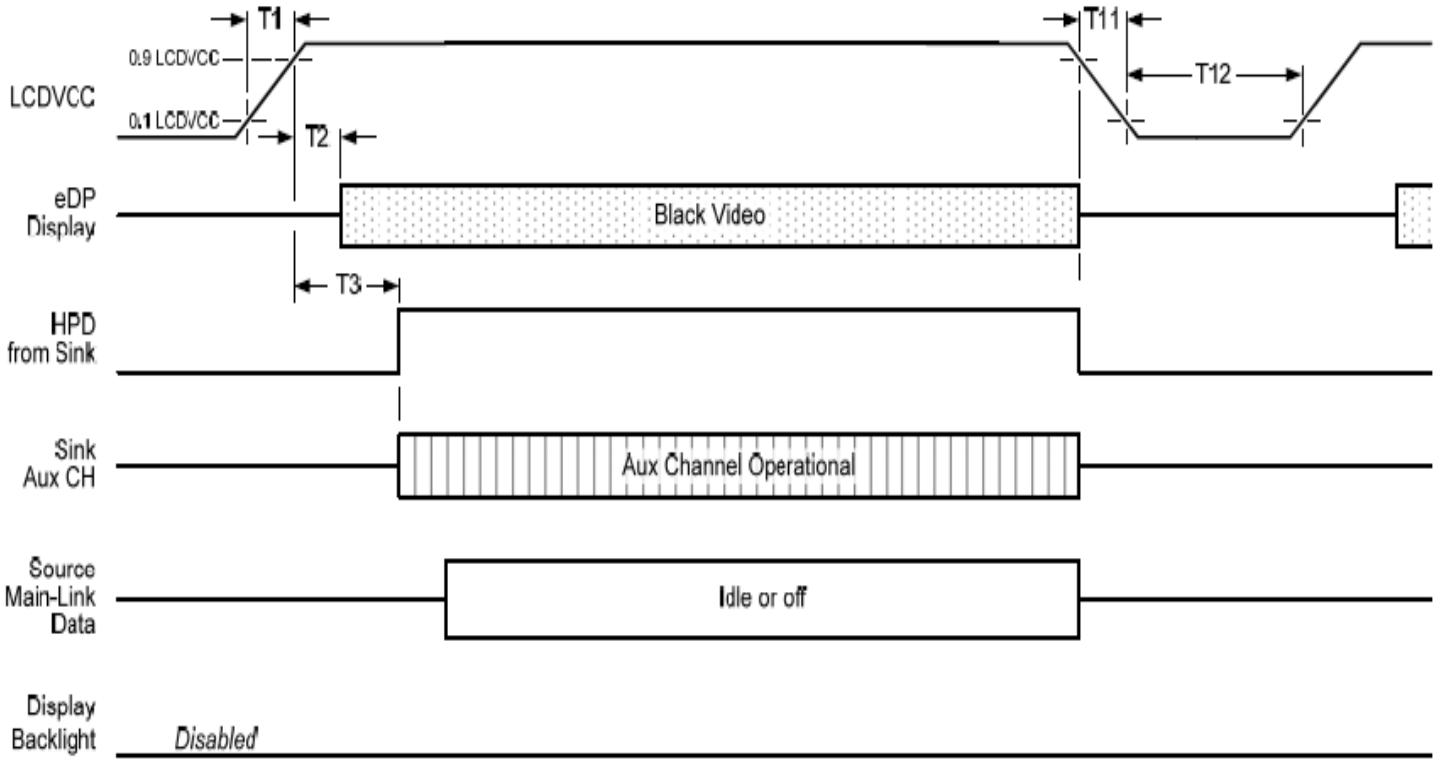
6.4 Power ON/OFF Sequence

6.4.1 Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

6.4.2 Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

6.4.3 Display Port panel power sequence timing parameter:

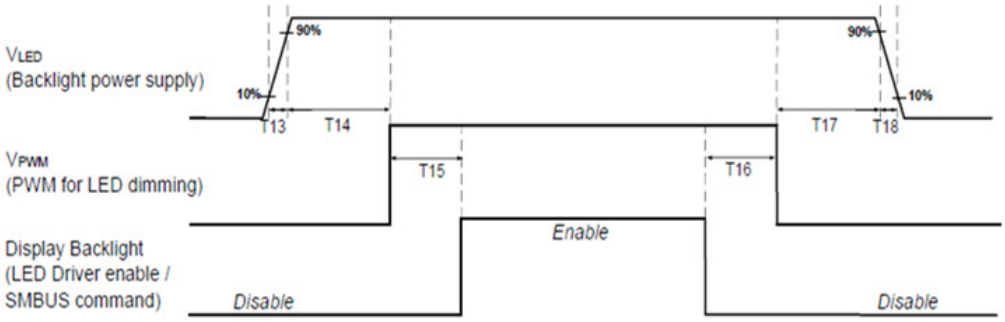
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

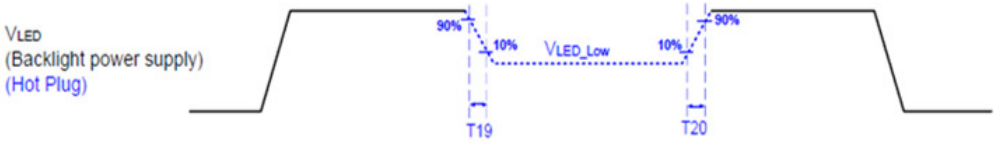
Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

6.4.4 Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



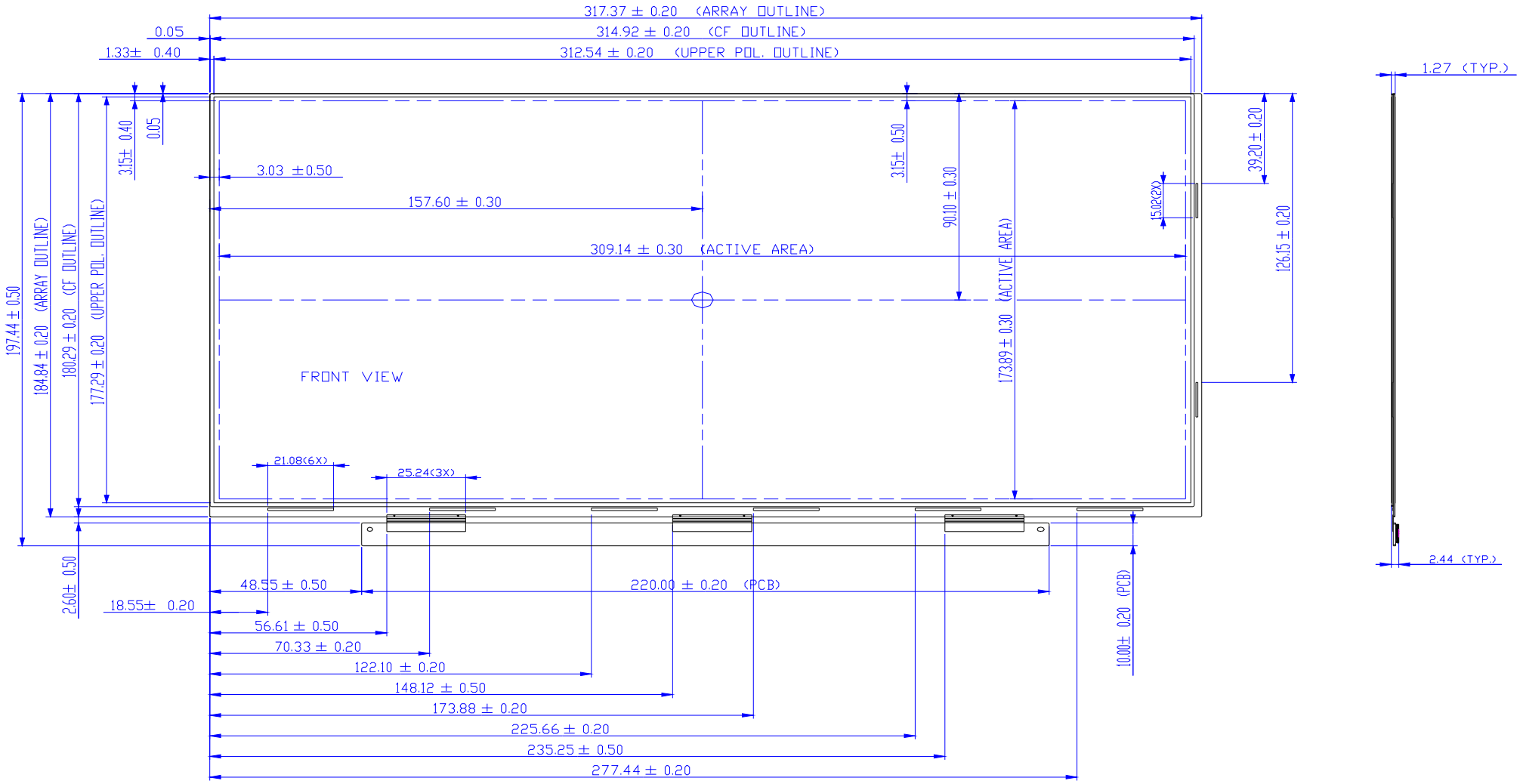
	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

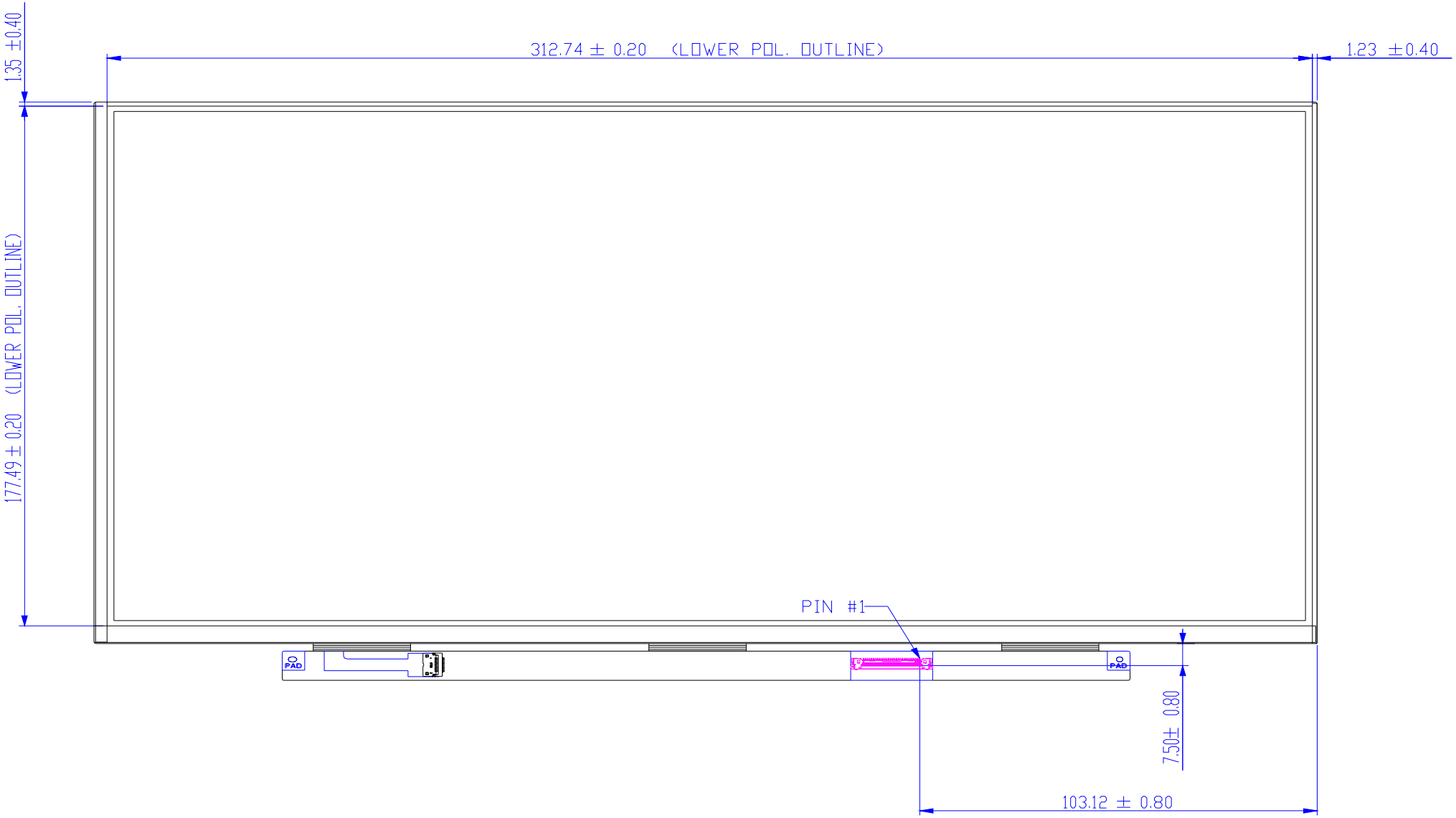
Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

7. Mechanical Characteristics

7.1 LCD Outline Dimension



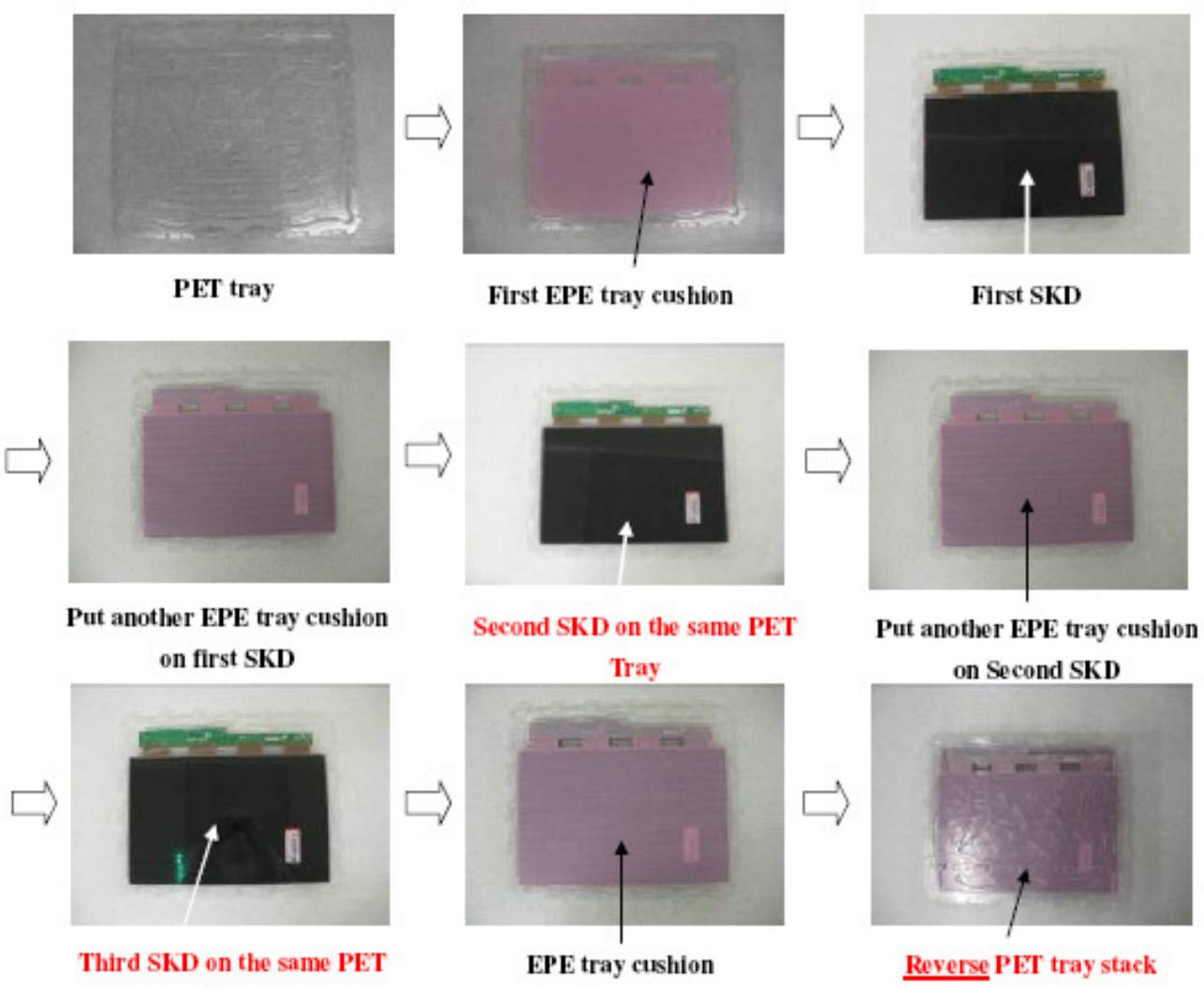

1.35 ±0.40
312.74 ± 0.20 (LOWER POL. OUTLINE)
1.23 ±0.40
177.49 ± 0.20 (LOWER POL. OUTLINE)
PIN #1
PAD
PAD
7.50± 0.80
103.12 ± 0.80

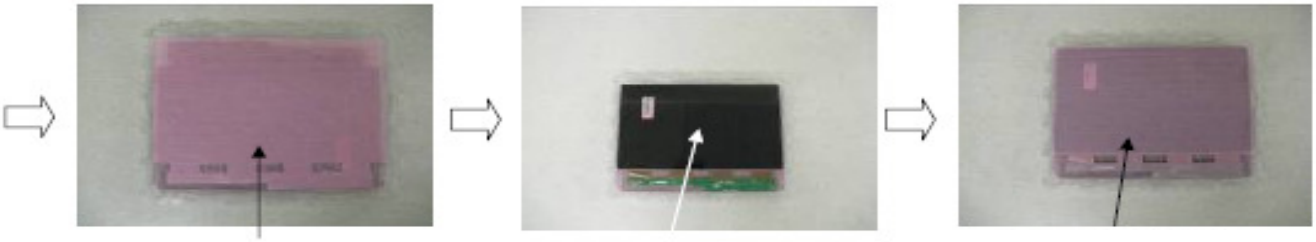
7.2 Carton Package

7.2.1 Carton label

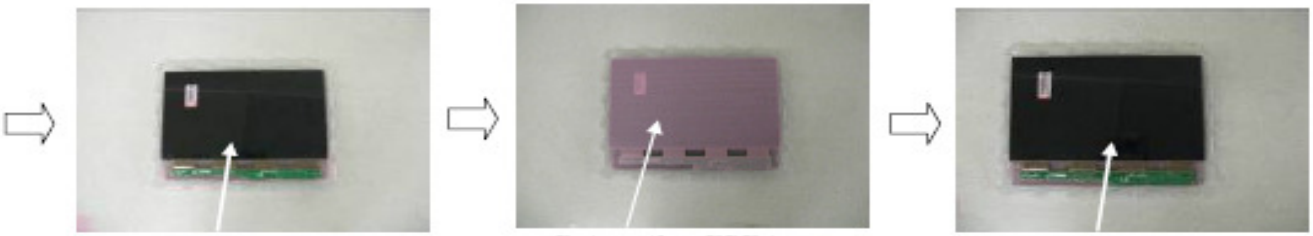
TBD

7.2.2 Packing instruction

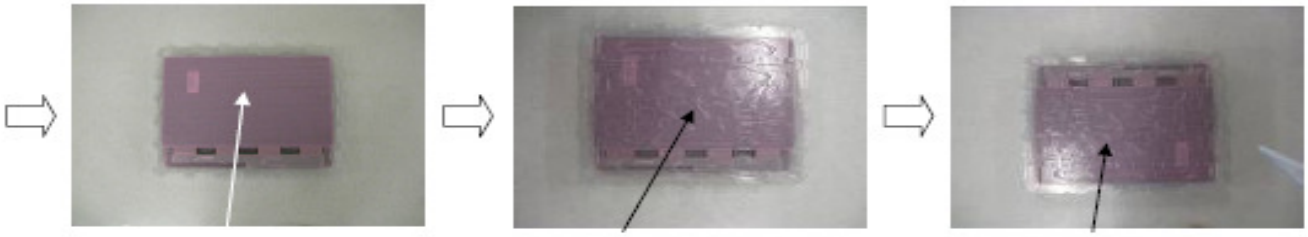




First EPE tray cushion | Reverse SKD | Put another EPE tray



Second SKD on the same PET Tray | Put another EPE tray cushion on Second SKD | Third SKD on the same PS Tray



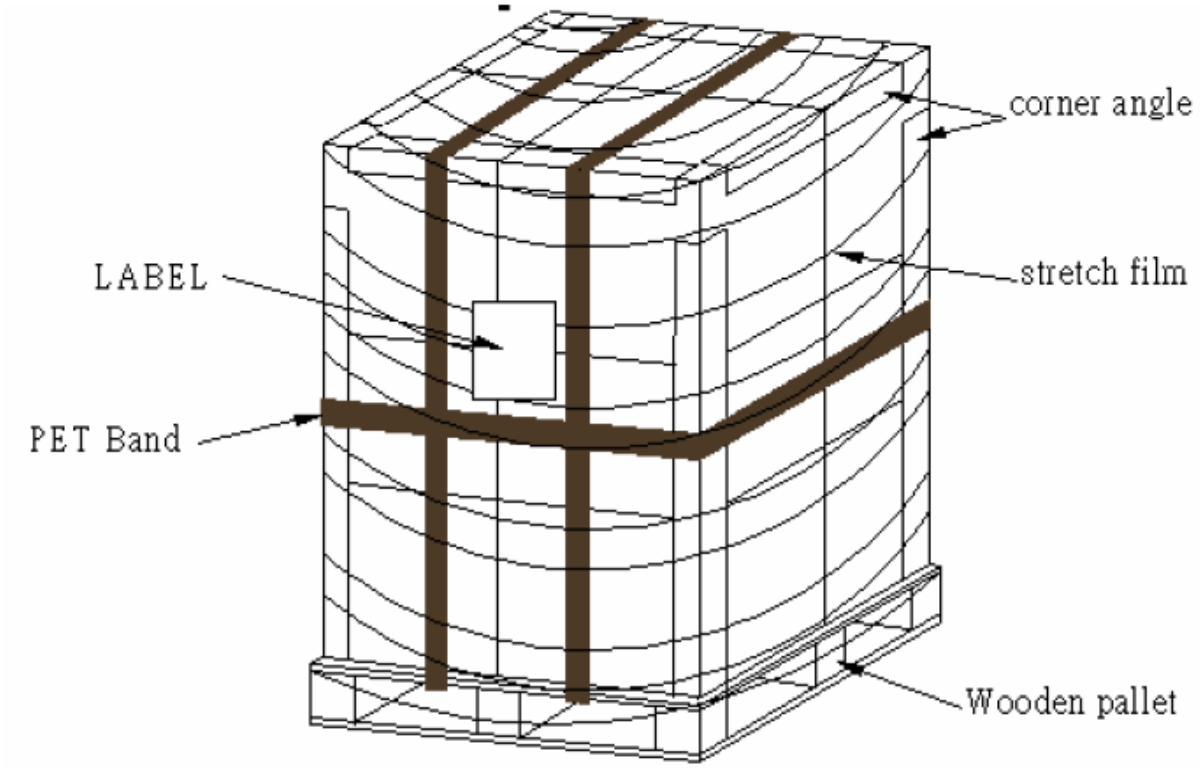
EPE tray cushion | Reverse PET tray stack again | 30 PCS SKD in 11 PCS tray

Put one PP BOARD | put 6pcs Tray Stack in the ANTI-STATIC bag | Tape fix

Put EPE bottom Cushion into Carton | Put Stack Package and EPE | Put TOP EPE Cushion into Carton

H Tape Fix

7.3 Shipping Package of Palletizing Sequence



單層 pallet 打棧示意圖

8. Appendix: EDID Description

TBD