( ) **Preliminary Specifications**
(V) **Final Specifications**

Module	**14.0" (13.98") HD+ 16:9 Color TFT-LCD with LED Backlight design**
Model Name	B140RW01 V0 (H/W:1A)
Note)	***LED Backlight with driving circuit design***

Customer	**Date**
Checked & Approved by	**Date**
Note: This Specification is subject to change without notice.	

Approved by	**Date**
Ivy Lee	04/17/2009
Prepared by	**Date**
Yiwen Chen	04/17/2009
NBBU Marketing Division AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
1.0 2009/04/16	All	First Final Spec. Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostic breakdown.

2. General Description

B140RW01 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1600(H) x900(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

BXXXEWXX VX is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	354.95			
Active Area	[mm]	309.60 X 174.15			
Pixels H x V		1600x3(RGB) x 900			
Pixel Pitch	[mm]	0.1935X0.1935			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I_{LED}=20mA) **(Note: ILED is LED current)**	[cd/m^2]	250 typ. (5 points average) 230 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	5.5 max. (Include Logic and Blu power)			
Weight	[Grams]	375 max.			
Physical Size **Include bracket**	[mm]		Min.	Typ.	Max.
		Length		323.5	324
		Width		192	192.5
		Thickness		-	5.4
Electrical Interface		2 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Glare, Hardness 3H,			
Support Color		262K colors (RGB 6-bit)			

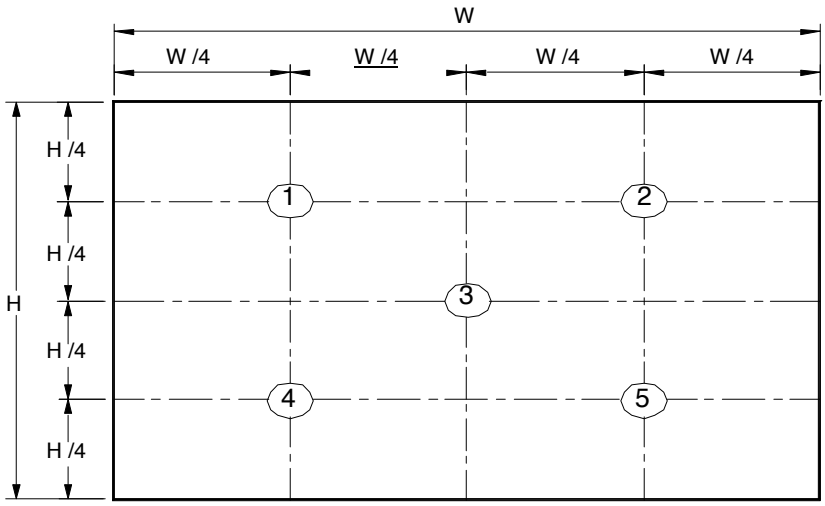
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

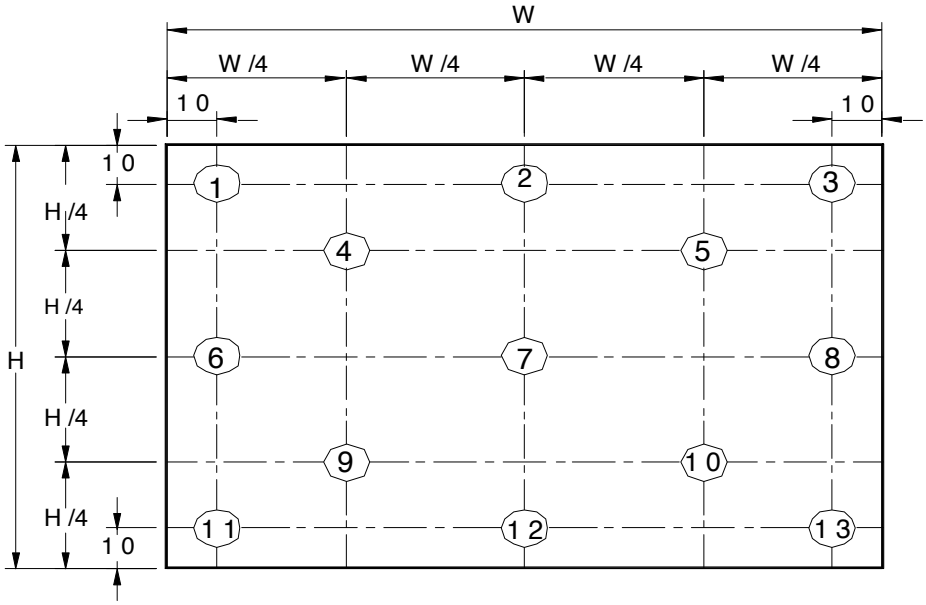
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA			5 points average	230	250	-	cd/m²1,	4, 5.
Viewing Angle		θ_R θ_L	Horizontal (Right) CR = 10 (Left)	60 60	65 65	- -	degree	4, 9
		ψ_H ψ_L	Vertical (Upper) CR = 10 (Lower)	50 50	55 55	- -		
Luminance Uniformity		δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity		δ_{13P}	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio		CR		400	500	-		4, 6
Cross talk		%				4		4, 7
Response Time		T_r	Rising	-	6	11.5	msec	4, 8
		T_f	Falling	-	2	4.5		
		T_{RT}	Rising + Falling	-	8	16		
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.590	0.620	0.650		4
		Ry		0.310	0.340	0.370		
	Green	Gx		0.300	0.330	0.360		
		Gy		0.540	0.570	0.600		
	Blue	Bx		0.120	0.150	0.180		
		By		0.030	0.060	0.090		
	White	Wx		0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		
NTSC		%		-	60	-		

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

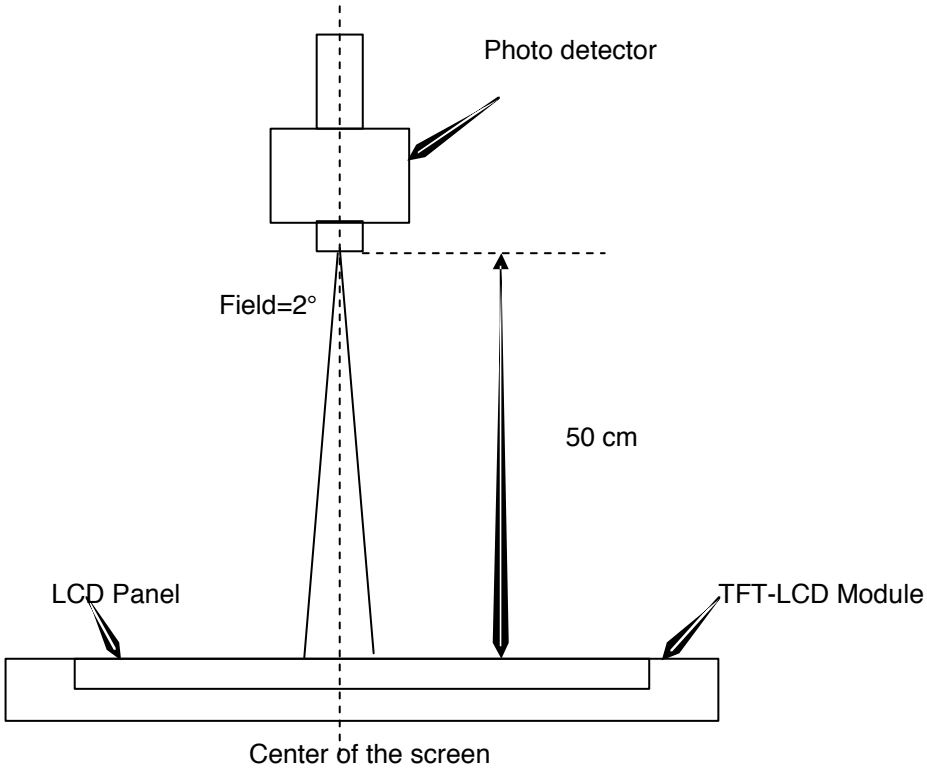
$$\delta W_5 = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta W_{13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

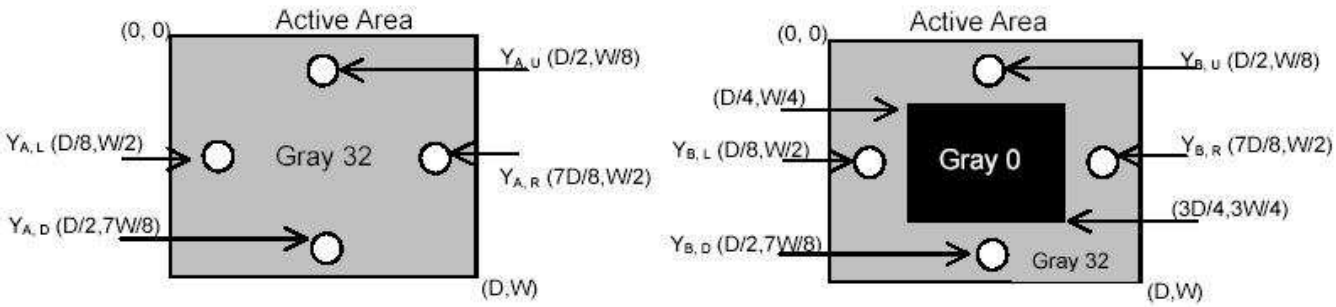
Note 7 Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where

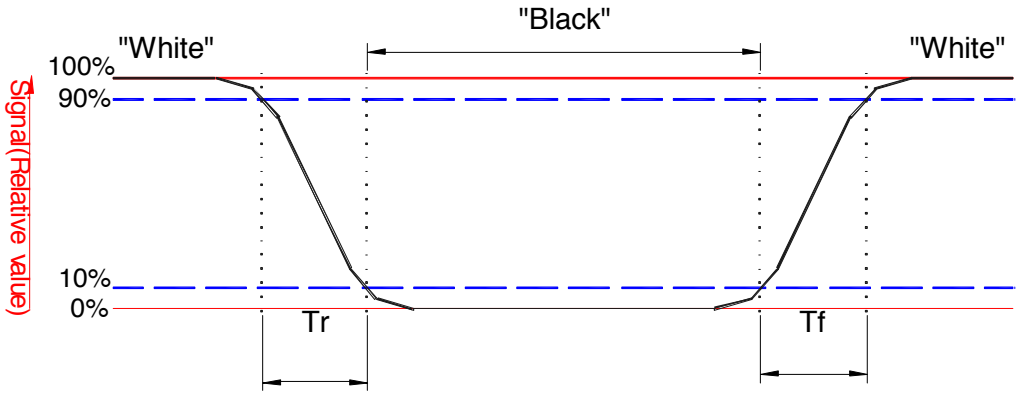
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



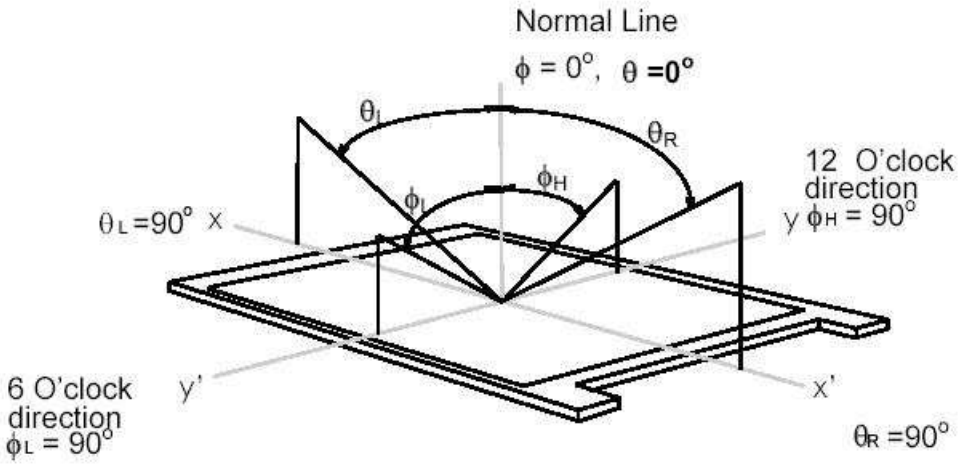
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



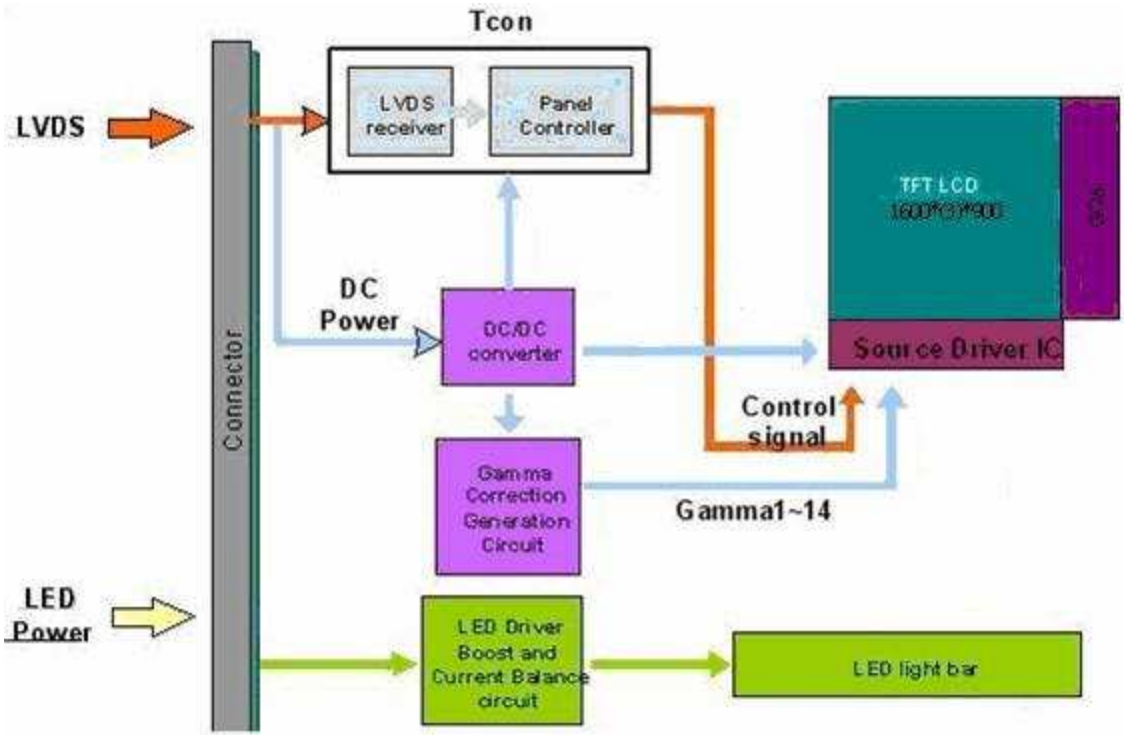
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14.0 inches wide Color TFT/LCD 40 Pin one channel Module



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

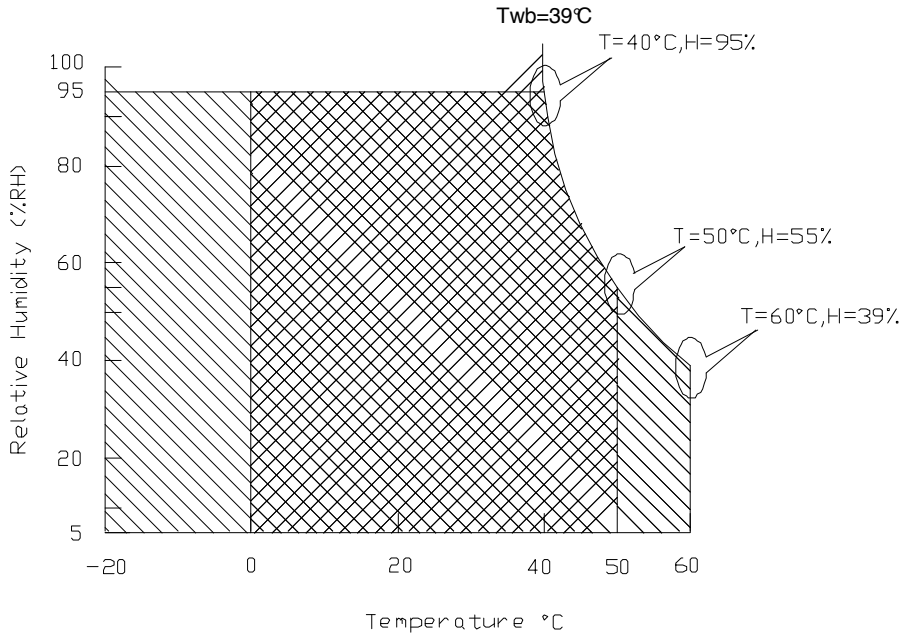
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[℃]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[℃]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

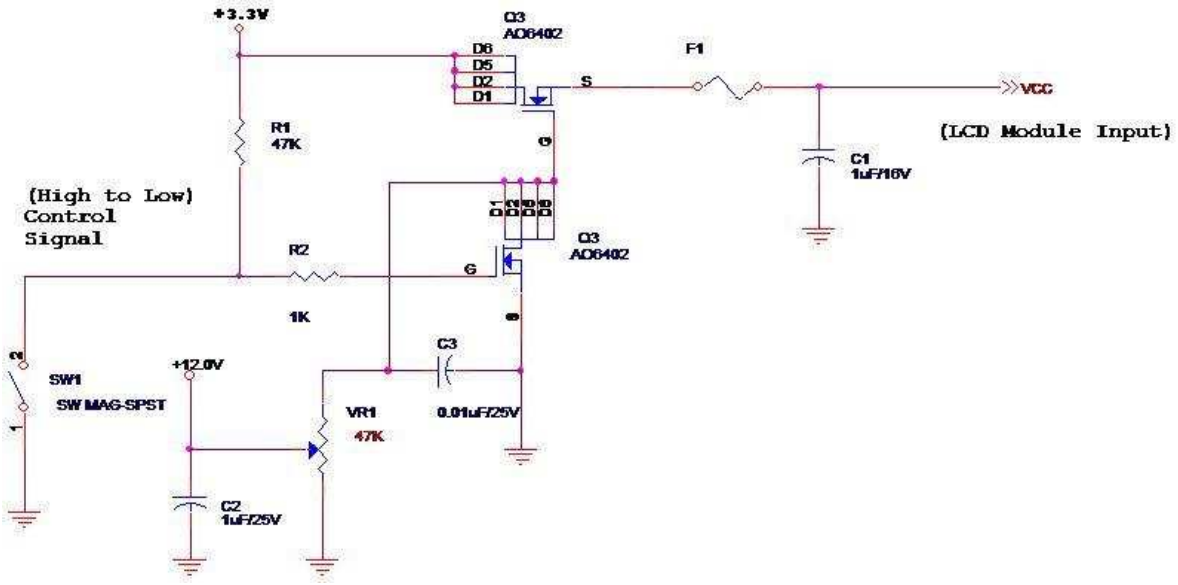
Input power specifications are as follows;

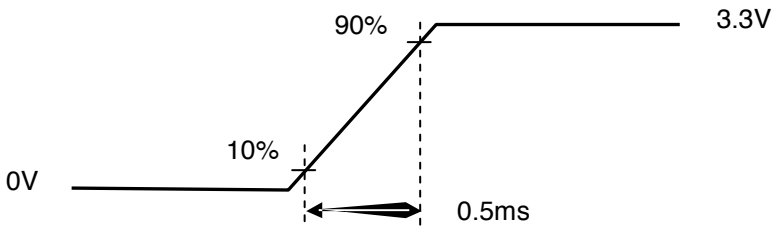
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.5	[Watt]	Note 1
IDD	IDD Current	-	-	454	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition Black Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{black}$)

Note 2 Measure Condition





Vin rising time

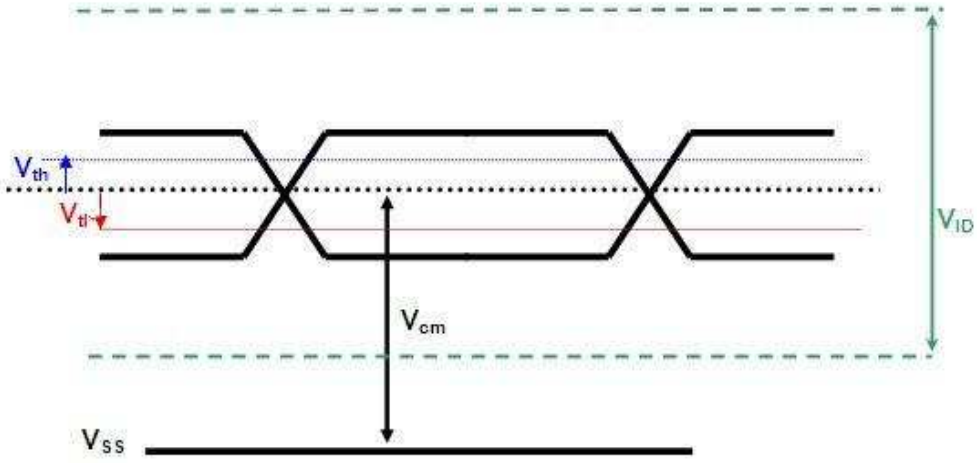
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
V_{tl}	Differential Input Low Threshold (Vcm=+1.2V)	-100	-	[mV]
V_{ID}	Differential Input Voltage	100	-	[mV]
V_{cm}	Differential Input Common Mode Voltage	0.05	1.9	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.67	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

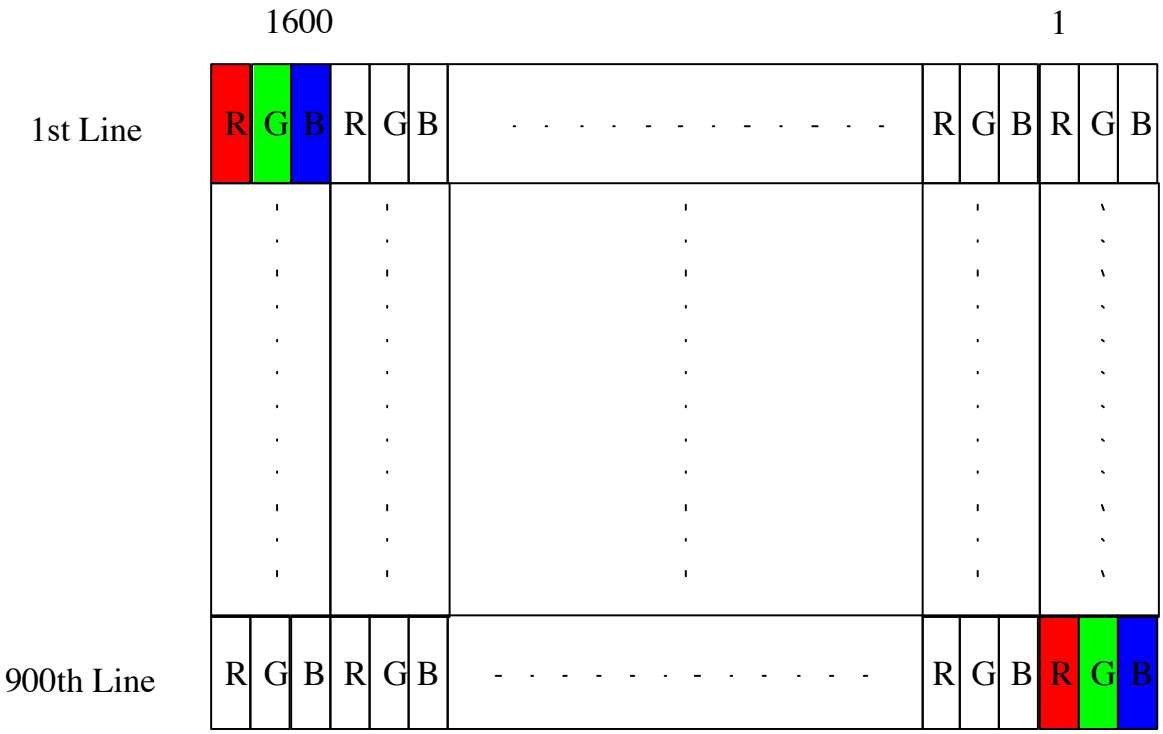
5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	100	-	20K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

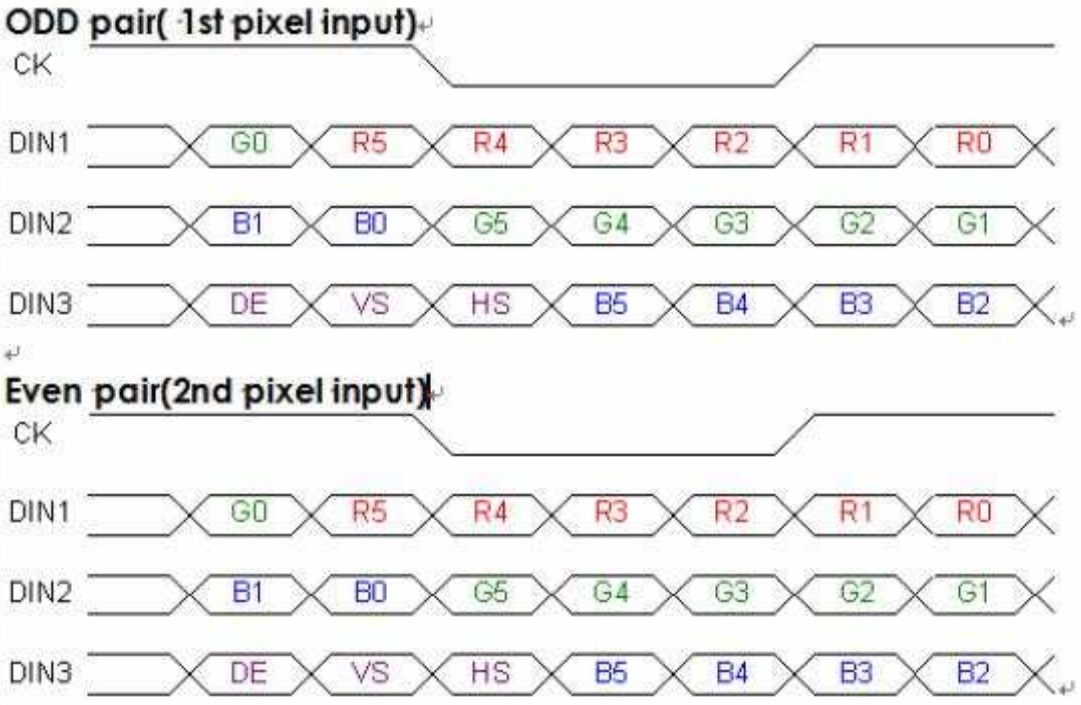
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock data and	The signal is used to strobe the pixel DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.

DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

6.3 Integration Interface Requirement

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

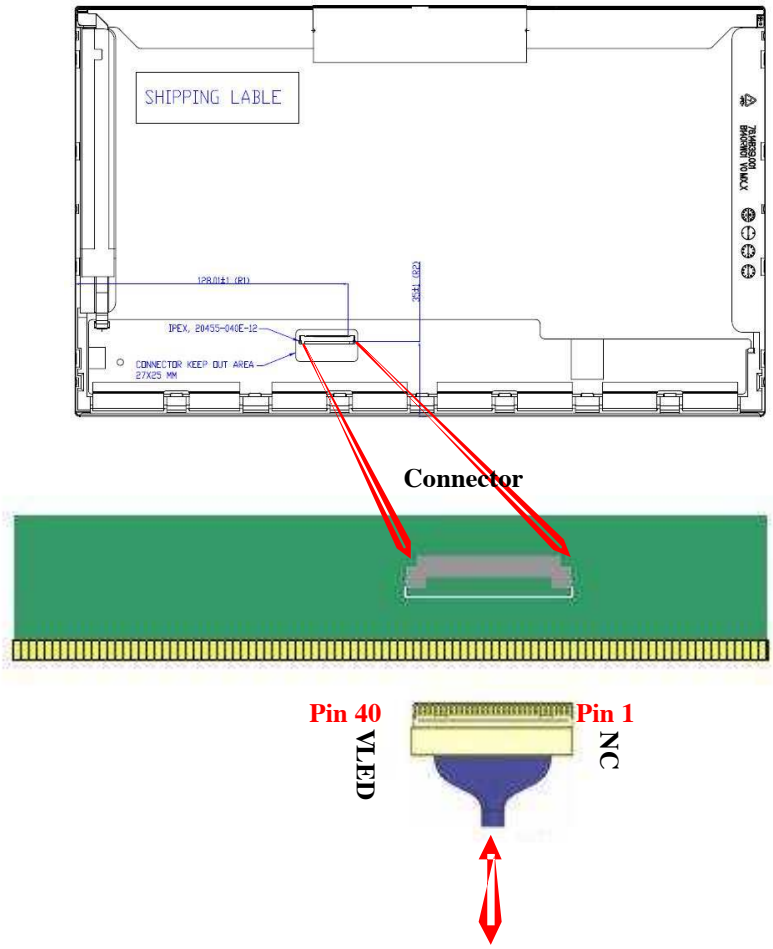
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or Compatiable
Type / Part Number	IPEX 20455-040E-12A or Compatiable
Mating Housing/Part Number	IPEX 20453-040T-11 or Compatiable

6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	DIAG_LOOP	Diag pin for Dell testing. Pin 1 & 34 must be connected together on the inverter board
2	VDD	Power Supply, 3.3 V (typical)
3	VDD	Power Supply, 3.3 V (typical)
4	V EEDID	DDC 3.3V power
5	TEST	Panel Self Test
6	Clk EEDID	DDC Clock
7	DATA EEDID	DDC Data
8	Odd_Rin0-	- LVDS differential data input (R0-R5, G0) (odd pixels)
9	Odd_Rin0+	+ LVDS differential data input (R0-R5, G0) (odd pixels)
10	VSS	Ground – Shield
11	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
12	Odd_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
13	VSS	Ground – Shield
14	Odd_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
15	Odd_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
16	VSS	Ground – Shield
17	Odd_ClkIN-	- LVDS differential clock input (odd pixels)
18	Odd_ClkIN+	+ LVDS differential clock input (odd pixels)
19	VSS	Ground – Shield
20	Even_Rin0-	- LVDS differential data input (R0-R5, G0) (even pixels)
21	Even_Rin0+	+ LVDS differential data input (R0-R5, G0) (even pixels)
22	VSS	Ground – Shield

23	Even_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (even pixels)
24	Even_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (even pixels)
25	VSS	Ground – Shield
26	Even_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
27	Even_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (even pixels)
28	VSS	Ground – Shield
29	Even_ClkIN-	- LVDS differential clock input (even pixels)
30	Even_ClkIN+	+ LVDS differential clock input (even pixels)
31	VSSLED	Ground - LED
32	VSSLED	Ground - LED
33	VSSLED	Ground - LED
34	DIAG_LOOP	Diag pin for Dell testing. Pin 1 & 34 must be connected together on the inverter board
35	PWM	System PWM Signal Input (+3.3V Swing)
36	LED_EN	LED enable pin (+3.3V Input)
37	NC	NC
38	VDDLED	7.5V – 21V LED power
39	VDDLED	7.5V – 21V LED power
40	VDDLED	7.5V – 21V LED power



Note1: Input signals shall be low or High-impedance state when VDD is off.

6.4 Interface Timing

6.4.1 Timing Characteristics

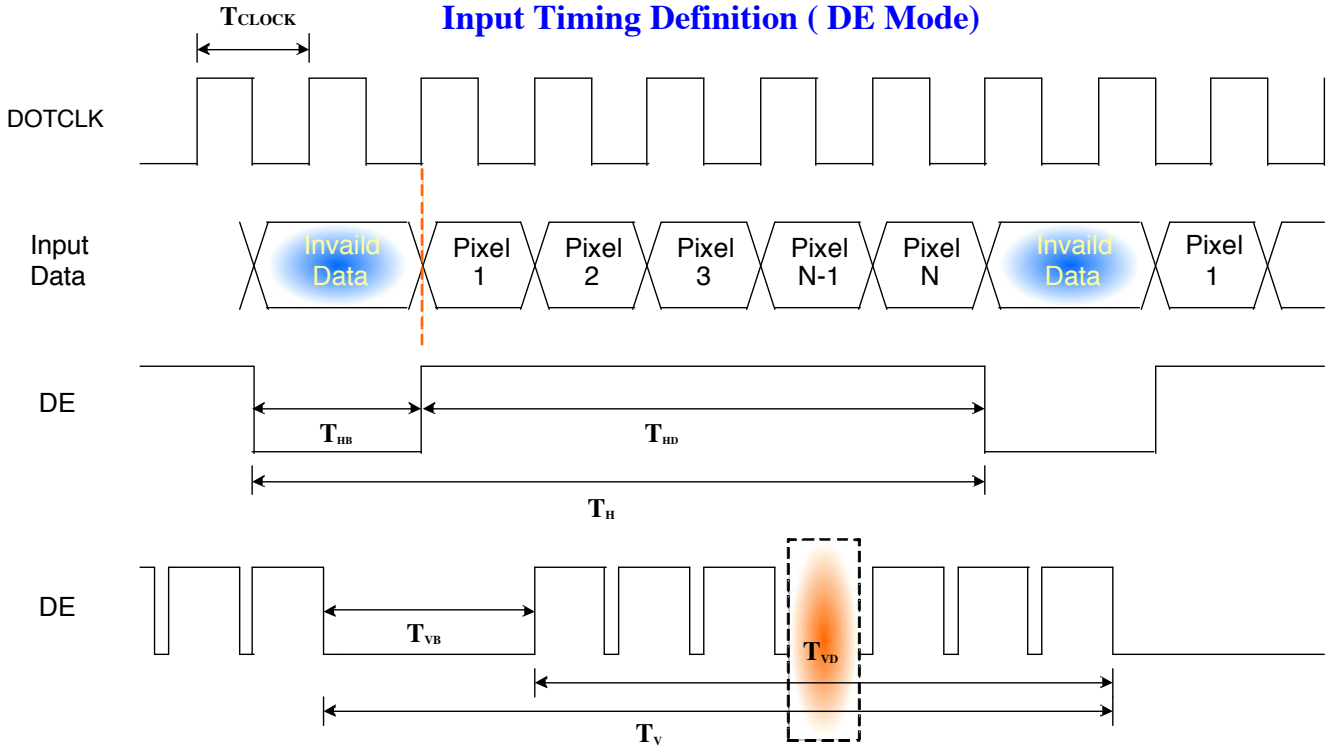
Basically, interface timings should match the 1600x900 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ T_{Clock}	20	53	85	MHz
Vertical Section	Period	T_V	908	912	2047	TLine
	Active	T_{VD}	900			
	Blanking	T_{VB}	8	12	-	
Horizontal Section	Period	T_H	830	965	1024	TClock
	Active	T_{HD}	800			
	Blanking	T_{HB}	30	165	-	

Note : DE mode only

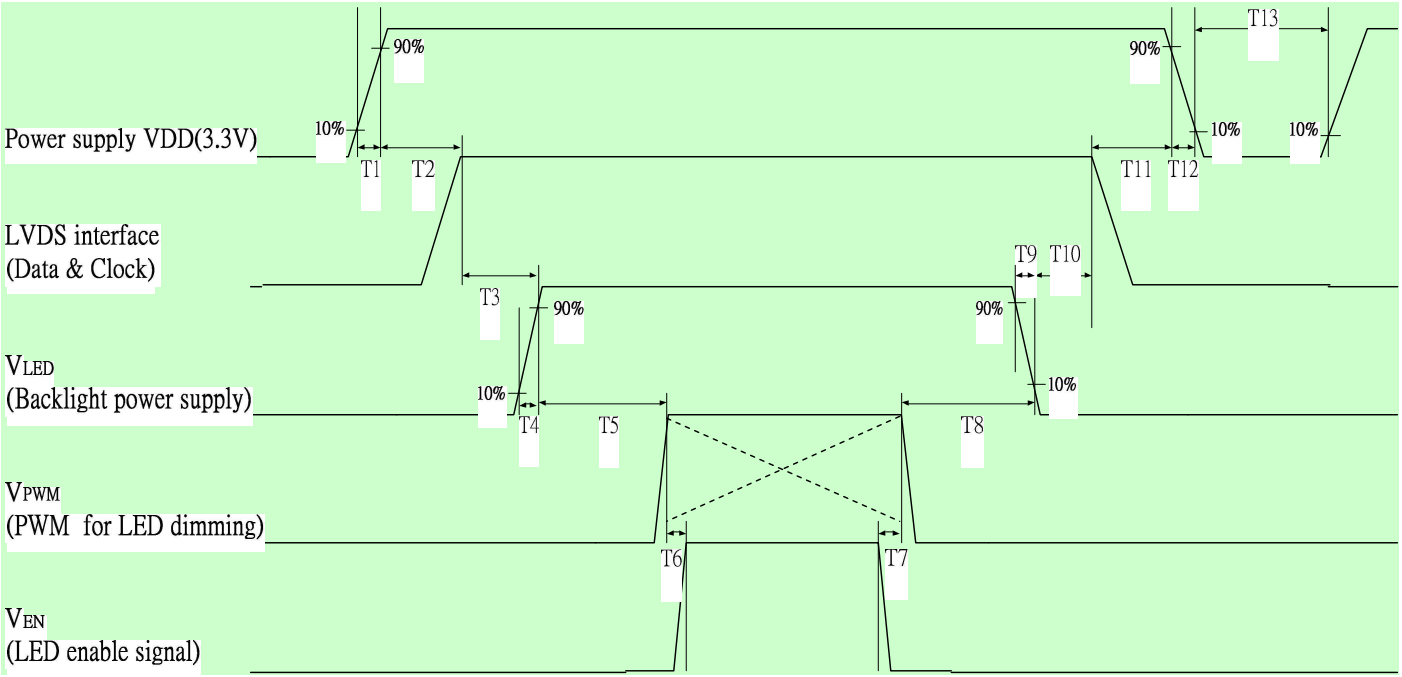
6.4.2 Timing diagram

Input Timing Definition (DE Mode)



6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Power Sequence Timing				
Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	5	-	50	
T3	0.5	-	50	
T4	400	-	-	
T5	200	-	-	
T6	200	-	-	
T7	0.5	-	10	
T8	10	-	---	
T9	10	-	---	
T10	10	-	---	
T11	10	-	---	
T12	0.5	-	10	
T13	5	-	50	

Note:If T3,T5,T6 couldn't match above specifications, must request T3+T5+T6 > 200ms at least

7. Panel Reliability Test

7.1 Vibration Test

Test Spec:

Test method: Non-Operation
Acceleration: 1.5 G
Frequency: 10 - 500Hz Random
Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test

Test Spec:

Test method: Non-Operation
Acceleration: 220 G , Half sine wave
Active time: 2 ms
Pulse: X,Y,Z .one time for each side

7.3 Reliability Test

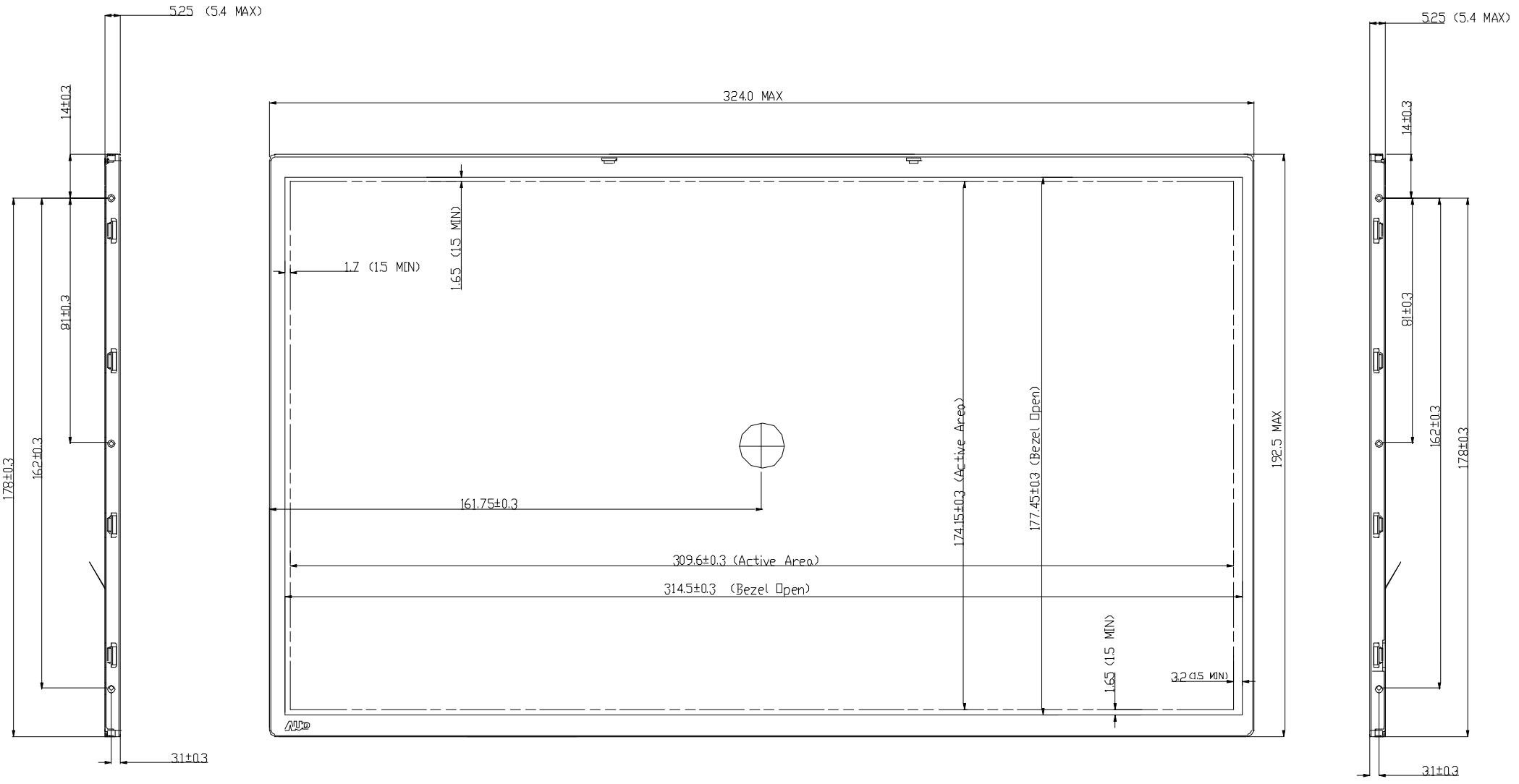
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 250h	
Thermal Shock Test	Ta=-20°Cto 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

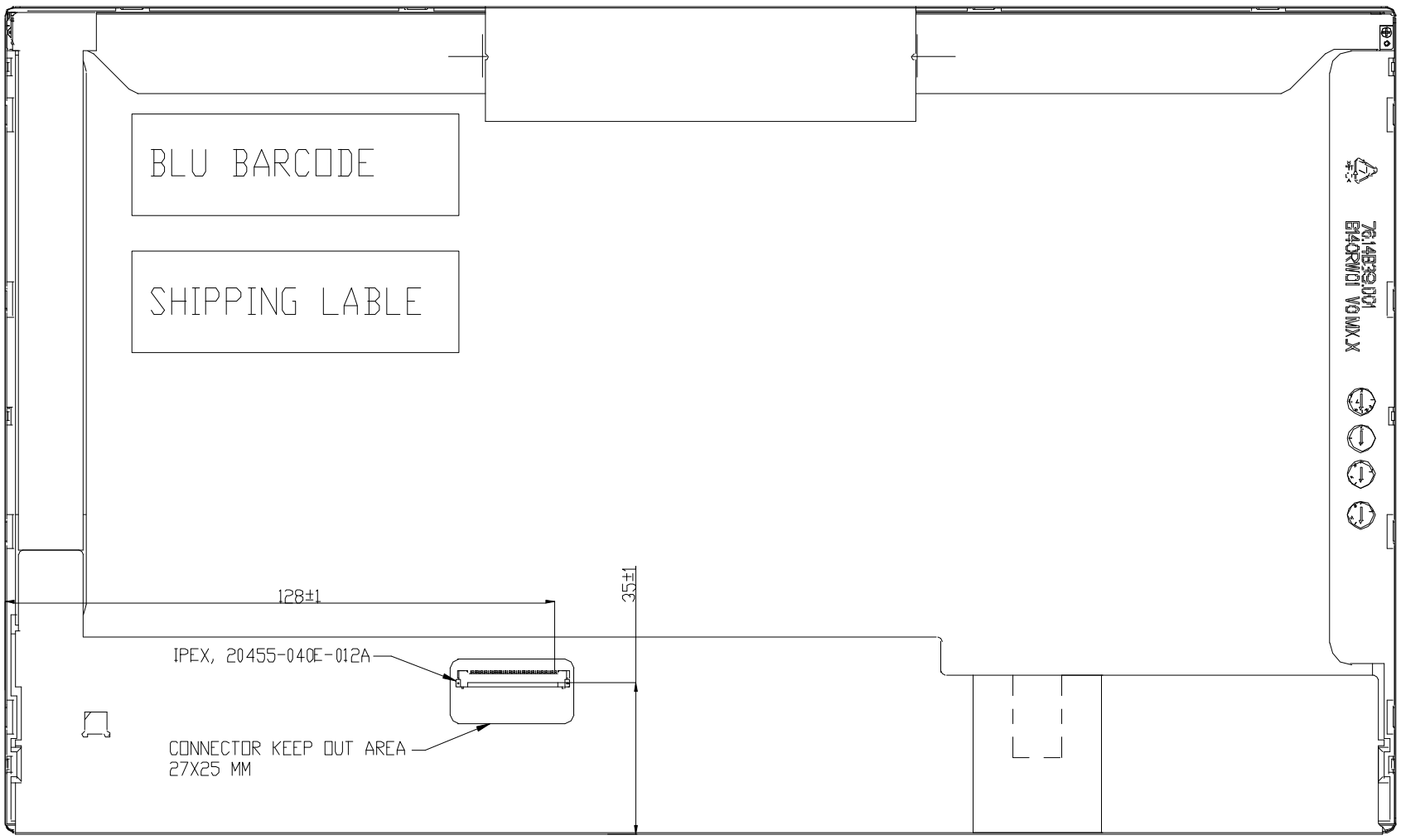
Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

8. Mechanical Characteristics

8.1 LCM Outline Dimension





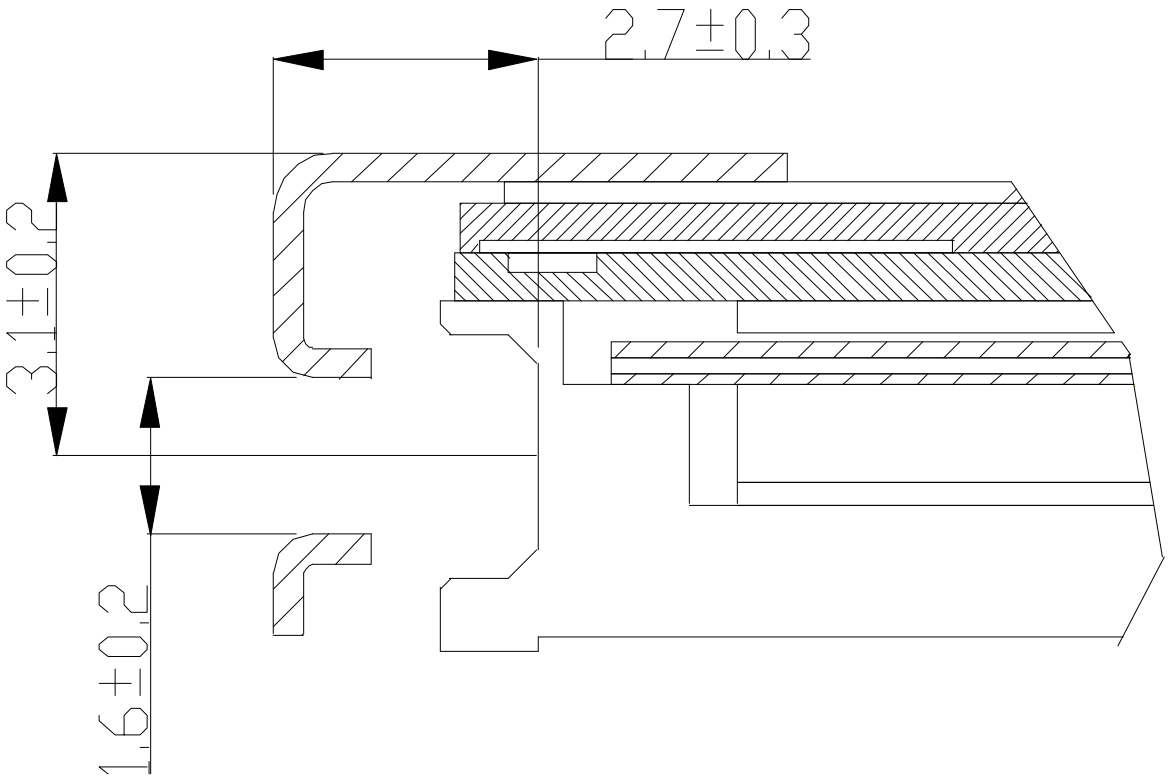
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

8.2 Screw Hole Depth and Center Position

Maximum Screw penetration from side surface is **2.4 mm**

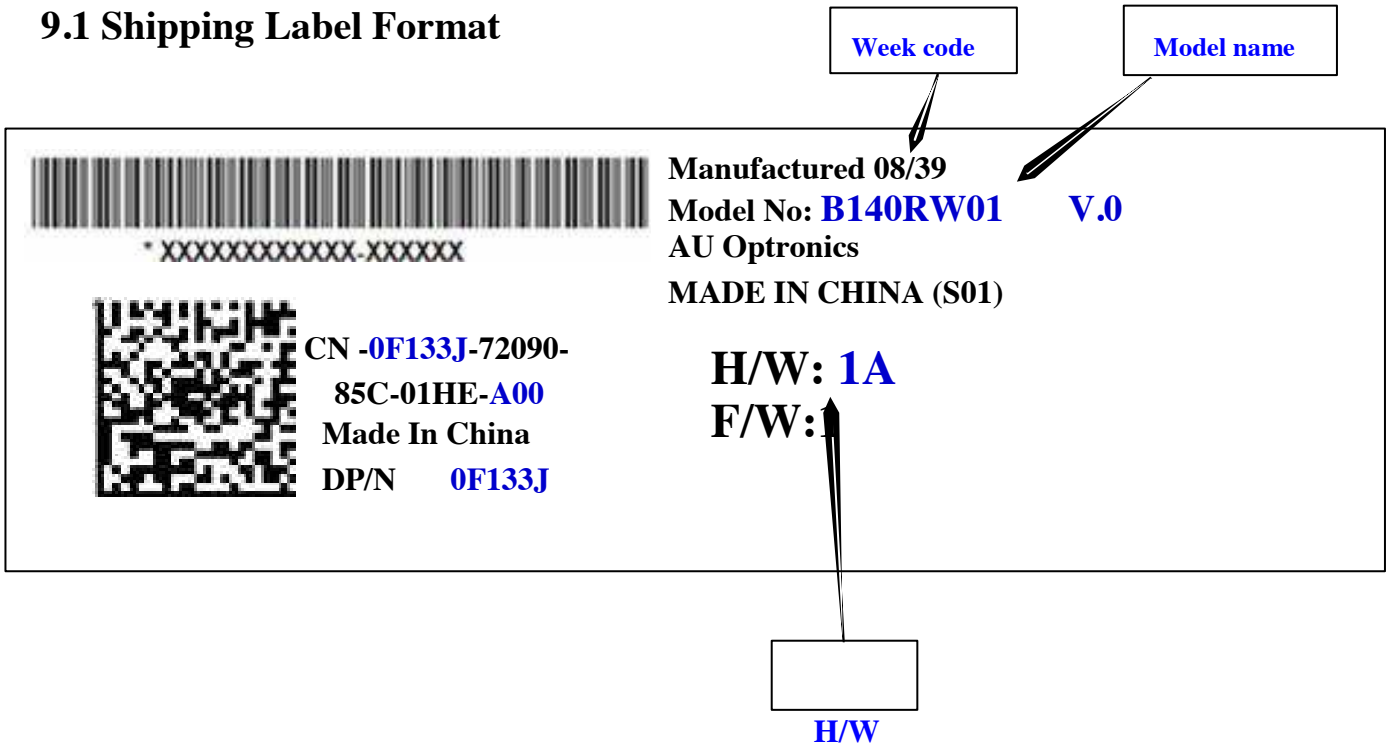
The center of screw hole center location is **3.1** ± 0.2mm from front surface

Screw Torque: Maximum 2.5 kgf-cm



9. Shipping and Package

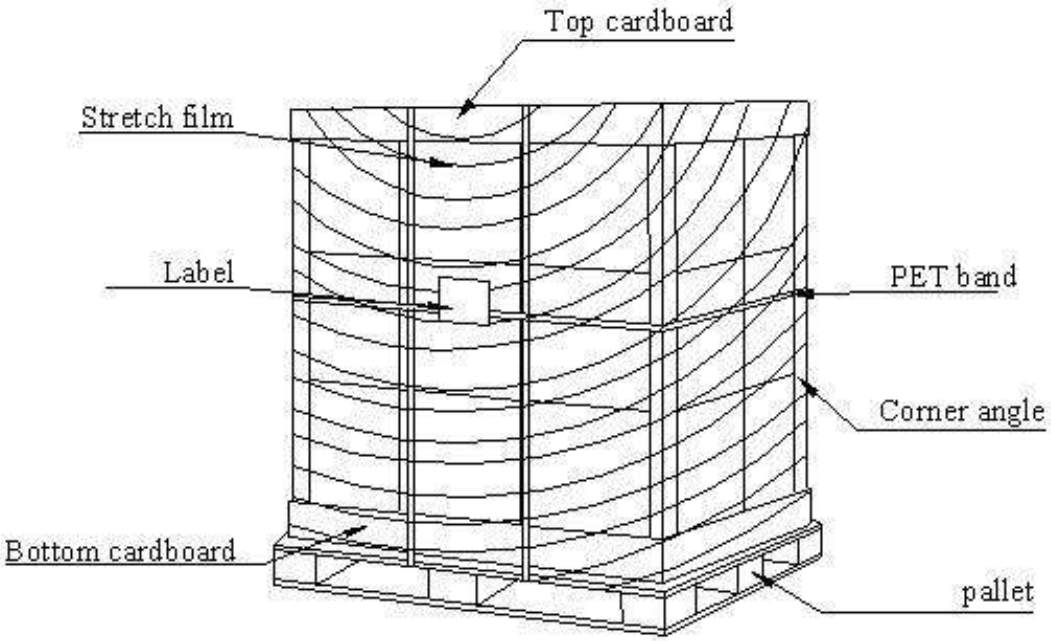
9.1 Shipping Label Format



9.2 Carton Package

The outside dimension of carton is 405(L)mm* 376(W)mm* 302(H)mm

9.3 Shipping Package of Palletizing Sequence



10. Appendix: EDID Description

	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
	0	Header	00	00000000	0
	1	Header	FF	11111111	255
	2	Header	FF	11111111	255
	3	Header	FF	11111111	255
	4	Header	FF	11111111	255
	5	Header	FF	11111111	255
	6	Header	FF	11111111	255
	7	Header	00	00000000	0
	8	EISA manufacture code = 3 Character ID	06	00000110	6
	9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
	0A	Panel Supplier Reserved – Product Code	3E	00111110	62
	0B	Panel Supplier Reserved – Product Code	10	00010000	16
	0C	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
	0D	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
	0E	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
	0F	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000	0
	10	Week of manufacture	01	00000001	1
	11	Year of manufacture	13	00010011	19
	12	EDID structure version # = 1	01	00000001	1
	13	EDID revision # = 3	03	00000011	3
	14	Video I/P definition = Digital I/P (90 (6-bit) or A0 (8-Bit))	90	10010000	144
	15	Max H image size = 31 cm(Rounded to cm)	1F	00011111	31
	16	Max V image size = 17 cm(Rounded to cm)	11	00010001	17
		Display gamma = (gamma Ч100)-100 = Example:			
	17	(2.2Ч100) – 100 = 120 Feature support (no DPMS, Active off, RGB, timing	78	01111000	120
	18	BLK 1) ==> fix=0A	0A	00001010	10
	19	Red/Green Low bit (RxRy/GxGy)			
	1A	Blue/White Low bit (BxBy/WxWy)			
	1B	Red X Rx = 0.620			
	1C	Red Y Ry = 0.340			
	1D	Green X Rx = 0.330			

C8	11001000	200
95	10010101	149
9E	10011110	158
57	01010111	87
54	01010100	84

Header

Display Parameters

	1E	Green Y Ry = 0.570	92	10010010	146
	1F	Blue X Rx = 0.150	26	00100110	38
	20	Blue Y Ry = 0.060	0F	00001111	15
	21	White X Rx = 0.313	50	01010000	80
	22	White Y Ry = 0.329	54	01010100	84
	23	Established timings 1 (00h if not used)	00	00000000	0
	24	Established timings 2 (00h if not used)	00	00000000	0
	25	Manufacturer's timings (00h if not used)	00	00000000	0
	26	Standard timing ID1 (01h if not used)	01	00000001	1
	27	Standard timing ID1 (01h if not used)	01	00000001	1
	28	Standard timing ID2 (01h if not used)	01	00000001	1
	29	Standard timing ID2 (01h if not used)	01	00000001	1
	2A	Standard timing ID3 (01h if not used)	01	00000001	1
	2B	Standard timing ID3 (01h if not used)	01	00000001	1
	2C	Standard timing ID4 (01h if not used)	01	00000001	1
	2D	Standard timing ID4 (01h if not used)	01	00000001	1
	2E	Standard timing ID5 (01h if not used)	01	00000001	1
	2F	Standard timing ID5 (01h if not used)	01	00000001	1
	30	Standard timing ID6 (01h if not used)	01	00000001	1
	31	Standard timing ID6 (01h if not used)	01	00000001	1
	32	Standard timing ID7 (01h if not used)	01	00000001	1
	33	Standard timing ID7 (01h if not used)	01	00000001	1
	34	Standard timing ID8 (01h if not used)	01	00000001	1
	35	Standard timing ID8 (01h if not used)	01	00000001	1
	36	Pixel Clock/10,000 (LSB)			
		01101000		104	
	37	Pixel Clock/10,000 (MSB)			
		00101001		41	
	38	Horizontal Active = 1600 pixels (lower 8 bits)			
		64			
	39	Horizontal Blanking (Thbp) = 330 pixels (lower 8 bits)	4A	01001010	74
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	61	01100001	97
	3B	Vertical Active = 900 lines	84	10000100	132
	3C	Vertical Blanking (Tvbp) = 12 lines (DE Blanking typ. for DE only panels)	0C	00001100	12
		Vertical Active : Vertical Blanking (Tvbp)			
	3D	(upper4:4 bits)	30	00110000	48
	3E	Horizontal Sync. Offset (Thfp) = 64 pixels			

Horizontal Sync, Pulse Width = 42 pixels	40	01000000	64
	2A	00101010	42

Established Timings

Timing Descripte r#1

	40	Vertical Sync, Offset (Tvfp) = 3 lines Sync Width = 3 lines	33	00110011	51	
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0	
	42	Horizontal Image Size =309.6 mm	35	00110101	53	
	43	Vertical image Size = 174.15 mm	AE	10101110	174	
	44	Horizontal Image Size / Vertical image size	10	00010000	16	
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0	
	46	Vertical Border = 0 (Zero for Notebook LCD) Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3==>	00	00000000	0	
	47	fix=1A	1A	00011010	26	
	48	Pixel Clock/10,000 (LSB)				68
		01101000		104		
	49	Pixel Clock/10,000 (MSB) 00101001		41		
	4A	Horizontal Active = xxxx pixels (lower 8 bits) 64				01000000
		Horizontal Blanking (Thbp) = xxxx pixels				
	4B	(lower 8 bits) Horizontal Active/Horizontal blanking (Thbp)	4A	01001010	74	
	4C	(upper4:4 bits)	61	01100001	97	
	4D	Vertical Active = xxxx lines	84	10000100	132	
		Vertical Blanking (Tvbp) = xxxx lines (DE Blanking				
	4E	typ. for DE only panels)	0C	00001100	12	
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48	
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	40	01000000	64	
	51	Horizontal Sync, Pulse Width = xxxx pixels	2A	00101010	42	
		Vertical Sync, Offset (Tvfp) = xx lines Sync				
	52	Width = xx lines	33	00110011	51	
	53	Horizontal Vertical Sync Offset/Width upper 2 bits				58
	54	Horizontal Image Size =xxx mm				Vertical
	55	Vertical image Size = xxx mm				Border = 0
	56	Horizontal Image Size / Vertical image size				(Zero for
	57	Horizontal Border = 0 (Zero for Notebook LCD)				Notebook

LCD)

00	00000000	0
35	00110101	53
AE	10101110	174
10	00010000	16
00	00000000	0
00	00000000	0

	59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
Timing Descripte r#3 De ll specific info rmation	5A	Flag	00	00000000	0
	5B	Flag	00	00000000	0
	5C	Flag	00	00000000	0
	5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
	5E	Flag	00	00000000	0
	5F	Dell P/N 1st Character	46	01000110	70
	60	Dell P/N 2nd Character	31	00110001	49
	61	Dell P/N 3rd Character	33	00110011	51
	62	Dell P/N 4th Character	33	00110011	51
	63	Dell P/N 5th Character	4A	01001010	74
	64	**EDID Revision Bit[6:0] See charts below Bit[7] 0: X-rev, 1: A-rev**	80	10000000	128
	65	Manufacturer P/N	42	01000010	66
	66	Manufacturer P/N	31	00110001	49
	67	Manufacturer P/N	34	00110100	52
	68	Manufacturer P/N	30	00110000	48
	69	Manufacturer P/N	52	01010010	82
	6A	Manufacturer P/N	57	01010111	87
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	31	00110001	49
Timing Descripte r#4	6C	Flag	00	00000000	0
	6D	Flag	00	00000000	0
	6E	Flag	00	00000000	0
	6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0
	70	Flag	00	00000000	0
	71	SMBUS Value = ?? Nits ==> fix=00(for M09)	00	00000000	0
	72	SMBUS Value = ?? Nits ==> fix=00(for M09)	00	00000000	0
	73	SMBUS Value = ?? Nits ==> fix=00(for M09)	00	00000000	0
	74	SMBUS Value = ?? Nits ==> fix=00(for M09)	00	00000000	0

	75	SMBUS Value = ?? Nits ==> fix=00(for M09)	00	00000000	0
	76	SMBUS Value = ?? Nits ==> fix=00(for M09)	00	00000000	0
	77	SMBUS Value = ?? Nits ==> fix=00(for M09)	00	00000000	0
	78	SMBUS Value = ?? Nits ==> fix=00(for M09)	00	00000000	0
	79	Bit[1:0] 00: reserved, 01: single LVDS, 10: dual LVDS, 11: reserved Bit[2] 0: No RTC support, 1: RTC support Bit[7:3] Reserved	02	00000010	2
	7A	Bit[0] 0: No BIST support, 1: BIST support Bit[7:1] Reserved	01	00000001	1
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	19	00011001	25

Checksum