Document Version: 8

Date: 2005/3/4

Product Functional Specification

15 inch XGA Color TFT LCD Module
Model Name : B150XG02 V.3

( ) Preliminary Specification
(◆) Final Specification

Note: This Specification is subject to change without notice.

I. Contents

II Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1. 2004/8/16	All	First Edition for Customer	All	
0.2. 2004/10/13	15		Update inverter spec.	
0.2. 2004/10/13	6	Luminance average (5pts) 170nit	Luminance average (5pts) 180nit	
0.2. 2004/10/13	6		Add luminance min (5pts) 150nit	
0.3. 2005/1/17	15		Update inverter output current	
0.3. 2005/1/17	16	Min. ICFL 3.0mA	Min. ICFL 2.0mA	
0.4 2005/2/25	6	-20 to +60	-25 to +65	Storage Temperature
0.4 2005/2/25	8	-20 to +60	-25 to +65	Storage Temperature
0.4 2005/2/25	9	N/A	150 min	White Luminance (CCFL 6.0 mA)
0.4 2005/2/25	11	LVDS differential data input (Blue2-Blue5, Hsync, Vsync, DSPTMG)	LVDS differential data input (Blue2-Blue5, DSPTMG)	Signal Description
0.4 2005/2/25	15	549 (min), 610 (typ), 671(max)	585 (min), 650 (typ), 715(max)	Output voltage
0.4 2005/2/25	16	N/A	150 min	White Luminance 5 points average
0.4 2005/2/25	17	With Hsync, Hsw, Hbp,Hfp, Vw, Vfp and Vbp	Deleted Hsync, Hsw, Hbp,Hfp, Vw, Vfp and Vbp	Timing Characteristics
0.4 2005/2/25	18	With Hsync & Vsync	Deleted Hsync & Vsync	Timing Definition
0.4 2005/2/25	18	With VDDrp & VDDns	Deleted VDDrp & VDDns	Power Consumption
0.4 2005/3/1	23		Add EDID Table	

1.0 Handing Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(2.11, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

2.0 General Description

This specification applies to the 15.0 inch Color TFT/LCD Module B150XG02 V.3.

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the XGA (1024(H) x 768(V)) screen and 262k colors (RGB 6-bits data driver).

All input signals are LVDS interface compatible.

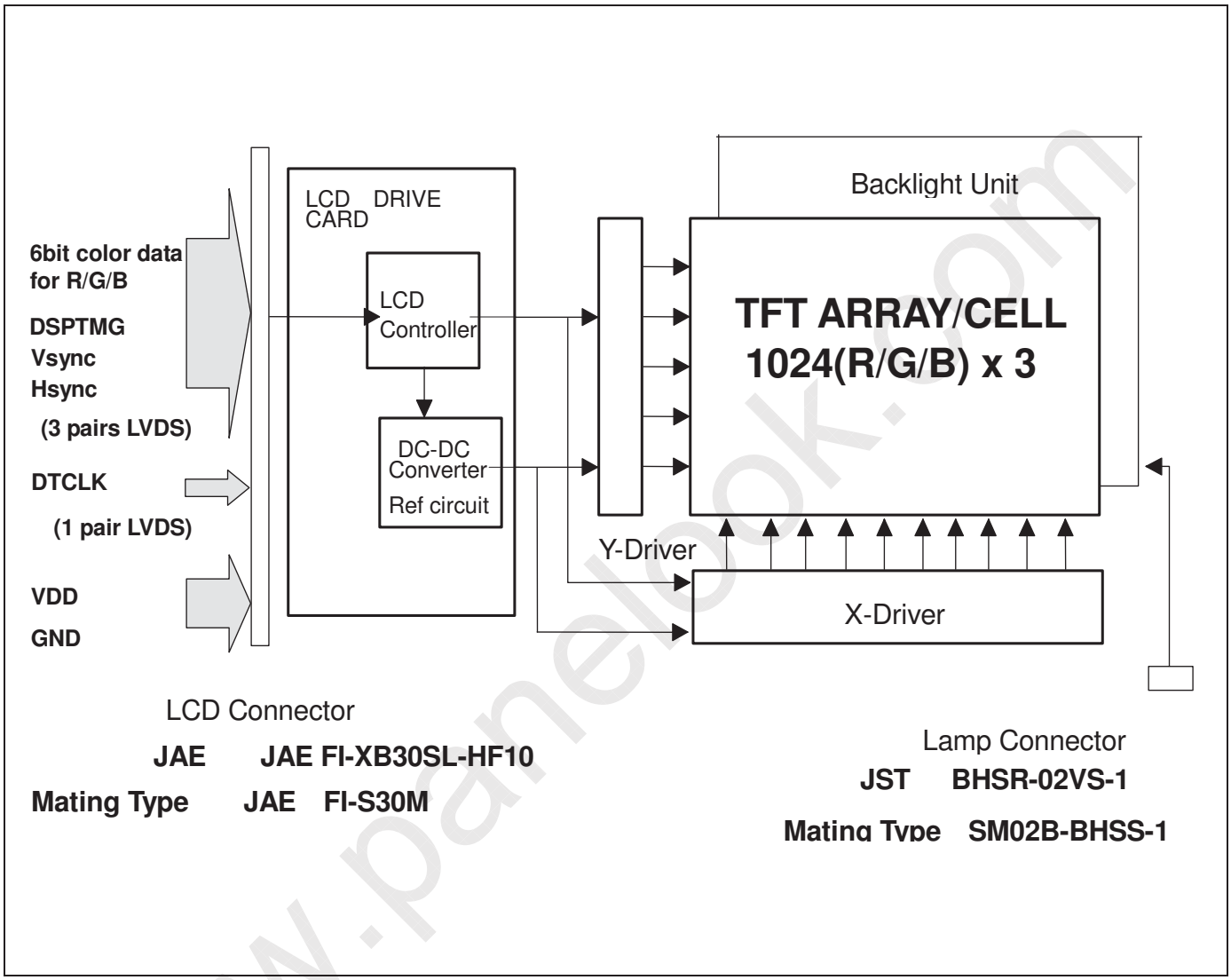
2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	381
Active Area	[mm]	304.1 X 228.1
Pixels H x V		1024(x3) x 768
Pixel Pitch	[mm]	0.297X0.297
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (ICFL=6.0mA)	[cd/m^2]	180 (5 point average) 150 (5 point min.)
Luminance Uniformity		1.25 max. (5 pts) 1.65 max. (13pts)
Contrast Ratio		300 typ.
Optical Rise Time/Fall Time	[msec]	16/9
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Typical Power Consumption (VDD line + VCFL line)	[Watt]	6.3W Max (w/o Inverter, All black pattern)@LCM circuit 2.1 (Max.),B/L input 4.2 (Max.)
Weight (Panel+Inverter)	[Grams]	600g max.
Physical Size	[mm]	317.3 x 242.0 x 6.5 max.
Electrical Interface		1 channel LVDS
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Shipping)	 [°C] [°C]	 0 to +50 -25 to +65
Surface Treatment		3H min
Color Gamut	NTSC	42% min

2.2 Functional Block Diagram

The following diagram shows the functional block of the 15.0 inches Color TFT/LCD Module:



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	[Volt]	
LVDS Input Voltage	$V_{LVDS\ in}$	-0.3	+2.6	[Volt]	
CCFL Current	ICFL	-	7	[mA] rms	
CCFL Ignition Voltage	Vs	-	1150	Vrms	
Operating Temperature	TOP	0	+50	[°C]	Note 1
Operating Humidity	HOP	8	95	[%RH]	Note 1
Storage Temperature	TST	-25	+65	[°C]	Note 1
Storage Humidity	HST	5	95	[%RH]	Note 1
Vibration			1.5 10-500 (random)	G Hz	2hr/axis, X,Y,Z
Shock			220 , 2	G ms	Half sine wave

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

Item		Conditions	Typ.	Note
Viewing Angle K: Contrast Ratio	[degree] [degree] [degree] [degree]	Horizontal (Right) K = 10 (Left) Vertical (Upper) K = 10 (Lower)	40 min. 40 min. 10 min. 30 min.	— — — —
Contrast ratio			300 typ.	200 min.
Luminance Uniformity			1.25 max. (5 pts) 1.65 max. (13pts)	
Response Time (Room Temp.)	[msec] [msec]	Rising Falling	16 typ. 9 typ.	24 Max. 11Max.
Color Chromaticity Coordinates (CIE)		Red x Red y Green x Green y Blue x Blue y White x White y	0.580+-0.02 0.340+-0.02 0.310+-0.02 0.550+-0.02 0.155+-0.02 0.155+-0.02 0.313+-0.02 0.329+-0.02	
White Luminance (CCFL 6.0 mA)	[cd/m^2]		180 typ. (5 points average)	150 min

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	JAE FI-XB30SL-HF10
Mating Housing/Part Number	FI-X30M, FI-X30C or FI-X30H
Mating Contact/Part Number	FI-C3-A1

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

5.2 Signal Pin

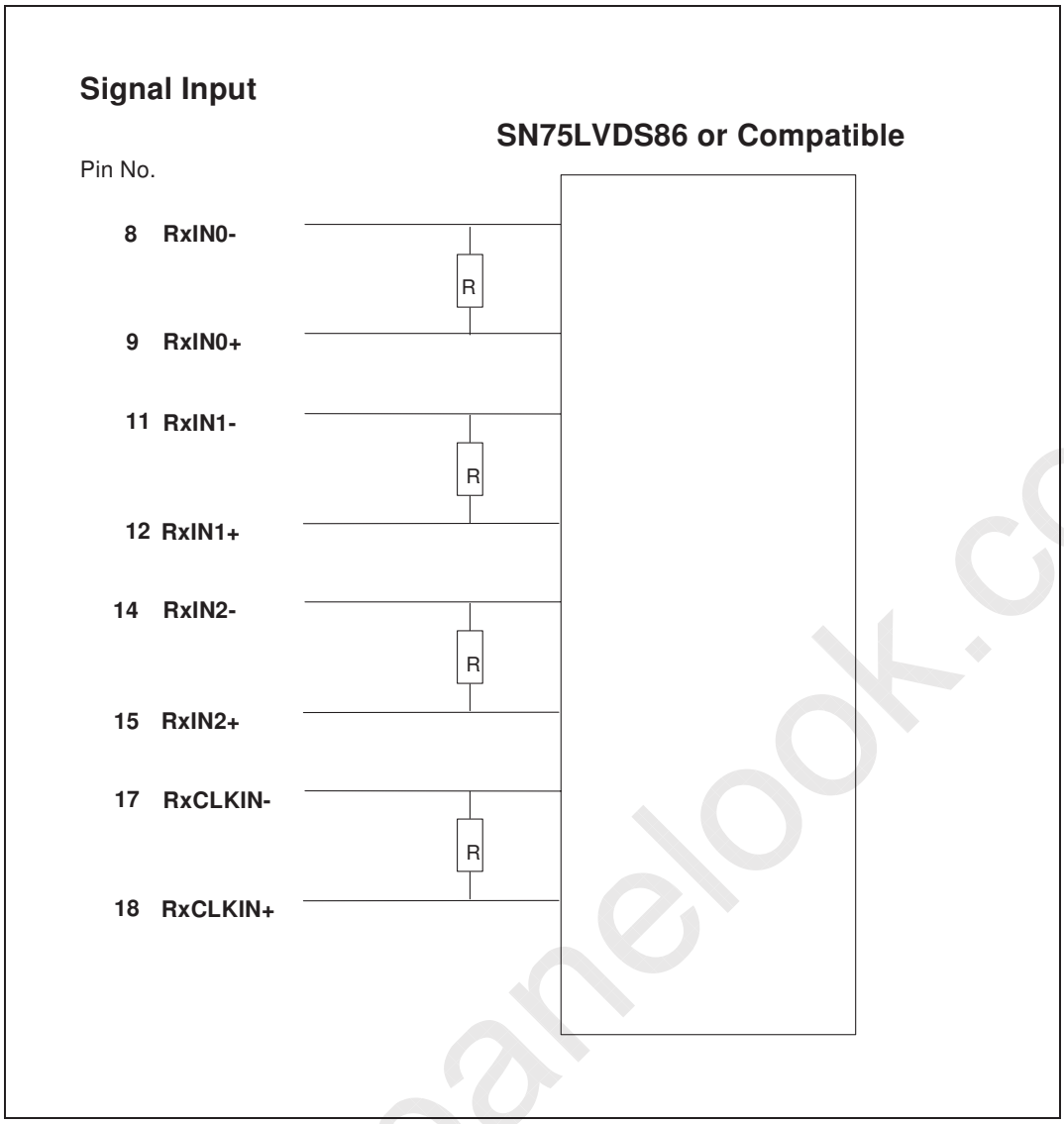
Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	VEDID
5	BIST Test	6	CLKEDID
7	DATAEDID	8	RxIN0-
9	RxIN0+	10	GND
11	RxIN1-	12	RxIN1+
13	GND	14	RxIN2-
15	RxIN2+	16	GND
17	RxCLKIN-	18	RxCLKIN+
19	GND	20	NC
21	NC	22	NC
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	NC	30	NC

5.3 Signal Description

The module using a LVDS receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Signal Name	Description
RxIN0-, RxIN0+	LVDS differential data input(Red0-Red5, Green0)
RxIN1-, RxIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
RxIN2-, RxIN2+	LVDS differential data input(Blue2-Blue5, DSPTMG)
RxCLKIN-, RxCLKIN0+	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note: Input signals shall be low or Hi-Z state when VDD is off.
Internal circuit of LVDS inputs are as following.



The module uses a 100ohm resistor between positive and negative data lines of each receiver input

Signal Name	Description	
RED5 RED4 RED3 RED2 RED1 RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.

GREEN 5 GREEN 4 GREEN 3 GREEN 2 GREEN 1 GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
BLUE 5 BLUE 4 BLUE 3 BLUE 2 BLUE 1 BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK	Data Clock	The typical frequency is 65.0 MHZ.. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	Display Timing	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

5.4 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

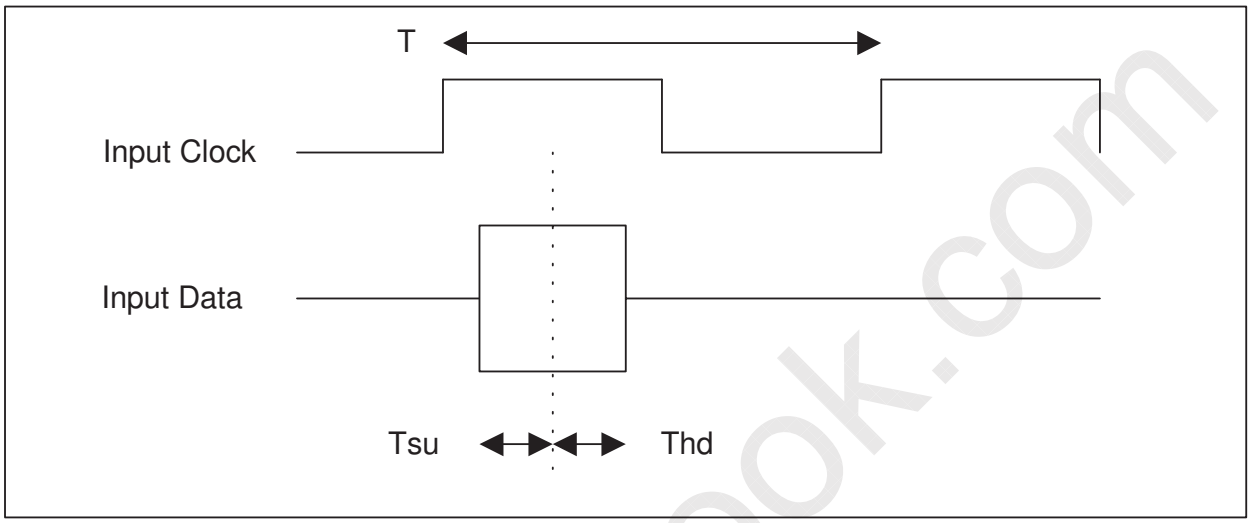
It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Symbol	Parameter	Condition	Min	Max	Unit
V_{TH}	Differential Input High Threshold	Vcm=+1.2V		100	[mV]
V_{TL}	Differential Input Low Threshold	Vcm=+1.2V	-100		[mV]

LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (T)	50MHZ	68MHZ
Data Setup Time (Tsu)	600ps	
Data Hold Time (Thd)	600ps	



5.5 Signal for Lamp connector

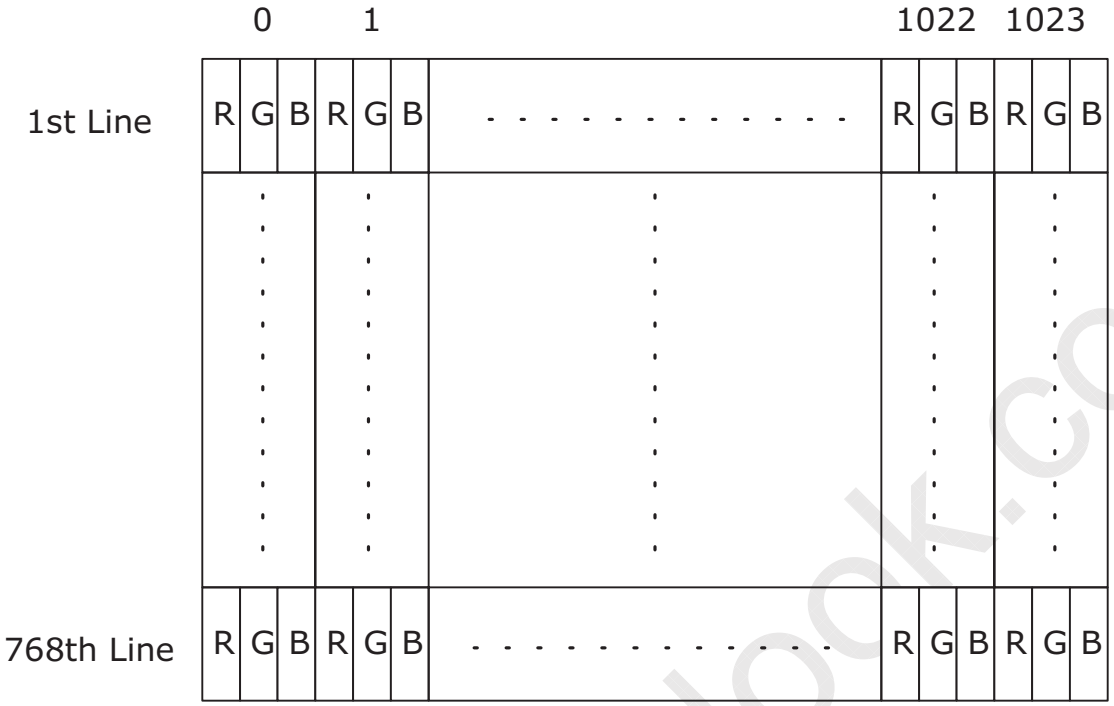
Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

5.6 Inverter Characteristic

.	Item	Symbol	Condition	Min.	Typ.	Max.	Uint
1	Input Voltage	Vin		**7.5**	**14.4**	**21**	V
2	Input Current	Iin	Vin=7.5V,SMData=00H	**590**	**650**	**710**	mA
3	Input Power	Pin	Vin=7.5V,SMData=00H		**5.25**		W
4	Input Signal Level for 5VSUS,5VALW			**4.85**	**5**	**5.2**	V
5	Backlight ON/OFF Control	ON	FPVEE=Hi	**2.0**	**-**	**5.25**	V
		OFF	FPVEE=Lo	**-0.3**	**-**	**0.8**	V
6	Brightness Adjust (Lamp Current Control)	SMData	Control by SMBus	**FFH**	**-**	**00H**	-
7	Output Voltage	Vout	SMData=00H	**585**	**650**	**715**	V(rms)
8	Output Current	Duty cycle	Vin(7.5V~21V)SMData=FFH Ta=25℃, after running 30 min.	**6**	**10**	**14**	% duty cycle
		Iout (Max)	Vin(7.5V~21V)SMData=00H Ta=25℃, after running 30 min.	**5.7**	**6.0**	**6.3**	mA(rms)
9	Frequency	Freq	Vin=7.5~21V	**45**	**55**	**65**	KHz
10	Output Power	Pout	Vin=21V,SMData=00H	**---**	**4.4**	**4.6**	W
11	Open Lamp Voltage	Vopen	No Load	**1400**	**-**	**1800**	V(rms)
12	Striking Time	Ts	Vin=7.5V~21V	**0.6**	**1**	**1.4**	Sec
13	Efficiency	η	Vin=7.5V, Iout=Max. Load=110Kohm//15 p farad	**80**	**---**	**---**	%

6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



7.0 Parameter guide line for CCFL Inverter

Parameter	Min	DP-1	Max	Units	Condition
White Luminance 5 points average	150	180	—	[cd/m^2]	(Ta=25℃)
CCFL current(ICFL)	2.0	6.0	7.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(FCFL)	40	50	60	[KHz]	(Ta=25℃) Note 3
CCFL Ignition Voltage(Vs)		—	1,150	[Volt] rms	(Ta= 0℃) Note 4
CCFL Voltage (Reference) (VCFL)	—	700	—	[Volt] rms	(Ta=25℃) Note 5
CCFL Power consumption (PCFL)	—	4.6	—	[Watt]	(Ta=25℃) Note 5

Note 1: DP-1 are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.
*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
*3 In designing an inverter, it is suggested to check safety circuit ver carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.
*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.
*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be emplyed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.
Note 3: CFL discharge frequency should
be carefully determined to avoid interference between inverter and TFT LCD.
Note 4: CFL inverter should be able to give out a power that has a generating capacity of over 1,400 voltage. Lamp units need 1,400 voltage minimum for ignition.
Note 5: Calculator value for reference (ICFL×VCFL=PCFL)

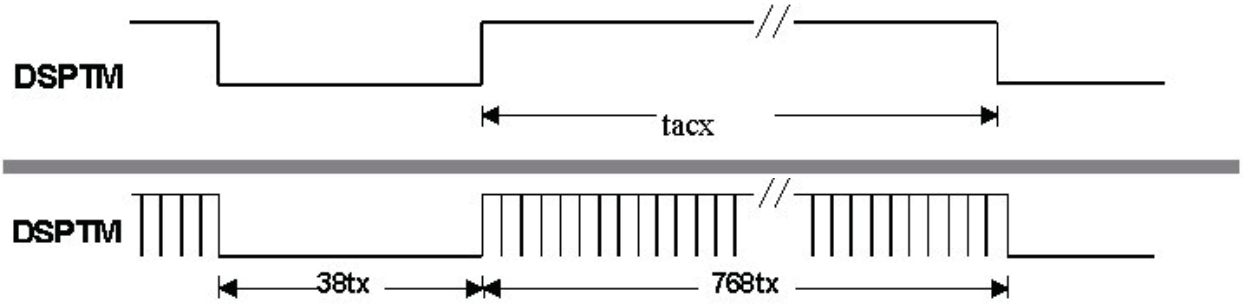
8.0 Interface Timings

Basically, interface timings should match the VESA 1024x768 /60Hz (VG901101) manufacturing guide line timing.

8.1 Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
fdck	DTCLK Frequency	50	65.00	68	[MHz]
tck	DTCLK cycle time		15.38		[nsec]
tx	X total time	1206	1344	1648	[tck]
tacx	X active time		1024		[tck]
tbkx	X blank time	90	320		[tck]
ty	Y total time	771	806	895	[tx]
Vsync	Frame rate	(55)	60	61	[Hz]
tacy	Y active time		768		[tx]

8.2 Timing Definition



9.0 Power Consumption

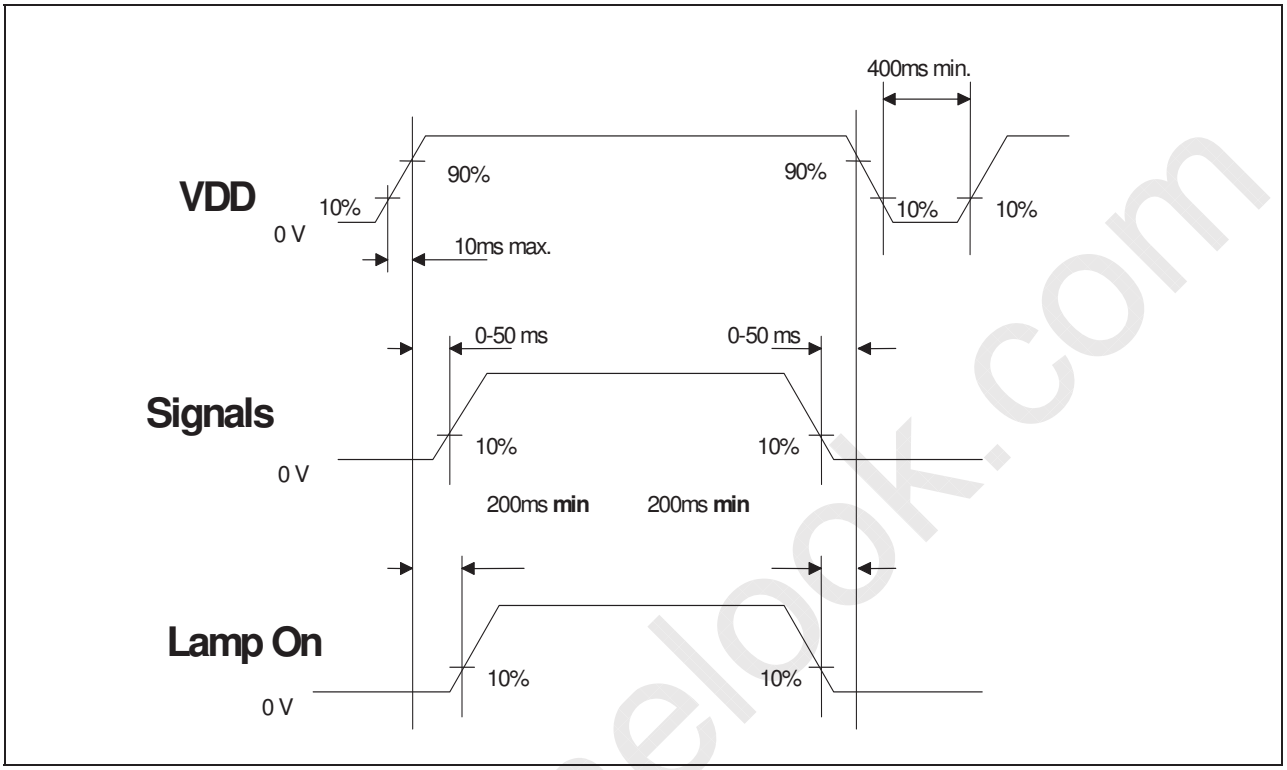
Input power specifications are as follows;

Symbol	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.26		[Watt]	All Black Pattern
PDD Max	VDD Power max			2.1	[Watt]	Max Pattern Note
IDD	IDD Current		380		mA	All Black Pattern
IDD Max	IDD Current max			580	mA	Max Pattern Note

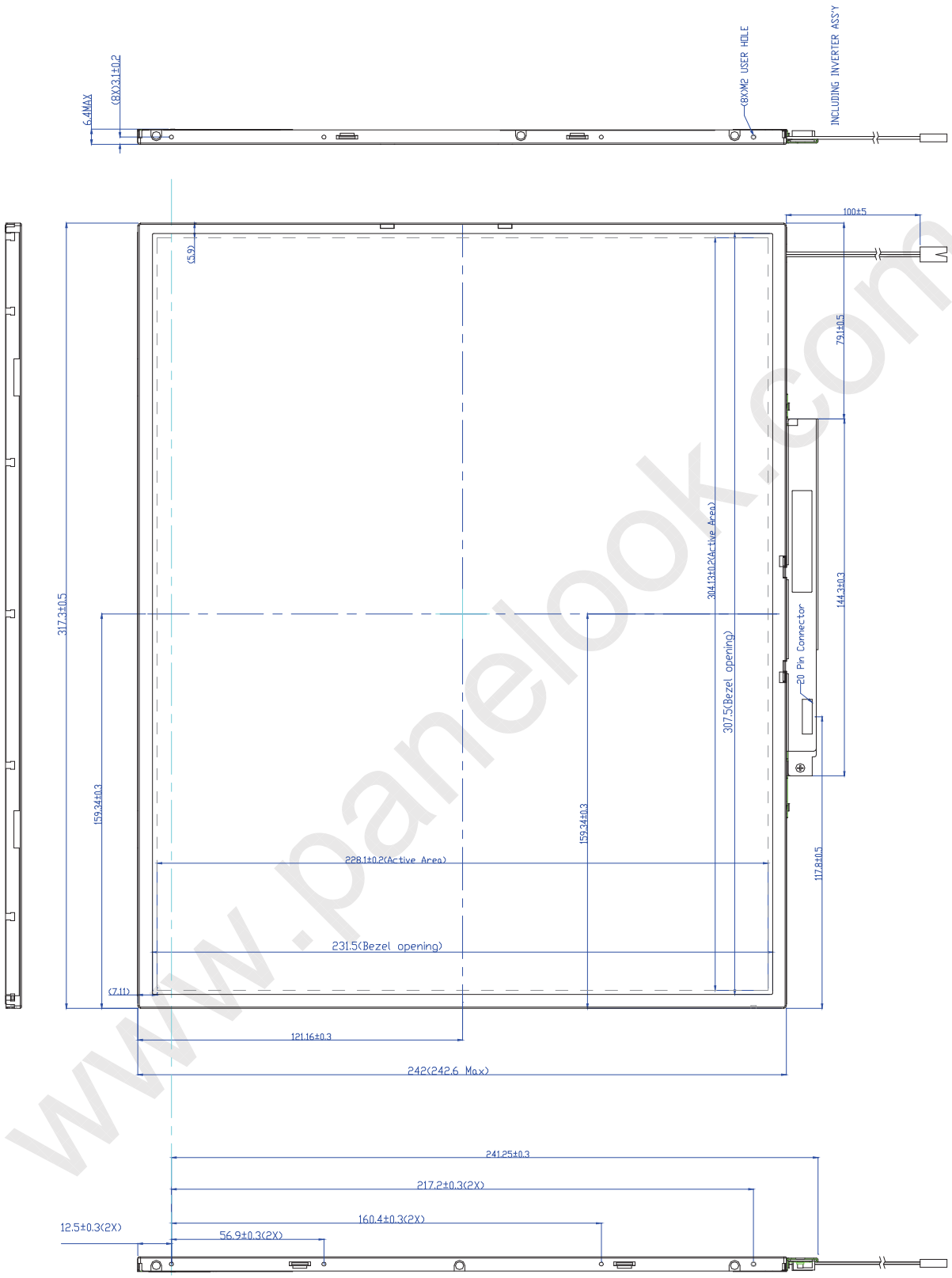
Note : VDD=3.3V

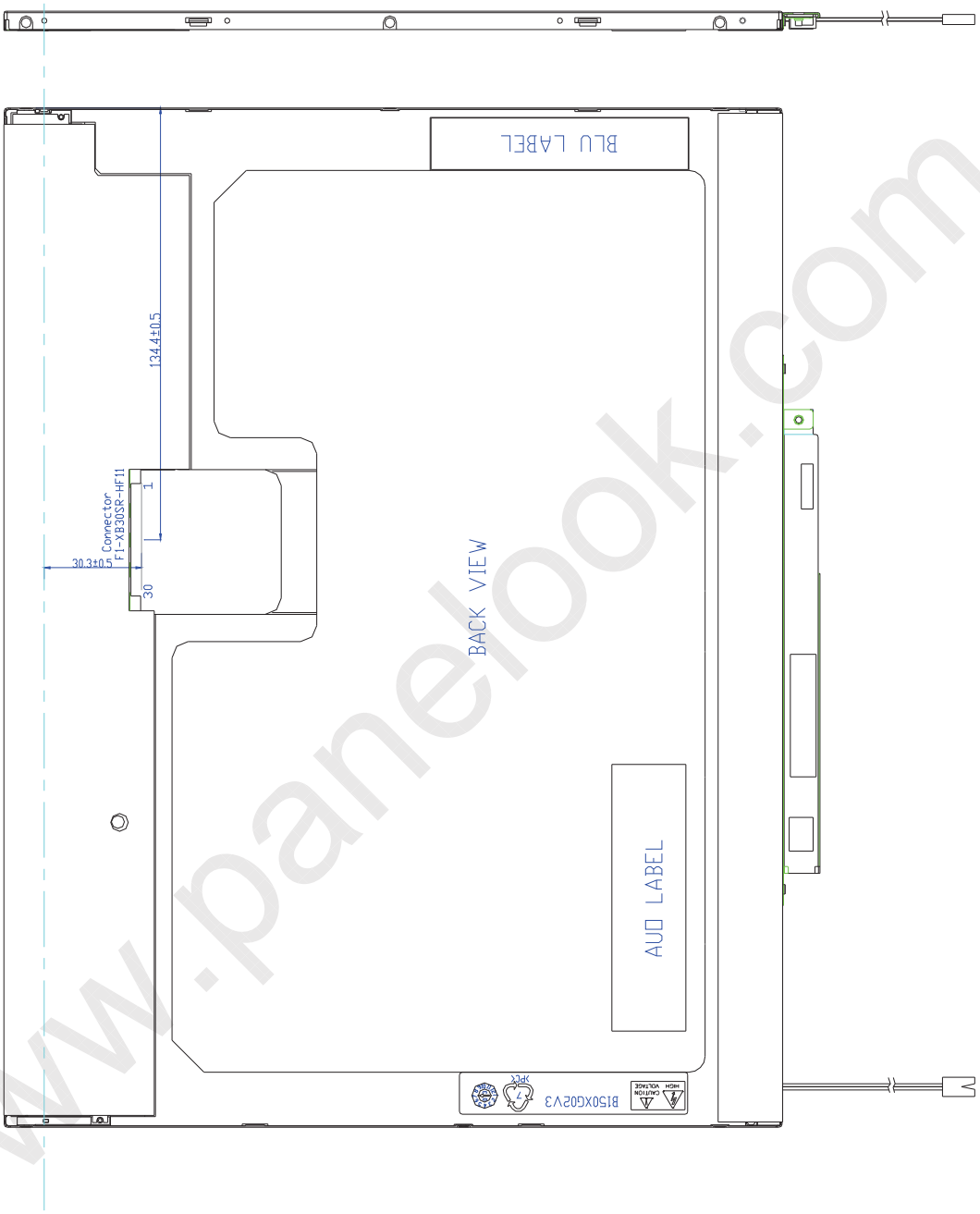
10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11.0 Mechanical Characteristics





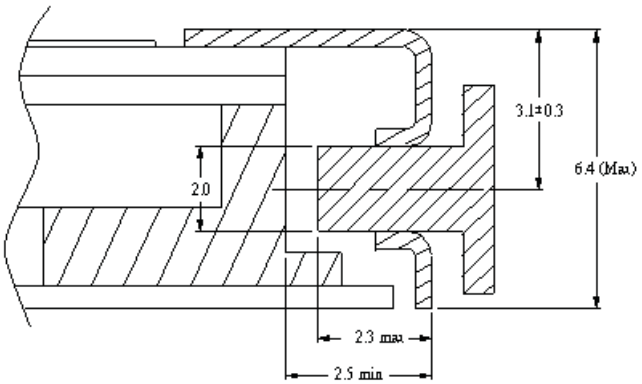


Fig. Screw hole depth and suggested screw penetration

Suggested torque is 2.0+/- 0.2kgf-cm, also shown in the module drawing.

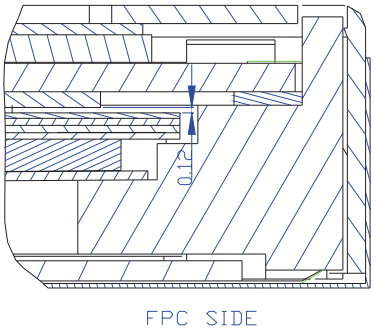


Fig. Gap between films and glass

12.0 EDID Table

	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
Header	0	Header	00	0
	1	Header	FF	11111111
	2	Header	FF	11111111
	3	Header	FF	11111111
	4	Header	FF	11111111
	5	Header	FF	11111111
	6	Header	FF	11111111
	7	Header	00	0
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06	110
	9	EISA manufacture code (Compressed ASCII)	AF	10101111
	0A	Panel Supplier Reserved – Product Code	07	111
	0B	Panel Supplier Reserved – Product Code	0F	1111
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	01	1
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	01	1
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	01	1
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	01	1
	10	Week of manufacture	01	1
	11	Year of manufacture	0E	1110
	12	EDID structure version # = 1	01	1
	13	EDID revision # = 3	03	11
Display Parameters	14	Video I/P definition = Digital I/P (80h)	80	10000000
	15	Max H image size = (Rounded to cm)	1E	11110
	16	Max V image size = (Rounded to cm)	17	10111
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	1111000
	18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A	1010
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	87	10000111
	1A	Blue/White Low bit (BxBy/WxWy)	F5	11110101
	1B	Red X Rx = 0.xxx	94	10010100
	1C	Red Y Ry = 0.xxx	57	1010111
	1D	Green X Gx = 0.xxx	4F	1001111
	1E	Green Y Gy = 0.xxx	8C	10001100
	1F	Blue X Bx = 0.xxx	27	100111
	20	Blue Y By = 0.xxx	27	100111
	21	White X Wx = 0.xxx	50	1010000
	22	White Y Wy = 0.xxx	54	1010100
Established Timings	23	Established timings 1 (00h if not used)	00	0
	24	Established timings 2 (00h if not used)	00	0
	25	Manufacturer’s timings (00h if not used)	00	0
da rd Ti mi	26	Standard timing ID1 (01h if not used)	01	1

	27	Standard timing ID1 (01h if not used)	01	1
	28	Standard timing ID2 (01h if not used)	01	1
	29	Standard timing ID2 (01h if not used)	01	1
	2A	Standard timing ID3 (01h if not used)	01	1
	2B	Standard timing ID3 (01h if not used)	01	1
	2C	Standard timing ID4 (01h if not used)	01	1
	2D	Standard timing ID4 (01h if not used)	01	1
	2E	Standard timing ID5 (01h if not used)	01	1
	2F	Standard timing ID5 (01h if not used)	01	1
	30	Standard timing ID6 (01h if not used)	01	1
	31	Standard timing ID6 (01h if not used)	01	1
	32	Standard timing ID7 (01h if not used)	01	1
	33	Standard timing ID7 (01h if not used)	01	1
	34	Standard timing ID8 (01h if not used)	01	1
	35	Standard timing ID8 (01h if not used)	01	1
Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	64	1100100
	37	Pixel Clock/10,000 (MSB)	19	11001
	38	Horizontal Active = xxxx pixels (lower 8 bits)	00	0
	39	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	40	1000000
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	41	1000001
	3B	Vertical Active = xxxx lines	00	0
	3C	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	26	100110
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	110000
	3E	Horizontal Sync, Offset (Thfp) = xxxx pixels	18	11000
	3F	Horizontal Sync, Pulse Width = xxxx pixels	88	10001000
	40	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	36	110110
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	0
	42	Horizontal Image Size =xxx mm	30	110000
	43	Vertical image Size = xxx mm	E4	11100100
	44	Horizontal Image Size / Vertical image size	10	10000
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	0
	46	Vertical Border = 0 (Zero for Notebook LCD)	00	0
	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives, **DE only note: LSB is set to "1" if panel is DE-timing only. H/V can be ignored.**	18	11000
Timing Descripter #2	48	Pixel Clock/10,000 (LSB)	00	0
	49	Pixel Clock/10,000 (MSB)	00	0
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	00	0
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	00	0
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	00	0
	4D	Vertical Active = xxxx lines	00	0
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	00	0
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	00	0
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	00	0
	51	Horizontal Sync, Pulse Width = xxxx pixels	00	0
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	00	0
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	0
	54	Horizontal Image Size =xxx mm	00	0

	55	Vertical image Size = xxx mm	00	0
	56	Horizontal Image Size / Vertical image size	00	0
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	0
	58	Vertical Border = 0 (Zero for Notebook LCD)	00	0
	59	Module "A" Revision = Example: 00, 01, 02, 03, etc.	00	0
Timing Descripter #3 Dell specific information	5A	Flag	00	0
	5B	Flag	00	0
	5C	Flag	00	0
	5D	Dummy Descriptor	FE	11111110
	5E	Flag	00	0
	5F	Dell P/N 1st Character	44	1000100
	60	Dell P/N 2nd Character	38	111000
	61	Dell P/N 3rd Character	33	110011
	62	Dell P/N 4th Character	38	111000
	63	Dell P/N 5th Character	31	110001
	64	LCD Supplier EEDID Revision #	00	0
	65	Manufacturer P/N	42	1000010
	66	Manufacturer P/N	31	110001
	67	Manufacturer P/N	35	110101
	68	Manufacturer P/N	30	110000
	69	Manufacturer P/N	58	1011000
	6A	Manufacturer P/N	47	1000111
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	32	110010
Timing Descripter #4	6C	Flag	00	0
	6D	Flag	00	0
	6E	Flag	00	0
	6F	Data Type Tag:	FE	11111110
	70	Flag	00	0
	71	SMBUS Value = 10 nits	D0	11010000
	72	SMBUS Value = 17 nits	C0	11000000
	73	SMBUS Value = 24 nits	B0	10110000
	74	SMBUS Value = 30 nits	A8	10101000
	75	SMBUS Value = 60 nits	88	10001000
	76	SMBUS Value = 110 nits	60	1100000
	77	SMBUS Value = 150 nits	40	1000000
	78	SMBUS Value = max nits (Typically = 00h, XXX nits)	00	0
	79	Number of LVDS receiver chips = '01' or '02'	01	1
	7A	BIST Enable: Yes = '01' No = '00'	01	1
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	1010

	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	100000
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	100000
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	0
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	2A	101010