AU OPTRONICS CORPORATION

Product Specification

15.0” XGA Color TFT-LCD Module

Model Name: B150XG02 V5

Approved by	Prepared by

NBBU Marketing Division / AU Optronics corporation

Customer	Checked & Approved by

Product Specification

15.0” XGA Color TFT-LCD Module
Model Name: B150XG02 V5

(V) Preliminary Specifications
( ) Final Specifications

Note: This Specification is subject to change without notice.

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2005/12/5	All	First Edition		
0.2 2005/12/7	25	7.1…JAE or compatible	7.1 …JAE	
0.2 2005/12/7	25	7.1…FI-XB30SL-HF10 or compatible	7.1…FI-XB30SL-HF10	
0.3 2006/2/21	6	180 typ. (5 points average) 150 min. (5 points average)	180 typ. (5 points average) 150 min. (5 points average)	
0.3 2006/2/21	7	Viewing angle (U/D/L/R): 10/30/40/40	Viewing angle (U/D/L/R): 20/45/42/42	
0.3 2006/2/21	17	White Luminance 5 points average: min:-;typ:180	White Luminance 5 points average: min: 120; typ: 160	
0.3 2006/2/21	24	T1: Min 0.5 T3: Max 50 T4: Min 400 T6: Min 200	T1: Min 0. T3: Max N/A T4: Min 150 T6: Min 0	
0.3 2006/2/21	28		Update LCM outline dimension	
0.4 2006/3/7	28		Update LCM outline dimension	
0.5 2006/3/8	23	Horizontal blanking (T_{HB}) Min: 30	Horizontal blanking (T_{HB}) Min: 28	
0.5 2006/3/8	28	CCFL cable position 11.64+/-1mm from the edge of bezel	Update LCM outline dimension (CCFL cable position: 11+/-1mm from the edge of bezel)	
0.5 2006/3/9	24	Frame rate: min: 55 Hz; typ: 60 Hz	Frame rate (normal): min: 55 Hz; typ: 60 Hz Frame rate (overall): min: 40 Hz; typ: 60 Hz Note 2: * When frame rate (overall) min 40, flicker might occur	
0.5 2006/3/9	24	Clock frequency: 50 MHz min	Clock frequency: 43.4 MHz min	
0.6 2006/3/10	33		Update 11.2. Carton package	
0.6 2006/3/10	34		Update 11.3 Shipping package of palletizing sequence	

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

2. General Description

B150XG02 V5 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the XGA (1024(H)

x 768(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter card of backlight is not included.

B150XG02 V5 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

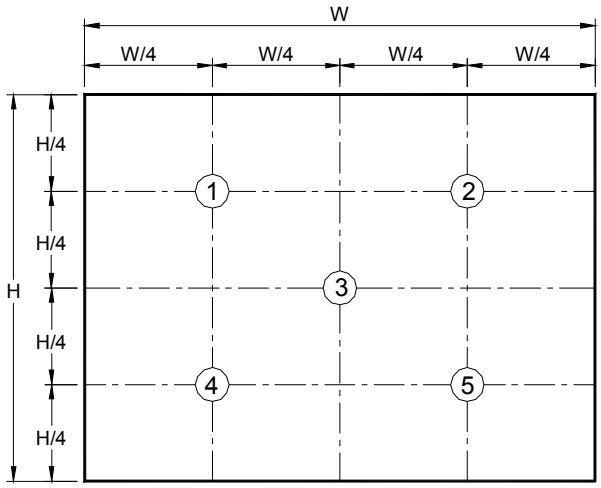
Items	Unit	Specifications
Screen Diagonal	[mm]	381 (15.0")
Active Area	[mm]	304.1 X 228.1
Pixels H x V		1024x3(RGB) x 768
Pixel Pitch	[mm]	0.297X0.297
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (ICFL=6.0mA)	[cd/m^2]	160 typ. (5 points average) 120 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		300 typ.
Optical Rise Time/Fall Time	[msec]	16/9 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Typical Power Consumption	[Watt]	5.6W max.
Weight	[Grams]	585g typ.
Physical Size	[mm]	317.3(typ.)x 242.0(typ.) x 6.5(max.)
Electrical Interface		1 channel LVDS
Surface Treatment		Anti-glare, Harness 3H, Haze 25%, Reflectance 4.3%
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

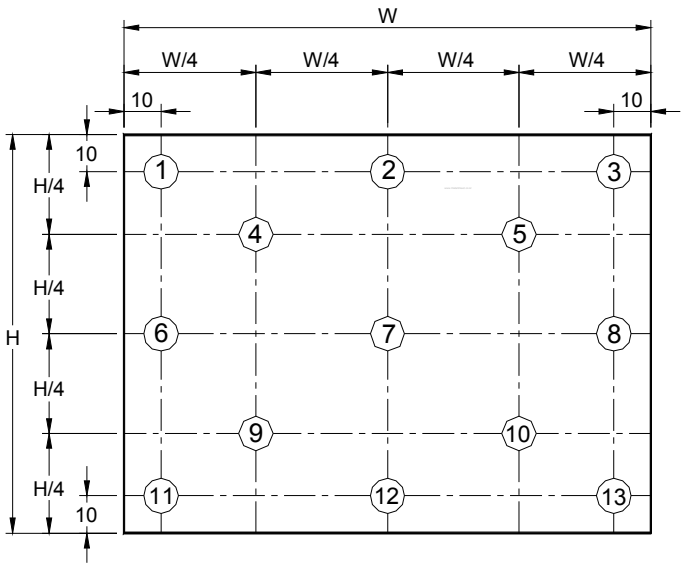
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance CCFL 6.0mA	[cd/m2]	5 points average	120	160	-	1,2,3
Viewing Angle	[degree]	Horizontal (Right)	-	42	-	2,7
	[degree]	CR = 10 (Left)	-	42	-	
	[degree]	Vertical (Upper)	-	20	-	
	[degree]	CR = 10 (Lower)	-	45	-	
Uniformity		5 Points			1.25	1
Uniformity		13 Points			1.50	
CR: Contrast Ratio			250	300	-	6
Cross talk	%				4	4
Response Time	[msec]	Rising	-	16	24	5
	[msec]	Falling	-	9	11	
	[msec]	Raising + Falling		25	35	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.565	0.580	0.595	2,7
		Red y	0.325	0.340	0.355	
		Green x	0.295	0.310	0.325	
		Green y	0.535	0.550	0.565	
		Blue x	0.140	0.155	0.170	
		Blue y	0.140	0.155	0.170	
		White x	0.298	0.313	0.328	
		White y	0.314	0.329	0.344	

Note 1: 5 points position (Display area : 304.5mm x 228.375mm)



Note 2: 13 points position



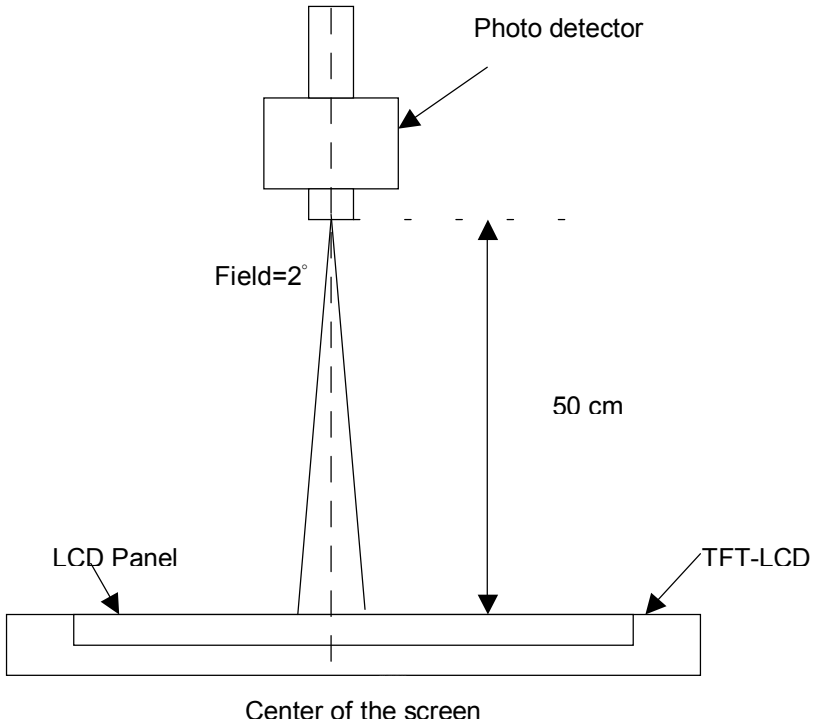
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

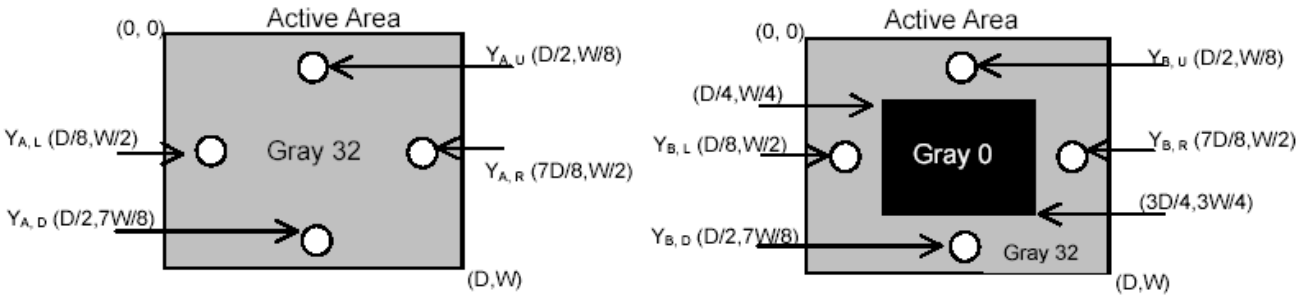
Note 7： Definition of Cross Talk (CT)

CT = | Y_B – Y_A | / Y_A × 100 (%)

Where

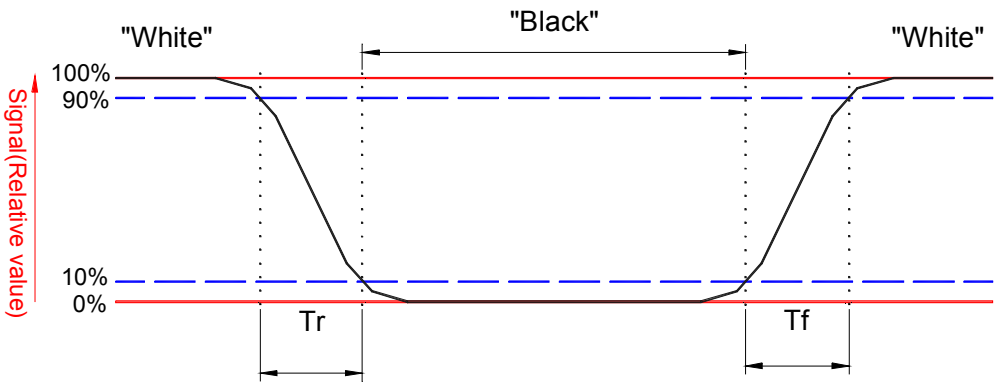
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



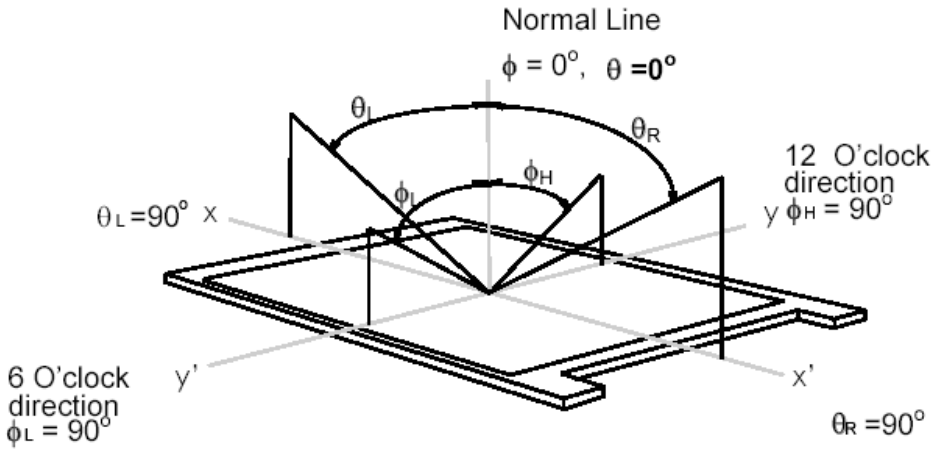
Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



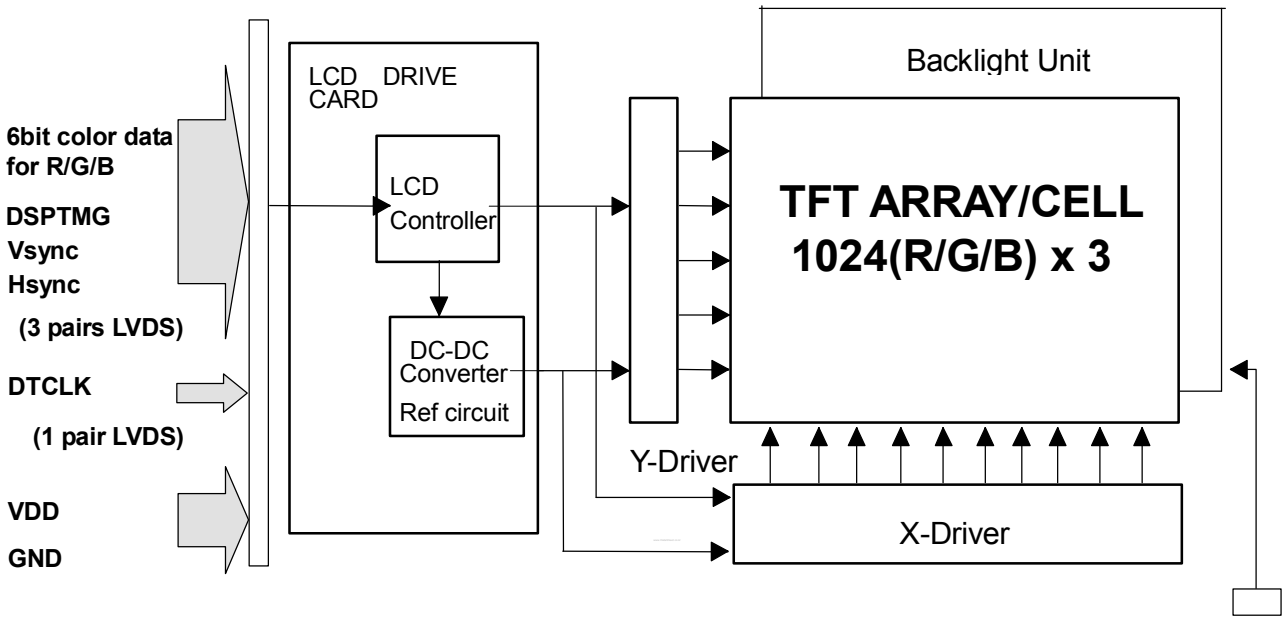
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.0 inches wide Color TFT/LCD Module:



LCD Connector

JAE JAE FI-XB30SL-HF10

Mating Type JAE FI-S30M

Lamp Connector

JST BHSR-02VS-1

Mating Type SM02B-BHSS-1

4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICFL	-	7.0	[mA] rms	Note 1,2

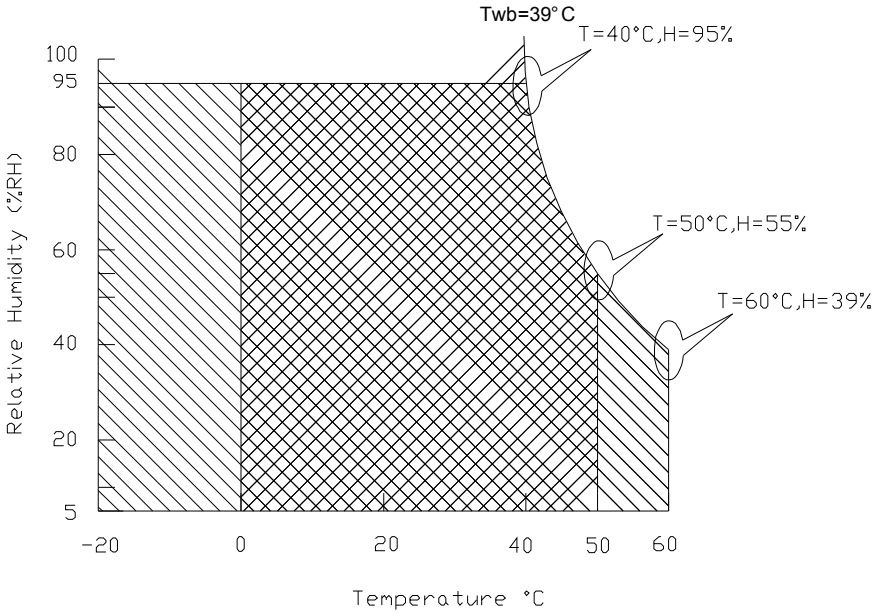
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: With in Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality perfermance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

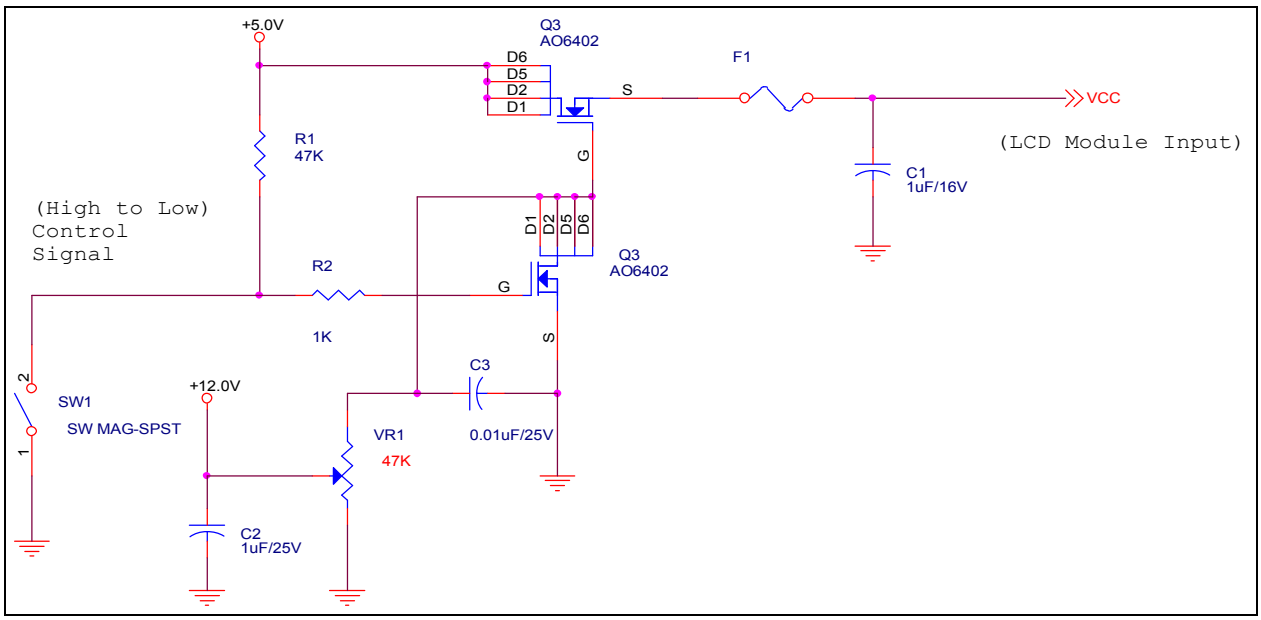
5.1 TFT LCD Module

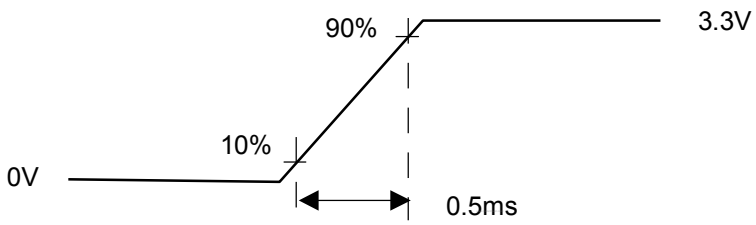
5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.1	1.4	[Watt]	Black Pattern
IDD	IDD Current		380	420	mA	Black Pattern
I_{Rush}	Inrush Current			1.5	A	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Measurement conditions:





Vin rising time

5.1.2 Signal Electrical Characteristics

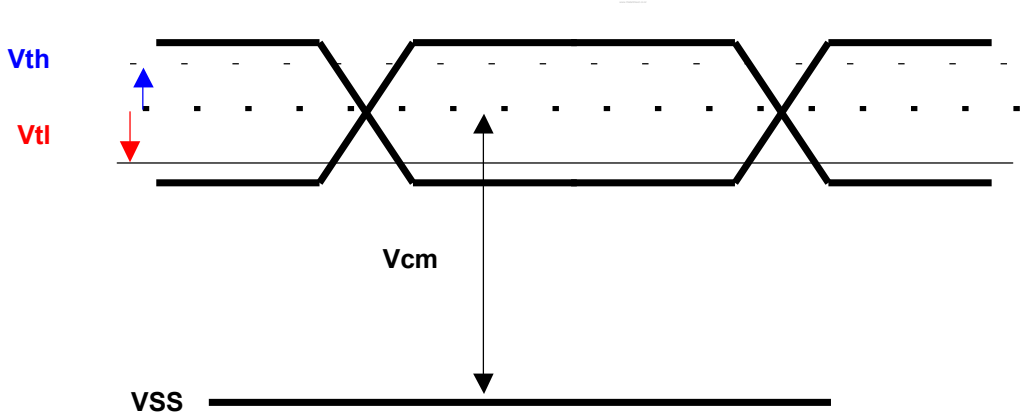
Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	120	160	-	[cd/m^2]	(Ta=25℃)
CCFL current(ICFL)	-	6.0	7.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(FCFL)	50	-	60	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)	1560	-	-	[Volt] rms	(Ta= 0℃) Note 5
CCFL Voltage (Reference) (VCFL)	585	650	715	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (PCFL)	-	3.9	5	[Watt]	(Ta=25℃) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.

Note 3: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CFL inverter should be able to give out a power that has a generating capacity of over 1,560 voltage. Lamp unit needs 1,560 voltage minimum for ignition.

Note 6: Calculator value for reference (ICFL×VCFL=PCFL)

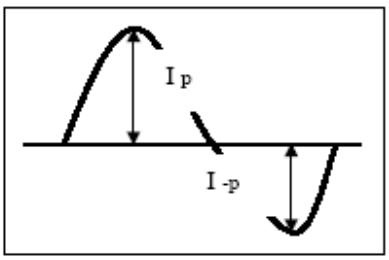
Note 7: Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp, are following.

It shall help increase the lamp lifetime and reduce leakage current.

a. The asymmetry rate of the inverter waveform should be less than 10%.

b. The distortion rate of the waveform should be within $\sqrt{2}$ ±10%.

* Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$| I_p - I_{-p} | / I_{rms} * 100\%$

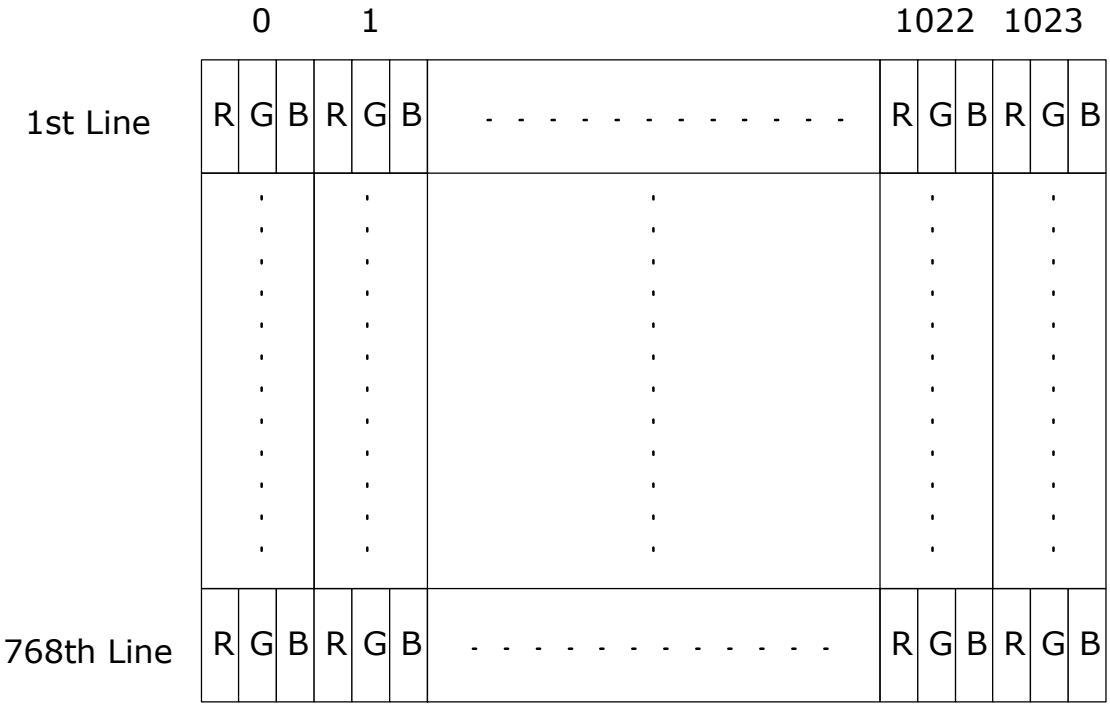
* Distortion rate

I_p (or I_{-p}) / I_{rms}

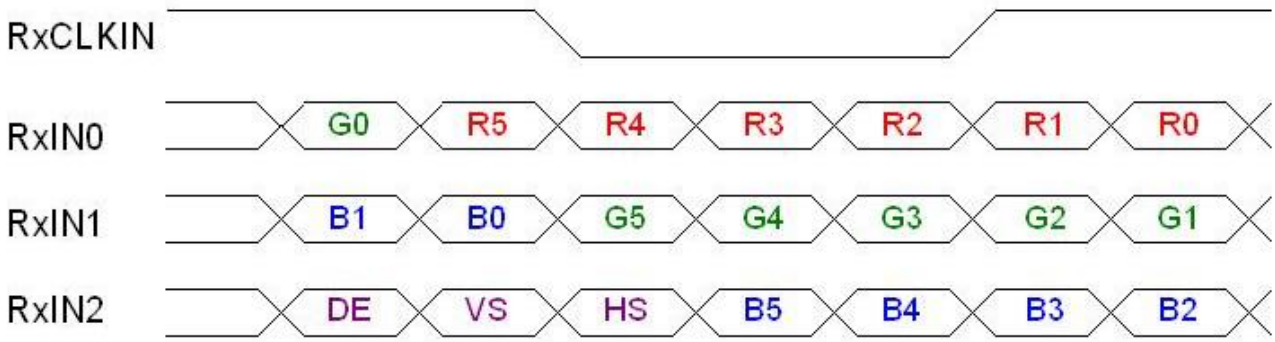
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 The input data format



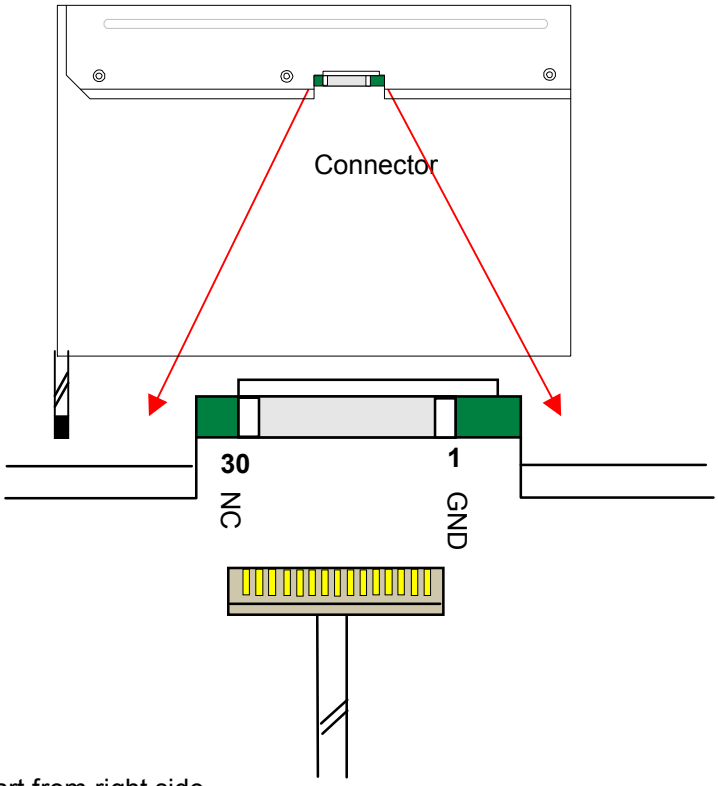
Signal Name	Description	
RED5 RED4 RED3 RED2 RED1 RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
GREEN 5 GREEN 4 GREEN 3 GREEN 2 GREEN 1 GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
BLUE 5 BLUE 4 BLUE 3 BLUE 2 BLUE 1 BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	Display Timing	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to -DTCLK .
HSYNC	Horizontal Sync	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

6.3 Signal Description

The LVDS receiver equipped in this LCD module is compatible with SN75LVDS86 standard. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

PIN#	Signal Name	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V_{EDID}	+3.3V EDID Power
5	NC	No Connection (For AUO test)
6	CLK_{EDID}	EDID Clock Input
7	$DATA_{EDID}$	EDID Data Input
8	RxIN0-	LVDS differential data input(Red0-Red5, Green0)
9	RxIN0+	LVDS differential data input(Red0-Red5, Green0)
10	GND	Ground
11	RxIN1-	LVDS differential data input(Green1-Green5, Blue0-Blue1)
12	RxIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
13	GND	Ground
14	RxIN2-	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
15	RxIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input
18	RxCLKIN+	LVDS differential clock input
19	GND	Ground
20	GND	Ground
21	NC	No Connection (For AUO test)
22	NC	No Connection (For AUO test)
23	NC	No Connection (For AUO test)
24	NC	No Connection (For AUO test)
25	NC	No Connection (For AUO test)
26	NC	No Connection (For AUO test)
27	NC	No Connection (For AUO test)
28	NC	No Connection (For AUO test)
29	NC	No Connection (For AUO test)
30	NC	No Connection (For AUO test)



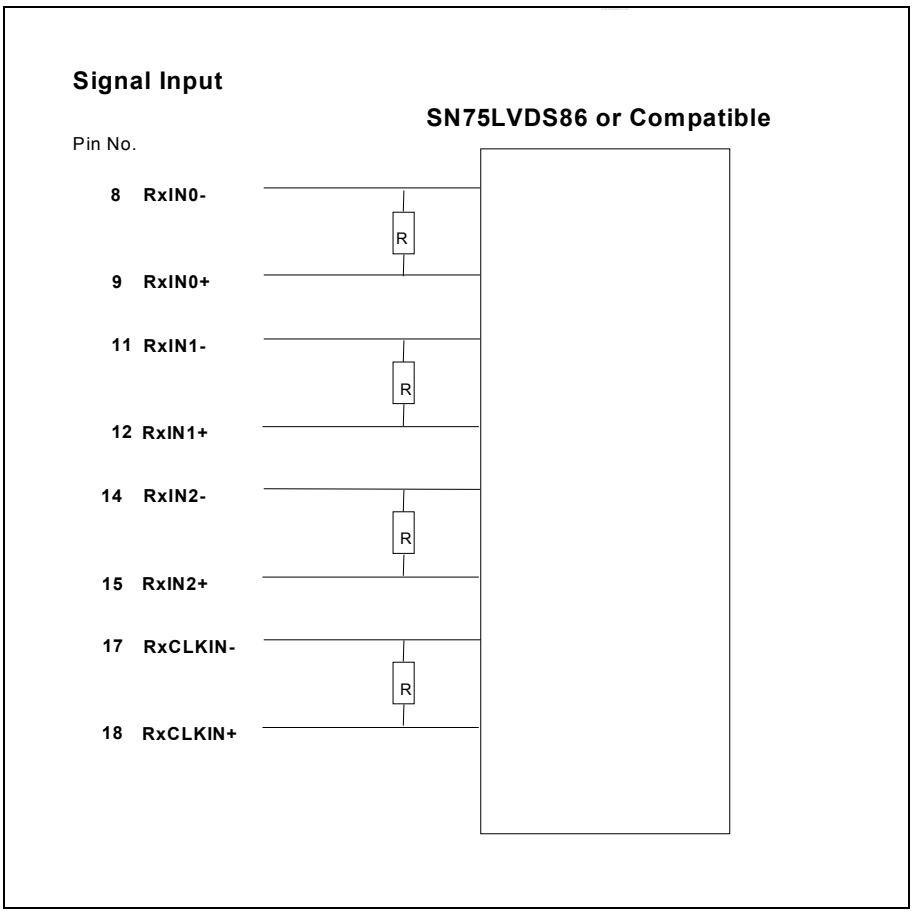
Note1: Start from right side

Note2: Please follow PSWG.

Note3: Input signals shall be low or Hi-Z state when VDD is off.

Internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input



6.4 Interface Timing

6.4.1 Timing Characteristics

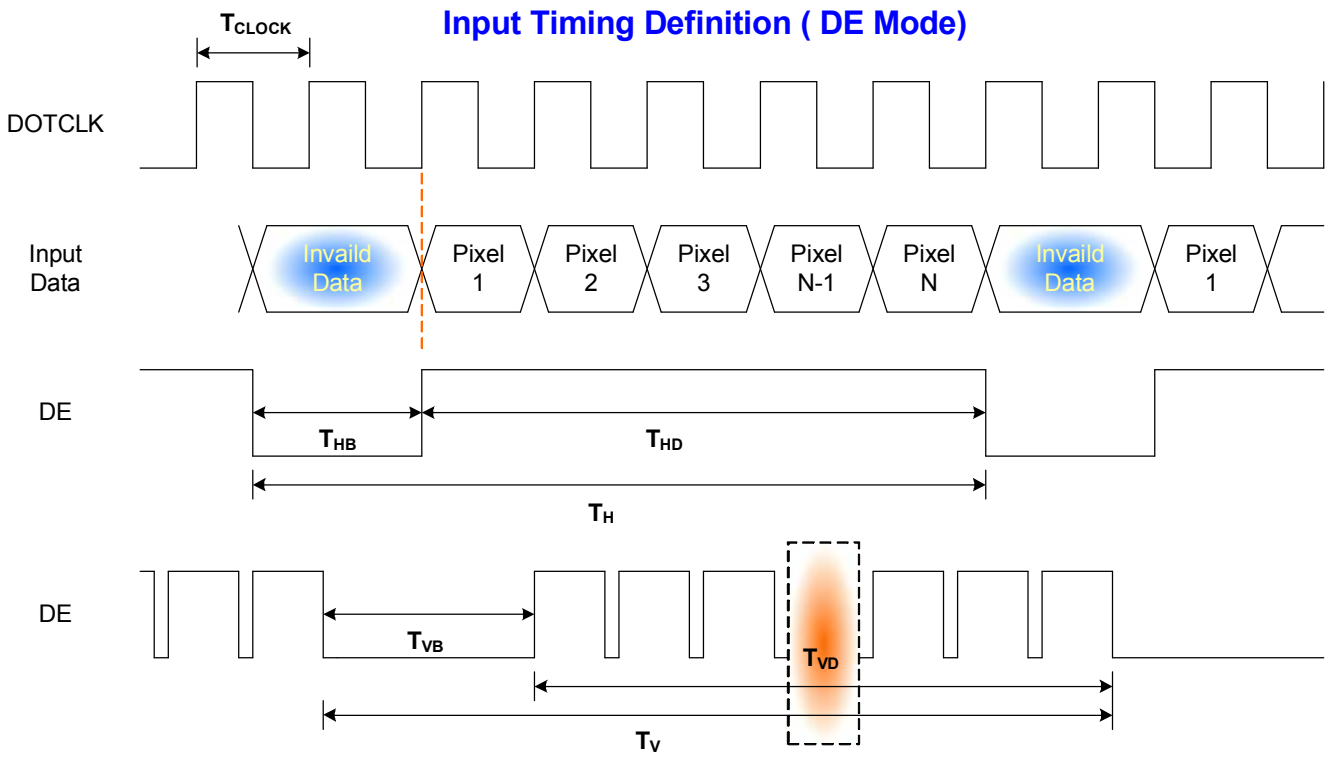
Basically, interface timings should match the 1024x768 /60Hz manufacturing guideline timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate (normal)		-	55	60	-	Hz
Frame Rate (overall)		-	40*	60	-	Hz
Clock frequency (overall)		1/ T_{Clock}	43.3	65	68	MHz
Vertical Section	Period	T_V	774	806	1024	T_{Line}
	Active	T_{VD}	-	768	-	
	Blanking	T_{VB}	6	38	256	
Horizontal Section	Period	T_H	1054	1344	1648	T_{Clock}
	Active	T_{HD}	-	1024	-	
	Blanking	T_{HB}	28	320	624	
End-frame checking period		tEF	2			T_H
DE checking period		tDE	4			T_H

Note1 : DE mode only

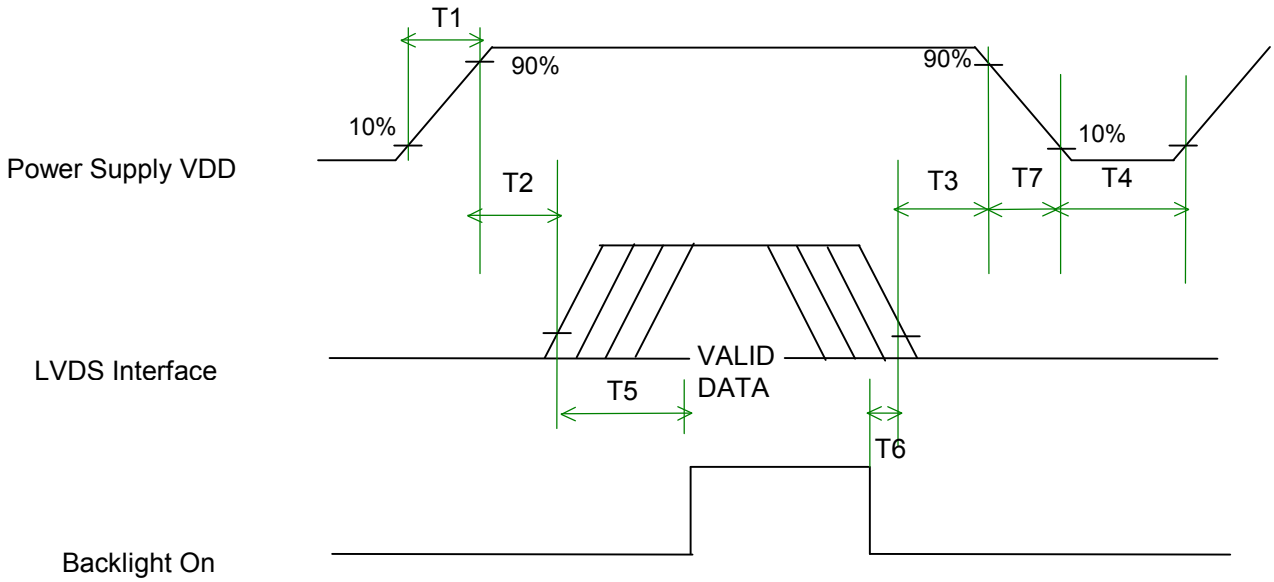
Note 2: * When frame rate (overall) min 40, flicker might occur

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0	-	10	(ms)
T2	0	-	50	(ms)
T3	50	-	N/A	(ms)
T4	150	-	-	(ms)
T5	200	-	-	(ms)
T6	0	-	-	(ms)
T7	0	-	10	(ms)

Note: If T4 is between 150~400 ms, display noise would occur

7. Connector & Pin Assignment

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30SL-HF10
Mating Housing/Part Number	FI-X30M, FI-X30C or FI-X30H

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40℃/90%,300Hr	
High Temperature Operation	50℃/Dry,300Hr	
Low Temperature Operation	0℃,300Hr	
On/Off Test	25℃,150hrs(ON/10 sec. OFF/10sec., 10,000 cycles)	
Hot Storage	60℃/35% RH ,250 hours	
Cold Storage	-20℃/50% RH ,250 hours	
Thermal Shock Test	-20℃/30 min ,60℃/30 min 100cycles	
Hot Start Test	50℃/1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	0℃/1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	220G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Random vibration, 1.5 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Room temperature Test	25℃, 2000hours, Operating with loop pattern	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

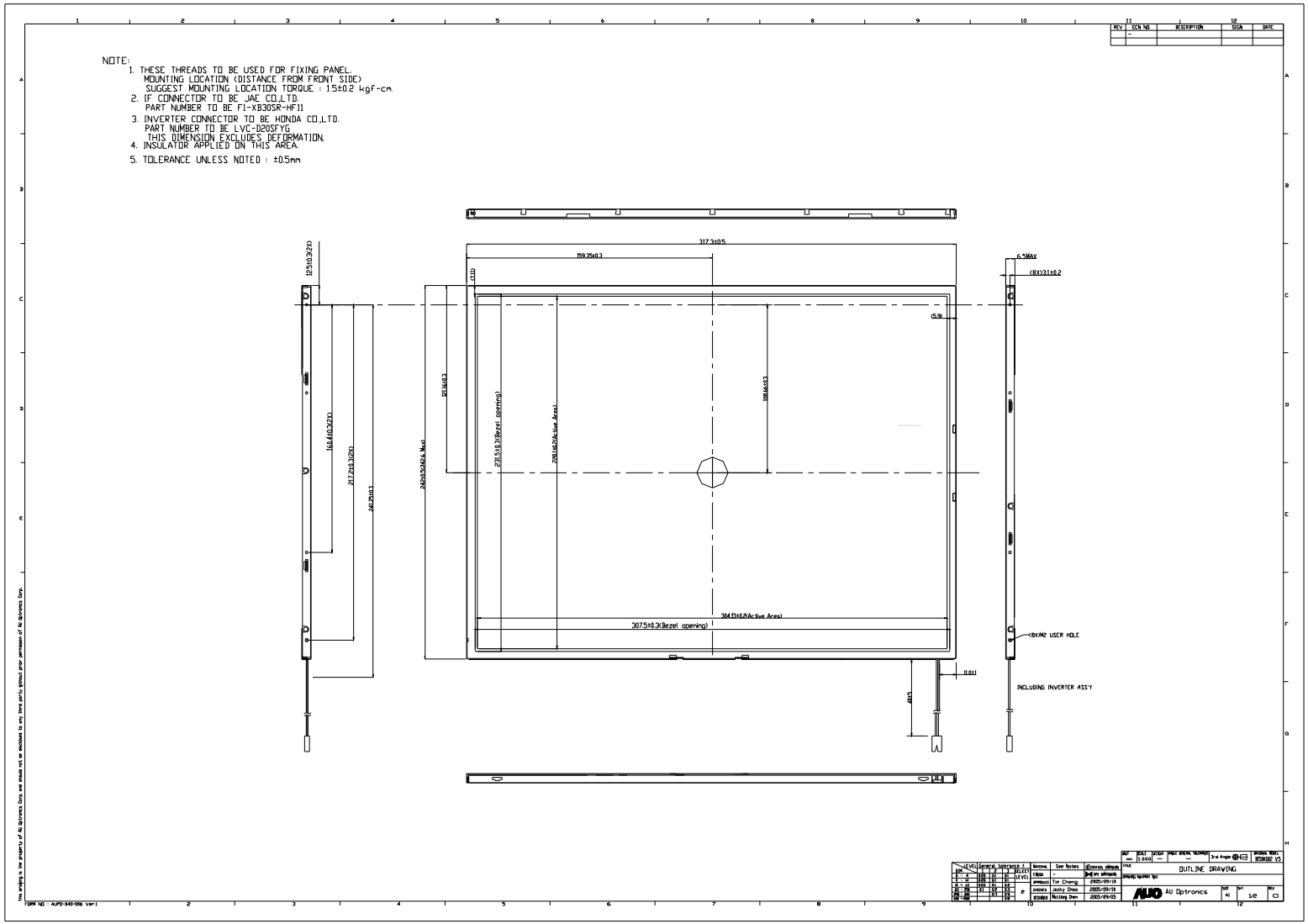
. Self-recoverable. No hardware failures.

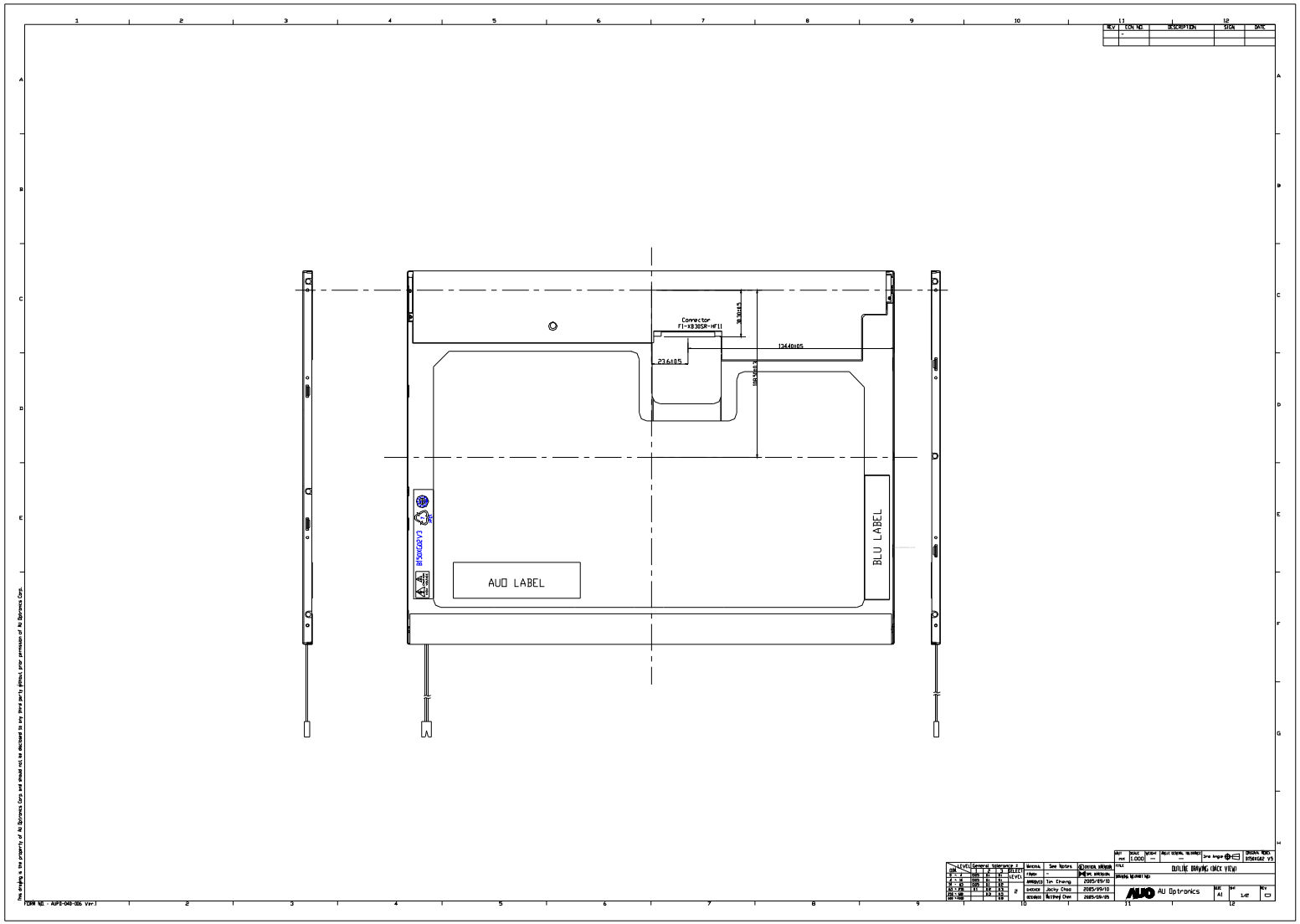
Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension

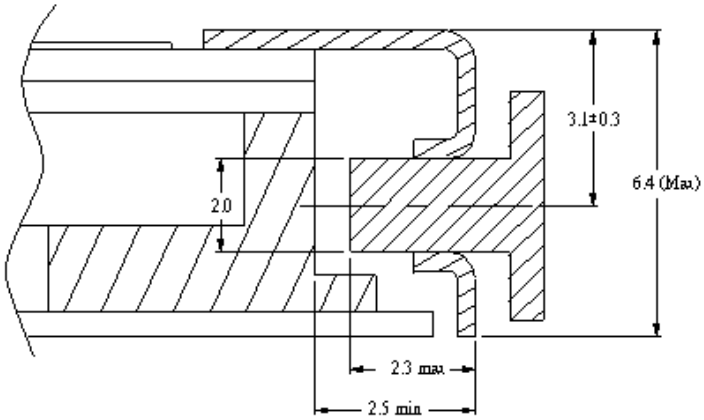



Connector
FI-XB30SR-HF11
AUO LABEL
BLU LABEL
OUTLINE DRAWING (BACK VIEW)

10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.5 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.3mm (See drawing)
Screw Torque: Maximum 2.5 kgf-cm



11.1 Shipping Label Format

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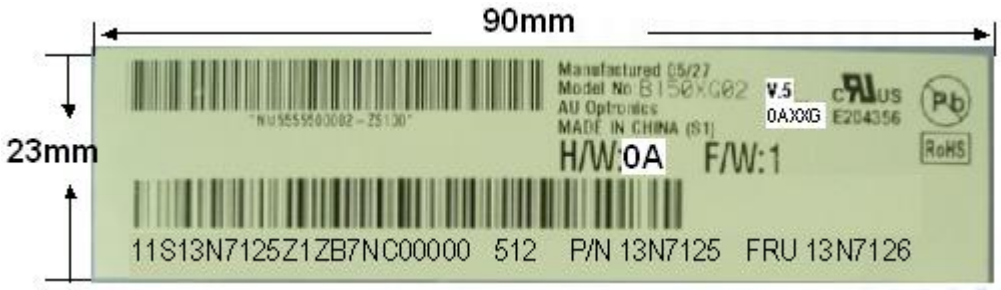
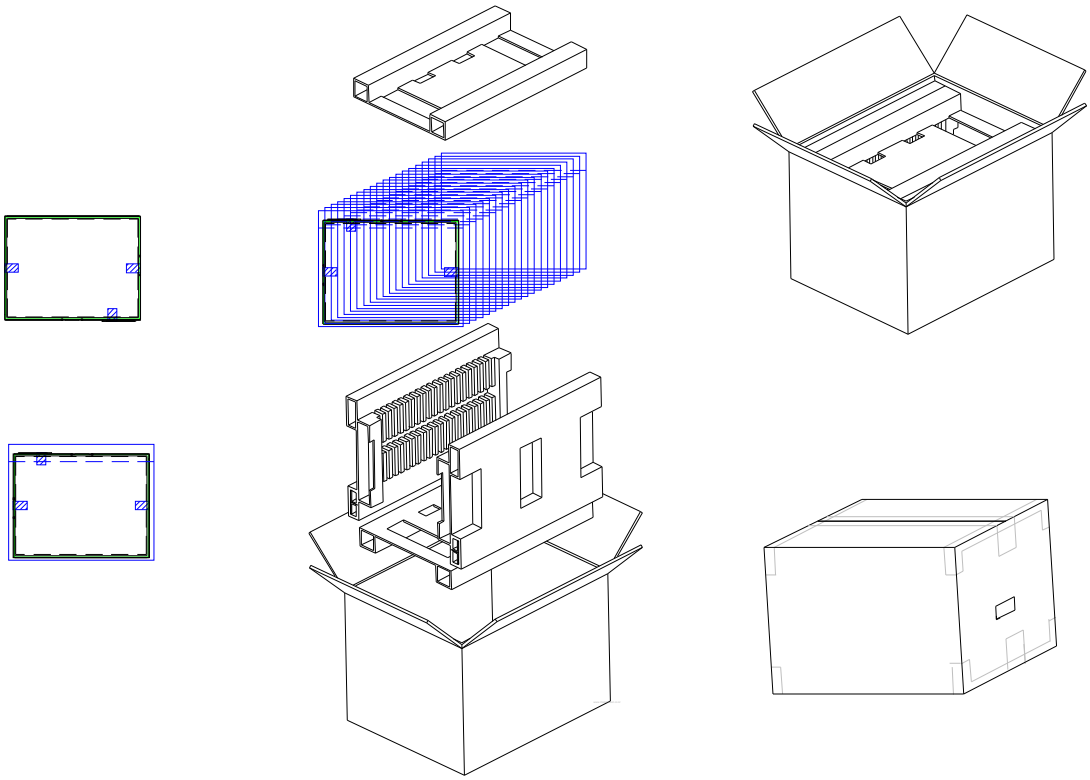


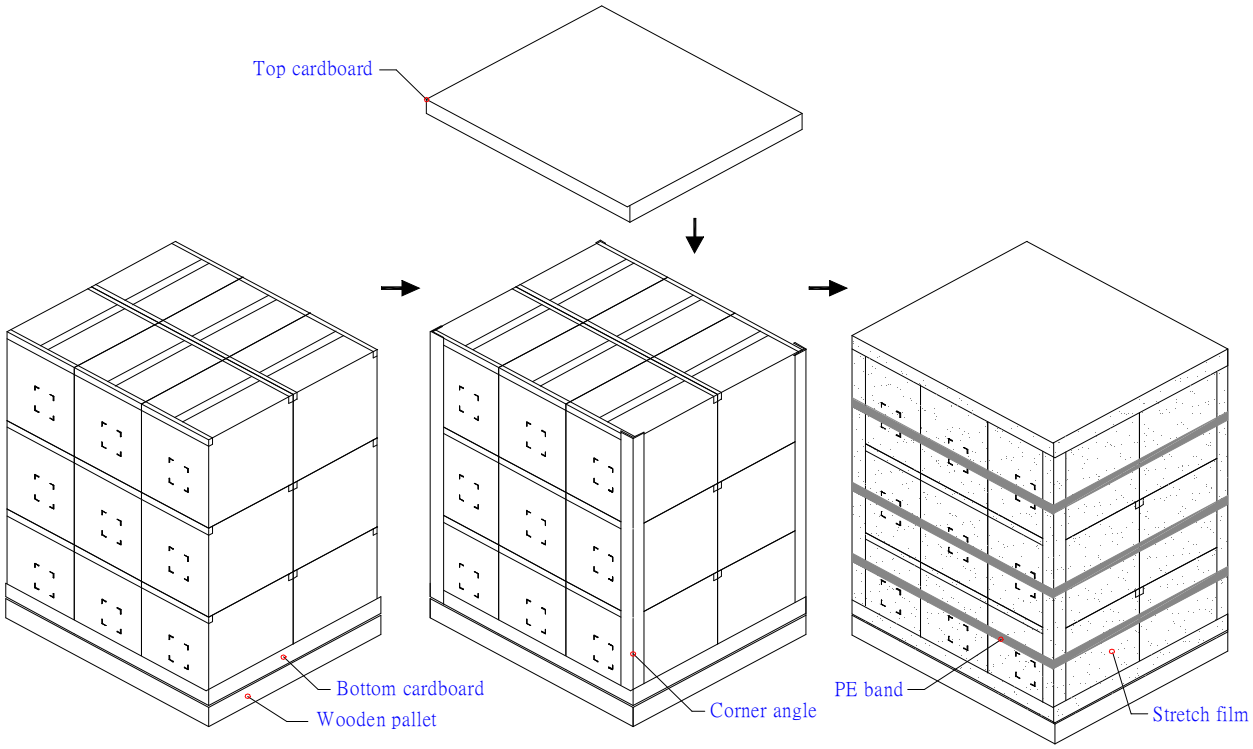
Note 1:

IC Combination	Control Code	H/W
Source IC: MEC MNF816BG-RD Gate IC: TSB JBT6LA2-AS	0AXXG	0A

11.2. Carton package



11.3 Shipping package of palletizing sequence



Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

12. Appendix: EDID description

Byte# (decimal)	Byte# (HEX)	Field Name and Comments	Value (HEX)		Data		
0	00	Header	0	0			Header
1	01	Header	F	F			
2	02	Header	F	F			
3	03	Header	F	F			
4	04	Header	F	F			
5	05	Header	F	F			
6	06	Header	F	F			
7	07	Header	0	0			
8	08	ID system Manufacturer Name	**3**	**0**	**LEN**		Vender/ Product ID
9	09	Compressed ASCII	**A**	**E**			
10	0A	ID Product Code	**4**	**0**	**XGA (4040)**		
11	0B	ID Product Code	**4**	**0**			
12	0C	LCD Module Serial No. = 0 (If not used)	0	0			
13	0D	LCD Module Serial No. = 0 (If not used)	0	0			
14	0E	LCD Module Serial No. = 0 (If not used)	0	0			
15	0F	LCD Module Serial No. = 0 (If not used)	0	0			
16	10	Week of Manufacture	0	1	week 01		
17	11	Year of Manufacture	0	F	15(2005-1990 =15)		
18	12	EDID Structure version	0	1	1		EDID Version/ Revision
19	13	EDID Revision	0	3	3		
20	14	Video Input Definition = Digital I/P,non TMDS CRGB	8	0			Display Parameter
21	15	Max H image size(cm) = 33.12 cm	1	E	30		
22	16	Max V image size(cm) = 20.70 cm	1	7	23		
23	17	Display gamma	7	8	2.2		
24	18	Feature support(DPMS) = Active off, RGB Color	**E**	**A**			
25	19	Red/Green low Bits	8	7	RxRyGxGy		Color Characteristic
26	1A	Blue/White Low Bits	F	5	BxByWxWy		
27	1B	Red X	9	4	Rx=0.580		
28	1C	Red Y	5	7	Ry=0.340		
29	1D	Green X	4	F	Gx=0.310		
30	1E	Green Y	8	C	Gy=0.550		
31	1F	Blue X	2	7	Bx=0.155		
32	20	Blue Y	2	7	By=0.155		
33	21	White X	5	0	Wx=0.313		

34	22	White Y	5	4	Wy=0.329		
35	23	Established Timing I = 00h(If not used)	**2**	**1**			**Established Timings**
36	24	Established Timing II = 00h(If not used)	**0**	**8**			
37	25	Manufacturer's Timings = 00h(If not used)	0	0			
38	26	Standard Timing Identification 1 was not used	0	1			**Standard Timing ID**
39	27	Standard Timing Identification 1 was not used	0	1			
40	28	Standard Timing Identification 2 was not used	0	1			
41	29	Standard Timing Identification 2 was not used	0	1			
42	2A	Standard Timing Identification 3 was not used	0	1			
43	2B	Standard Timing Identification 3 was not used	0	1			
44	2C	Standard Timing Identification 4 was not used	0	1			
45	2D	Standard Timing Identification 4 was not used	0	1			
46	2E	Standard Timing Identification 5 was not used	0	1			
47	2F	Standard Timing Identification 5 was not used	0	1			
48	30	Standard Timing Identification 6 was not used	0	1			
49	31	Standard Timing Identification 6 was not used	0	1			
50	32	Standard Timing Identification 7 was not used	0	1			
51	33	Standard Timing Identification 7 was not used	0	1			
52	34	Standard Timing Identification 8 was not used	0	1			
53	35	Standard Timing Identification 8 was not used	0	1			
54	36	Pixel Clock/10,000 (LSB)	6	4	65.00MHz		**Timing Descriptor #1**
55	37	Pixel Clock/10,000 (MSB) /	1	9			
56	38	Horizontal Active	0	0	1024 pixels		
57	39	Horizontal Blanking	4	0	320 pixels		
58	3A	Horizontal Active : Horizontal Blanking	4	1			
59	3B	Vertical Avtive	0	0	768 lines		
60	3C	Vertical Blanking	2	6	38 lines		
61	3D	Vertical Active : Vertical Blanking	3	0			
62	3E	Horizontal Sync. Offset	1	8	24 pixels		
63	3F	Horizontal Sync Pulse Width	8	8	136 pixels		
64	40	Vertical Sync Offset : Sync Width	3	6	3/6 lines		
65	41	Horizontal Vertical Sync Offset/Width upper 2bits = 0	0	0	0		
66	42	Horizontal Image Size	3	0	304		
67	43	Vertical Image Size	E	4	228		
68	44	Horizontal & Vertical Image Size	1	0			
69	45	Horizontal Border = 0	0	0			
70	46	Vertical Border = 0	0	0			
71	47	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol	1	8			

		negatives					
72	48	Pixel Clock/10,000 (LSB) 50Hz	2	8	54.16MHz		Timing Description #2
73	49	Pixel Clock/10,000 (MSB) / 50Hz	1	5			
74	4A	Horizontal Active	0	0	1024 pixels		
75	4B	Horizontal Blanking	4	0	320 pixels		
76	4C	Horizontal Active : Horizontal Blanking	4	1			
77	4D	Vertical Avtive	0	0	768 lines		
78	4E	Vertical Blanking	2	6	38 lines		
79	4F	Vertical Active : Vertical Blanking	3	0			
80	50	Horizontal Sync. Offset	1	8	24 pixels		
81	51	Horizontal Sync Pulse Width	8	8	136 pixels		
82	52	Vertical Sync Offset : Sync Width	3	6	3/6 lines		
83	53	Horizontal Vertical Sync Offset/Width upper 2bits = 0	0	0	0		
84	54	Horizontal Image Size	3	0	304		
85	55	Vertical Image Size	E	4	228		
86	56	Horizontal & Vertical Image Size	1	0			
87	57	Horizontal Border = 0	0	0			
88	58	Vertical Border = 0	0	0			
89	59	Non-interlaced,Normal display,no stereo,Digital separate sync,H/V pol negatives	1	8			
90	5A	Detailed Timing Descriptor #3	0	0	0		Timing Description #3
91	5B		0	0	0		
92	5C		0	0	0		
93	5D		0	F	15		
94	5E		0	0	0		
95	5F	(Horizontal active pixel /8)-31	6	1	129		
96	60	Image Aspect Ratio(16:10)	4	3	4 : 3		
97	61	Low Refresh Rate #1(50Hz)	3	2	50		
98	62	(Horizontal active pixel /8)-31	6	1	129		
99	63	Image Aspect Ratio(16:10)	4	3	4 : 3		
100	64	Low Refresh Rate #2(40Hz)	2	8	40		
101	65	Brightness(1/10nit)	**0**	**F**	**15**		
102	66	Feature flag(TN mode)	0	1	1		
103	67	Reserved 00h	0	0	0		
104	68	EISA manufacturer code(3 Character ID)	0	6	AUO?		
105	69	Compressed ASCII	A	F			
106	6A	Panel Supplier Reserved - Product code	5	1			
107	6B	(Hex, LSB first)	2	5			

108	6C	Detailed Timing Descriptor #4	0	0			
109	6D		0	0			
110	6E		0	0			
111	6F		F	E			
112	70		0	0			
113	71	(Supplier S/N)	4	1	A		
114	72	(Supplier S/N)	5	5	U		
115	73	(Supplier S/N)	4	F	O		**Timing**
116	74	(Supplier S/N)	4	2	B		**Description**
117	75	(Supplier S/N)	3	1	1		**#4**
118	76	(Supplier S/N)	3	5	5		
119	77	(Supplier S/N)	3	0	0		
120	78	(Supplier S/N)	5	8	X		
121	79	(Supplier S/N)	4	7	G		
122	7A	(Supplier S/N)	3	0	0		
123	7B	(Supplier S/N)	3	2	2		
124	7C	(Supplier S/N)	5	6	V		
125	7D	(Supplier S/N)	3	5	5		
126	7E	Extension flag = 00	0	0			**Extension Flag**
127	7F	Checksum	**5**	**1**			**Checksum**