AU OPTRONICS CORPORATION

Product Specification

15.4" WXGA Color TFT-LCD Module

Model Name: B154EW01 V9

Approved by	Prepared by
Joselyn Liu	*Zephyr Hsu*

MDBU Marketing Division / AU Optronics corporation

Customer	Checked & Approved by

Product Specification

15.4" WXGA Color TFT-LCD Module
Model Name: B154EW01 V9

(V) Preliminary Specifications
( ) Final Specifications

Note: This Specification is subject to change without notice.

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2005/04/27	All	First Edition for Customer		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.

10)At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.

11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside.   Otherwise the TFT Module may be damaged.

12)Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.

13)Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.

14)The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

2. General Description

B154EW01 V9 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter card of backlight is not included.

B154EW01 V9 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

| Items	Unit	Specifications
Screen Diagonal	[mm]	391 (15.4W")
Active Area	[mm]	331.2 X 207.0
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.2588X0.2588
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance (ICFL=6.0mA)	[cd/m^2]	180 typ. (5 points average) 150 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 typ.
Optical Rise Time/Fall Time	[msec]	12/4 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Typical Power Consumption	[Watt]	6.5W max.
Weight	[Grams]	585g typ.
Physical Size (typ.*typ.*max)	[mm]	344.0x 222.0 x 6.5 max.
Electrical Interface		1 channel LVDS
Surface Treatment		Glare, Harness 3H, Reflectance 4.3%
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range 　Operating 　Storage (Non-Operating)	[^{o}C] [^{o}C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 ℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance CCFL 6.0mA	[cd/m2]	5 points average	150	180	-	1,2,3
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	- -	45 45	- -	2,7
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	- -	15 35	- -	
Uniformity		5 Points			1.25	1
Uniformity		13 Points			1.50	
CR: Contrast Ratio			350	400	-	6
Cross talk	%				4	4
Response Time	[msec]	Rising	-	12	17	5
	[msec]	Falling	-	4	8	
	[msec]	Raising + Falling		16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.570	0.600	0.630	2,7
		Red y	0.300	0.340	0.370	
		Green x	0.280	0.310	0.340	
		Green y	0.530	0.560	0.590	
		Blue x	0.120	0.150	0.180	
		Blue y	0.085	0.115	0.145	
		White x	0.290	0.313	0.343	
		White y	0.299	0.329	0.350	

Note 1: 5 points position (Display area : 331.2mm x 207.0mm)
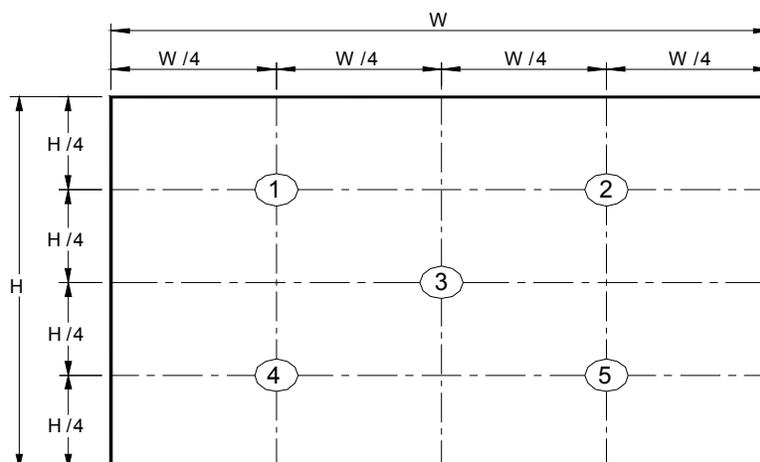
Note 2: 13 points position
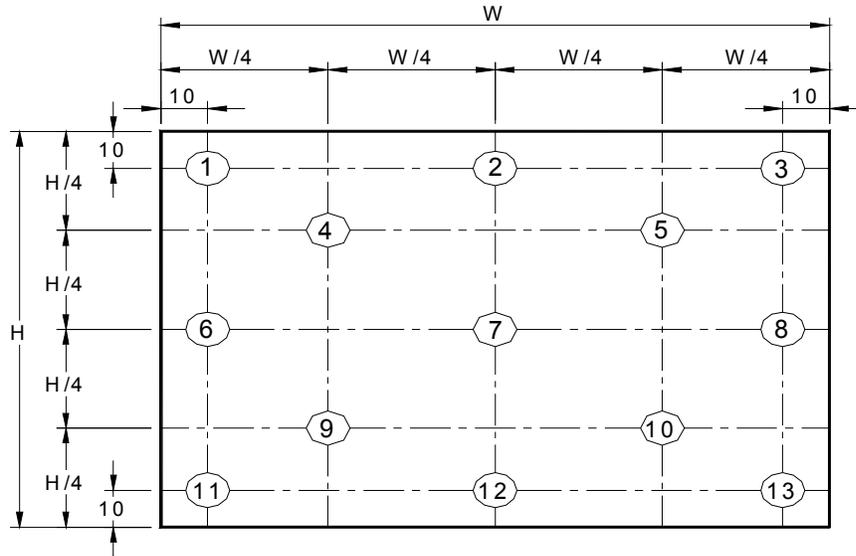
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.

Photo detector

Field=2°

50 cm

LCD Panel

TFT-LCD

Center of the screen
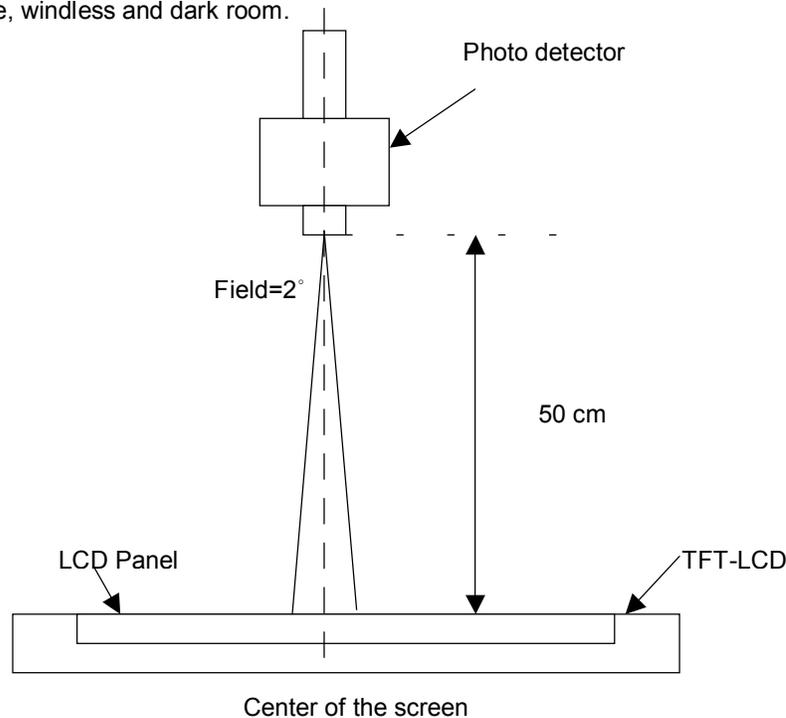
Note 5 : Definition of Cross Talk (CT)

$CT = |Y_B - Y_A| / Y_A \times 100\ (\%)$

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)
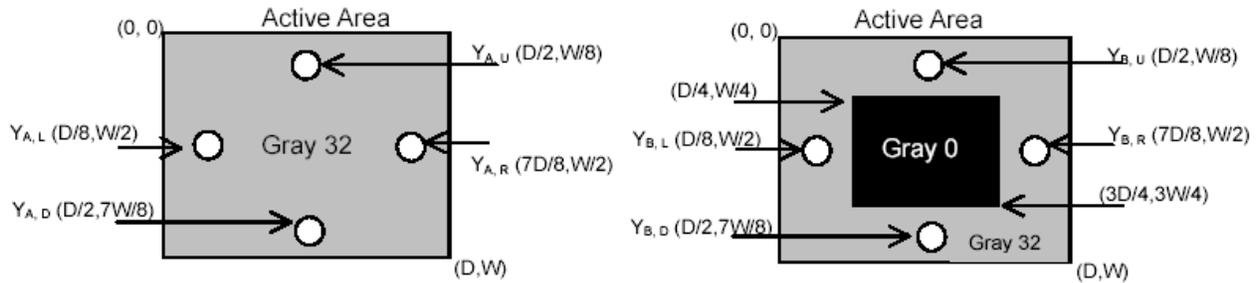
Note 6: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.
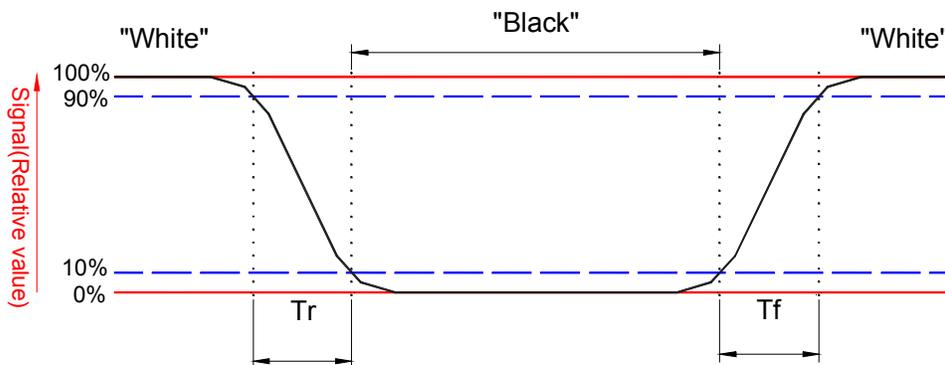
Note 7. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.
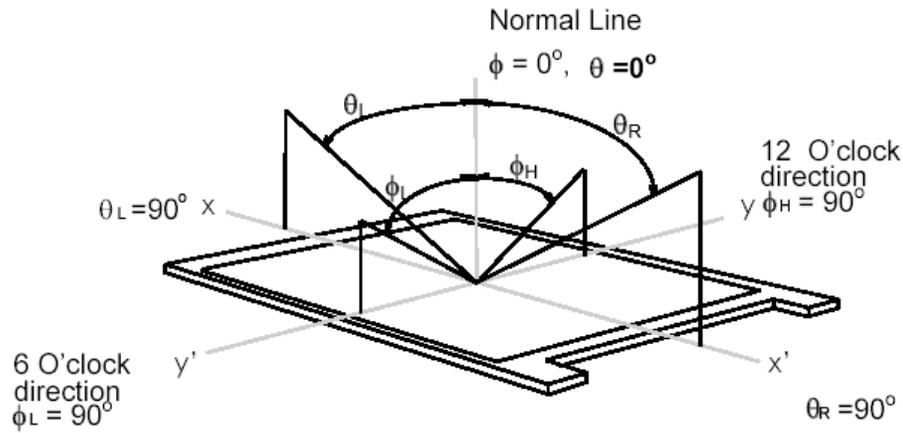
3. Functional Block Diagram

The following diagram shows the functional block of the 15.4 inches wide Color TFT/LCD Module:

Product Specification
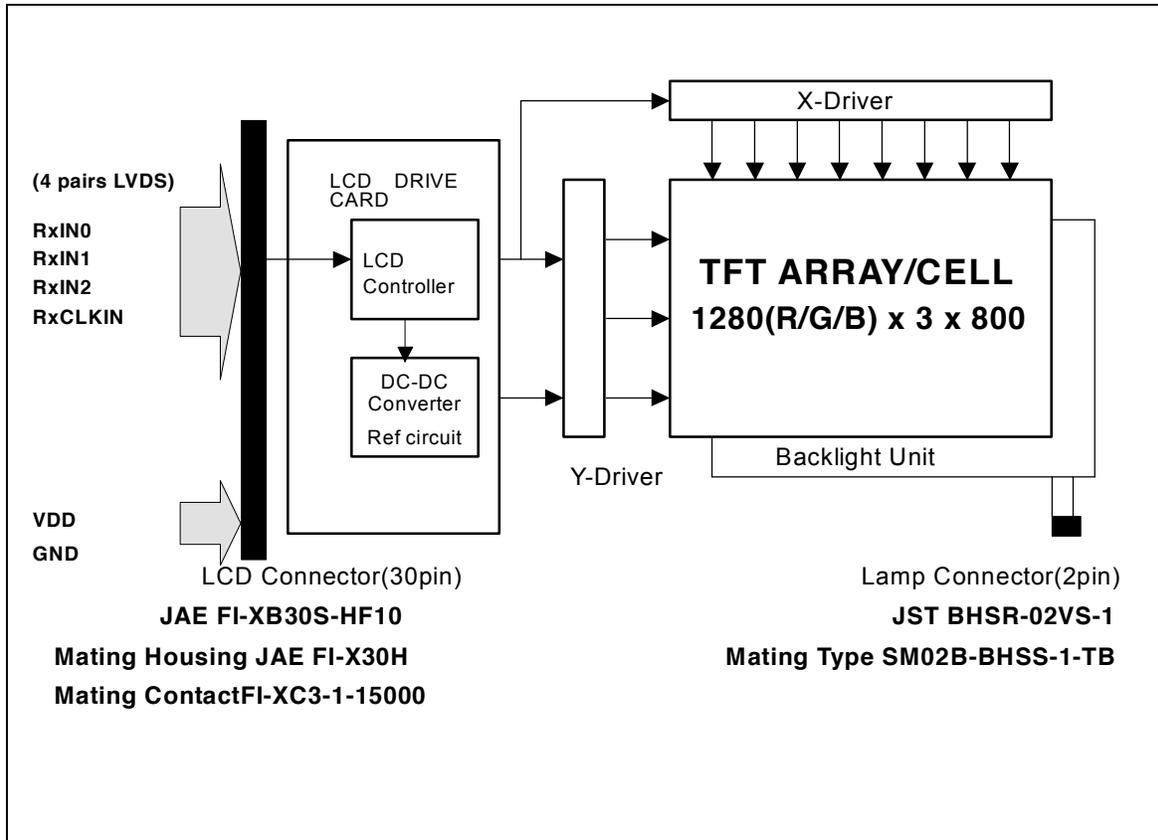
4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings ofBacklight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICFL	-	6.5	[mA] rms	Note 1,2

4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[^{o}C]	Note 3
Operation Humidity	HOP	8	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[^{o}C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: With in Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality perfermance, please refer to AUO IIS(Incoming Inspection Standard).
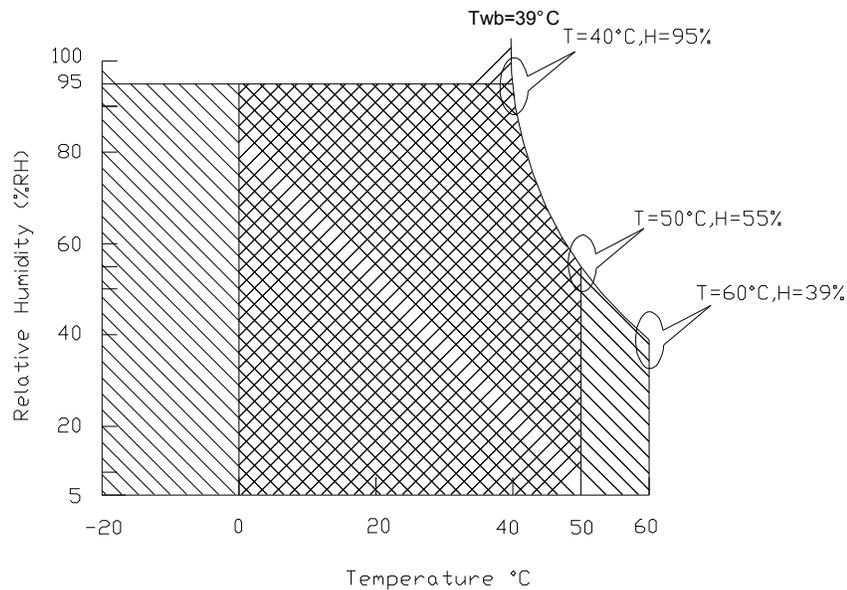
Operating Range · Storage Range

5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power			2	[Watt	Max:All Black Pattern
IDD	IDD Current		500	600	mA	Max:All Black Pattern
IRush	Inrush Current			1800	mA	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

Note 1 : Measurement conditions:
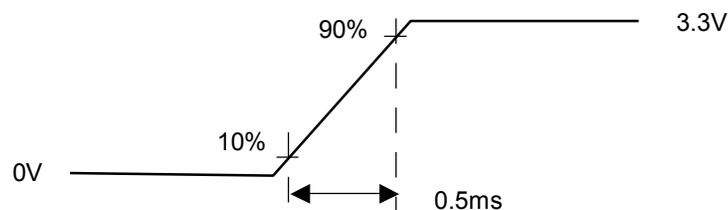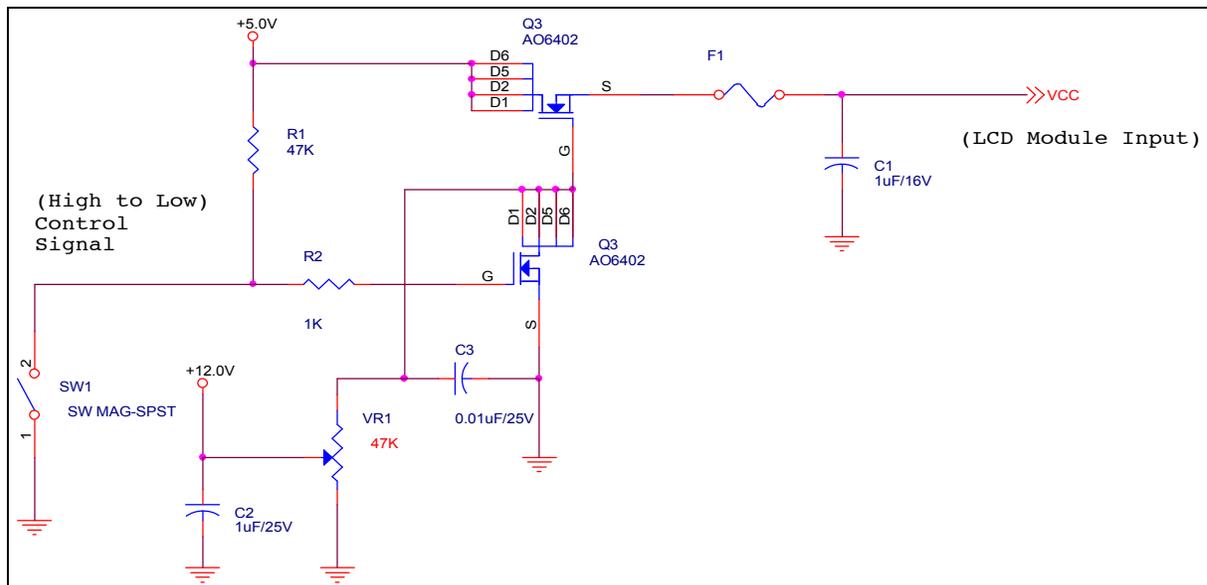
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]

Note: LVDS Signal Waveform
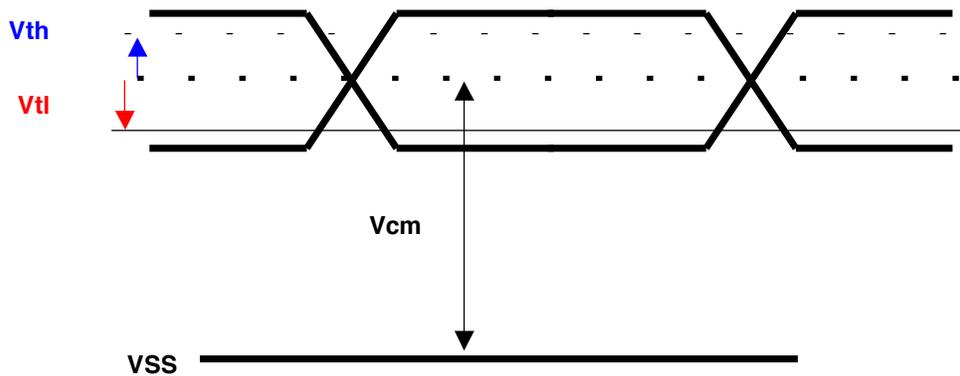
LVDS Macro AC characteristics are as follows:

	Min.	Max.
Clock Frequency (T)	50MHz	85MHz
Data Setup Time (Tsu)	1ns	
Data Hold Time (Thd)	1ns	

Product Specification
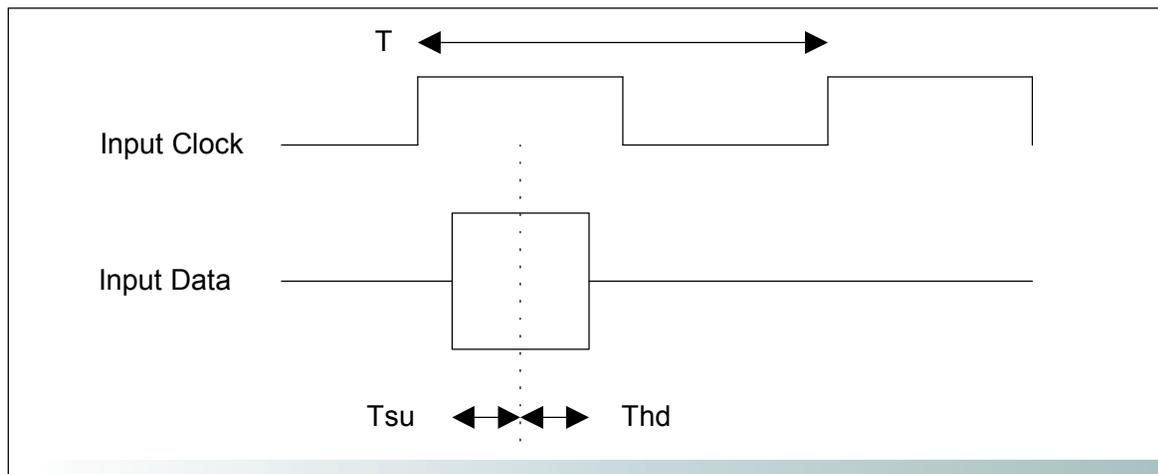
5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	-	180	-	[cd/m^2]	(Ta=25℃)
CCFL current(ICFL)	3.0	6.0	6.5	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(FCFL)	50	60	70	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)	1430			[Volt] rms	(Ta= 0℃) Note 5
CCFL Voltage (Reference) (VCFL)	-	720	-	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (PCFL)	3.87	4.30	4.50	[Watt]	(Ta=25℃) Note 6

Note 1: Typ are AUO recommended Design Points.
　　*1 All of characteristics listed are measured under the condition using the AUO Test inverter.
　　*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
　　*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.
　　*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
　　*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.
　　*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.
Note 2: It should be employed the inverter which has "Duty Dimming", if ICFL is less than 4mA.
Note 3: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.
Note 4: The frequency range will not affect to lamp life and reliability characteristics.
Note 5: CFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.
Note 6: Calculator value for reference (ICFL×VCFL=PCFL)

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.
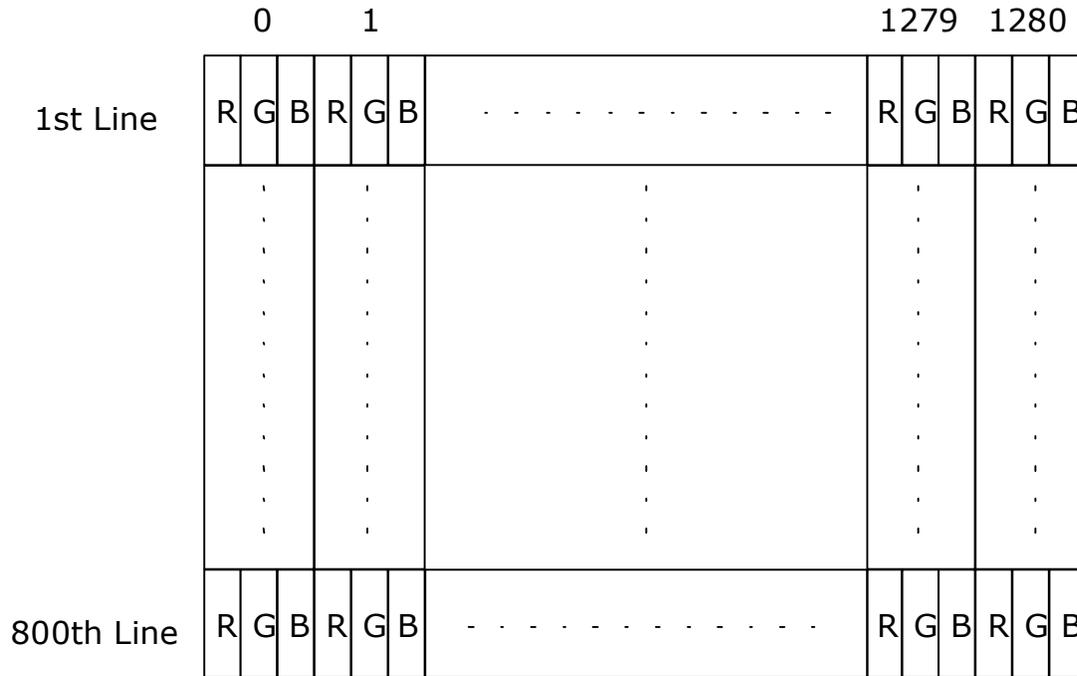
6.2 The input data format

Signal Name	Description	
RED5 RED4 RED3 RED2 RED1 RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
GREEN 5 GREEN 4 GREEN 3 GREEN 2 GREEN 1 GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
BLUE 5 BLUE 4 BLUE 3 BLUE 2 BLUE 1 BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	Display Timing	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to -DTCLK .
HSYNC	Horizontal Sync	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

6.3 Signal Description

The LVDS receiver equipped in this LCD module is compatible with SN75LVDS86 standard. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

PIN#	Signal Name	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V_{EDID}	+3.3V EDID Power
5	NC	No Connection (For AUO test)
6	CLK_{EDID}	EDID Clock Input
7	$DATA_{EDID}$	EDID Data Input
8	RxIN0-	LVDS differential data input(Red0-Red5, Green0)
9	RxIN0+	LVDS differential data input(Red0-Red5, Green0)
10	GND	Ground
11	RxIN1-	LVDS differential data input(Green1-Green5, Blue0-Blue1)
12	RxIN1+	LVDS differential data input(Green1-Green5, Blue0-Blue1)
13	GND	Ground
14	RxIN2-	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
15	RxIN2+	LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input
18	RxCLKIN+	LVDS differential clock input
19	GND	Ground
20	GND	Ground
21	NC	No Connection (For AUO test)
22	NC	No Connection (For AUO test)
23	NC	No Connection (For AUO test)
24	NC	No Connection (For AUO test)
25	NC	No Connection (For AUO test)
26	NC	No Connection (For AUO test)
27	NC	No Connection (For AUO test)
28	NC	No Connection (For AUO test)
29	NC	No Connection (For AUO test)
30	NC	No Connection (For AUO test)

Connector

30

N C

1

GND
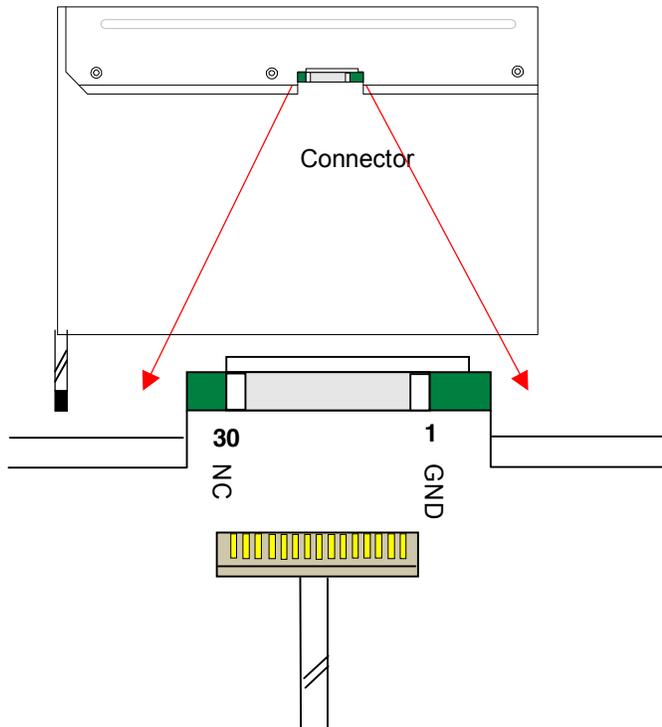
Note1: Start from right side

Note2: Please follow PSWG.

Note3: Input signals shall be low or Hi-Z state when VDD is off.

Internal circuit of LVDS inputs are as following.

The module uses a 100ohm resistor between positive and negative data lines of each receiver input

Signal Input

SN75LVDS86 or Compatible

Pin No.

8   RxIN0-

R

9   RxIN0+

11 RxIN1-

R

12 RxIN1+

14 RxIN2-

R

15 RxIN2+

17 RxCLKIN-

R

18 RxCLKIN+

Product Specification
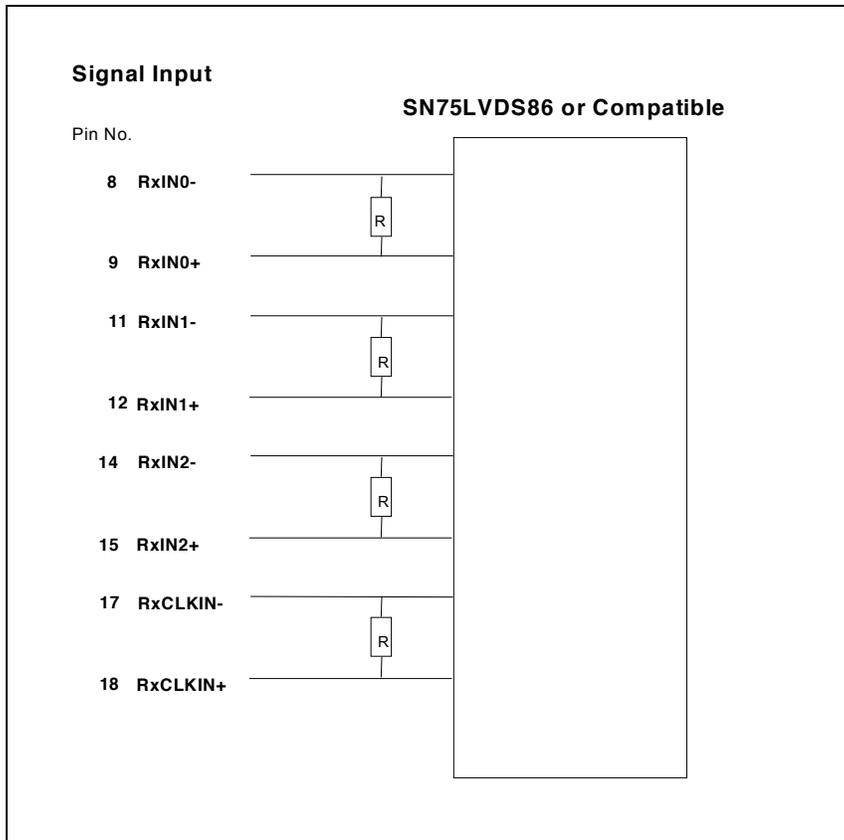
6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz   manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		1/ T_{Clock}	50	68.9	85	MHz
Vertical Section	Period	T_V	803	816	832	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	16	32	
Horizontal Section	Period	T_H	1302	1408	1700	T_{Clock}
	Active	T_{HD}	-	1280	-	
	Blanking	T_{HB}	22	128	420	
End-frame checking period		tEF		2		T_{Line}
DE checking period		tDE		6400		T_{Line}

Note : DE mode only

6.4.2 Timing diagram
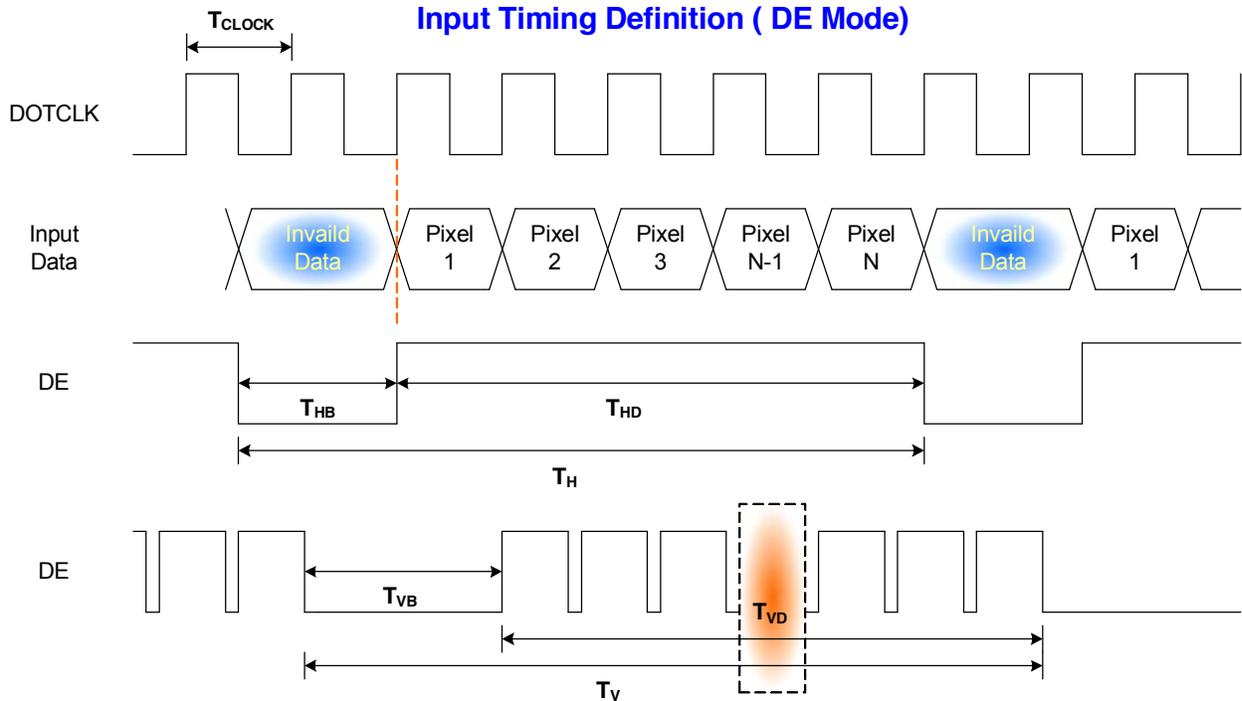
6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.
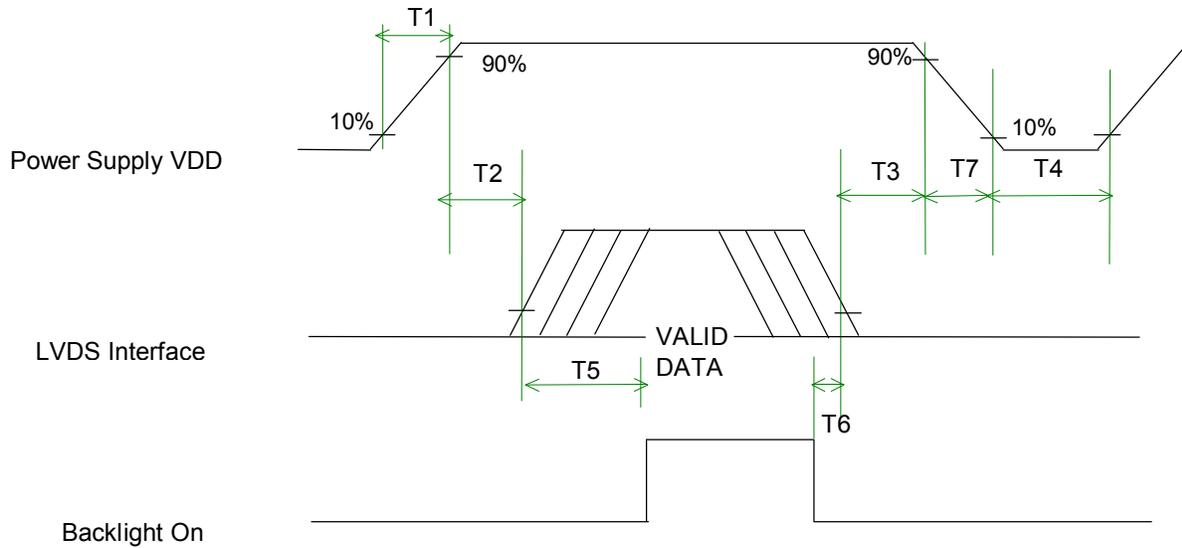
Power Sequence Timing

Parameter	Value			Units
	Min.	**Typ.**	**Max.**	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector & Pin Assignment

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30M, FI-X30C or FI-X30H
Mating Contact/Part Number	FI-C3-A1

Pin#	Signal Name	Pin#	Signal Name
1	GND	2	VDD
3	VDD	4	VEDID
5	NC	6	CLKEDID
7	DATAEDID	8	RxIN0-
9	RxIN0+	10	GND
11	RxIN1-	12	RxIN1+
13	GND	14	RxIN2-
15	RxIN2+	16	GND
17	RxCLKIN-	18	RxCLKIN+
19	GND	20	GND
21	NC	22	NC
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	NC	30	NC

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

Test method:	Non-Operation
Acceleration:	2.16G
Frequency:	10 - 500Hz Random
Sweep:	30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

Test method:	Non-Operation
Acceleration:	220 G , Half sine wave
Active time:	2 ms
Pulse:	X,Y,Z .one time for each side

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40℃/90%,300Hr	
High Temperature Operation	60℃/Dry,300Hr	
Low Temperature Operation	0℃,300Hr	
On/Off Test	25℃,150hrs(ON/10 sec. OFF/10sec., 10,000 cycles)	
Hot Storage	60℃/35% RH ,250 hours	
Cold Storage	-20℃/50% RH ,250 hours	
Thermal Shock Test	-20℃/30 min ,60℃/30 min 100cycles	
Hot Start Test	50℃/1 Hr min.　power on/off per 5 minutes, 5 times	
Cold Start Test	0℃/1 Hr min.　power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	220G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Random vibration, 2.16 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact : ±8KV/ operation Air : ±15KV / operation	Note 1
Room temperature Test	25℃, 2000hours, Operating with loop pattern	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

　　.　Self-recoverable. No hardware failures.

Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

10.1 LCM Outline Dimension

NOTES:
1. NUMBER OF PIXELS: 1280X3(R,G,B)X800.
2. SIGNAL INTERFACE CONNECTOR SPEC:
   MAKER: JAE OR COMPATIBLE.
   INPUT: JAE FI-XB30SL-HF10.
3. BACKLIGHT CCFL CONNECTOR SPEC:
   MAKER: JST.
   PART NO: BHSR-02VS-1.
4. ALLOWED DEPTH OF USERHOLE SCREW INSERTION IS MAX 2.5MM.
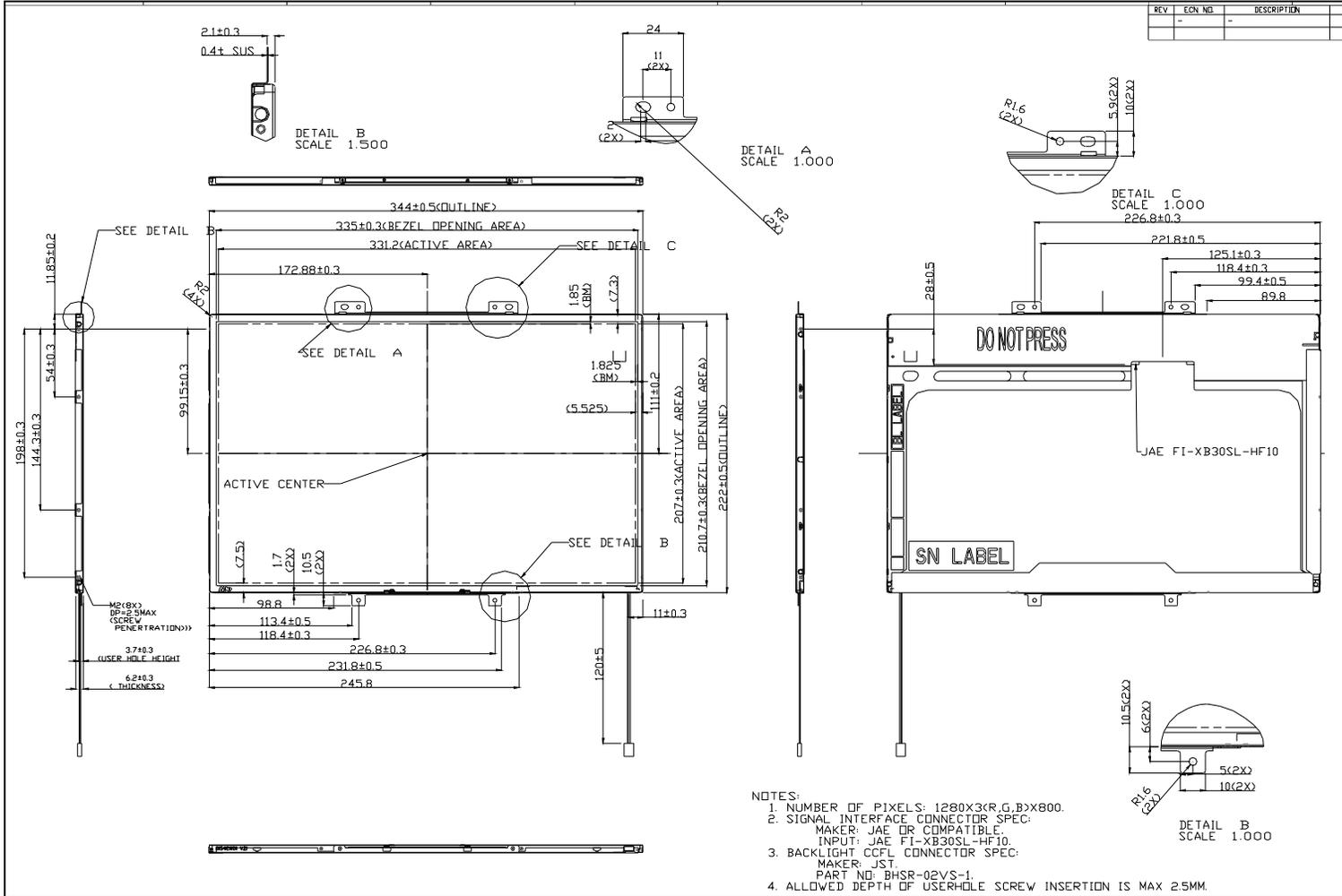
10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.5 mm (See drawing)

Screw hole center location, from front surface = 3.7 ± 0.2mm (See drawing)
Screw Torque: Maximum 2.5 kgf-cm
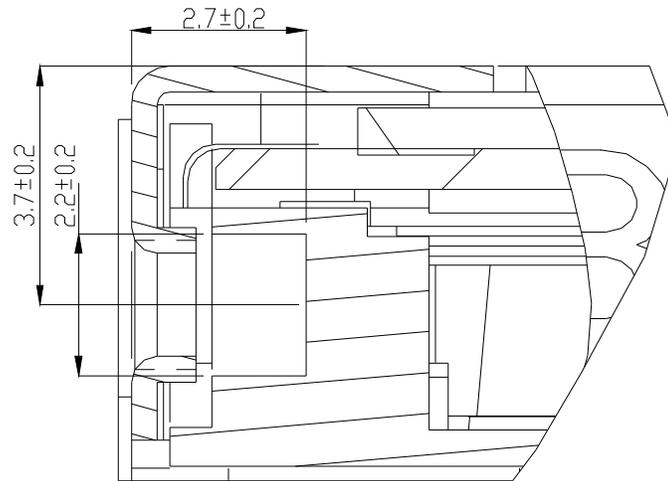
11. Shipping and Package

11.1 Shipping Label Format

| Model name | Week code | Manufacturing area |

Model No B154EW01 V9   04/01
AU optronics   0AXXX G

*XXXXXXXXXXXX-XXXXX

H/W : **0A**   F/W : **1**

Control code

Hardware : Note1

Firmware
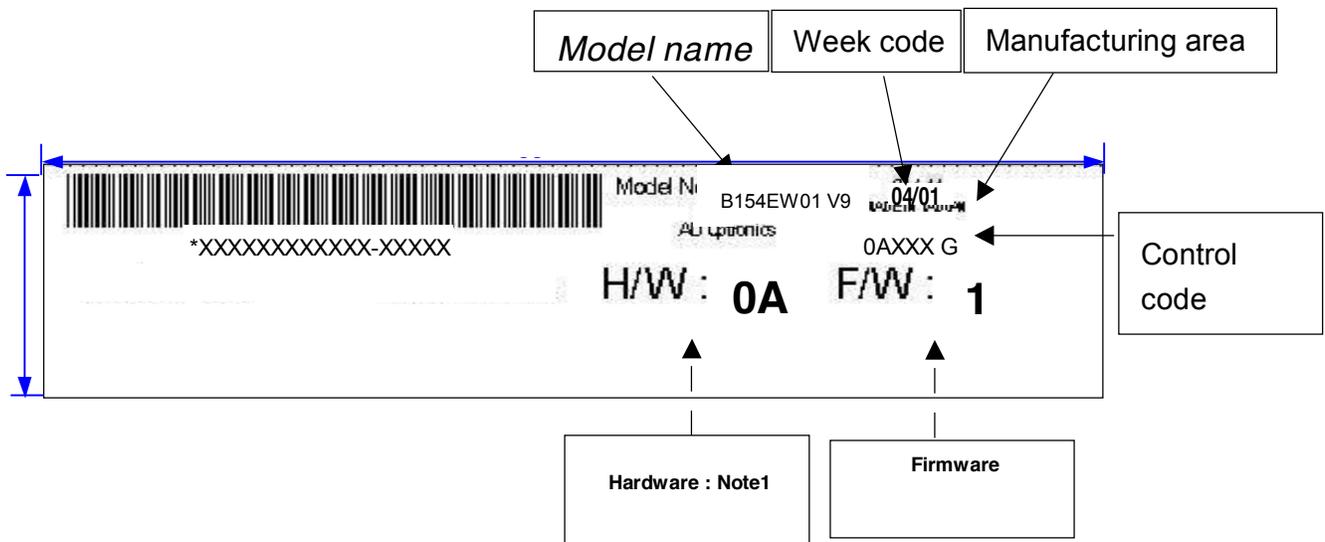
Note 1:

IC Combination	Control Code	H/W
Source IC:NT39360 Gate IC: NT 3959C	OAXXX	OA
Source TSBT6L92A Gate IC: NECupd160703	1AXXX	1A

11.2. Carton package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm
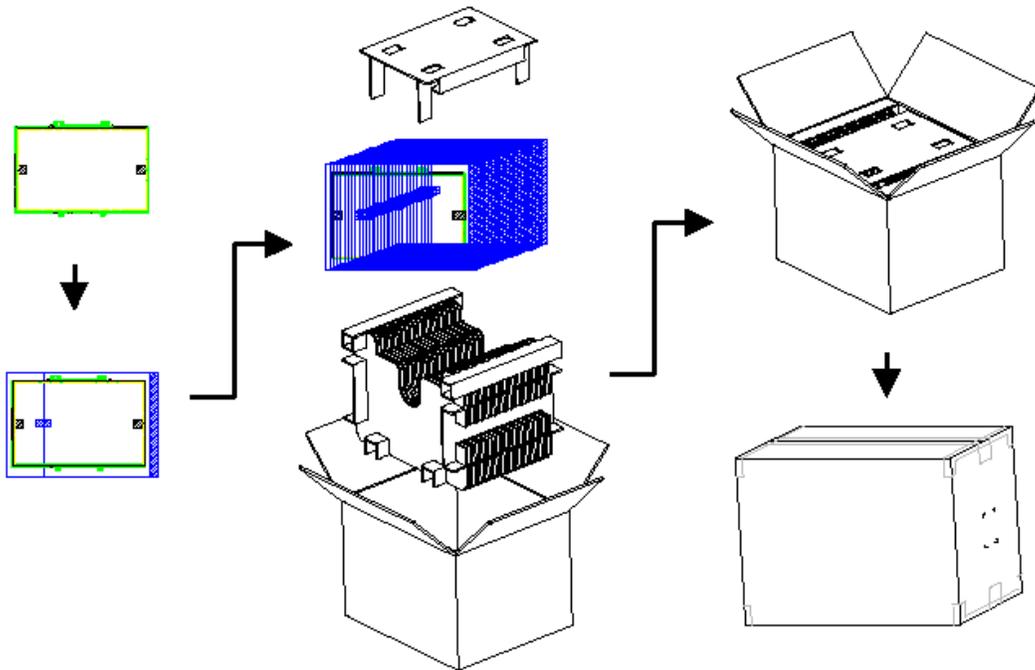
11.3 Shipping package of palletizing sequence

Top cardboard

Bottom cardboard

Wooden pallet

Corner angle

PE band

Stretch film
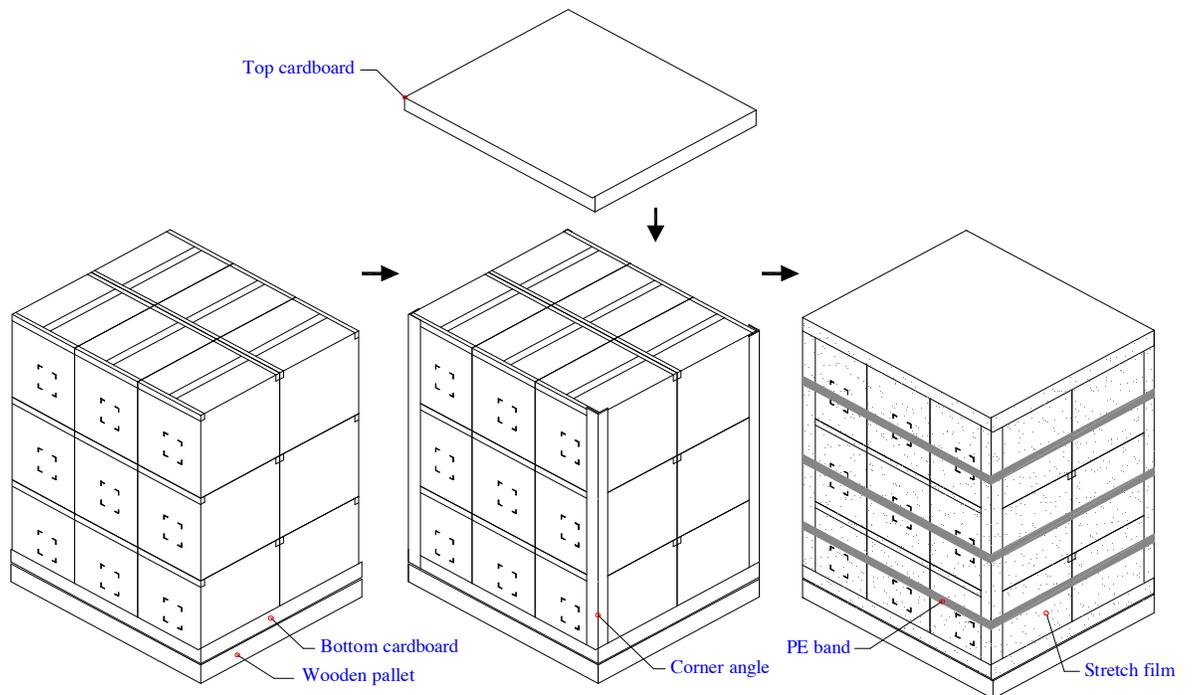
Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

12. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Notes
HEX		HEX	BIN	DEC	Date: Apr/19/2005
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	ASCII Data String:B154EW01
09	Compressed ASCII	AF	10101111	175	AUO
0A	Product Code	74	01110100	116	15.4"(0111)+1280x800(0100)
0B	hex, LSB first	19	00011001	25	B154EW01(0001)+V9(1001)
0C	32- bit ser #	00	00000000	0	unused
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	01	00000001	1	Week 42
11	Year of manufacture	0F	00001111	15	15(2005- 1990=15)
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	Video input definition	80	10000000	128	Digital Input
15	Max H image size	21	00100001	33	33.12cm
16	Max V image size	15	00010101	21	20.7cm
17	Display Gamma	78	01111000	120	Gamma 2.2
18	Feature support	0A	00001010	10	no DPMS,Active off,RGB color
19	Red/green low bits	85	10000101	133	
1A	Blue/white low bits	A5	10100101	165	
1B	Red x/ high bits	99	10011001	153	Rx=0.6
1C	Red y	57	01010111	87	Ry=0.34
1D	Green x	4F	01001111	79	Gx=0.31
1E	Green y	8F	10001111	143	Gy=0.56
1F	Blue x	26	00100110	38	Bx=0.15
20	Blue y	1D	00011101	29	By=0.115
21	White x	50	01010000	80	Wx=0.313
22	White y	54	01010100	84	Wy=0.329
23	Established timing 1	00	00000000	0	unused
24	Established timing 2	00	00000000	0	__
25	Manufacturer's Timing	00	00000000	0	

26	Standard timing #1	01	00000001	1	unused
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10,000 (LSB)	EA	11101010	234	**Timing Descriptor #1**
37	Pixel Clock/10,000 (MSB)	1A	00011010	26	**1280x800 @60_mode:pixel clock=68.9MHz**
38	Horiz. Active pixels(Lower 8 bits)	00	00000000	0	**Horiz active=1280 pixels**
39	Horiz.Blanking (Lower 8 bits)	80	10000000	128	**Horiz blanking=128 pixels**
3A	Horiz. Active pixels:Horiz. Blanking (Upper4:4 bits)	50	01010000	80	
3B		20	00100000	32	**Vertcal active=800 lines**
3C		10	00010000	16	**Vertical blanking=16 lines**
3D	Vert. Active pixels:Vert. Blanking (Upper4:4 bits)	30	00110000	48	
3E		15	00010101	21	**Horiz sync. Offset=21 pixels**
3F		20	00100000	32	**Horiz sync. Pulse Width=32 pixels**
40	Vert. Sync. Offset=xx lines, Sync Width=xx lines	44	01000100	68	**Verti sync. Offset=4 lines, Sync Width=4 lines**
41	Horz. Ver. Sync/Width (upper 2 bits)	00	00000000	0	
42	Hori. Image size (Lower 8 bits)	4B	01001011	75	**Hori image size= 331 mm**
43	Vert. Image size (Lower 8 bits)	CF	11001111	207	**Verti image size = 207mm**
44	Hori. Image size : Vert. Image size (Upper 4 bits)	10	00010000	16	
45		00	00000000	0	**Horizontal Border = 0**
46		00	00000000	0	**Vertical Border = 0**

47		18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	ASCII Data String:B154EW01
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		02	00000010	2	
5A	Detailed timing/monitor	00	00000000	0	ASCII Data String:B154EW01
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F		41	01000001	65	A
60		55	01010101	85	U
61		4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	Monitor Name: Color LCD
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	

70		00	00000000	0	
71		42	01000010	66	B
72		31	00110001	49	1
73		35	00110101	53	5
74		34	00110100	52	4
75		45	01000101	69	E
76		57	01010111	87	W
77		30	00110000	48	0
78		31	00110001	49	1
79		20	00100000	32	
7A		56	01010110	86	V
7B		39	00111001	57	9
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	CC	11001100	204	