




# Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications

(✓) Final Specifications

Module	15.6" (15.55) FHD 16:9 Color TFT-LCD with <i>LED Backlight</i> design
Model Name	B156HTN03.2 (H/W:0A)
Note (  )	LED Backlight with driving circuit design

<b>Customer</b>	<b>Date</b>
_____	_____
<b>Checked &amp; Approved by</b>	<b>Date</b>
_____	_____
Note: This Specification is subject to change without notice.	

<b>Approved by</b>	<b>Date</b>
<u>Buffy Chen</u>	<u>08/03/2013</u>
<b>Prepared by</b>	<b>Date</b>
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# Product Specification

AU OPTRONICS CORPORATION

## Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/09/18	All	Preliminary Edition for Customer		
0.2 2012/11/30	Page 23,25&27		Update Outline Dimension , Shipping Label & EDID	
0.3 2013/02/22	Page 6 & 27		Update Color / Chromaticity Coodinates & EDID	
1.0 2013/03/08	All		Final Edition for Customer	

## 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

## 2. General Description

B156HTN03.2 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 FHD (1920(H) x 1080(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B156HTN03.2 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

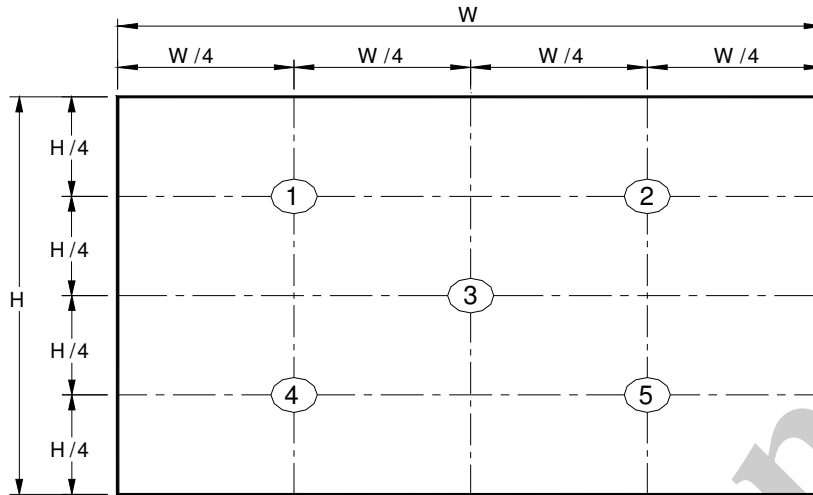
Items	Unit	Specifications			
Screen Diagonal	[mm]	15.6" (15.55)			
Active Area	[mm]	344.16 x 193.59			
Pixels H x V		1920 x 3(RGB) x 1080			
Pixel Pitch	[mm]	0.17925 x 0.17925			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance ( <b>I<sub>LED</sub>=21mA</b> ) <b>(Note: I<sub>LED</sub> is LED current)</b>	[cd/m <sup>2</sup> ]	300 Typ. (5 points average) 255 Min. (5 points average)			
Luminance Uniformity		1.25 Max. (5 points)			
Contrast Ratio		500 :1 Typ			
Response Time	[ms]	8 Typ / 16 Max.			
Nominal Input Voltage VDD	[Volt]	+3.3 Typ.			
Power Consumption	[Watt]	7.0 Max. (Include Logic and BLU Power)			
Weight	[Grams]	380 Max.			
Physical Size <b>Without inverter, bracket.</b>	[mm]		Min.	Typ.	Max.
		Length	359.0	359.5	360.0
		Width	223.3	223.8	224.3
		Thickness			3.2
Electrical Interface		2 channel LVDS			
Glass Thickness	[mm]	0.4			
Surface Treatment		Glare			
Support Color		262K colors ( RGB 6-bit )			
Temperature Range					
Operating	[°C]	0 to +50			
Storage (Non-Operating)	[°C]	-20 to +60			
RoHS Compliance		RoHS Compliance			

## 2.2 Optical Characteristics

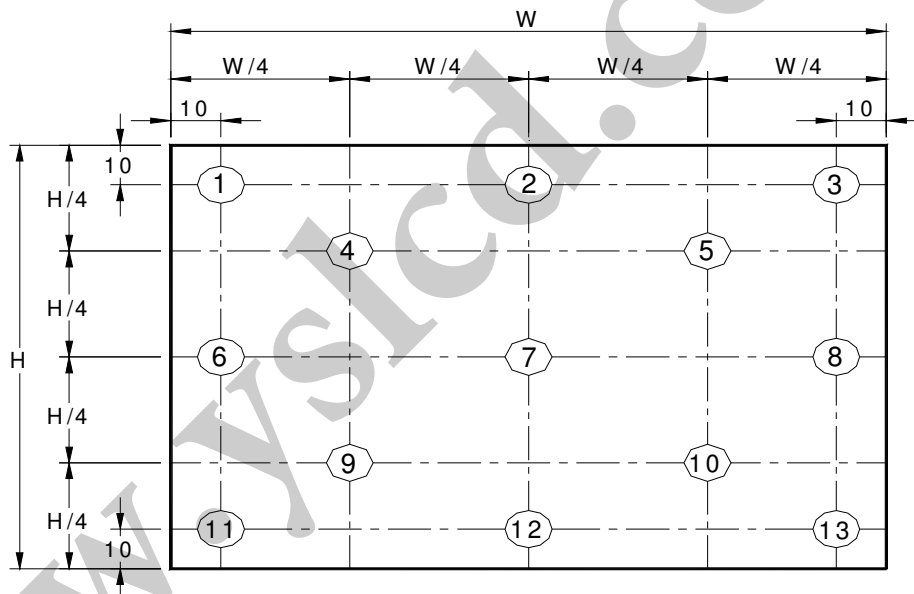
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance ILED=20mA		5 points average	255	300	-	cd/m <sup>2</sup>	1, 4, 5
Viewing Angle	$\theta_R$ $\theta_L$	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	degree	4, 9
	$\psi_H$ $\psi_L$	Vertical (Upper) CR = 10 (Lower)	10 30	15 35	- -		
Luminance Uniformity	$\delta_{5P}$	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	$\delta_{13P}$	13 Points	-	-	1.53		2, 3, 4
Contrast Ratio	CR		400	500	-		4, 6
Cross talk	%				4		4, 7
Response Time	$T_{RT}$	Rising + Falling	-	8	16	msec	4, 8
Color Chromaticity Coordinates	Red	Rx	0.590	0.620	0.650	CIE 1931	4
		Ry	0.320	0.350	0.380		
	Green	Gx	0.290	0.320	0.350		
		Gy	0.570	0.600	0.630		
	Blue	Bx	0.120	0.150	0.180		
		By	0.090	0.120	0.150		
	White	Wx	0.283	0.313	0.343		
		Wy	0.299	0.329	0.359		
NTSC	%		--	60			

**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance.

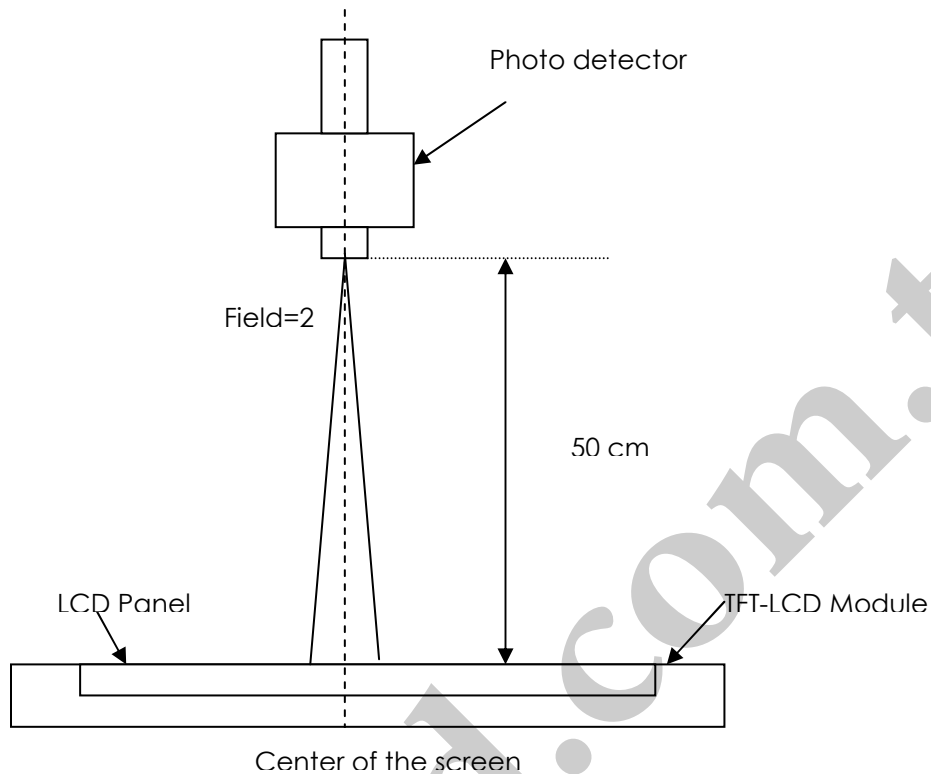
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4:** Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the

center of screen.



**Note 5 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ·  $Y_L = [L (1) + L (2) + L (3) + L (4) + L (5)] / 5$

$L (x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

**Note 7 :** Definition of Cross Talk (CT)

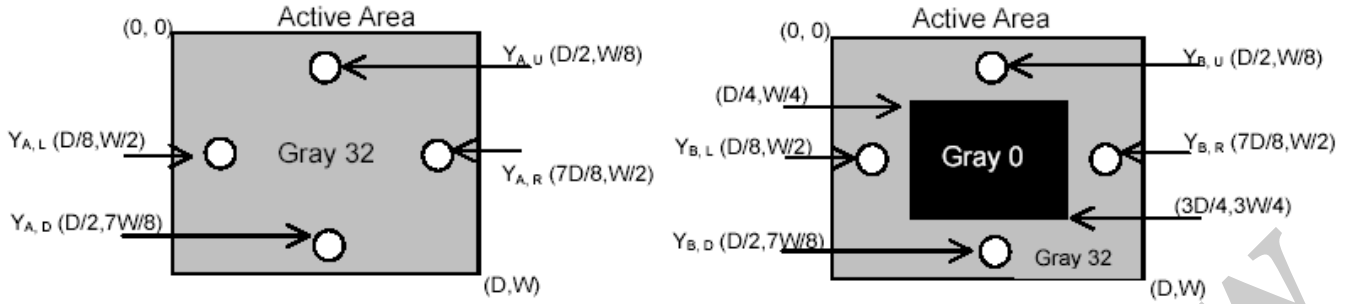
$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where

$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

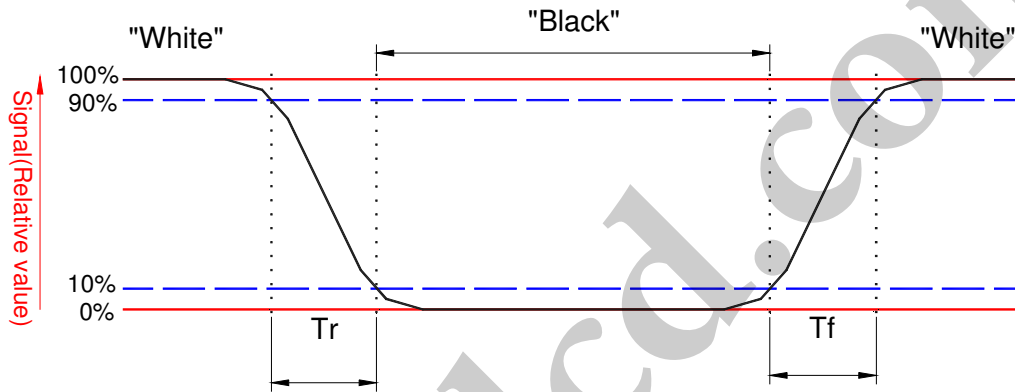
$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)





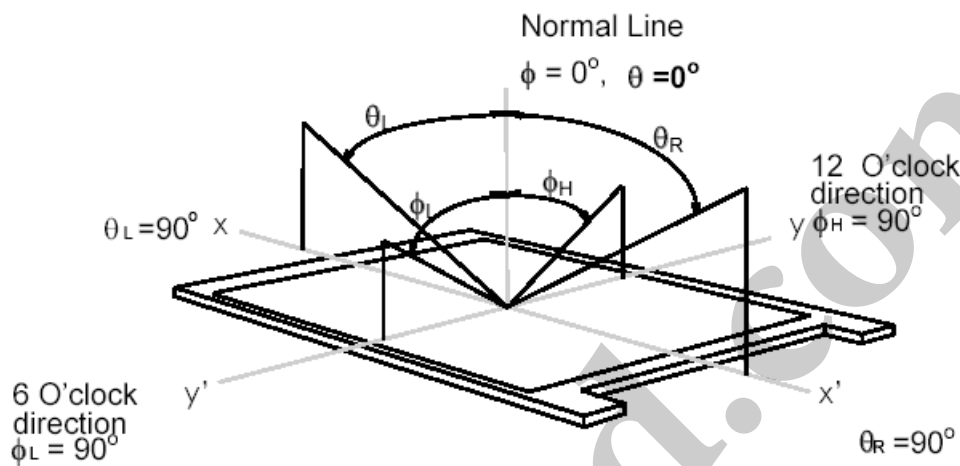
**Note 8 :** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



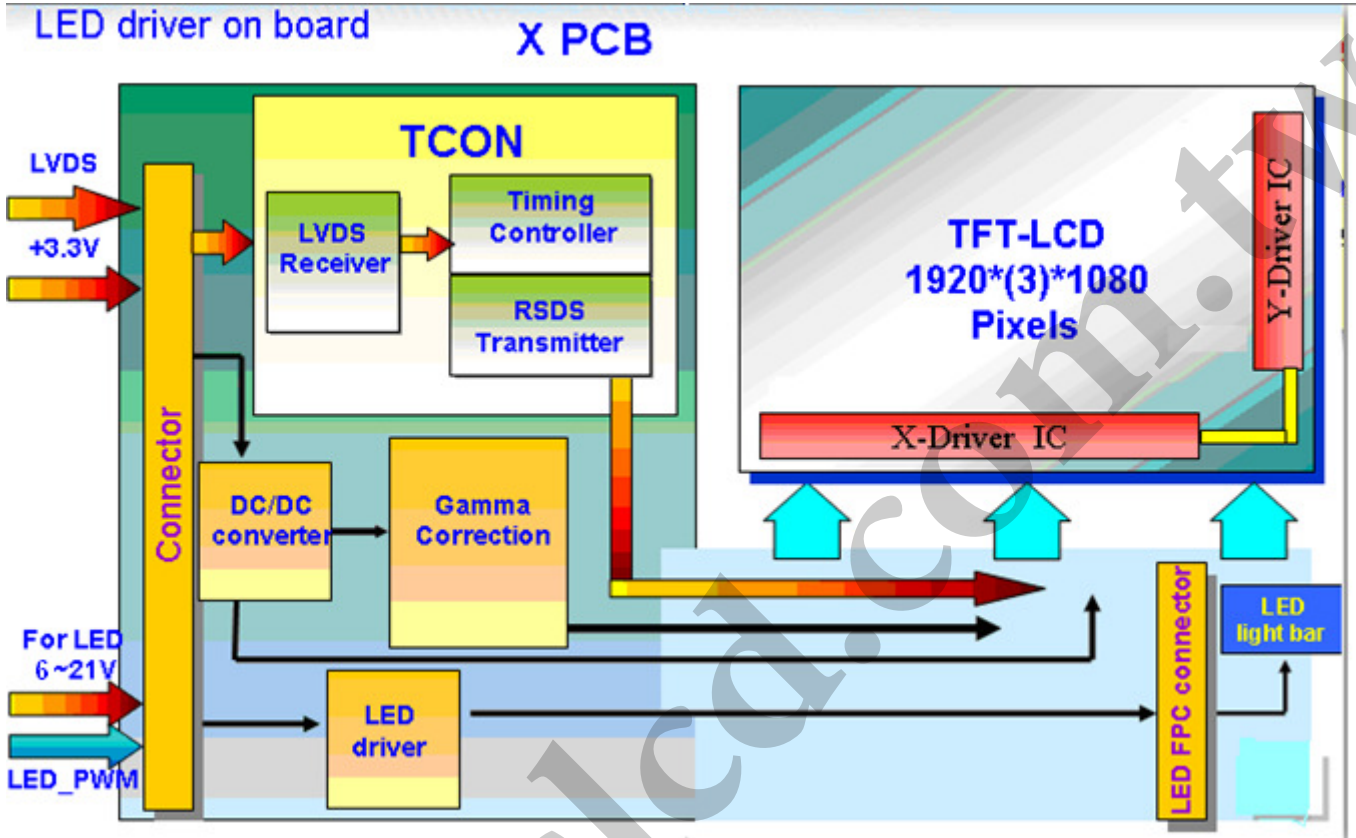
**Note 9 :** Definition of view angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° ( $\theta$ ) horizontal left and right and 90° ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 40 Pin.



## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Environment

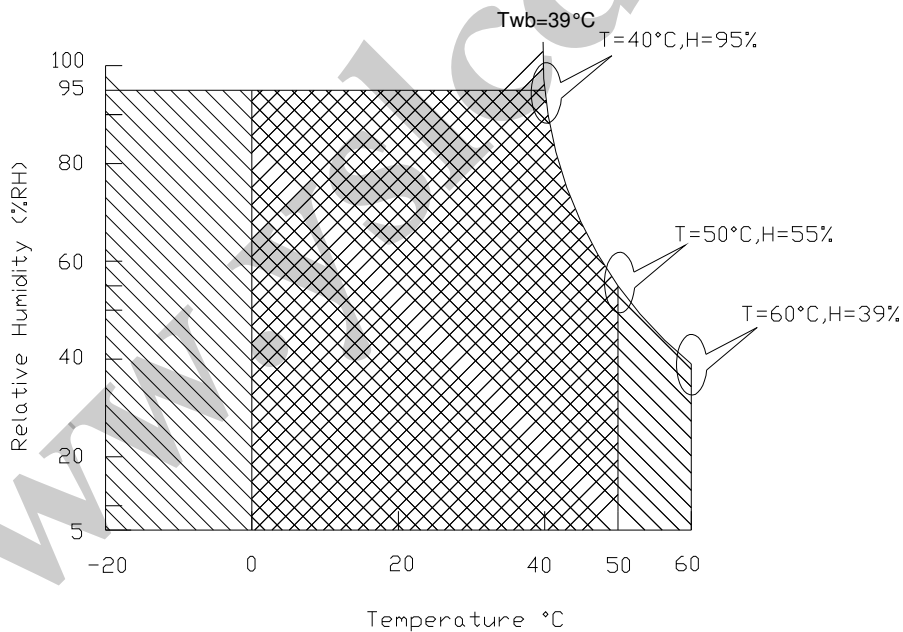
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	8	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C )

Note 2: Permanent damage to the device may occur if exceed maximum values



Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range

 + 

## 5. Electrical characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

Input power specifications are as follows;

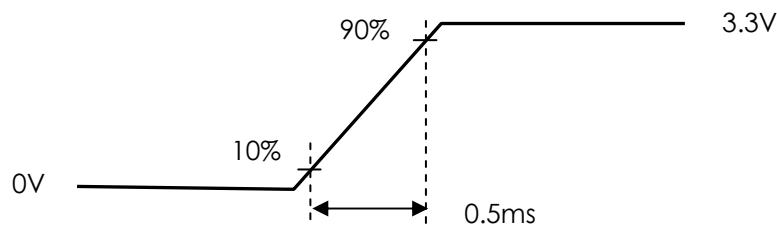
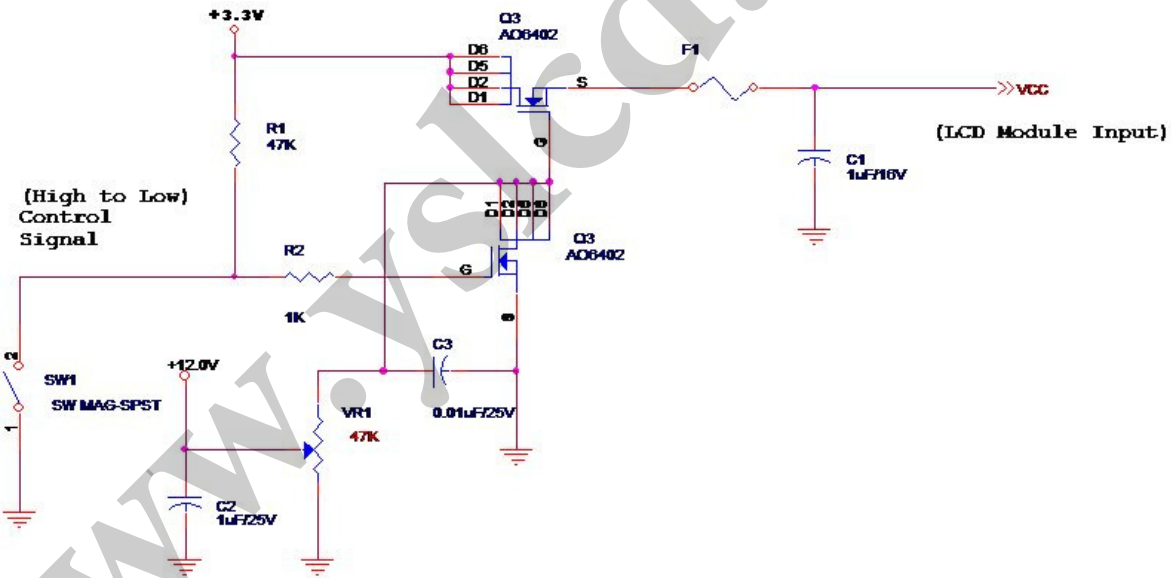
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	2.0	[Watt]	Note 1/2
IDD	IDD Current	-	-	606	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern, XP Desktop Pattern

Note 2 : Typical Measurement Condition: Mosaic Pattern, XP Desktop Pattern

Note 3 : Measure Condition



Vin rising time

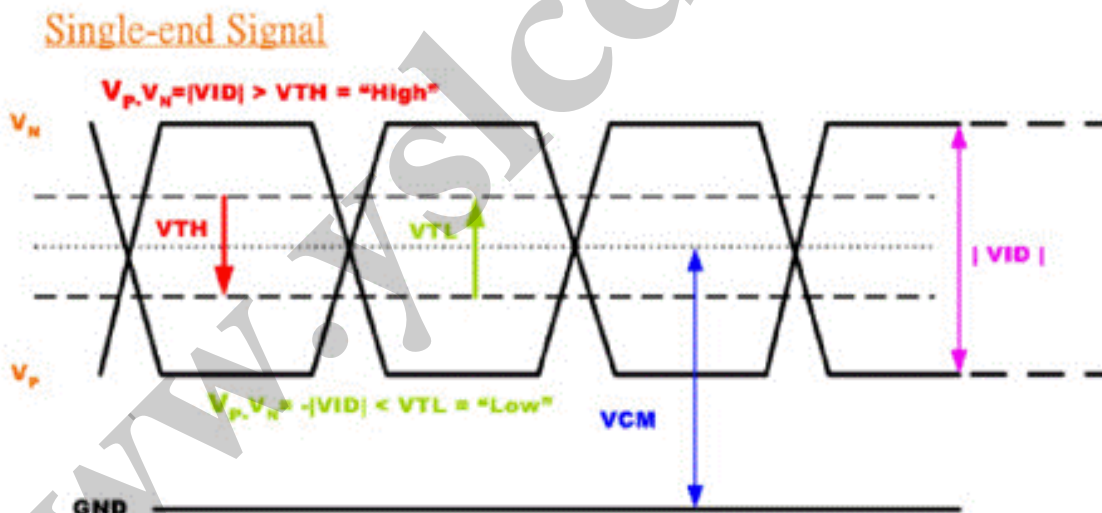
## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
$V_{TH}$	Differential Input High Threshold ( $V_{cm}=+1.2V$ )	-	100	[mV]
$V_{TL}$	Differential Input Low Threshold ( $V_{cm}=+1.2V$ )	-100	-	[mV]
$ V_{ID} $	Differential Input Voltage	100	600	[mV]
$V_{CM}$	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform





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## 5.2 Backlight Unit

### 5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	5.0	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25°C), Note 2 If=20 mA

**Note 1:** Calculator value for reference  $P_{LED} = V_F$  (Normal Distribution) \*  $I_F$  (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

### 5.2.2 Backlight input signal characteristics

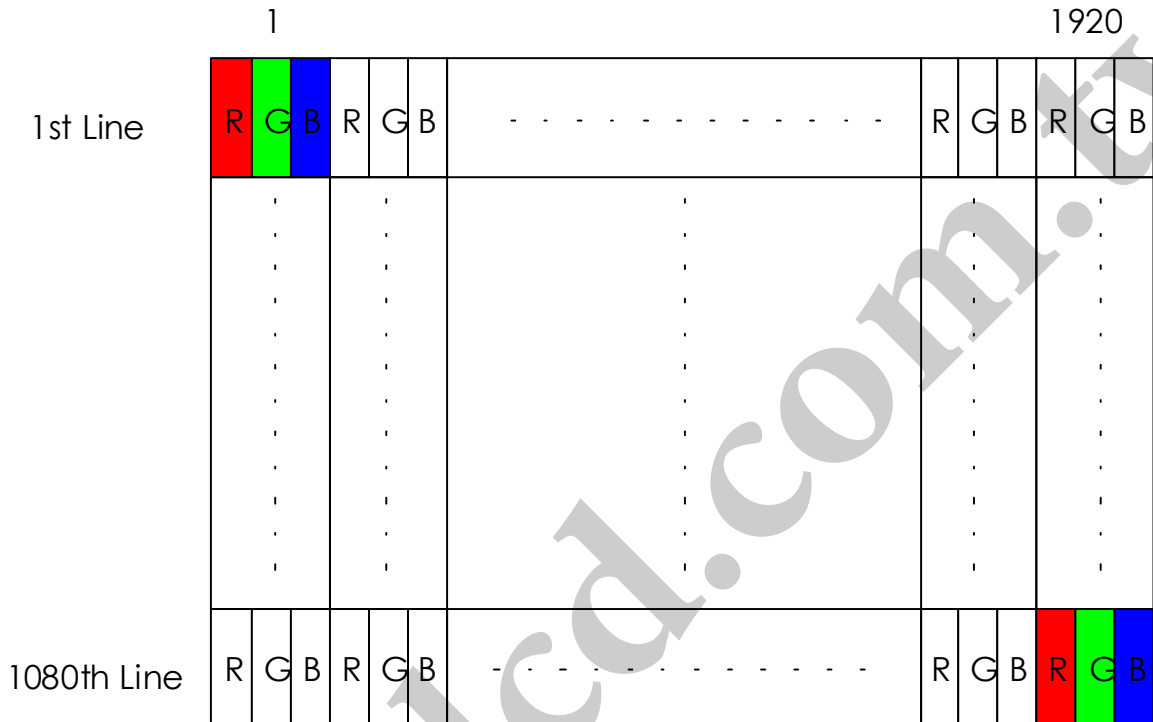
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

**Note 1 :** Recommend system pull up/down resistor no bigger than 10kohm

## 6. Signal Characteristic

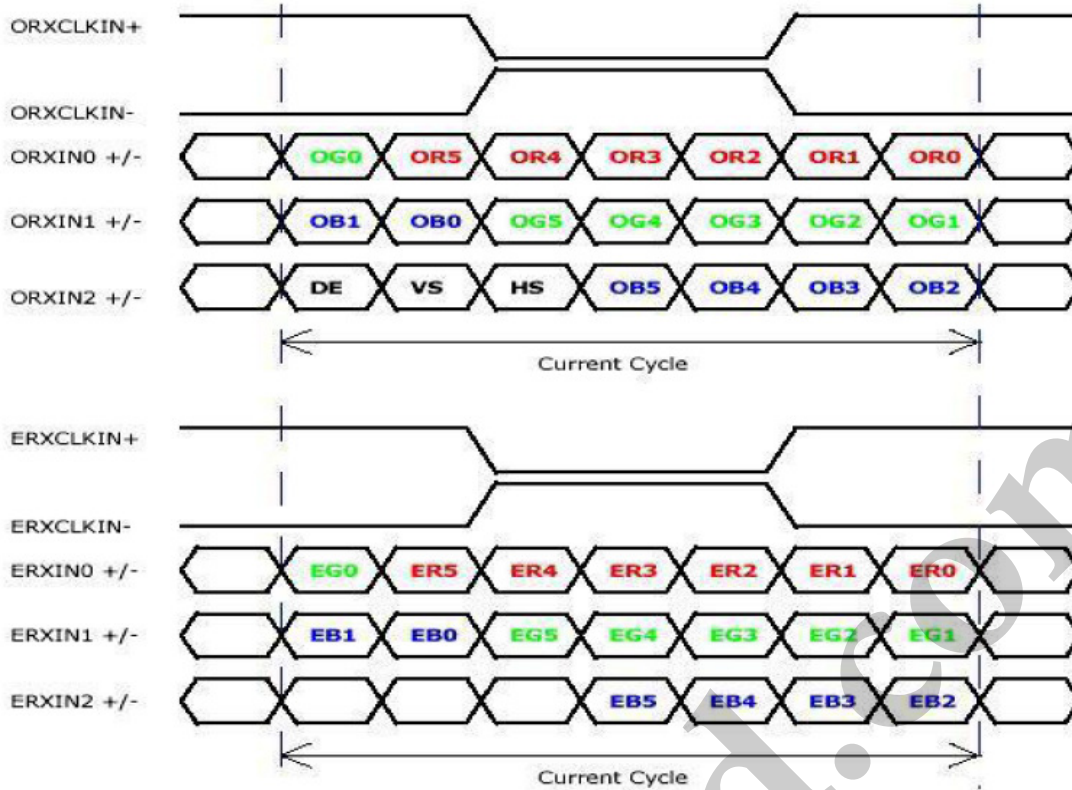
### 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.





## 6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN.
HS	Horizontal Sync	The signal is synchronized to RxCLKIN.

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

## 6.3 Integration Interface and Pin Assignment

### 6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

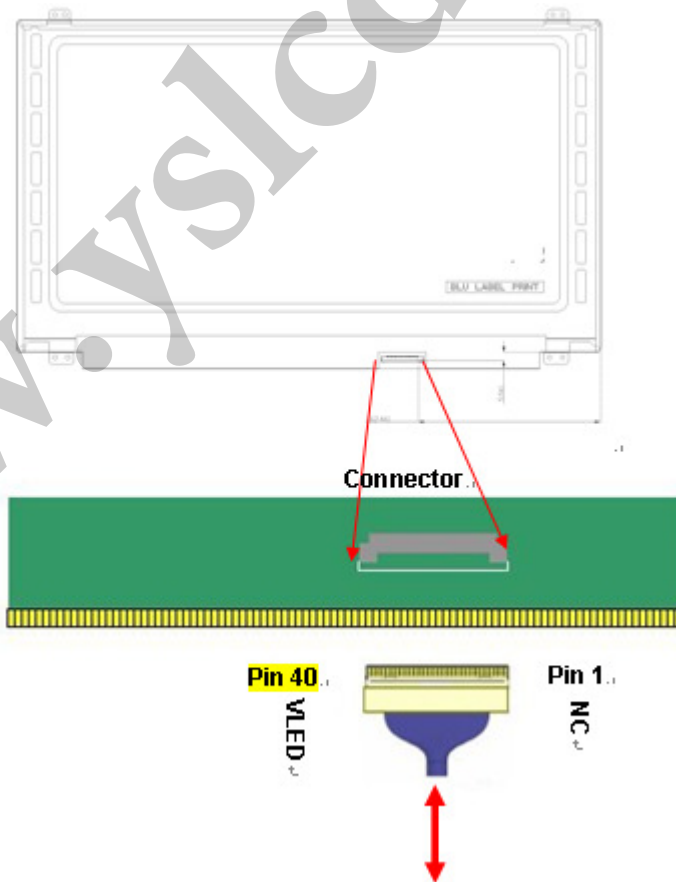
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-040E-12 or compatible
Mating Housing/Part Number	IPEX 20453-040T-11 or compatible

### 6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	NC	No Connection (Reserve)
2	VDD	Power Supply +3.3V
3	VDD	Power Supply +3.3V
4	VEDID	EDID +3.3V Power
5	BIST	Panel Self Test
6	CLK_EDID	EDID Clock Input
7	DAT_EDID	EDID Data Input
8	RxOIN0-	-LVDS Differential Data INPUT(Odd R0-R5,G0)
9	RxOIN0+	+LVDS Differential Data INPUT(Odd R0-R5,G0)
10	VSS	Ground
11	RxOIN1-	-LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
12	RxOIN1+	+LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
13	VSS	Ground
14	RxOIN2-	-LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
15	RxOIN2+	+LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
16	VSS	Ground
17	RxOCKIN-	-LVDS Odd Differential Clock INPUT
18	RxOCKIN+	+LVDS Odd Differential Clock INPUT
19	CM_EN	CM_EN
20	RxEIN0-	-LVDS Differential Data INPUT(Even R0-R5,G0)
21	RxEIN0+	+LVDS Differential Data INPUT(Even R0-R5,G0)
22	VSS	Ground
23	RxEIN1-	-LVDS Differential Data INPUT(Even G1-G5,B0-B1)

24	RxEIN1+	+LVDS Differential Data INPUT(Even G1-G5,B0-B1)
25	VSS	Ground
26	RxEIN2-	-LVDS Differential Data INPUT(Even B2-B5,HS,VS,DE)
27	RxEIN2+	+LVDS Differential Data INPUT(Even B2-B5,HS,VS,DE)
28	VSS	Ground
29	RxECKIN-	-LVDS Even Differential Clock INPUT
30	RxECKIN+	+LVDS Even Differential Clock INPUT
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection
35	S_PWMIN	System PWM Logic Input level
36	LED_EN	LED enable input level
37	DCR_EN	DCR_EN
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply



Note1: Input signals shall be low or High-impedance state when VDD is off.

## 6.4 Interface Timing

### 6.4.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

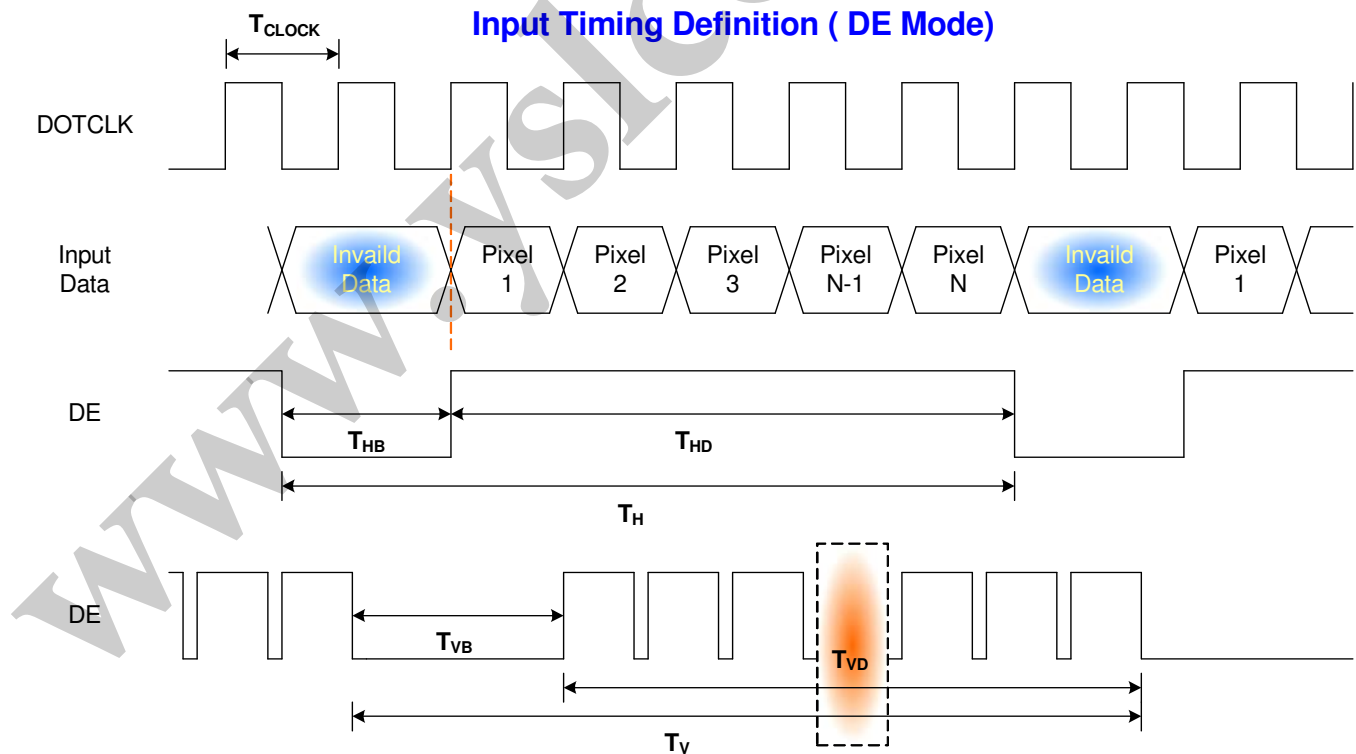
Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	40	60	-	Hz	
Clock frequency	$1/T_{\text{Clock}}$	66.6	72	80	MHz	
Vertical Section	Period	$T_V$	1100	1130	1080+A	$T_{\text{Line}}$
	Active	$T_{VD}$	1080			
	Blanking	$T_{VB}$	20	50	A	
Horizontal Section	Period	$T_H$	1010	1050	960+B	$T_{\text{Clock}}$
	Active	$T_{HD}$	960			
	Blanking	$T_{HB}$	50	90	B	

**Note 1 :** The above is as optimized setting

**Note 2 :** DE mode only

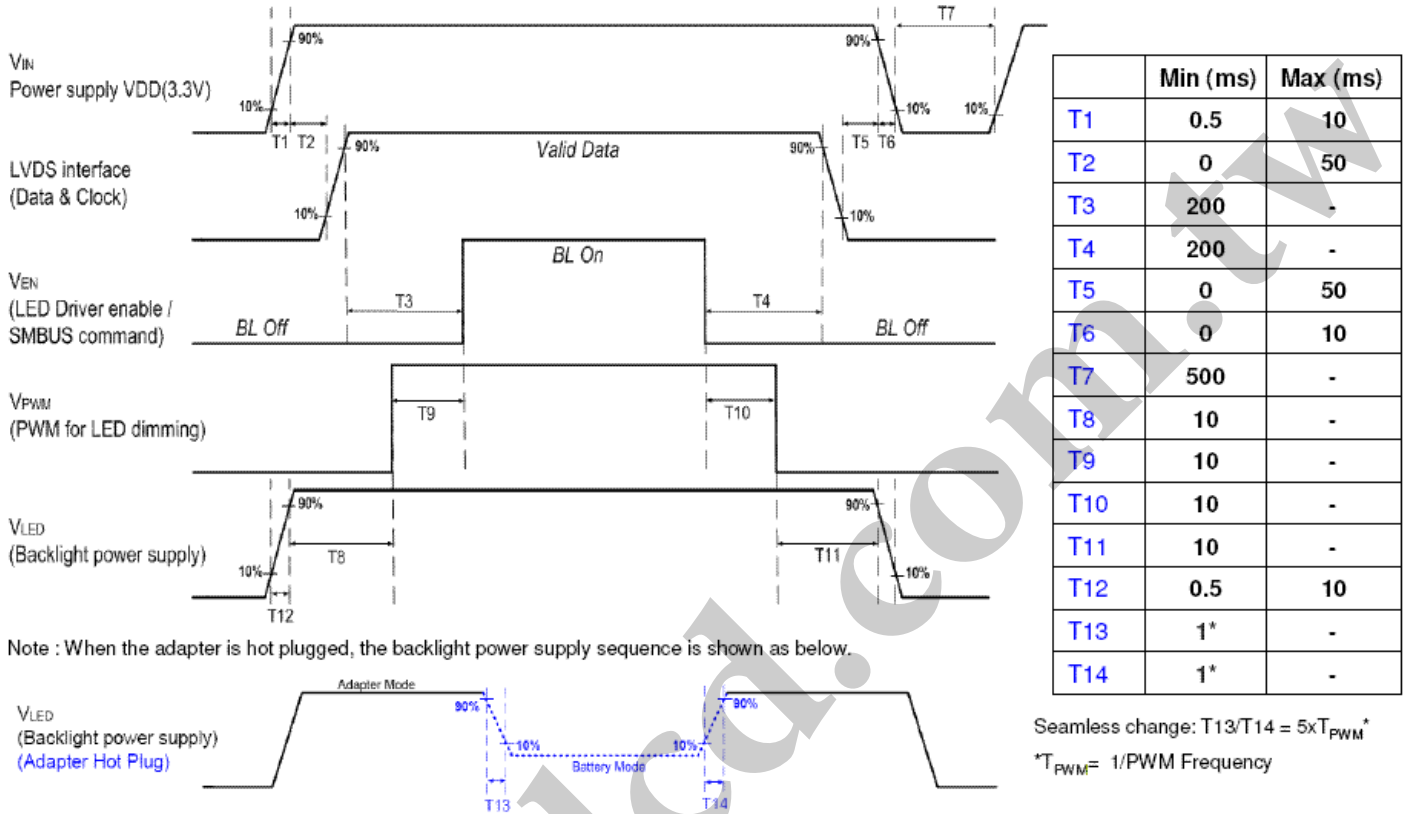
**Note 3 :** The maximum clock frequency =  $(960+B) \cdot (1080+A) \cdot 60 < 80\text{MHz}$

### 6.4.2 Timing diagram



## 6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



**Note 1 :** If  $T3 < 200ms$ , the display garbage may occur. ( $T3 > 200ms$  is recommended)

**Note 2 :** If  $T1$  or  $T12 < 0.5ms$ , the inrush current may cause the damage of fuse. If  $T1$  or  $T12 < 0.5ms$ , the inrush current  $I^2t$  is under typical melt of fuse Spec, there is no mentioned problem.

## 7. Vibration and Shock Test

### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test Spec:

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3. Reliability

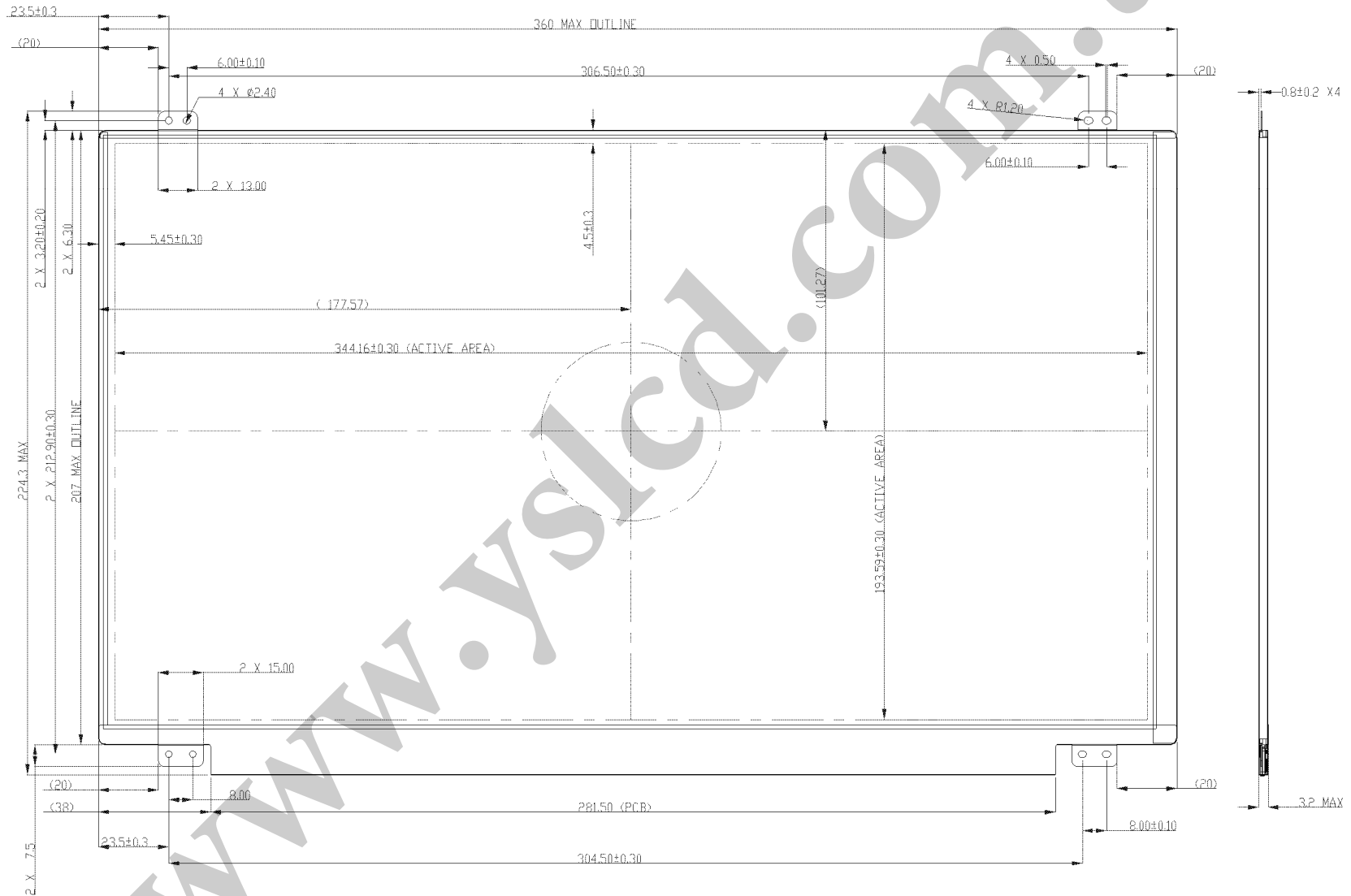
Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C , 90%RH, 300h	
High Temperature Operation	Ta= 50°C , Dry, 300h	
Low Temperature Operation	Ta= 0°C , 300h	
High Temperature Storage	Ta= 60°C , 35%RH, 300h	
Low Temperature Storage	Ta= -20°C , 50%RH, 300h	
Thermal Shock Test	Ta=-20°C to 60°C , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

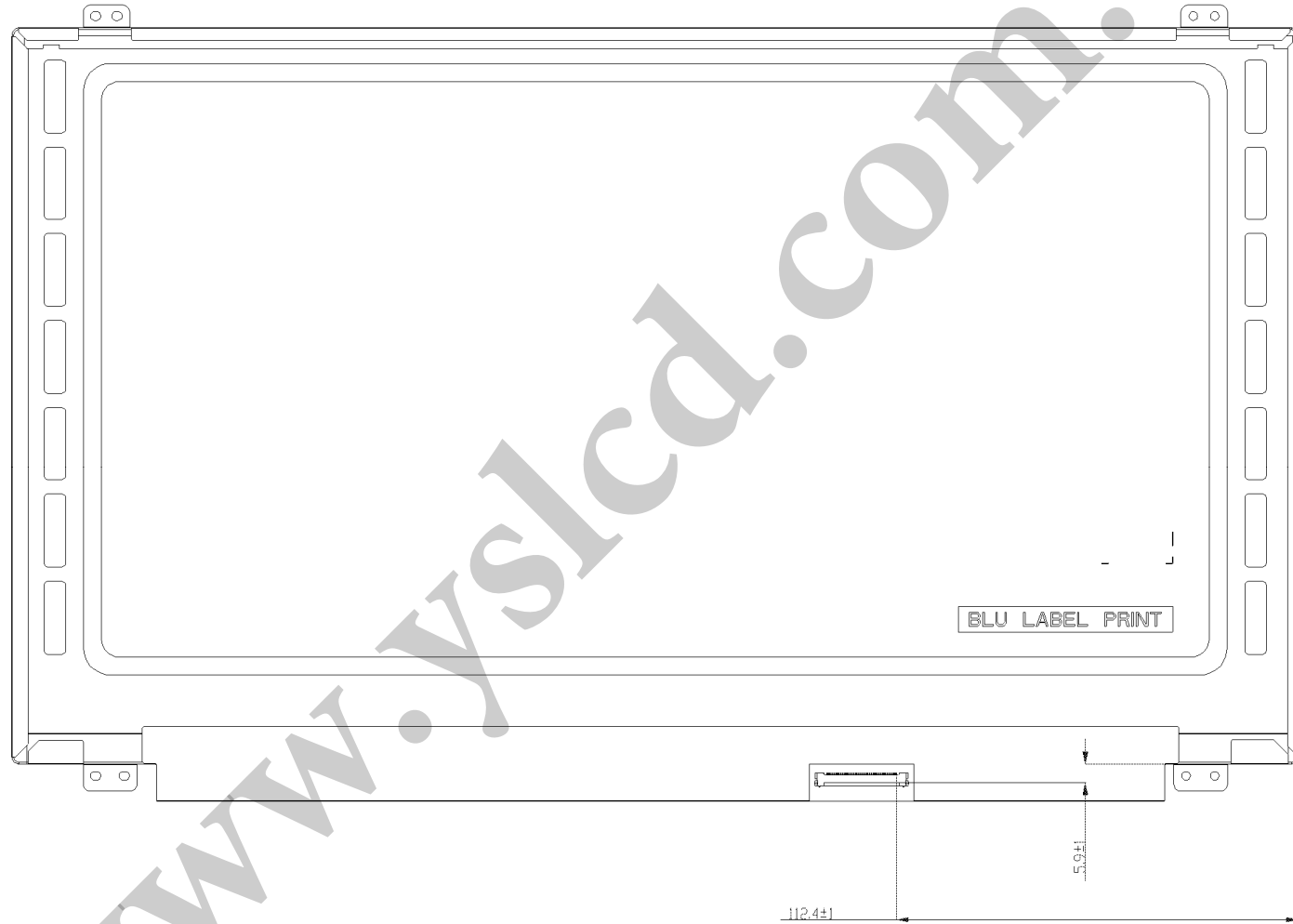
**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

## 8. Mechanical Characteristics

### 8.1 LCM Outline Dimension





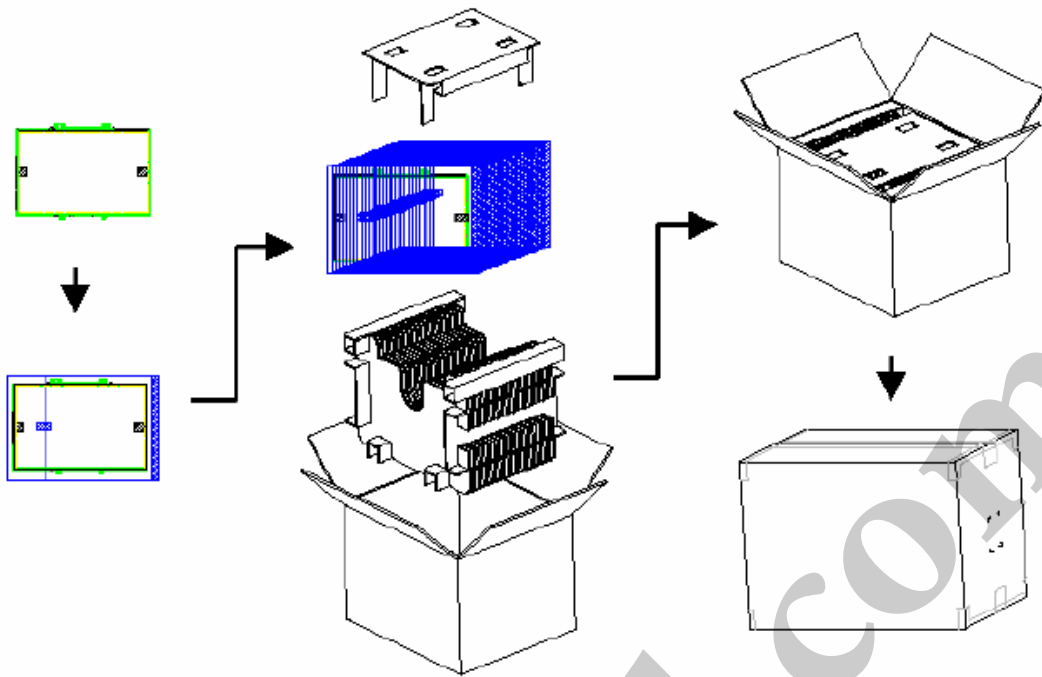


## 9. Shipping and Package

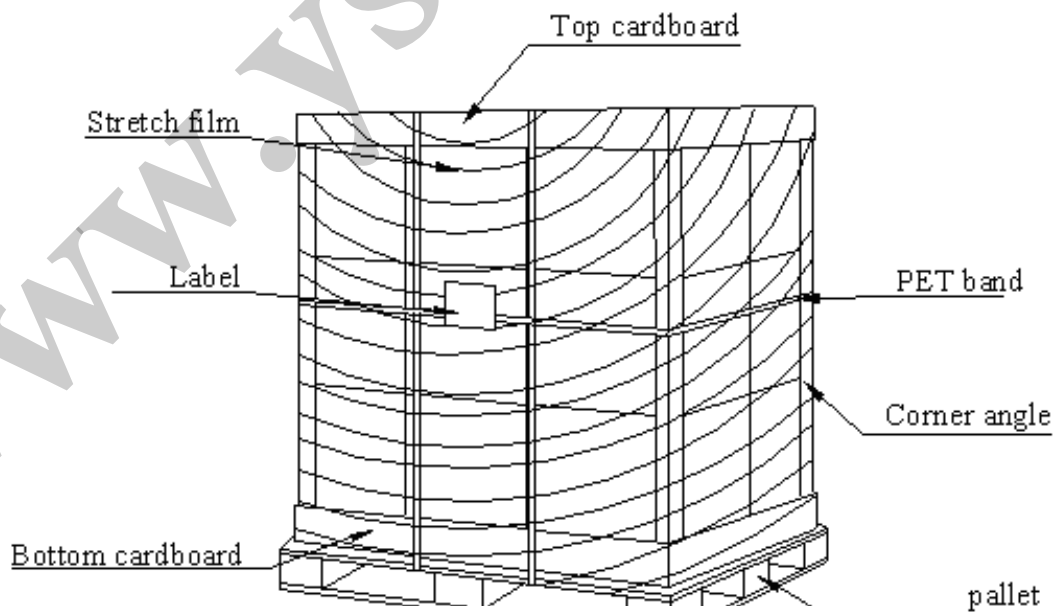
### 9.1 Shipping Label Format

 XXXXXXXXXXXXXXXX-XXXXXX	Manufactured MM/WW Model No: B156HTN03.2 AU Optronics MADE IN CHINA (S01) H/W: 0A F/W:1	c   RoHS 
 CT : CDGYF 01XXXXXXXX		

## 9.2 Carton package



## 9.3 Shipping package of palletizing sequence





# Product Specification

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## 10. Appendix: EDID description

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	0000000 0	0	
01		FF	1111111 1	255	
02		FF	1111111 1	255	
03		FF	1111111 1	255	
04		FF	1111111 1	255	
05		FF	1111111 1	255	
06		FF	1111111 1	255	
07		00	0000000 0	0	
08	EISA Manuf. Code LSB	06	0000011 0	6	
09	Compressed ASCII	AF	1010111 1	175	
0A	Product Code	ED	1110110 1	237	
0B	hex, LSB first	32	0011001 0	50	
0C	32-bit ser #	00	0000000 0	0	
0D		00	0000000 0	0	
0E		00	0000000 0	0	
0F		00	0000000 0	0	
10	Week of manufacture	00	0000000 0	0	
11	Year of manufacture	16	0001011 0	22	
12	EDID Structure Ver.	01	0000000 1	1	
13	EDID revision #	04	0000010 0	4	
14	<b>Video input def.</b> ( <i>digital I/P, non-TMDS, CRGB</i> )	90	1001000 0	144	
15	<b>Max H image size</b> ( <i>rounded to cm</i> )	22	0010001 0	34	
16	<b>Max V image size</b> ( <i>rounded to cm</i> )	13	0001001 1	19	
17	<b>Display Gamma</b> ( <i>=(gamma*100)-100</i> )	78	0111100 0	120	
18	<b>Feature support</b> ( <i>no DPMS, Active OFF, RGB, tmg Blk#1</i> )	02	0000001 0	2	
19	Red/green low bits ( <b>Lower 2:2:2:2 bits</b> )	D1	1101000 1	209	
1A	Blue/white low bits ( <b>Lower 2:2:2:2 bits</b> )	15	0001010 1	21	
1B	Red x ( <b>Upper 8 bits</b> )	9E	1001111 0	158	
1C	Red y/ highER 8 bits	59	0101100 1	89	
1D	Green x	53	0101001 1	83	
1E	Green y	9B	1001101 1	155	
1F	Blue x	27	0010011 1	39	



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20	Blue y	1E	0001111 0	30	
21	White x	50	0101000 0	80	
22	White y	54	0101010 0	84	
23	Established timing 1	00	0000000 0	0	
24	Established timing 2	00	0000000 0	0	
25	Established timing 3	00	0000000 0	0	
26	Standard timing #1	01	0000000 1	1	
27		01	0000000 1	1	
28	Standard timing #2	01	0000000 1	1	
29		01	0000000 1	1	
2A	Standard timing #3	01	0000000 1	1	
2B		01	0000000 1	1	
2C	Standard timing #4	01	0000000 1	1	
2D		01	0000000 1	1	
2E	Standard timing #5	01	0000000 1	1	
2F		01	0000000 1	1	
30	Standard timing #6	01	0000000 1	1	
31		01	0000000 1	1	
32	Standard timing #7	01	0000000 1	1	
33		01	0000000 1	1	
34	Standard timing #8	01	0000000 1	1	
35		01	0000000 1	1	
36	Pixel Clock/10000 LSB	B0	1011000 0	176	
37	Pixel Clock/10000 USB	36	0011011 0	54	
38	Horz active <b>Lower 8bits</b>	80	1000000 0	128	
39	Horz blanking <b>Lower 8bits</b>	B4	1011010 0	180	
3A	HorzAct:HorzBlnk <b>Upper 4:4 bits</b>	70	0111000 0	112	
3B	Vertical Active <b>Lower 8bits</b>	38	0011100 0	56	
3C	Vertical Blanking <b>Lower 8bits</b>	1E	0001111 0	30	
3D	Vert Act : Vertical Blanking <b>(upper 4:4 bit)</b>	40	0100000 0	64	
3E	HorzSync. Offset	30	0011000 0	48	
3F	HorzSync.Width	64	0110010 0	100	
40	VertSync.Offset : VertSync.Width	31	0011000 1	49	
41	Horz&Vert Sync Offset/Width <b>Upper 2bits</b>	00	0000000 0	0	
42	Horizontal Image Size <b>Lower 8bits</b>	58	0101100 0	88	



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43	Vertical Image Size <b>Lower 8bits</b>	C1	1100000 1	193	
44	Horizontal & Vertical Image Size <b>(upper 4:4 bits)</b>	10	0001000 0	16	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	0000000 0	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	0000000 0	0	
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	0001100 0	24	
48	Pixel Clock/10,000 (LSB)	75	0111010 1	117	40Hz frame rate
49	Pixel Clock/10,000 (MSB)	24	0010010 0	36	
4A	Horizontal Addressable Pixels, lower 8 bits	80	1000000 0	128	
4B	Horizontal Blanking Pixels, lower 8 bits	B4	1011010 0	180	
4C	H Pixels, upper nibble : H Blanking, upper nibble	70	0111000 0	112	
4D	Vertical Addressable Lines, lower 8 bits	38	0011100 0	56	
4E	Vertical Blanking Lines, lower 8 bits	1E	0001111 0	30	
4F	V lines, upper nibble : V blanking, upper nibble	40	0100000 0	64	
50	Horizontal Front Porch, lower 8 bits	30	0011000 0	48	
51	Horizontal Sync Pulse, lower 8 bits	64	0110010 0	100	
52	V Front Porch, lower nibble : V Sync Pulse, lower nibble	31	0011000 1	49	
53	VFP, 2 bits: VSP 2 bits: HFP 2 bits: HFP 2 bits	00	0000000 0	0	
54	Horizontal Image Size in mm, lower 8 bits	58	0101100 0	88	
55	Vertical Image Size in mm, lower 8 bits	C1	1100000 1	193	
56	H Image Size, upper nibble : V Image Size, upper nibble	10	0001000 0	16	
57	Horizontal Border	00	0000000 0	0	
58	Vertical Border	00	0000000 0	0	
59	Bit Encode Sync Information	18	0001100 0	24	
5A	DC	00	0000000 0	0	nVDPS Reserved 00
5B	HTOTAL	00	0000000 0	0	
5C	HA	00	0000000 0	0	
5D	HBL	00	0000000 0	0	
5E	HFP	00	0000000 0	0	
5F	HFPe	00	0000000 0	0	
60	HBP	00	0000000 0	0	
61	HB	00	0000000 0	0	
62	HSO	00	0000000 0	0	
63	HS	00	0000000 0	0	
64	VTOTAL	00	0000000 0	0	
	VA				



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			0		
66	VBL	00	0000000 0	0	
67	VFP	00	0000000 0	0	
68	VBP	00	0000000 0	0	
69	VB	00	0000000 0	0	
6A	VSO	00	0000000 0	0	
6B	VS	00	0000000 0	0	
6C	Detail Timing Description #4	00	0000000 0	0	
6D	Flag	00	0000000 0	0	
6E	Reserved	00	0000000 0	0	
6F	For Brightness Table and Power Consumption	02	0000001 0	2	
70	Flag	00	0000000 0	0	Header
71	PWM % [7:0] @ Step 0	0C	0000110 0	12	
72	PWM % [7:0] @ Step 5	3D	0011110 1	61	
73	PWM % [7:0] @ Step 10	FF	1111111 1	255	
74	Nits [7:0] @ Step 0	0C	0000110 0	12	
75	Nits [7:0] @ Step 5	3C	0011110 0	60	
76	Nits [7:0] @ Step 10	7D	0111110 1	125	Brightness Table
77	Panel Electronics Power @ 32x32 Chess Pattern =	1B	0001101 1	27	
78	Backlight Power @ 60 nits =	0D	0000110 1	13	
79	Backlight Power @ Step 10 =	1C	0001110 0	28	
7A	Nits @ 100% PWM Duty =	7D	0111110 1	125	Power Consumption
7B	Flag	20	0010000 0	32	
7C	Flag	20	0010000 0	32	
7D	Flag	20	0010000 0	32	
7E	Extension Flag	00	0000000 0	0	
7F	Checksum	E5	1110010 1	229	