Ver 1.1

12-Bit 11-Channel Serial Analog to Digital Converter

Datasheet

Part Number：B2543ARH

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- Sample rate: 66ksps
- Linearity Error: ±1.5 LSB Max
- End-of-Conversion Output is EOC
- Unipolar or Bipolar Output Operation
- Programmable MSB or LSB First
- Programmable Output Data Length
- Total Ionizing Dose ≥ 60 Krad(Si)
- The Single Event Latch-up threshold≥75MeV•cm^2/mg

2. Description

The B2543ARH is a 12-bit switched capacitor, successive-approximation, radiation harden, analog to digital converters. The device allows high-speed data transfers from the host processor, and can get high level resolution. The transfer mode is serial input, which can reduce the I/O interface quantity of the processor 51.

3. Functional block diagram

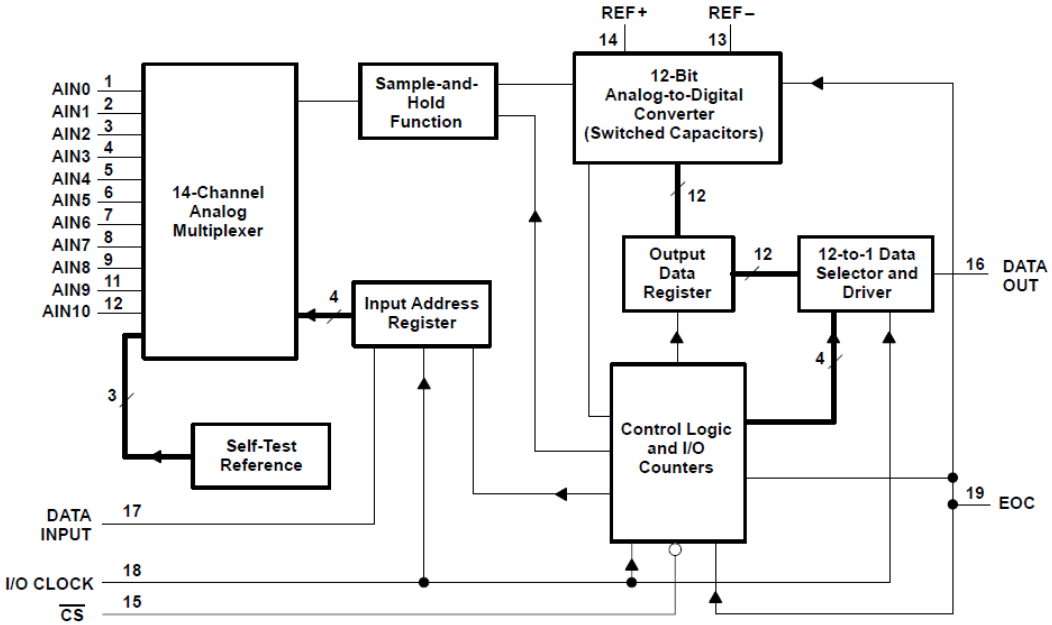


Figure 3-1. Functional block diagram

4. Pin configuration

The pins description of device are shown in figure 4-1.

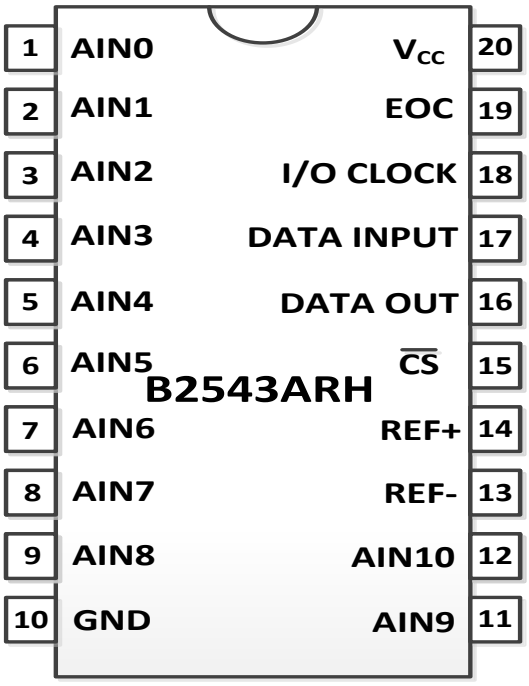


Figure 4-1. Pin description

Table 4-1. The pin configuration

No	name	I/O	description
1-9，11，12	AIN0-AIN10	I	Analog input. These 11 analog-signal inputs are internally multiplexed. The driving source impedance should be less than or equal to 50Ω for 4.1MHz I/O CLOCK operation and be capable of slewing the analog input voltage into a capacitance of 60 pF.
15	$\overline{CS}$	I	Chip select. A high to low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, DATA INPUT, and I/O CLOCK. A low to high transition disables DATA INPUT and I/O CLOCK within a setup time.
17	DATAINPUT	I	Serial data input. A 4-bit serial address selects the desired analog input
16	DATA OUT	O	The 3 state serial output for the A/D conversion result. DATA OUT is in the high impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low.
19	EOC	O	End of conversion. EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and the data is ready for transfer.
10	GND		Ground. GND is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND
18	I/O CLOCK	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of the I/O CLOCK. 3. It shifts the 11 remaining bits of the previous conversion data out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. It transfers control of the conversion to the internal state controller on the falling edge of the last I/O CLOCK
14	REF+	I	Positive reference voltage. The upper reference voltage value (nominally VCC) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the voltage applied to the REF– terminal
13	REF-	I	Negative reference voltage. The lower reference voltage value(nominally ground) is applied to REF–
20	Vcc		Positive supply voltage

5. Pin definition

Table 5-1. The pin configuration

Pin NO.	Symbol	IO	Function description	Pin NO.	Symbol	IO	Function description
1	AIN0	I	Analog input	11	AIN9	I	Analog input
2	AIN1	I	Analog input	12	AIN10	I	Analog input
3	AIN2	I	Analog input	13	REF-	I	Negative reference voltage.
4	AIN3	I	Analog input	14	REF-	I	Positive reference voltage
5	AIN4	I	Analog input	15	$\overline{CS}$	I	chip select
6	AIN5	I	Analog input	16	DATA OUT	O	The 3-state serial output
7	AIN6	I	Analog input	17	DATAINPUT	I	Serial-data input. A 4-bit serial address selects the desired analog input
8	AIN7	I	Analog input	18	I/O CLOCK	I	Input/ Output Clock
9	AIN8	I	Analog input	19	EOC	O	End of conversion
10	GND	G	GND	20	V_{CC}	P	Power source

6. Device description

6.1 Function description

The chip operation begin from writing 8 bit control code to the control register, with the 8,12,16 I/O clock. The I/O clock length is defined by 2bits. At the last clock cycle fall edge, the A/D convert start. Then with the 8,12,16 I/O clock cycle, the data can be read from DATAOUT pin. The control code is defined as:

Table 6-1. Control Code Define

Function select	**Input data byte**							
	Address bits				**L1**	**L0**	**LSBF**	**BIP**
	D7(MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0(LSB)**
Select input channel								
AIN0	0	0	0	0				
AIN1	0	0	0	1				

AIN2	0	0	1	0				
AIN3	0	0	1	1				
AIN4	0	1	0	0				
AIN5	0	1	0	1				
AIN6	0	1	1	0				
AIN7	0	1	1	1				
AIN8	1	0	0	0				
AIN9	1	0	0	1				
AIN10	1	0	1	0				
AIN11	1	0	1	1				
select test voltage								
（Vref+-Vref-）/2	1	0	1	1				
Vref-	1	1	0	0				
Vref+	1	1	0	1				
Software power down	1	1	1	0				
Output data length								
8 bits	—	—	—	—	0	1		
12 bits	—	—	—	—	xt	0		
16 bits	—	—	—	—	1	1		
Output data format								
MSB First	—	—	—	—	—	—	0	
LSB First	—	—	—	—	—	—	1	
Unipolar（binary）	—	—	—	—	—	—	—	0
Bipolar	—	—	—	—	—	—	—	1

The four MSBs (D7 – D4) of the data register address one of the 11 input channels. When it's 1100-1110,a reference test voltage is selected, When it's 1111,the power down mode is selected, and the AD converter's current is only 25uA.

The next two bits (D3 and D2) of the data register select the output data length. With bits D3 and D2 set to 01, the 8-bit data-length mode is selected, With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, With bits D3 and D2 set to X0, the 12-bit data-length mode is selected, X can be set to 0 or1.

D1 in the input data register controls the direction of the output binary data transfer. When D1 is reset to 0, the conversion result is shifted out MSB first. When set to 1, the data is shifted out LSB first.

D0 (BIP) in the input data register controls the binary data format used to represent the conversion result. When D0 is cleared to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to Vref– is a code of all zeros (000 . . . 0), the conversion result of

an input voltage equal to Vref+ is a code of all ones (111 . . . 1).

When D0 is set to 1, the conversion result is represented as bipolar (signed binary) data. When input voltage is higher than (Vref+ + Vref–) /2, the first bit of result is 0. When input voltage is lower than (Vref+ + Vref–) /2, the first bit of result is 1. And conversion of an input voltage equal to Vref+ is a code of a zero followed by all ones (011 . . . 1), conversion of an input voltage equal to Vref– is a code of a one followed by zeros (100 . . . 0), and the conversion of (Vref+ + Vref–) /2 is a code of all zeros (000 . . . 0).

There are four transfer type can achieve the all 12 bit resolution, every conversion and every data transfer can use the 12 or 16 IO clock cycle.

The chip select pulse $\overline{CS}$ comes before every conversion. Or the chip select pulse $\overline{CS}$ change just one time before the conversion sequence, then the chip select $\overline{CS}$ hold on 0, until to the sequence completed.

The operation sequence figures is shown in Figure 6-1 to Figure 6-6.

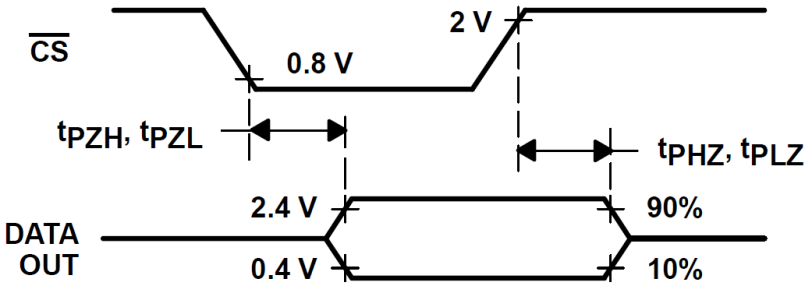


Figure 6-1. $\overline{CS}$ and DATA OUT Waveforms

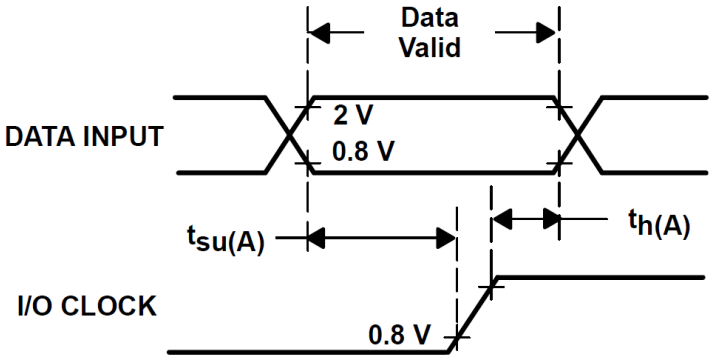


Figure 6-2. DATA INPUT and I/O CLOCK Voltage Waveforms

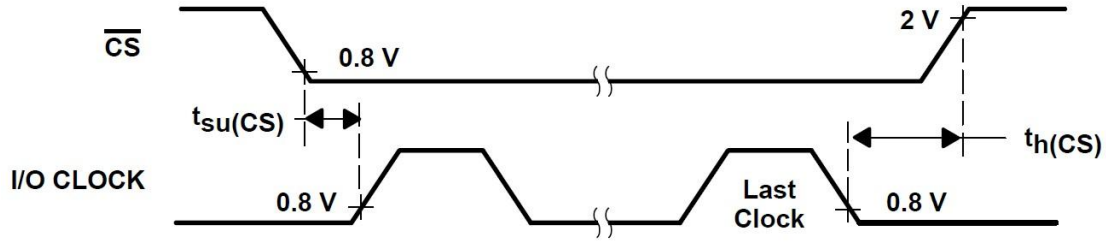


Figure 6-3. CS and I/O CLOCK Voltage Waveforms

Note: To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

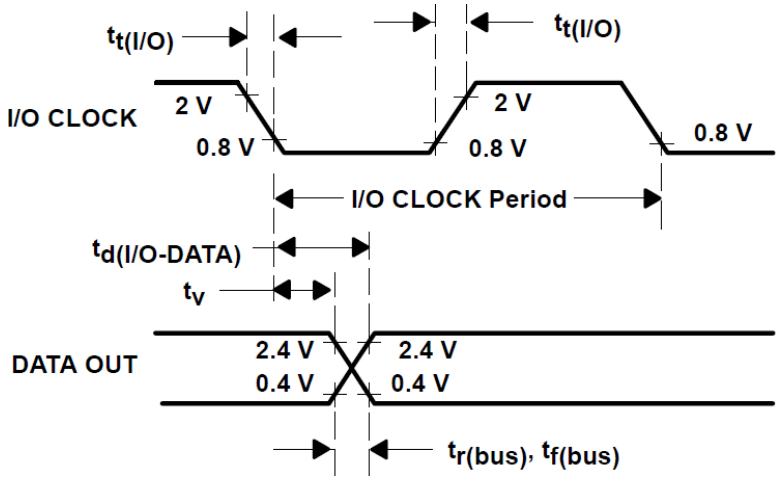


Figure 6-4. I/O CLOCK and DATA OUT Voltage Waveforms

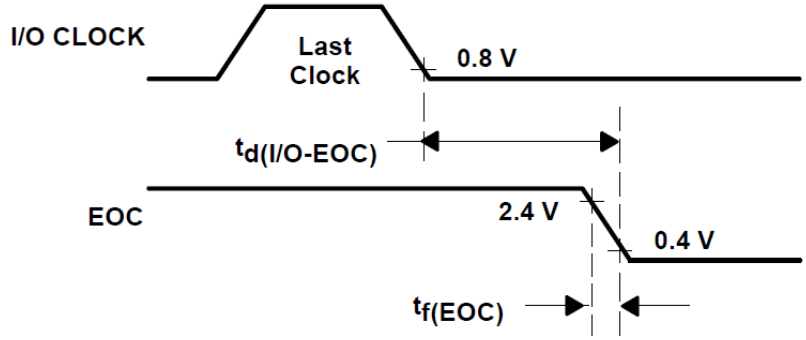


Figure 6-5. I/O CLOCK and EOC Voltage Waveforms

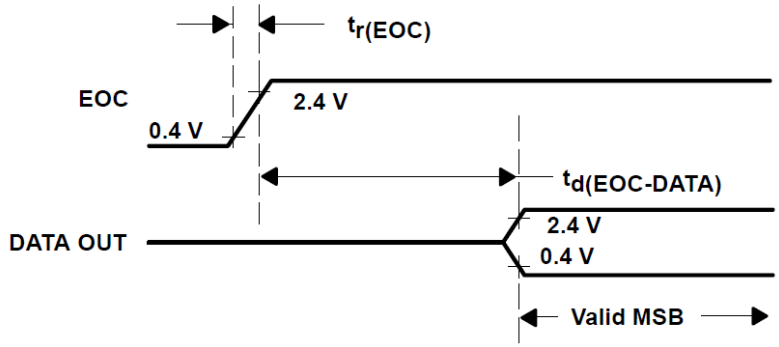


Figure 6-6. EOC and DATA OUT Voltage Waveforms

This figure 6-7 shows the $\overline{CS}$ control sequence which be plugged in the every conversion data transfer(used 16 clock cycle) and the every delivery CLOCK cycle.

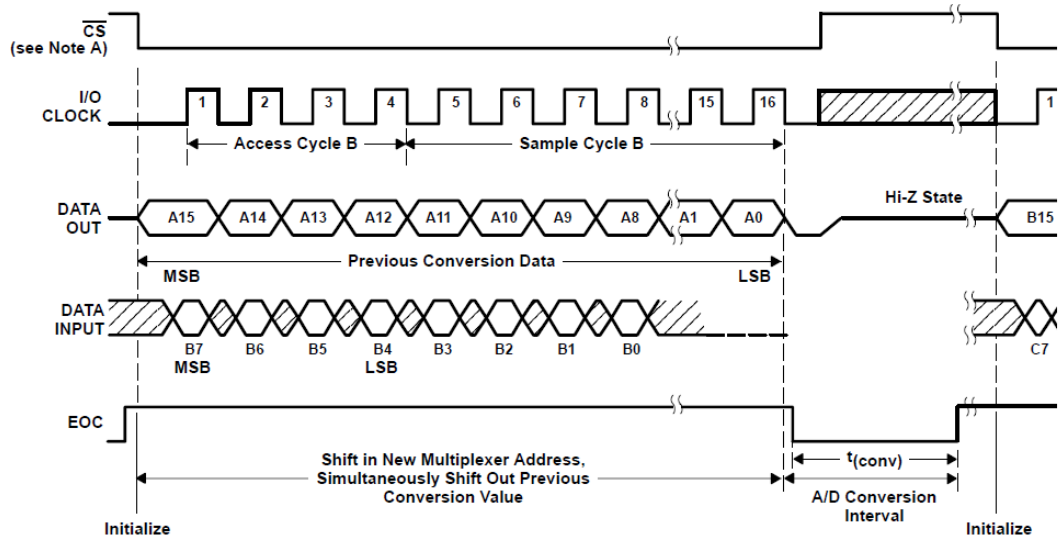


Figure 6-7. Timing for 16-Clock Transfer Using $\overline{CS}$ With MSB First

This figure 6-8 shows the $\overline{CS}$ control sequence which be plugged just one time in the sequence start. the every conversion and data transfer in 16 clock cycle.

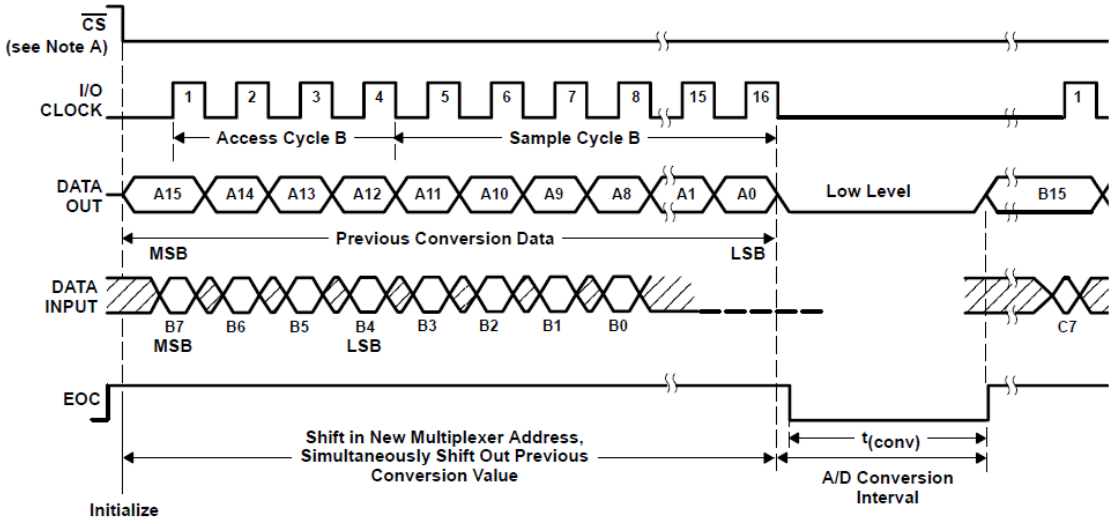


Figure 6-8. Timing for 16-Clock Transfer Not Using $\overline{CS}$ With MSB First

6.2 Principles of operation

Initially, with chip select $\overline{CS}$ high, I/O CLOCK and DATA INPUT are disabled and DATA OUT is in the high-impedance state. $\overline{CS}$ going low begins the conversion sequence by enabling I/O CLOCK and DATA INPUT and removes DATA OUT from the high-impedance state.

The input data is an 8-bit data stream consisting of a 4-bit analog channel address (D7–D4), a 2-bit data length select (D3–D2), an output MSB or LSB first bit (D1), and a unipolar or bipolar output select bit (D0) that are applied to DATA INPUT. The

I/O CLOCK sequence applied to the I/O CLOCK terminal transfers this data to the input data register.

During this transfer, the I/O CLOCK sequence also shifts the previous conversion result from the output data register to DATA OUT. I/O CLOCK receives the input sequence of 8, 12, or 16 clock cycles long depending on the data-length selection in the input data register. Sampling of the analog input begins on the fourth falling edge of the input I/O CLOCK sequence and is held after the last falling edge of the I/O CLOCK sequence. The last falling edge of the I/O CLOCK sequence also takes EOC low and begins the conversion.

I/O cycle

The I/O cycle is defined by the externally provided I/O CLOCK and lasts 8, 12, or 16 clock periods, depending on the selected output data length.

During the I/O cycle, the following two operations take place simultaneously.

An 8-bit data stream consisting of address and control information is provided to DATA INPUT. This data is shifted into the device on the rising edge of the first eight I/O CLOCKs. DATA INPUT is ignored after the first eight clocks during 12- or 16-clock I/O transfers.

The data output, with a length of 8, 12, or 16 bits, is provided serially on DATA OUT. When $\overline{CS}$ is held low, the first output data bit occurs on the rising edge of EOC. When $\overline{CS}$ is negated between conversions, the first output data bit occurs on the falling edge of CS. This data is the result of the previous conversion period, and after the first output data bit, each succeeding bit is clocked out on the falling edge of each succeeding I/O CLOCK.

Conversion cycle

The conversion cycle is transparent to the user, and it is controlled by an internal clock synchronized to I/O CLOCK. During the conversion period, the device performs a uccessive approximation conversion on the analog input voltage. The EOC output goes low at the start of the conversion cycle and goes high when conversion is complete and the output data register is latched. A conversion cycle is started only after the I/O cycle is completed, which minimizes the influence of external digital noise on the accuracy of the conversion.

Power up and initialization

After power up, $\overline{CS}$ must be taken from high to low to begin an I/O cycle. EOC is

initially high, and the input data register is set to all zeroes. The contents of the output data register are random, and the first conversion result should be ignored. To initialize during operation, $\overline{CS}$ is taken high and is then returned low to begin the next I/O cycle. The first conversion after the device has returned from the power-down state may not read accurately due to internal device settling.

Operational Terminology

Table 6-2. Operational Terminology

Current (N) I/O cycle	The entire I/O CLOCK sequence that transfers address and control data into the data register and clocks. the digital result from the previous conversion from DATA OUT
Current (N) conversion cycle	The conversion cycle starts immediately after the current I/O cycle. The end of the current I/O cycle is the last clock falling edge in the I/O CLOCK sequence. The current conversion result is loaded into the output register when conversion is complete.
Current (N) conversion result	The current conversion result is serially shifted out on the next I/O cycle
Previous（N-1）conversion result	The conversion cycle just prior to the current I/O cycle
Next（N+1）I/O conversion result	The I/O period that follows the current conversion cycle

Example: In the 12-bit mode, the result of the current conversion cycle is a 12-bit serial-data stream clocked out during the next I/O cycle. The current I/O cycle must be exactly 12 bits long to maintain synchronization, even when this corrupts the output data from the previous conversion. The current conversion is begun immediately after the twelfth falling edge of the current I/O cycle.

Data input

The data input is internally connected to an 8-bit serial-input address and control register. The register defines the operation of the converter and the output data length. The host provides the data word with the MSB first. Each data bit is clocked in on the rising edge of the I/O CLOCK sequence

Table 6-3 The data input-register format

Function select	**Input data byte**							
	Address bits				**L1**	**L0**	**LSBF**	**BIP**
	D7(MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0(LSB)**
Select input channel								
AIN0	0	0	0	0				

AIN1	0	0	0	1				
AIN2	0	0	1	0				
AIN3	0	0	1	1				
AIN4	0	1	0	0				
AIN5	0	1	0	1				
AIN6	0	1	1	0				
AIN7	0	1	1	1				
AIN8	1	0	0	0				
AIN9	1	0	0	1				
AIN10	1	0	1	0				
select test voltage								
（Vref+-Vref-）/2	1	0	1	1				
Vref-	1	1	0	0				
Vref+	1	1	0	1				
Software power down	1	1	1	0				
Output data length								
8 bits	—	—	—	—	0	1		
12 bits	—	—	—	—	xt	0		
16 bits	—	—	—	—	1	1		
Output data format								
MSB First	—	—	—	—	—	—	0	
LSB First	—	—	—	—	—	—	1	
Unipolar（binary）	—	—	—	—	—	—	—	0
Bipolar	—	—	—	—	—	—	—	1

xt represents a do not care condition

Data input address bits

The four MSBs (D7 – D4) of the data register address one of the 11 input channels, a reference test voltage, or the power-down mode. The address bits affect the current conversion, which is the conversion that immediately follows the current I/O cycle. The reference voltage is nominally equal to Vref+ or Vref–.

Data output length

The next two bits (D3 and D2) of the data register select the output data length. The data-length selection is valid for the current I/O cycle (the cycle in which the data is read). The data-length selection, being valid for the current I/O cycle, allows device start-up without losing I/O synchronization. A data length of 8, 12, or 16 bits can be selected. Since the converter has 12-bit resolution, a data length of 12 bits is suggested.

With D3 and D2 set to 00 or 10, the device is in the 12-bit data-length mode and the result of the current conversion is output as a 12-bit serial data stream during the next I/O cycle. The current I/O cycle must be exactly 12 bits long for proper synchronization, even when this means corrupting the output data from a previous conversion. The current conversion is started immediately after the twelfth falling edge of the current I/O cycle.

With bits D3 and D2 set to 11, the 16-bit data-length mode is selected, which allows convenient communication with 16-bit serial interfaces. In the 16-bit mode, the result of the current conversion is output as a 16bit serial data stream during the next I/O cycle with the four LSBs always reset to 0. The current I/O cycle must be exactly 16 bits long to maintain synchronization even when this means corrupting the output data from the previous conversion. The current conversion is started immediately after the sixteenth falling edge of the current I/O cycle.

Since D3 and D2 take effect on the current I/O cycle when the data length is programmed, there can be a conflict with the previous cycle when the data-word length is changed from one cycle to the next. This may occur when the data format is selected to be least significant bit first.

since at the time the data length change becomes effective (six rising edges of I/O CLOCK), the previous conversion result has already started shifting out. In actual operation, when different data lengths are required within an application and the data length is changed between two conversions, no more than one conversion result can be corrupted and only when it is shifted out
in LSB-first format.

Sampling period

During the sampling period, one of the analog inputs is internally connected to the capacitor array of the converter to store the analog input signal. The converter starts sampling the selected input immediately after the four address bits have been clocked into the input data register. Sampling starts on the fourth falling edge of I/O CLOCK. The converter remains in the sampling mode until the eighth, twelfth, or sixteenth falling edge of the I/O CLOCK depending on the data-length selection. After the EOC delay time from the last I/O CLOCK falling edge, the EOC output goes low indicating that the sampling period is over and the conversion period has begun. After EOC goes low, the analog input can be changed without affecting the conversion result. Since the delay from the falling edge of the last I/O CLOCK to EOC low is fixed,

time-varying analog input signals can be digitized at a fixed rate without introducing systematic harmonic distortion or noise due to timing uncertainty. After the 8-bit data stream has been clocked in, DATA INPUT should be held at a fixed digital level until EOC goes high (indicating that the conversion is complete) to maximize the sampling accuracy and minimize theinfluence of external digital noise.

Data register, LSB first

D1 in the input data register (LSB first) controls the direction of the output binary data transfer. When D1 is reset to 0, the conversion result is shifted out MSB first. When set to 1, the data is shifted out LSB first. Selection of MSB first or LSB first always affects the next I/O cycle and not the current I/O cycle. When changing from one data direction to another, the current I/O cycle is never disrupted.

Data register, bipolar format

D0 (BIP) in the input data register controls the binary data format used to represent the conversion result. When D0 is cleared to 0, the conversion result is represented as unipolar (unsigned binary) data. Nominally, the conversion result of an input voltage equal to Vref– is a code of all zeros (000 . . . 0), the conversion result of an input voltage equal to Vref+ is a code of all ones (111 . . . 1), and the conversion result of (Vref + + Vref–) /2 is a code of a one followed by zeros (100 . . . 0).

When D0 is set to 1, the conversion result is represented as bipolar (signed binary) data. Nominally, conversion of an input voltage equal to Vref– is a code of a one followed by zeros (100 . . . 0), conversion of an input voltage equal to Vref+ is a code of a zero followed by all ones (011 . . . 1), and the conversion of (Vref+ + Vref–) /2 is a code of all zeros (000 . . . 0). The MSB is interpreted as the sign bit. The bipolar data format is related to the unipolar format in that the MSBs are always each other’s complement.

Selection of the unipolar or bipolar format always affects the current conversion cycle, and the result is output during the next I/O cycle. When changing between unipolar and bipolar formats, the data output during the current I/O cycle is not affected.

EOC output

The EOC signal indicates the beginning and the end of conversion. In the reset state, EOC is always high. During the sampling period (beginning after the fourth falling edge of the I/O CLOCK sequence), EOC remains high until the internal sampling

switch of the converter is safely opened. The opening of the sampling switch occurs after the eighth, twelfth, or sixteenth I/O CLOCK falling edge, depending on the data-length selection in the input data register. After the EOC signal goes low, the analog input signal can be changed without affecting the conversion result.

The EOC signal goes high again after the conversion is completed and the conversion result is latched into the output data register. The rising edge of EOC returns the converter to a reset state and a new I/O cycle begins. On the rising edge of EOC, the first bit of the current conversion result is on DATA OUT when $\overline{CS}$ is low. When $\overline{CS}$ is negated between conversions, the first bit of the current conversion result occurs at DATA OUT on the falling edge of $\overline{CS}$.

Data format and pad bits

D3 and D2 of the input data register determine the number of significant bits in the digital output that represent the conversion result. The LSB-first bit determines the direction of the data transfer while the BIP bit determines the arithmetic conversion. The numerical data is always justified toward the MSB in any output format.

The internal conversion result is always 12 bits long. When an 8-bit data transfer is selected, the four LSBs of the internal result are discarded to provide a faster one-byte transfer. When a 12-bit transfer is used, all bits are transferred. When a 16-bit transfer is used, four LSB pad bits are always appended to the internal conversion result. In the LSB-first mode, four leading zeros are output. In the MSB-first mode, the last four bits output are zeros.

When $\overline{CS}$ is held low continuously, the first data bit of the newly completed conversion occurs on DATA OUT on the rising edge of EOC. When a new conversion is started after the last falling edge of I/O CLOCK, EOC goes low and the serial output is forced to a setting of 0 until EOC goes high again.

When $\overline{CS}$ is negated between conversions, the first data bit occurs on DATA OUT on the falling edge of $\overline{CS}$. On each subsequent falling edge of I/O CLOCK after the first data bit appears, the data is changed to the next bit in the serial conversion result until the required number of bits has been output.

Chip-select input ($\overline{CS}$)

$\overline{CS}$ enables and disables the device. During normal operation, $\overline{CS}$ should be low. Although the use of $\overline{CS}$ is not necessary to synchronize a data transfer, it can be brought high between conversions to coordinate the data transfer of several devices sharing the same bus.

When $\overline{CS}$ is brought high, the serial-data output is immediately brought to the high impedance state, releasing its output data line to other devices that may share it. After an internally generated debounce time, I/O CLOCK is inhibited, thus preventing any further change in the internal state.

When $\overline{CS}$ is subsequently brought low again, the device is reset. $\overline{CS}$ must be held low for an internal debounce time before the reset operation takes effect. After $\overline{CS}$ is debounced low, I/O CLOCK must remain inactive (low) for a minimum time before a new I/O cycle can start.

$\overline{CS}$ can interrupt any ongoing data transfer or any ongoing conversion. When $\overline{CS}$ is debounced low long enough before the end of the current conversion cycle, the previous conversion result is saved in the internal output buffer and shifted out during the next I/O cycle.

Power-down features

When a binary address of 1110 is clocked into the input data register during the first four I/O CLOCK cycles, the power-down mode is selected. Power down is activated on the falling edge of the fourth I/O CLOCK pulse.

During power down, all internal circuitry is put in a low-current standby mode. No conversions are performed, and the internal output buffer keeps the previous conversion cycle data results provided that all digital inputs are held above V_{CC}–0.5V or below 0.5V. The I/O logic remains active so the current I/O cycle must be completed even when the power-down mode is selected. Upon power-on reset and before the first I/O cycle, the converter normally begins in the power-down mode. The device remains in the power-down mode until a valid input address (other than 1110) is clocked in. Upon completion of that I/O cycle, a normal conversion is performed with the results being shifted out during the next I/O cycle.

Analog input, test, and power-down mode

The 11 analog inputs, three internal voltages, and power-down mode are selected by the input multiplexer according to the input addresses shown in Tables. The input multiplexer is a break-before-make type to reduce input-to-input noise rejection resulting from channel switching. Sampling of the analog input starts on the falling edge of the fourth I/O CLOCK and continues for the remaining I/O CLOCK pulses. The sample is held on the falling edge of the last I/O CLOCK pulse. The three internal test inputs are applied to the multiplexer, then sampled and converted in the same manner as the external analog inputs. The first conversion after the device has

returned from the power-down state may not read accurately due to internal device settling.

Table 6-4. Analog Channel Select Address

Analog input select	Value shifted into data input	
	Binary	Hex
AIN0	0000	0
AIN1	0001	1
AIN2	0010	2
AIN3	0011	3
AIN4	0100	4
AIN5	0101	5
AIN6	0110	6
AIN7	0111	7
AIN8	1000	8
AIN9	1001	9
AIN10	1010	A

Table 6-5. Test Mode Select Address

Internal self test voltage selected	Value shifted into data input		Unipolar output result Hex
	Binary	Hex	
$(V_{ref+}+V_{ref-})/2$	1011	B	800
V_{ref-}	1100	C	000
V_{ref+}	1101	D	FFF

Note 1： V_{ref+} is the voltage applied to REF+ .V_{ref-} is the voltage applied to REF-.

Note 2：The output results shown are the ideal values and may vary with the reference stability and with internal

Table 6-6. Power Down Select Address

Input command	Value shifted into data input		Result
	Binary	Binary	
Low Power	1110	E	I_{CC}≤25uA

Converter and analog input

The CMOS threshold detector in the successive approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors. In the first phase of the conversion process, the analog input is sampled by closing the SC switch and all ST switches simultaneously.This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all ST and SC switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, 12 capacitors are examined separately until all 12 bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 4096). Node 4096 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. When the voltage at the summing node is greater than the trip point of the threshold detector (approximately 1/2 VCC), a bit 0 is placed in the output register and the 4096-weight capacitor is switched to REF–. When the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 4096-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 2048-weight capacitor, the 1024-weight capacitor, and so forth down the line until all bits are determined. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

Reference voltage inputs

The two reference inputs used with the device are the voltages applied to the REF+ and REF– terminals. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero-scale reading respectively. These voltages and the analog input should not exceed the positive supply or be lower than ground consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ terminal voltage and at zero when the input signal is equal to or lower than REF– terminal voltage.

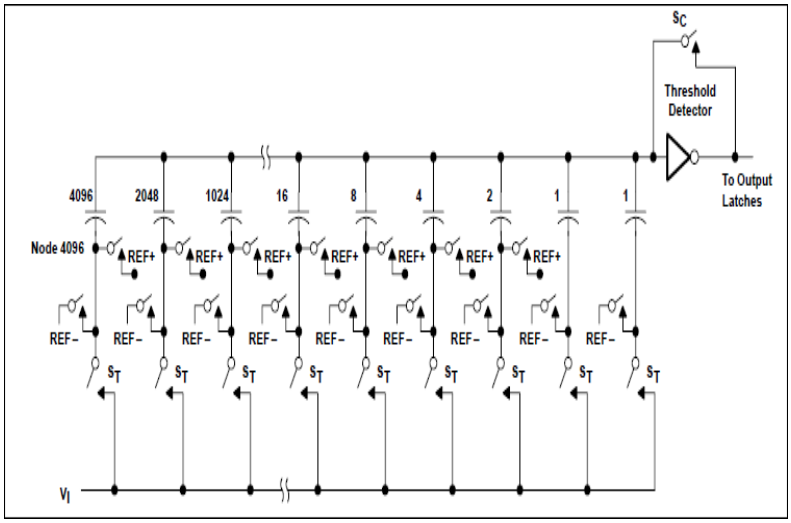


Figure 6-9. Simplified Model of the Successive-Approximation System

Application information

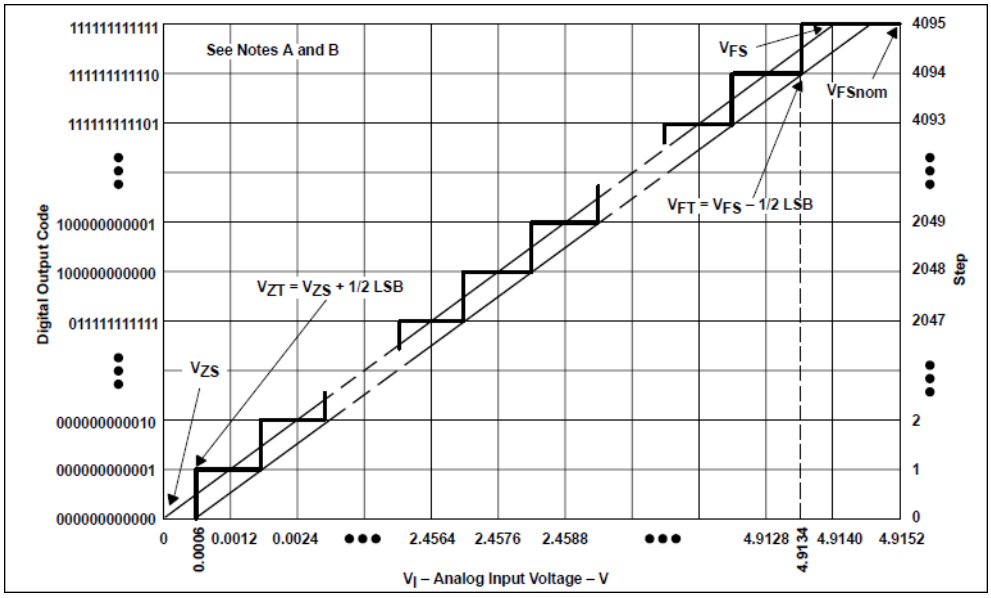


Figure 6-10. Ideal Conversion Characteristics

Note A: This curve is based on the assumption that Vref+ and Vref– have been adjusted so that the voltage at the transition from digital 0 to 1 (VZT) is 0.0006 V and the transition to full scale (VFT) is 4.9134 V. 1 LSB = 1.2 mV.

Note B: The full-scale value (VFS) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (VZS) is the step whose nominal midstep value equals zero.

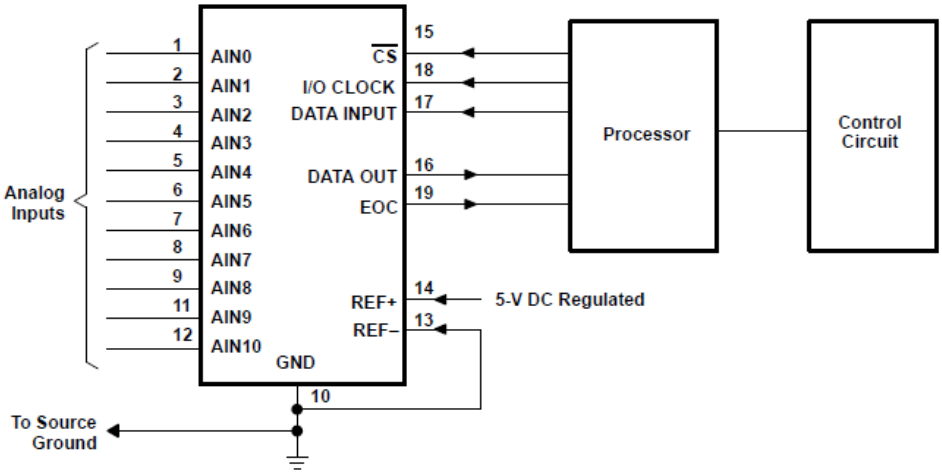


Figure 6-11. Serial Interface

6.3 Storage Condition

The warehouse environment of B2543ARH should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be controlled within a certain range as follow:

Table 6-7. The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

6.4 Recommend operating conditions

a) Supply power vlotage（V_{DDA},V_{DDD}）…… 5V

b) Temperature for work（T_A）…….. -55℃ ～ 125℃

6.5 Radiation hardened performance

a） Total Ionizing Dose：≥60K Rad(Si)

b） The Single Event Latch-up threshold：≥75MeV cm^2/mg

7. Electrical characteristics

Table 7-1. Electrical characteristics table

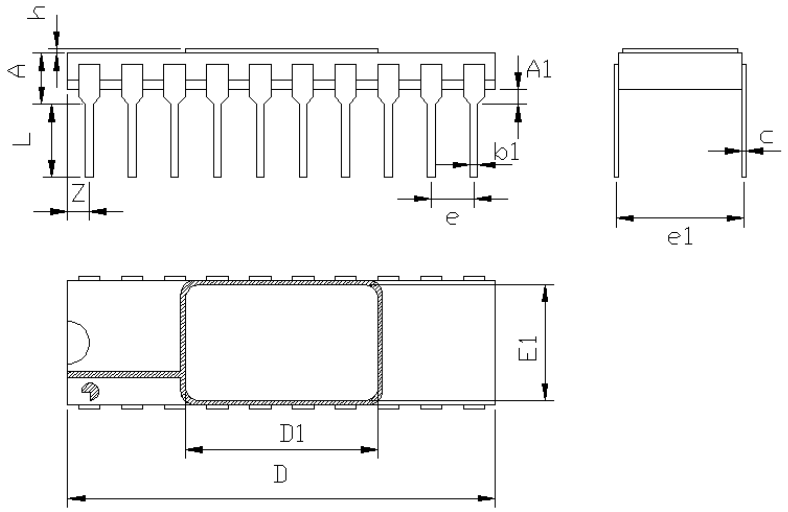
Parameter	Symbol	Condition		B2543ARH		Units
		Unless otherwise specified, -55℃≤T_A≤125℃ V_{CC}=5.0V，f(I/O CLOCK)=4.03MHz		Min	Max	
High level output voltage	V_{OH}	Vcc=4.5V, I_{OH}=-1.6mA		2.4	--	V
		Vcc=4.5V , I_{OH}=-20uA		4.0	--	
Low level output voltage	V_{OL}	Vcc=4.5V, I_{OL}=-1.6mA		--	0.4	V
		Vcc=4.5V , I_{OL}=-20uA		--	0.3	
High impedance off state output current	I_{OZ}	V_O=V_{CC} , $\overline{CS}$ at V_{CC}		--	2.5	uA
			After Total Ionizing Dose	--	20	
		V_O=0, $\overline{CS}$ at V_{CC}		--	-2.5	
			After Total Ionizing Dose	--	-20	
High level input current	I_{IH}	V_{IN}=V_{CC}		--	10	uA
			After Total Ionizing Dose	--	50	
Low level input current	I_{IL}	V_{IN}=0		--	-10	uA
			After Total Ionizing Dose	--	-50	
resolution	RES	Vref+= Vcc， Vref-= 0		12	--	Bits
Operating supply current	I_{CC}	$\overline{CS}$ at 0V		--	2.5	mA
			After Total Ionizing Dose	--	6	
Power-down current	$I_{CC（PD）}$	For all digital inputs：0≤VI≤0.5VI≥ V_{CC} -0.5V		--	25	uA
			After Total Ionizing Dose	--	100	
Selected channel leakage Selected channel leakage current		Selected channel at VCC, Unselected channel at 0 V		--	10	uA
			After Total Ionizing Dose	--	50	
		Selected channel at 0V, Unselected channel at V_{CC}		--	-10	
			After Total Ionizing Dose	--	-50	

Parameter	Symbol	Condition		B2543ARH		Units
		Unless otherwise specified, -55℃≤T_A≤125℃ V_{CC}=5.0V，f(I/O CLOCK)=4.03MHz		Min	Max	
Maximum static analog reference current into REF+		Vref+= Vcc，Vref-= 0		--	2.5	uA
			After Total Ionizing Dose	--	20	
Linearity error	EL	\		--	±1.5	LSB
Differential linearity error	ED	\		-1	+1.5	LSB
Offset error	EO	\		--	±4.5	LSB
Gain error	EG	\		--	±4.5	LSB
Total unadjusted error	ET	Include Line error、0 scale error, full scale error		--	±5.5	LSB
Conversion time	$t_{(CONV)}$	See Figure 6-7,6-8		--	10	us
Total cycle time	t_C	See Figure 6-7,6-8		--	10+ total I/O CLOCK periods +td(I/O-EOC)	us
Channel acquisition time	t_{acq}	See Figure 6-7,6-8		4	12	I/O CLOCK periods
Valid time	t_v	DATA OUT remains valid after I/O CLOCK↓		10	--	ns
Delay time	$t_{d(I/O-DATA)}$	I/O CLOCK↓ to DATA OUT valid		--	150	ns
Delay time	$t_{d(I/O-EOC)}$	See figure 6-5 (last I/O CLOCK↓ to EOC↓)		--	2.2	us
			After Total Ionizing Dose	--	2.8	
Delay time	$t_{d(EOC-DATA}$	See figure 6-6(EOC↑ to DATA OUT (MSB/LSB))		--	100	ns
Enable time	t_{PZH}，t_{PZL}	See figure 6-1($\overline{CS}$↓ to DATA OUT		--	1.3	us
			After Total	--	2.0	

Parameter	Symbol	Condition		B2543ARH		Units
		Unless otherwise specified, -55℃≤T_A≤125℃ V_{CC}=5.0V，f(I/O CLOCK)=4.03MHz		Min	Max	
		(MSB/LSB driven))	Ionizing Dose			
Disable time	t_{PHZ}，t_{PLZ}	See figure 6-1($\overline{CS}$↑ to DATA OUT (high impedance))		--	150	ns
Rise time, EOC	$t_{r(EOC)}$	See Figure 6-6		--	50	ns
Fall time, EOC	$t_{f(EOC)}$	See Figure 6-5		--	50	ns
Rise time, data bus	$t_{r(BUS)}$	See Figure 6-4		--	50	ns
Fall time, data bus	$t_{f(BUS)}$	See Figure 6-4		--	50	ns
Delay time	$t_{d(I/O-CS)}$	last I/O CLOCK↓ to $\overline{CS}$↓ to abort conversion		--	5	us

8. Package outline dimension

The chip is 20 leads DIP ceramic package，the chip outline dimension is shown in Figure 8-1.



symbol	Value(Unit:mm)		
	min	typical	max
D	25.14	--	25.66
D1	11.50	--	12.40
E1	6.98	--	7.98
h	0.22	--	0.28
e1	--	7.62	--
e	--	2.54	--
c	0.20	--	0.36
Z	1.08	--	2.54
A	2.50	--	5.1
A1	0.51	--	1.14
b1	0.35	--	0.59
L	2.54	--	5.0

Figure 8-1. the chip outline dimension

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