Ver 1.2

Radiation Hardened 5V Quad Differential Line Diver

Datasheet

Part Number：B26C31CERH

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Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.1	20170324	——	——	
1.2	20180227	——	change version	

TABLE OF CONTENTS

1. Features

- Single 5V Supply
- CMOS Inputs
- High Impedance Outputs when Disabled or Powered Down
- EIA RS-422 Compatible Outputs
- Full -55°C to +125°C Military Temperature Range
- Radiation-hardened design：
  Total-dose: 100 krad(Si)
  Latchup immune (LET > 75MeV-cm^2/mg)
- Packaging options:
  16-lead Flatpack
  16-lead Dual-In-Line Package
- Low quiescent current

2. General Description

The B26C31CERH is a quad differential line driver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

3. Function Block Diagram

B26C31CERH function block diagram is shown in figure 3-1.

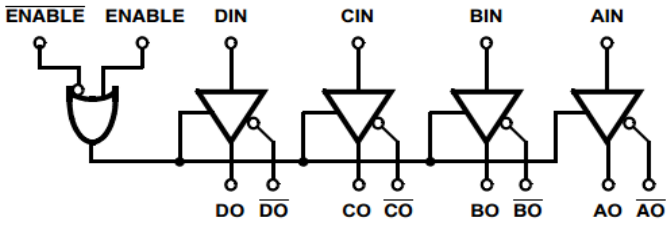


Figure 3-1 B26C31CERH function block digram

4. Packages and Pin Function Descriptions

The provided package is: FP16 and DIP16

B26C31CERH- pin configuration is shown in 4-1.

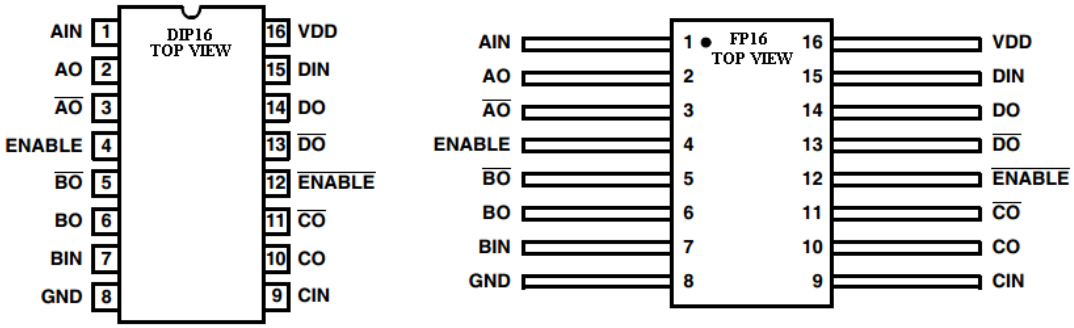


Figure 4-1 B26C31CERH pin configuration

Talble 4-1 B26C31CERH Pin Function Descriptions

Pin No.	Name	Description
1，7，9，15	AIN,BIN,CIN,DIN	Driver input pin
2，6，10，14	AO,BO,CO,DO	Non-inverting driver output pin
3，5，11，13	$\overline{AO}$, $\overline{BO}$, $\overline{CO}$, $\overline{DO}$	Inverting driver output pin
4	ENABLE	Active high enable pin
12	$\overline{ENABLE}$	Active low enable pin
16	VDD	Power supply pin
8	GND	Ground pin

5. Pin List

B26C31CERH –pin list is shown in table 5-1.

Table 5-1 B26C31CERH–pin list

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	AIN	INPUT DATA1	9	CIN	INPUT DATA3
2	AO	OUTPUT DATA1 POSITIVE	10	CO	OUTPUT DATA3 POSITIVE
3	$\overline{AO}$	OUTPUT DATA1 NEGATIVE	11	$\overline{CO}$	OUTPUT DATA3 NEGATIVE
4	ENABLE	Active high enable pin	12	$\overline{ENABLE}$	Active low enable pin
5	$\overline{BO}$	OUTPUT DATA2 NEGATIVE	13	$\overline{DO}$	OUTPUT DATA4 NEGATIVE
6	BO	OUTPUT DATA2 POSITIVE	14	DO	OUTPUT DATA4 POSITIVE
7	BIN	INPUT DATA2	15	DIN	INPUT DATA4
8	GND	GND	16	VDD	POWER

6. Detailed Description

6.1 Function Description

The B26C31CERH accepts CMOS signal levels and converts them to RS-422 compatible outputs. This circuit uses special outputs that enable the drivers to power-down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independently. truth table is shown in table 6-1.

Table 6-1 truth table

ENABLE	$\overline{ENABLE}$	Input	Non-inverting Output	Inverting Output
L	H	X	Z	Z

All other combinations of ENABLE inputs	L	L	H
	H	H	L

L = Low logic state

X = Irrelevant

H = High logic state

Z = TRI-STATE (high impedance)

6.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 10℃～30℃ and relative humidity less than 70%. There should be no acid , alkali or other radiant gas in the environment,

6.3 Absolute Maximum Ratings

a) Supply voltage range to ground potential（V_{DD}）： -0.5V to 7.0 V
b) DC input voltage range（V_{in}）： -0.5V to（V_{DD}+0.5V）
c) DC output voltage (V_{OUT}) power off : -0.5V to 7.0 V
d) Storage temperature（T_{stg}）： -65℃ to 150℃
e) Lead temperature（T_h）： 260℃
f) Junction temperature (TJ)： 150℃

6.4 Recommended Operation Conditions

a) Supply voltage relative to ground（V_{DD}）： 4.5 V ~ 5.5 V
b) Case operation temperature range(TA)： -55℃ to 125℃

7. Specifications

All electrical characteristics are shown in table 7-1，Propagation Delay and Transition Time Waveforms are shown in Figure 7-1，Three-State Delay Waveform is shown in Figure 7-2.

Table 7-1 B26C31CERH electrical characteristics

PARAMETER	SYMBOL	CONDITION	LIMIT		UNIT
		（-55℃≤TA≤125℃，V_{DD}=5.0×（1±10%）V）unless otherwise specified	MIN	MAX	
High-level input voltage	V_{IH}	V_{DD}=4.5V，5.5V	0.7* V_{DD}	—	V
Low-level input voltage	V_{IL}	V_{DD}=4.5V，5.5V	—	0.3* V_{DD}	V
High-level output voltage	V_{OH}	V_{DD}=4.5V and 5.5V，I_O=-20mA	2.5	—	V
Low-level output voltage	V_{OL}	V_{DD}=4.5V and 5.5V，I_O=20mA	—	0.5	V
Input leakage current	I_{IN}	V_{IN}= 0V,5.5V，V_{DD}=5.5V	-1.0	1.0	μA
Differential Output Voltage	VT,$\overline{VT}$	V_{DD}=V_{IH}=4.5V, V_{IL}=0V,R_L=100Ω	2.0	—	V
Difference in differential output	$\lvert VT\rvert - \lvert\overline{VT}\rvert$	V_{DD}=VIH=4.5V, V_{IL}=0V,R_L=100Ω	—	400	mV
Common mode output voltage	V_{OS}	V_{DD}=V_{IH}=4.5V, V_{IL}=0V,R_L=100Ω	—	3.0	V
Difference in common mode output voltage	$\lvert VOS\rvert - \lvert\overline{VOS}\rvert$	V_{DD}=V_{IH}=4.5V, V_{IL}=0V,R_L=100Ω	—	400	mV
Input clamp voltage	V_{IC}	I_{IC} =-1 mA	-1.5	—	V
		I_{IC} =1 mA	—	1.5	V
Output Short Circuit Current[a]	I_{OS}	V_{IN}=V_{DD},V_{OUT}=0V and V_{IN}=0V,V_{OUT}=0V，V_{DD}=5.5V	-30	-150	mA
Output Three-State Current	I_{OZ}	V_{DD}=5.5V, ENABLE=0V，$\overline{ENABLE}$ =5.5V，V_{IN}=V_{DD} or GND	-5.0	5.0	μA
Standby supply current	I_{DDSB}	V_{DD}=5.5V, V_{IN}=V_{DD} and GND Outputs= open	—	500	uA
Output leakage current power OFF	Ioff	V_{DD}=0V, V_{OUT}=6V, -250mV	-100	100	uA

Function test	FT	f =10MHz			
Differential Propagation Delay High to Low	t_{PHLD}	V_{DD}=4.5V，R_L=100Ω，C_L=40p Figure 7-1	2	22	ns
Differential Propagation Delay Low to High	t_{PLHD}	V_{DD}=4.5V，R_L=100Ω，C_L=40p Figure 7-1	2	22	ns
Differential Skew (tPHLD - tPLHD)	t_{SKD}	V_{DD}=4.5V，R_L=100Ω，C_L=40p Figure 7-1	—	3.0	ns
Rise Time	t_{TLH}	V_{DD}=4.5V，R_L=100Ω，C_L=40p Figure 7-1	1.0	10	ns
Fall Time	t_{THL}	V_{DD}=4.5V，R_L=100Ω，C_L=40p Figure 7-1	1.0	10	ns
Disable Time High to Z	t_{PHZ}	V_{DD}=4.5V ,Figure 7-2	2.0	22	ns
Disable Time Low to Z	t_{PLZ}	V_{DD}=4.5V ,Figure 7-2	2.0	22	ns
Enable Time Z to High	t_{PZH}	V_{DD}=4.5V ,Figure 7-2	5.0	28	ns
Enable Time Z to Low	t_{PZL}	V_{DD}=4.5V ,Figure 7-2	5.0	28	ns
Input capacitance[b]	C_{IN}	V_{DD} = open, f = 1 MHz	—	12	pF
Output capacitance[b]	C_{OUT}	V_{DD} = open, f = 1 MHz	—	12	pF

Notes：

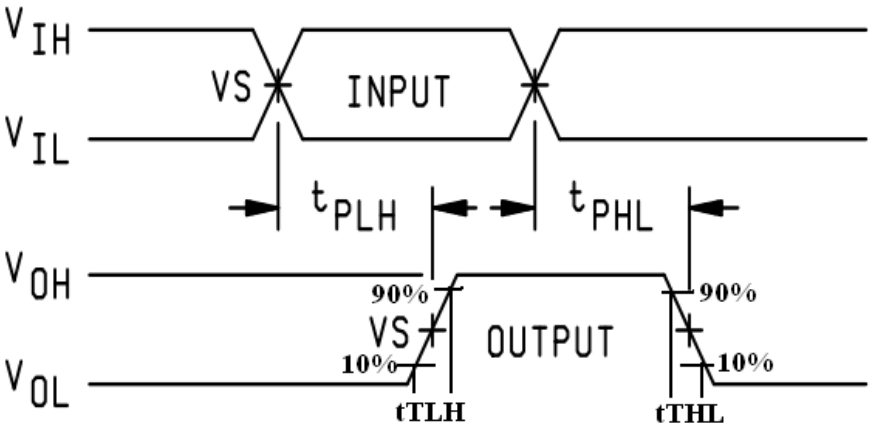
1、Devices are tested @ V_{DD} = 4.5V&5.5V.

2、Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.

3、Generator waveform for all tests unless otherwise specified: f = 1 MHz, tr < 6 ns, and tf < 6 ns.

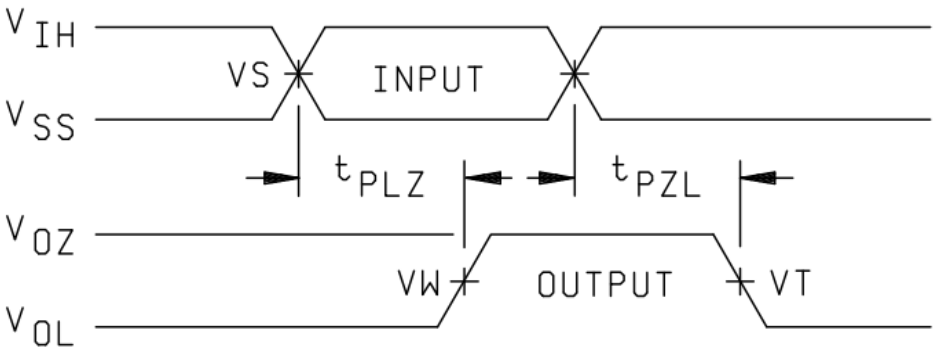
a Only one output at a time may be shorted.

b Parameter is guaranteed by design or process, but not tested.

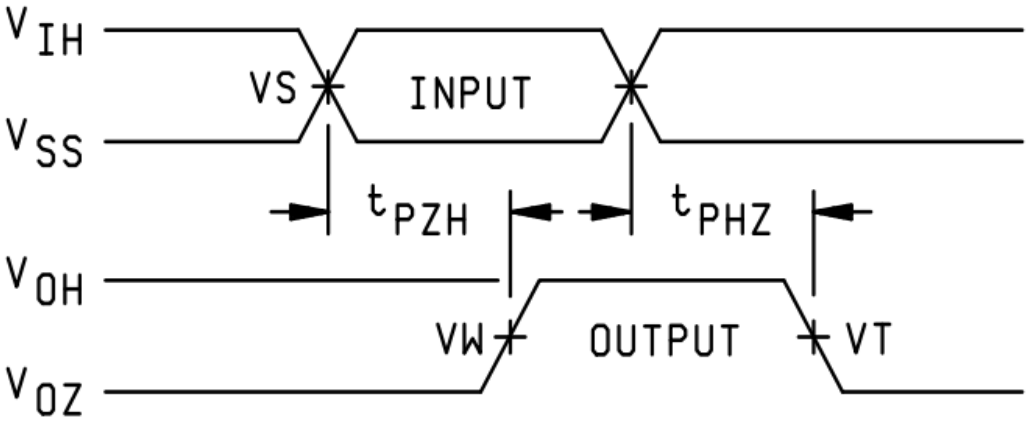


Note： V_{DD} = 4.50 V V_{IH} = 4.50 V V_{IL} = 0 V V_S = 50 %

Figure.7-1. Driver Propagation Delay and Transition Time Waveforms



Note： V_{DD} = 4.50 V V_{IH} = 4.50 V V_S = 50 % $V_W = V_{OL}$ + 0.3 V V_T = 0.80 V



Note： V_{DD} = 4.50 V V_{IH} = 4.50 V V_S = 50 % $V_W = V_{OL}$ + 0.3 V V_T = 2.00 V

Figure.7-2. Driver Three-State Delay Waveform

8. Package Specifications

B26C31CERHF adopt 16-Lead Ceramic Quad Flat package, as in Figure 8-1 and the size is listed in Table 8-1. B26C31CERHD adopt 16-lead Dual-In-Line Package, as in Figure 8-2 and the size is listed in Table 8-2.

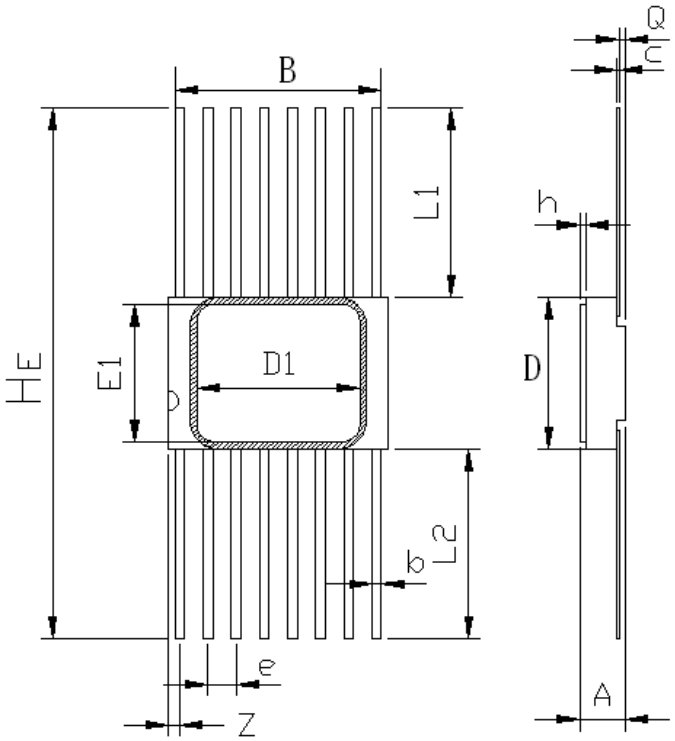


Figure 8-1 Flat Package Outline

Table 8-1 Flat Package Size

Symbol	Value（unit：mm）		
	Min	Normal	Max
A	1.60	——	2.50
B	8.94	——	9.69
b	0.25	——	0.54
c	0.07	——	0.20
D	6.55	——	7.25
e	——	1.27	——

He	18.76	19.41	20.06
Q	0.13	——	0.90
L1	5.75	——	6.75
L2	5.75	——	6.75
Z	——	——	1.27
D1	——	7.366	——
E1	——	6.223	——
h	0.22	——	0.28

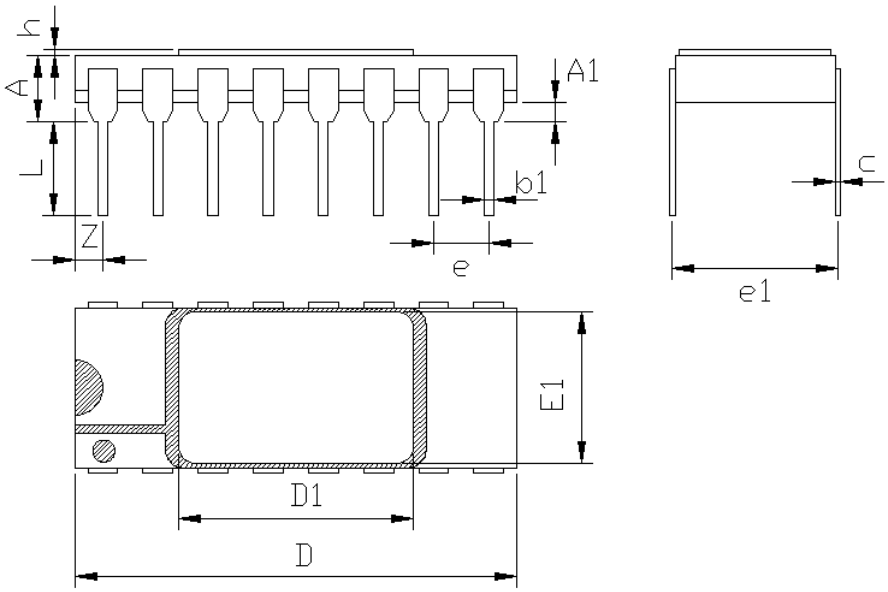


Figure.8-2. Dual-In-Line Package Outline

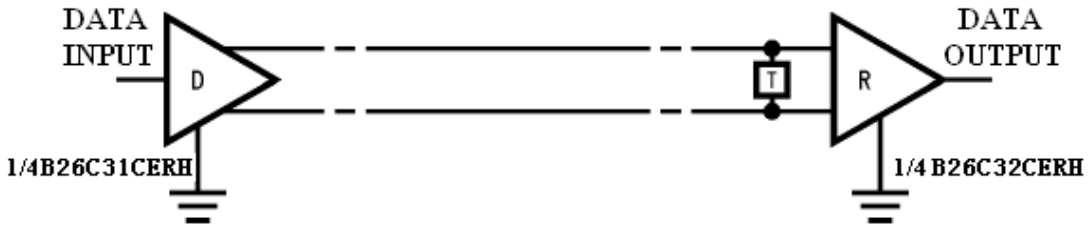
Table 8-2 Dual-In-Line Package Size

Symbol	Value（unit：mm）		
	Min	Normal	Max
D	20.00	——	20.58
D1	——	10.795	——
E1	——	6.985	——

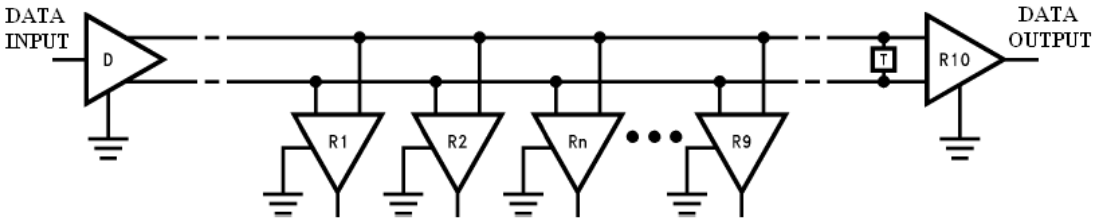
h	0.22	——	0.28
e1	——	7.62	——
e	——	2.54	——
c	0.20	——	0.36
Z	——	——	2.54
A	——	——	5.1
A1	0.51	——	——
b1	0.35	——	0.59
L	2.54	——	5.0

9. Appendix I Typical Application Example

The B26C31CERH driver's intended use is primarily in an uncomplicated point-to-point configuration as is shown in Appendix figure.1-1. This configuration provides a clean signaling environment for quick edge rates of the drivers. The receiver is connected to the driver through a balanced media such as a standard twisted pair cable. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media and is located as close to the receiver input pins as possible. Other configurations are possible such as a multireceiver configuration, Multidrop configuration as is shown in Appendix figure.1-2.



Appendix figure.1-1. Point-to-Point Application



Appendix figure.1-2. Multidrop Application

10. Appendix II Replaced Product

Appendix table1-1

Device Type	Substituted Device Type
B26C31CERHD	HS1-26C31RH-Q
B26C31CERHF	HS9-26C31RH-Q

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