Ver 1.2

Radiation Hardened Bidirectional Multipurpose Transceiver

Datasheet

Part Number：B54ACS164245SARH

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Beijing Microelectronics Technology Institute

Page of Revise Control

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1. Features

- **Electrical characteristics**
  - Voltage translation：
    -- 5V bus to 3.3V bus
    -- 5V bus to 5V bus
    -- 3.3V bus to 5V bus
    -- 3.3V bus to 3.3V bus
  - Cold sparing：
    1MΩminimum input impedance power-off
  - Warm sparing：
    Guaranteed out tri-state while one power supply is "off" and the other is "on"
  - Power up 3 states
  - High speed, low power consumption
  - Schmitt trigger inputs to filter noisy signals
  - 0.5um Commercial CMOS
- **Reliability features**
  - Operating temperature ： -55℃ ～ +125℃
  - ESD feature （human body model）：2000V
  - Electrical latch up feature：200mA
  - Total ionizing dose：≥100Krad（Si）
  - Single event latch-up threshold：≥75MeV·cm^2/mg
- **Packaging options**
  - 48-lead flatpack

2. General Description

The 16-bit wide B54ACS164245SARH Multipurpose transceiver is designed to perform multiple functions including: asynchronous two-way communication, Schmitt input buffering, voltage translation, cold sparing, warm sparing, power up. With either or both V_{DD1} and V_{DD2} are equal to zero volts, the B54ACS164245SARH outputs and inputs present a minimum impedance of 1MΩ making it ideal for “cold spare” or “warm spare” applications. The B54ACS164245SARH enables system designers to interface 3.3 volt CMOS compatible components with 5 volt CMOS components. For voltage translation, the A port interfaces with the 3.3 volt bus; the B port interfaces with the 5 volt bus. The direction control (DIRx) controls the direction of data flow. The output enable ($\overline{OE}$x) overrides the direction control and disables both ports. These signals can be driven from either port A or B.

The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver.

3. Function Block Diagram

B54ACS164245SARH function block diagram is shown in figure 3-1.

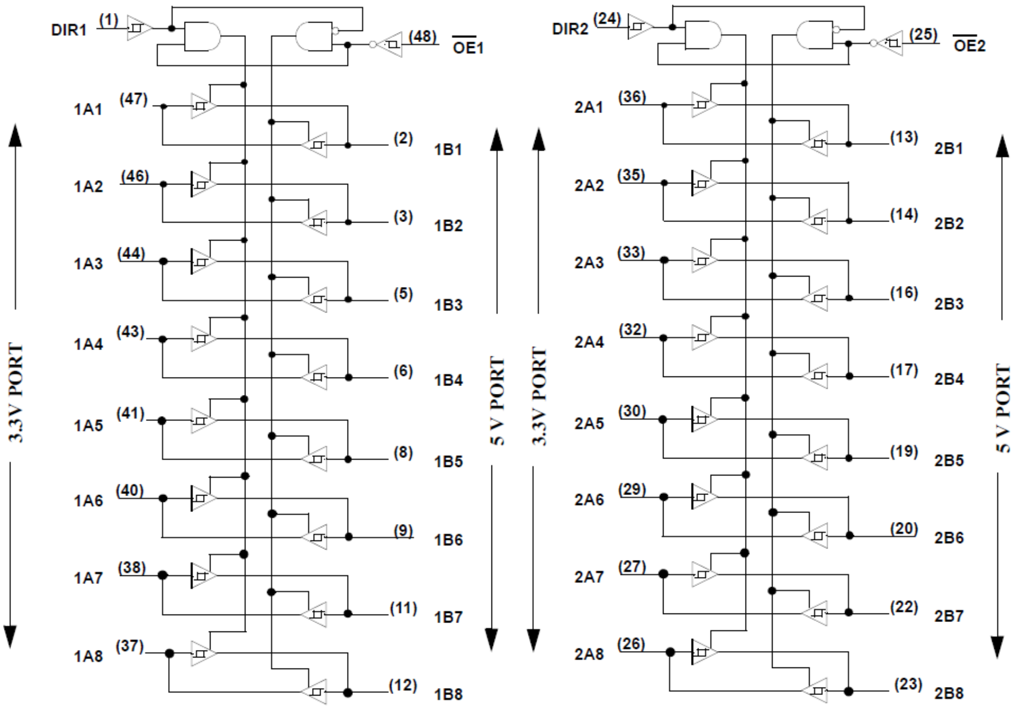


Figure 3-1 B54ACS164245SARH function block digram

4. Packages and Pin Function Descriptions

The provided package is: FP48.

B54ACS164245SARH FP48 pin configuration is shown in 4-1.

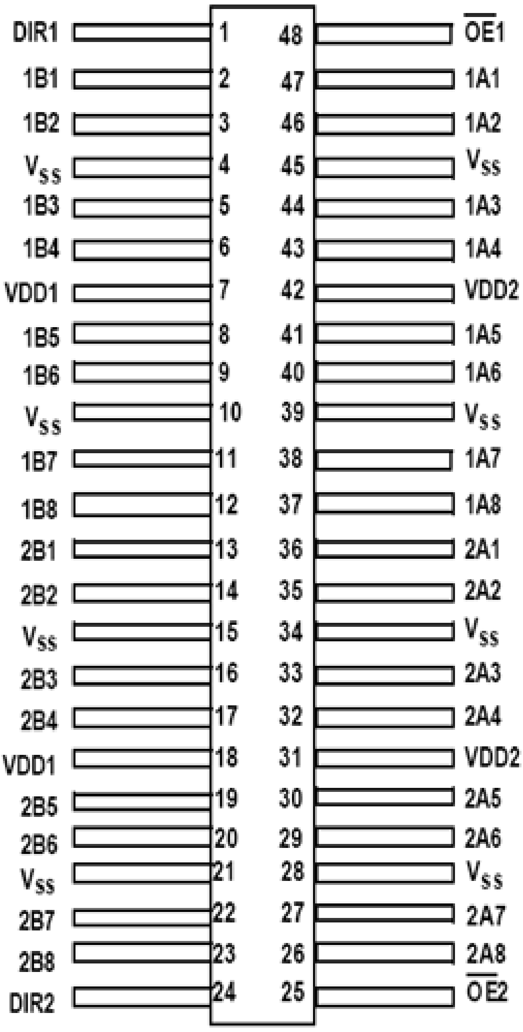


Figure 4-1 B54ACS164245SARH pin configuration

Talble 4-1 B54ACS164245SARH Pin Function Descriptions

Pin Names	Description
$\overline{\text{OE}}$x	Output Enable Input (Active Low)
DIRx	Direction Control Inputs
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)

5. Pin List

B54ACS164245SARH pin list is shown in table 5-1.

Table 5-1 B54ACS164245SARH pin list

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	DIR1	I	48	$\overline{OE}_1$	I
2	1B1	I/O	47	1A1	I/O
3	1B2	I/O	46	1A2	I/O
4	VSS	G	45	V_{SS}	G
5	1B3	I/O	44	1A3	I/O
6	1B4	I/O	43	1A4	I/O
7	V_{DD1}	P	42	V_{DD2}	P
8	1B5	I/O	41	1A5	I/O
9	1B6	I/O	40	1A6	I/O
10	V_{SS}	G	39	V_{SS}	G
11	1B7	I/O	38	1A7	I/O
12	1B8	I/O	37	1A8	I/O
13	2B1	I/O	36	2A1	I/O
14	2B2	I/O	35	2A2	I/O
15	V_{SS}	G	34	V_{SS}	G
16	2B3	I/O	33	2A3	I/O
17	2B4	I/O	32	2A4	I/O
18	V_{DD1}	P	31	V_{DD2}	P
19	2B5	I/O	30	2A5	I/O
20	2B6	I/O	29	2A6	I/O
21	V_{SS}	G	28	V_{SS}	G
22	2B7	I/O	27	2A7	I/O
23	2B8	I/O	26	2A8	I/O
24	DIR2	I	25	$\overline{OE}_2$	I

6. Detailed Description

6.1 Function Description

The 16-bit wide B54ACS164245SARH multipurpose transceiver is designed to perform multiple functions including: asynchronous two-way communication, Schmitt input buffering, voltage translation, cold sparing, warm sparing, power up. With either or both V_{DD1} and V_{DD2} are equal to zero volts, the B54ACS164245SARH outputs and inputs present a minimum impedance of 1MΩ making it ideal for “cold spare” or “warm spare” applications. The B54ACS164245SARH enables system designers to interface 3.3 volt CMOS compatible components with 5 volt CMOS components. For voltage translation, the A port interfaces with the 3.3 volt bus; the B port interfaces with the 5 volt bus. The direction control (DIRx) controls the direction of data flow. The output enable ($\overline{\text{OE}}$x) overrides the direction control and disables both ports. These signals can be driven from either port A or B.

The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver.

Table 6-1 FUNCTION TABLE

Enables $\overline{\text{OE}}$x	Direction DIRx	Operation
L	L	B Data To A Bus
L	H	A Data To B Bus
H	X	Isolation

Table 6-2 POWER TABLE

Port B	Port A	OPERATION
5 Volts	3.3 Volts	Voltage Translator
5 Volts	5 Volts	Non Translating
3.3 Volts	3.3 Volts	Non Translating
V_{SS}	V_{SS}	Cold Spare
V_{SS}	3.3V or 5V	Port A Warm Spare
3.3V or 5V	V_{SS}	Port B Warm Spare

For proper operation, connect power to all V_{DD} pins and ground all V_{SS} pins (i.e., no floating V_{DD} or V_{SS} input pins). By virtue of the B54ACS164245SARH warm spare feature, power supplies V_{DD1} and V_{DD2} may be applied to the device in any order.

To ensure the device is in cold spare mode, both supplies, V_{DD1} and V_{DD2} must be equal to V_{SS}. Warm spare operation is in effect when one power supply is on and the other power supply is equal to V_{SS}. If V_{DD1} has a power on ramp longer than 1 second, then V_{DD2} should be powered on first to ensure proper control of DIRx and OEx. During normal operation of the part, after power-up, ensure $V_{DD1}>V_{DD2}$. By definition, warm sparing occurs when half of the chip receives its normal V_{DD} supply value while the V_{DD} supplying the other half of the chip is set to 0.0V. When the chip is "warm spared", the side that has V_{DD} set to a normal operational value is "actively" tri-stated because the chip's internal OE signal is forced low. The side of the chip that has V_{DD} set to 0.0V is "passively" tri-stated by the cold spare circuitry. In order to minimize transients and current consumption, the user is encouraged to first apply a high level to the OEx pins and then power down the appropriate supply.

6.2 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 15℃～25℃ and relative humidity less than 65%. There should be no acid , alkali or other radiant gas in the environment, well-ventilated, corresponding anti static measure.

6.3 Absolute Maximum Ratings

a) Supply voltage range to ground potential（V_{DD1},V_{DD2}）： -0.3 V ～6.0V
b) Voltage any pin（V_I,V_O）： -0.3 V ～V_{DD1}+0.3 V
c) DC input current（I_{IN}）： -10mA ～+10mA
d) Storage temperature（T_{stg}）： -65℃～ 150℃
e) Lead temperature（T_h,10s）： 300℃
f) Thermal resistance junction to case（$R_{th(J-C)}$）： 28℃/W

6.4 Recommended Operation Conditions

a) Supply voltage relative to ground（V_{DD1},V_{DD2}）：
3.0V ～ 3.6V 或 4.5V ～ 5.5V
b) Input voltage any pin（V_{DD1},V_{DD2}）： 0 ～V_{DD1}
c) Case operation temperature range(T_A) ： -55℃~125℃

d) Minimum power-up ramp rate(△t/V_{DD}) ： 200us/V

e) Maximum input rise and fall time（tr，tf）： 1ns/V(Typical)

7. Specifications

All electrical characteristics are shown in table 7-1.

Table 7-1 B54ACS164245SARH electrical characteristics

PARAMETER	SYMBOL	Test conditions	Limits		Unit
		(4.5V≤V_{DD1}≤5.5V,3V≤V_{DD2}≤3.6V,-55℃<T_C<125℃)	Min	Max	
Schmitt trigger positive going threshold	V_{T+}	A Port=3.3V,V_{DD1}=5.5V and 4.5V,V_{DD2}=3.6V and 3.0V; A Port=5V,V_{DD1}=5.5V and 4.5V,V_{DD2}=5.5V and 4.5V.		0.7V_{DD2}	V
		B Port=3.3V,V_{DD1}=3.6V and 3.0V,V_{DD2}=3.6V and 3.0V; B Port=5V,V_{DD1}=5.5V and 4.5V,V_{DD2}=3.6V and 3.0V.		0.7V_{DD1}	V
Schmitt trigger negative going threshold	V_{T-}	A Port=3.3V,V_{DD1}=5.5V and 4.5V,V_{DD2}=3.6V and 3.0V; A Port=5V,V_{DD1}=5.5V and 4.5V,V_{DD2}=5.5V and 4.5V.	0.3V_{DD2}		V
		B Port=3.3V,V_{DD1}=3.6V and 3.0V,V_{DD2}=3.6V and 3.0V; B Port=5V,V_{DD1}=5.5V and 4.5V,V_{DD2}=3.6V and 3.0V.	0.3V_{DD1}		V
Schmitt trigger range of hysteresis[a]	V_{H1}	A Port=3.3V,V_{DD1}=5.5V and 4.5V,V_{DD2}=3.6V and 3.0V; B Port=3.3V,V_{DD1}=3.0V and 3.6V,V_{DD2}=3.0V and 3.6V.	0.4		V
Schmitt trigger range of hysteresis[a]	V_{H2}	A Port=5V,V_{DD1}=5.5V and 4.5V,V_{DD2}=5.5V and 4.5V; B Port=5V,V_{DD1}=5.5V and 4.5V， V_{DD2}=3.6V and 3.0V.	0.6		V
Three-state output leakage current high	I_{OZH}	APort=3.3V,V_{DD1}=5.5V,V_{DD2}=3.6V,V_{IN}=V_{DD2}/V_{SS}， V_{OUT}= V_{DD}; APort=5.0V,V_{DD1}=5.5V=V_{DD2} ,V_{IN}=V_{DD2}/V_{SS} ， V_{OUT}= V_{DD2}; BPort=3.3V,V_{DD2}=V_{DD1}=3.6V ,V_{IN}=V_{DD1}/V_{SS} ， V_{OUT}= V_{DD1}; BPort=5.0V,V_{DD2}=3.6V,V_{DD1}=5.5V,V_{IN}=V_{DD1}/V_{SS}， V_{OUT}= V_{DD1}.	-	1	μA
Three-state output leakage current low	I_{OZL}	APort=3.3V,V_{DD1}=5.5V,V_{DD2}=3.6V,V_{IN}=V_{DD2}/V_{SS}， V_{OUT}= V_{SS}; APort=5.0V,V_{DD1}=5.5V=V_{DD2} ,V_{IN}=V_{DD2}/V_{SS} ， V_{OUT}= V_{SS}; BPort=3.3V,V_{DD2}=V_{DD1}=3.6V ,V_{IN}=V_{DD1}/V_{SS} ， V_{OUT}= V_{SS}; BPort=5.0V,V_{DD2}=3.6V,V_{DD1}=5.5V,V_{IN}=V_{DD1}/V_{SS}， V_{OUT}= V_{SS}.	-1	-	μA
Input current cold spare mode	I_{CS}	A Port=B Port=V_{IN}=5.5V， V_{DD}=V_{SS}.	-1	5	μA
Warm sparing input leakage current	I_{WS}	V_{IN}=5.5V, V_{DD1}=V_{SS} & V_{DD2}=3.0V to 5.5V or V_{DD1} = 3.0V to 5.5V & V_{DD2} = V_{SS}	-1	5	μA
Three-state output current,power-up[a]	I_{OZPU}	V_{DD} =0-1.2V, V_{OUT} = 0.5 V to 3.0 V, $\overline{OE}$ =Don‘t care		±100	μA
Three-state output current,power-down[a]	I_{OZPD}	V_{DD} =1.2V - 0, V_{OUT} = 0.5 V to 3.0 V, $\overline{OE}$ =Don‘t care		±100	μA

PARAMETER	SYMBOL	Test conditions	Limits		Unit
		(4.5V≤V_{DD1}≤5.5V,3V≤V_{DD2}≤3.6V,-55℃<T_C<125℃)	Min	Max	
Input current high	I_{IH}	APort=3.3V,V_{DD1}=5.5V,V_{DD2}=3.6V,V_{IN}=V_{DD2}/V_{SS}; APort=5.0V,V_{DD1}=5.5V=V_{DD2} ,V_{IN}=V_{DD2}/V_{SS} ; BPort=3.3V,V_{DD2}=V_{DD1}=3.6V ,V_{IN}=V_{DD1}/V_{SS} ; BPort=5.0V,V_{DD2}=3.6V,V_{DD1}=5.5V,V_{IN}=V_{DD1}/V_{SS}.	-	1	μA
Input current low	I_{IL}	APort=3.3V,V_{DD1}=5.5V,V_{DD2}=3.6V,V_{IN}=V_{DD2}/V_{SS}; APort=5.0V,V_{DD1}=5.5V=V_{DD2} ,V_{IN}=V_{DD2}/V_{SS} ； BPort=3.3V,V_{DD2}=V_{DD1}=3.6V ,V_{IN}=V_{DD1}/V_{SS}; BPort=5.0V,V_{DD2}=3.6V,V_{DD1}=5.5V,V_{IN}=V_{DD1}/V_{SS}.	-1		μA
Low level output voltage	V_{OL1}	APort=3.3V,I_{OL}=8mA,V_{IN}=V_{DD2}/V_{SS},V_{DD1}=4.5V,V_{DD2}=3.0V.		0.5	V
		BPort=3.3V,I_{OL}=8mA,V_{IN}=V_{DD1}/V_{SS},V_{DD1}=3.0V,V_{DD2}=3.0V.		0.5	V
		APort=5V,I_{OL}=8mA,V_{IN}=V_{DD2}/V_{SS},V_{DD1}=4.5V,V_{DD2}=4.5V.		0.4	V
		BPort=5V,I_{OL}=8mA,V_{IN}=V_{DD1}/V_{SS},V_{DD1}=4.5V,V_{DD2}=3.0V.		0.4	V
Low level output voltage	V_{OL2}	APort=3.3V,I_{OL}=100μA,V_{IN}=V_{DD2}/V_{SS},V_{DD1}=4.5V,V_{DD2}=3.0V.		0.2	V
		BPort=3.3V,I_{OL}=100μA,V_{IN}=V_{DD1}/V_{SS},V_{DD1}=3.0V,V_{DD2}=3.0V.		0.2	V
		APort=5V,I_{OL}=100μA,V_{IN}=V_{DD2}/V_{SS},V_{DD1}=4.5V,V_{DD2}=4.5V.		0.2	V
		BPort=5V,I_{OL}=100μA,V_{IN}=V_{DD1}/V_{SS},V_{DD1}=4.5V,V_{DD2}=3.0V.		0.2	V
High level output voltage	V_{OH1}	APort=3.3V,I_{OH}=-8mA,V_{IN}=V_{DD2}/V_{SS},V_{DD1}=4.5V,V_{DD2}=3.0V.	V_{DD2}-0.9		V
		BPort=3.3V,I_{OH}=-8mA,V_{IN}=V_{DD1}/V_{SS},V_{DD1}=3.0V,V_{DD2}=3.0V.	V_{DD1}-0.9		V
		APort=5V,I_{OH}=-8mA,V_{IN}=V_{DD2}/V_{SS},V_{DD1}=4.5V,V_{DD2}=4.5V.	V_{DD2}-0.7		V
		BPort=5V,I_{OH}=-8mA,V_{IN}=V_{DD1}/V_{SS},V_{DD1}=4.5V,V_{DD2}=3.0V.	V_{DD1}-0.7		V
High level output voltage	V_{OH2}	APort=3.3V,I_{OH}=-100μA,V_{IN}=V_{DD2}/V_{SS},V_{DD1}=4.5V,V_{DD2}=3.0V;	V_{DD2}-0.2		V
		APort=5V,I_{OH}=-100μA,V_{IN}=V_{DD2}/V_{SS},V_{DD1}=4.5V,V_{DD2}=4.5V.			
		BPort=3.3V,I_{OH}=-100μA,V_{IN}=V_{DD1}/V_{SS},V_{DD1}=3.0V,V_{DD2}=3.0V;			
		BPort=5V,I_{OH}=-100μA,V_{IN}=V_{DD1}/V_{SS},V_{DD1}=4.5V,V_{DD2}=3.0V.	V_{DD1}-0.2		V
Quiescent supply current	I_{DDQ1}	V_{DD}=5.5V， V_{IN}=V_{DD}/V_{SS} ， T_A=25℃		10	μA
	I_{DDQ2}	V_{DD}=5.5V， V_{IN}=V_{DD}/V_{SS} ， T_A= -55℃， T_A=125℃		100	μA
	I_{DDQ3}	V_{DD}=5.5V， V_{IN}=V_{DD}/V_{SS}（Post-Rad 25℃）		500	μA
Input capacitance	C_{IN}	T_C=25℃ f=1MH_Z		15	pF
Output capacitance	C_{OUT}	T_C=25℃ f=1MH_Z		15	pF
Functional test		V_{IH}=0.7V_{DD}, V_{IL}=0.3 V_{DD}, V_{DD1}=4.5V and 5.5V, V_{DD2}=3.0V and 3.6V	L	H	

SYMBOL	Test conditions	Limits		Unit
	(4.5V≤V_{DD1}≤5.5V,3V≤V_{DD2}≤3.6V,-55℃<T_C<125℃)	Min	Max	
t_{PLH}	PORT B 5V,PORT A 3.3V， V_{DD1}=4.5V and 5.5V,V_{DD2}=3.0V and 3.6V. Shown as Figure7-1.	1.0	20	ns
t_{PHL}		1.0	20	ns
t_{PZL}		1.0	18	ns
t_{PZH}		1.0	18	ns
t_{PLZ}[a]		1.0	20	ns
t_{PHZ}[a]		1.0	20	ns
t_{SKEW}[a]		-	900	ps
t_{DSKEW}[a]		-	1.5	ns
t_{PLH}	PORT B PORT A 5V， V_{DD1}=4.5V and 5.5V,V_{DD2}=4.5V and 5.5V. Shown as Figure7-2.	1.0	15	ns
t_{PHL}		1.0	15	ns
t_{PZL}		1.0	12	ns
t_{PZH}		1.0	12	ns
t_{PLZ}[a]		1.0	15	ns
t_{PHZ}[a]		1.0	15	ns
t_{SKEW}[a]		-	900	ps
t_{DSKEW}[a]		-	1.5	ns
t_{PLH}	PORT B＝PORT A＝3.3V ， V_{DD1}=3.0Vand 3.6V,V_{DD2}=3.0V and 3.6V. Shown as Figure7-3	1.0	20	ns
t_{PHL}		1.0	20	ns
t_{PZL}		1.0	18	ns
t_{PZH}		1.0	18	ns
t_{PLZ}[a]		1.0	20	ns
t_{PHZ}[a]		1.0	20	ns
t_{SKEW}[a]		-	900	ps
t_{DSKEW}[a]		-	1.5	ns

[a] Guaranteed。

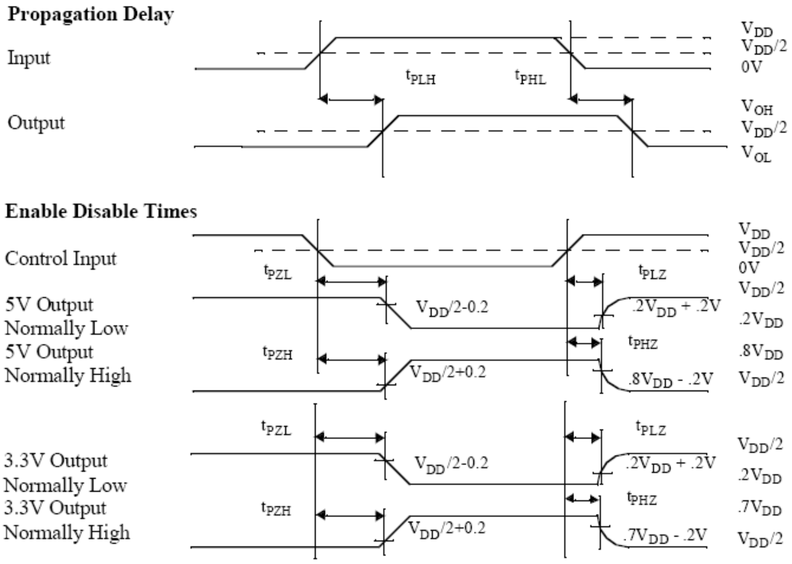


Figure 7-1 Propagation Delay and Enable Disable Times(PORTB 5V,PORTA 3.3V)

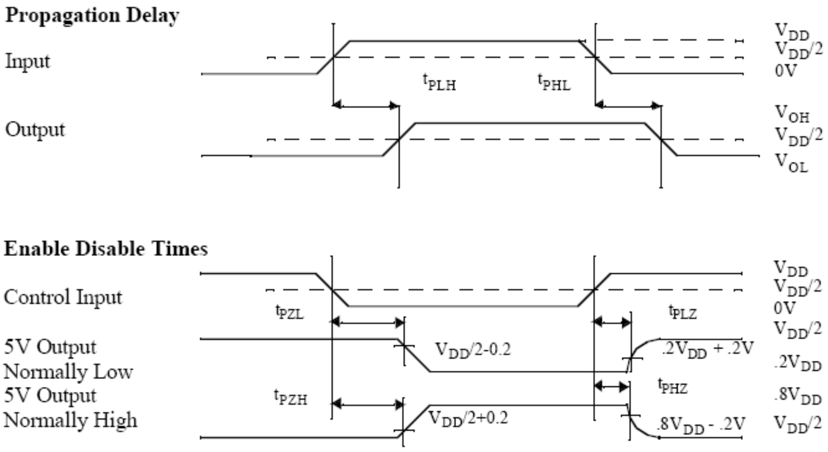


Figure 7-2 Propagation Delay and Enable Disable Times(PORT B,PORT A 5V)

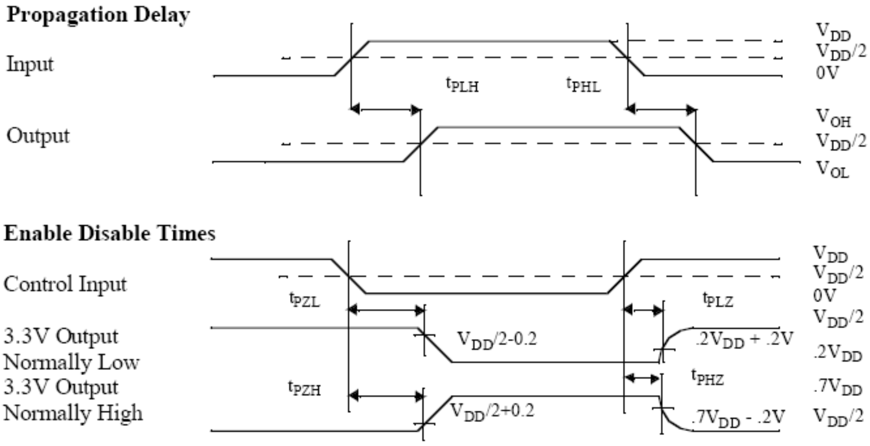


Figure 7-3 Propagation Delay and Enable Disable Times(PORT B,PORT A 3.3V)

8. Package Specifications

The specifications of FP48 package are shown in figure8-1.

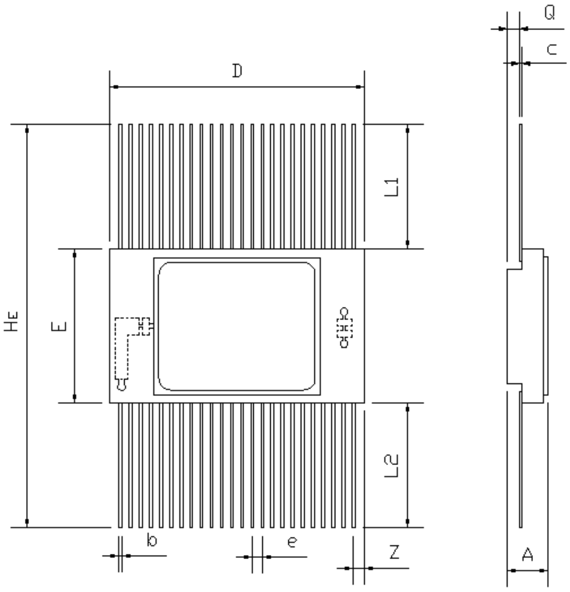


Figure 8-1 FP48 package specifications

Table 8-1 size symbol list

Symbol	Value（unit：mm）		
	Min	Normal	Max
A	——	——	3.40
b	0.20	——	0.51
c	0.07	——	0.22
e	——	0.635	——
D	15.675	——	16.075
E	9.452	——	9.852
L1	1.924	——	8.024
L2	1.924	——	8.024
H_E	13.70	——	25.50
Q	0.13	——	0.55
Z	——	——	1.27

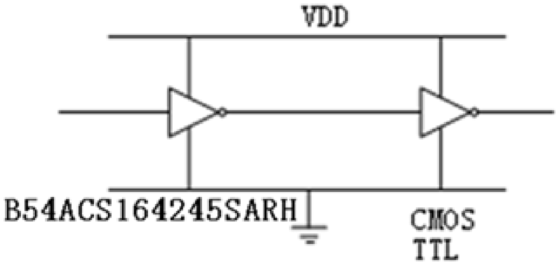
9. Appendix I Typical Application Example

The 16-bit wide B54ACS164245SARH Multipurpose transceiver is designed to perform multiple functions including: asynchronous two-way communication, Schmitt input buffering, voltage translation, cold sparing.

The B54ACS164245SARH enables system designers to interface 3.3 volt CMOS compatible components with 5 volt CMOS components. For voltage translation, the A port interfaces with the 3.3 volt bus; the B port interfaces with the 5 volt bus. The direction control (DIRx) controls the direction of data flow. The output enable ($\overline{\text{OE}}$x) overrides the direction control and disables both ports. These signals can be driven from either port A or B. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver.

9.1 B54ACS164245SARH drivers CMOS or TTL

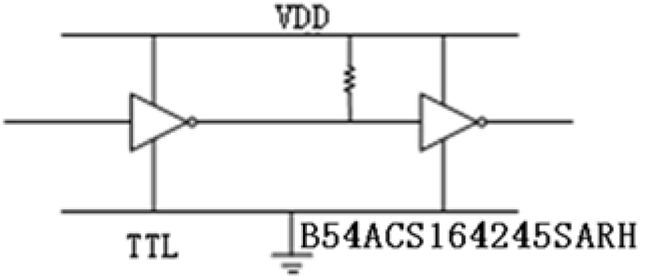
The B54ACS164245SARH is standard-logic product. The output pins can be connected to CMOS or TTL devices input pins directly when under the same supply voltage, as is shown in Appendix figure 1-1.



Appendix figure 1-1 B54ACS164245SARH driver CMOS and TTL

9.2 TTL drivers B54ACS164245SARH

The B54ACS164245SARH can be connected to CMOS or TTL devices as shown in Appendix figure 1-2.



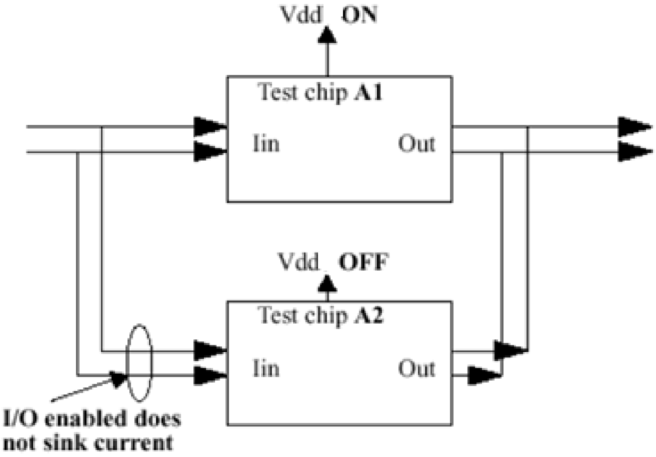
Appendix figure 1-2 TTL driver B54ACS164245SARH

If the supply voltage is 3.3V,the output voltage of TTL device $V_{OH}\geqslant 2.4V$,$V_{OL}\leqslant 0.4V$.The output pins of TTL device can be connected to B54ACS164245SARH input pins directly.

If the supply voltage is 5V, the output voltage of TTL device $V_{OH}\geqslant 2.4V$,$V_{OL}\leqslant 0.4V$.The input voltage of B54ACS164245SARH should content $V_{IH}\geqslant 3.5V$，$V_{IL}\leqslant 1.5V$.In that case, about 4.7kΩ pull-up resistor can be placed between output pin of TTL device and power, as shown in Appendix figure 1-2.

9.3 Utilizing the B54ACS164245SARH as Cold-Sparing Buffer

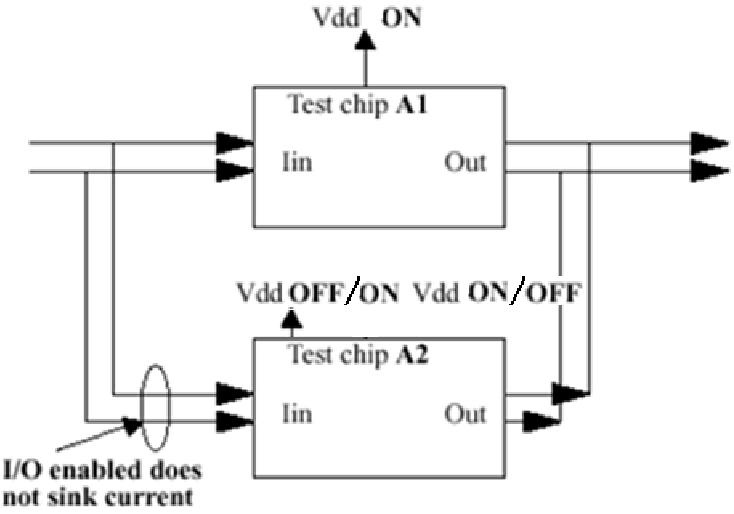
The inputs and outputs of the B54ACS164245SARH, while no power is being supplied to the device, can be tied to an active bus while remaining in a high impedance state. With V_{DD} equal to zero volts, the B54ACS164245SARH outputs and inputs present a minimum impedance of 1MΩ making it ideal for cold-sparing applications. The “cold spare” application is shown Appendix figure 1-3.



Appendix figure 1-3 “Cold spare” Application

9.4 Utilizing the B54ACS164245SARH as Warm-Sparing Buffer

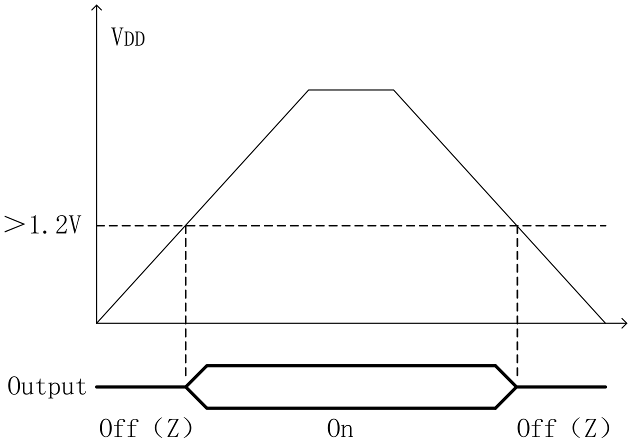
The inputs and outputs of the B54ACS164245SARH, while one power is being supplied to the device, the other one is off, can be tied to an active bus while remaining in a high impedance state. The B54ACS164245SARH outputs and inputs present a minimum impedance of 1MΩ making it ideal for warm-sparing applications. The “warm spare” application is shown in Appendix figure 1-4.



Appendix figure 1-4 “Warm spare” Application

9.5 Power Up

PU3S circuitry disables the logic device outputs at power-supply range from 0 V to 1.2V, regardless of the state of the output enable pin. The output enable pin (OE) must be tied high (to V_{DD}) through an external pull-up resistor ,ensures valid output levels during power up and ensures the valid high-impedance state during power down. **The power-up and power-down ramp rates also affect the internal circuitry, but a ramp rate faster than 200us/V is not recommended**. Shown in Appendix figure 1-5.



Appendix figure 1-5 Implementation PU3S Circuit

10. Appendix II Notice

(1) For proper operation, connect power to all V_{DD} pins and ground all V_{SS} pins (i.e., no floating V_{DD} or V_{SS} input pins). By virtue of the B54ACS164245SARH warm spare feature, power supplies V_{DD1} and V_{DD2} may be applied to the device in any order. To ensure the device is in cold spare mode, both supplies, V_{DD1} and V_{DD2} must be equal to V_{SS} +/- 0.3V. Warm spare operation is in effect when one power supply is >1V and the other power supply is equal to V_{SS} +/- 0.3V. If V_{DD1} has a power on ramp longer than 1 second, then V_{DD2} should be powered on first to ensure proper control of DIRx and OEx. During normal operation of the part, after power-up, ensure $V_{DD1}>V_{DD2}$.

(2) PU3S circuitry disables the logic device outputs at power-supply range from 0 V to 1.2V. The power-up and power-down ramp rates should be faster than 200us/V.

(3) It is recommended that all unused inputs be tied to V_{SS} through a 1KΩ to 10KΩ resistor.

(4) It is recommended that all outputs which in high-impedance state should be tied to V_{SS} through a 1KΩ to 10KΩ resistor.

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