Ver 1.1

Radiation-Hardened LVDS Serializer

Datasheet

Part Number：B54LVDS217ARH

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Page of Revise Control

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1.0	03.24.2018	——	——	
1.1	10.09.2018	6.2	Advance Absolute Maximum ratings information	

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1. Features

- 15 to 75 MHz shift clock support
- Low power consumption
- Power-down mode <216μW (max)
- Cold sparing all pins
- Narrow bus reduces cable size and cost
- Up to 1.575 Gbps throughput
- Up to 197 Megabytes/sec bandwidth
- 325 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge strobe
- Packaging: 48-lead flatpack (dual in-line)
- Compatible with ANSI/TIA/EIA 644-1996 LVDS Standard
- Operating temperature：-55℃~～+125℃
- ESD feature (human body model)：2000V
- Electrical latch up feature：200mA
- Total ionizing dose：≥100Krad(Si)
- Single event latch-up threshold：≥75MeV·cm2/mg

2. General Description

The B54LVDS217ARH Serializer converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. At a transmit clock frequency of 75MHz, 21 bits of TTL data are transmitted at a rate of 525 Mbps per LVDS data channel. Using a 75MHz clock, the data throughput is 1.575 Gbit/s (197Mbytes/sec).

The B54LVDS217ARH Serializer allows the use of wide, high speed TTL interfaces while reducing overall EMI and cable size.

All pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS}.

3. Function Block Diagram

B54LVDS217ARH function block diagram is shown in figure 1.

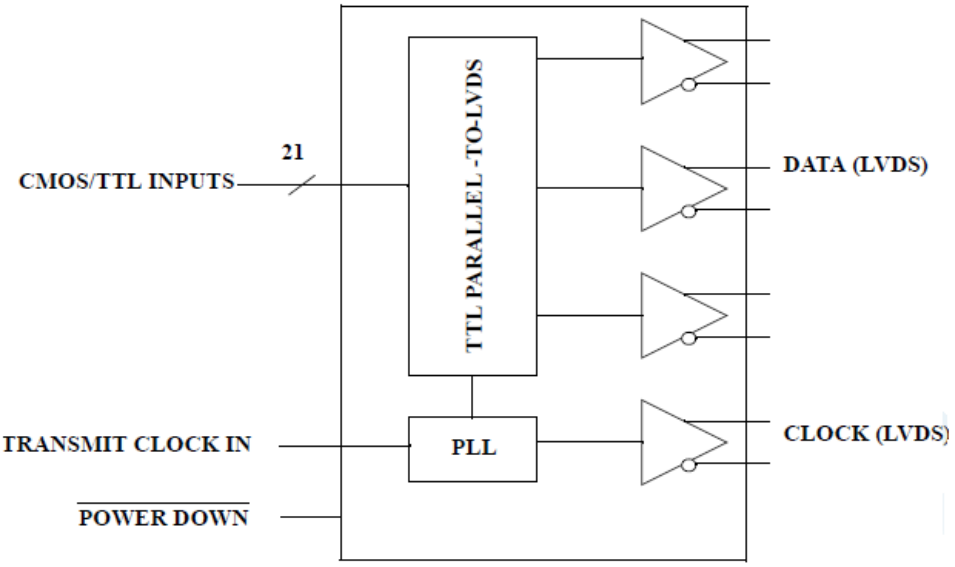


Figure1. B54LVDS217ARH Serializer Block Diagram

4. Packages and Pin Description Descriptions

The provided package is: FP48

B54LVDS0217ARH - pin configuration is shown in Figure 2.

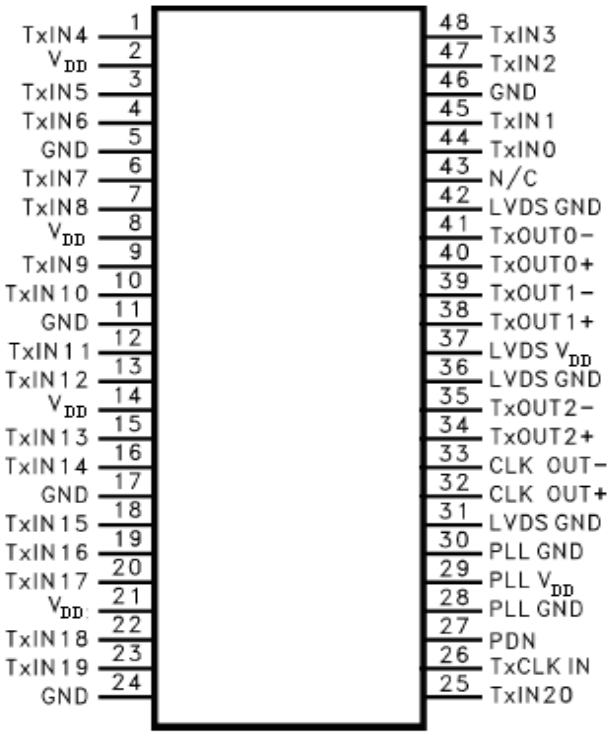


Figure2. B54LVDS217ARH Pinout

Table 1 B54LVDS217ARH Pin Function Descriptions

Name	I/O	No	Description
TxIN	I	21	TTL level input
TxOUT+	O	3	Positive LVDS differential data output
TxOUT-	O	3	Negative LVDS differential data output
TxCLK IN	I	1	TTL level clock input. The rising edge acts as data strobe. Pin name TxCLK IN
CLKOUT+	O	1	Positive LVDS differential clock output
CLK OUT-	O	1	Negative LVDS differential clock output
PDN	I	1	TTL level input. Assertion (low input) TRISTATEs the clock and data outputs, ensuring low current at power down.
VDD	I	4	Power supply pins for TTL inputs and logic
GND	I	5	Ground pins for TTL inputs and logic
PLL VDD	I	1	Power supply pins for PLL
PLL GND	I	2	Ground pins for PPL
LVDS VDD	I	1	Power supply pin for LVDS output
LVDS GND	I	3	Ground pins for LVDS outputs

5. Pin List

Table 2 B54LVDS217ARH Pin list

Pin No	Name	Dir	Description	Pin No	Name	Dir	Description
1	TxIN4	I	Data Input 4	25	TxIN20	I	Data Input 20
2	VDD	P	Digital power supply	26	CLK_IN	I	clock input
3	TxIN5	I	Data Input 5	27	PDN	I	Power down(low active)
4	TxIN6	I	Data Input 6	28	PLL GND	P	PLL ground supply
5	GND	P	Digital ground supply	29	PLL VDD	P	PLL power supply
6	TxIN7	I	Data Input 7	30	PLL GND	P	PLL ground supply
7	TxIN8	I	Data Input 8	31	LVDS GND	P	LVDS ground supply

8	VDD	P	Digital power supply	32	CLK_OUT+	O	Positive LVDS clock output
9	TxIN9	I	Data Input 9	33	CLK_OUT-	O	Negative LVDS clock output
10	TxIN10	I	Data Input 10	34	TxOUT2+	O	Positive LVDS data output 2
11	GND	P	Digital ground supply	35	TxOUT2-	O	Negative LVDS data output 2
12	TxIN11	I	Data Input 11	36	LVDS GND	P	LVDS ground supply
13	TxIN12	I	Data Input 12	37	LVDS VDD	P	LVDS power supply
14	VDD	P	Digital power supply	38	TxOUT1+	O	Positive LVDS data output 1
15	TxIN13	I	Data Input 13	39	TxOUT1-	O	Negative LVDS data output 1
16	TxIN14	I	Data Input 14	40	TxOUT0+	O	Positive LVDS data output 0
17	GND	P	Digital ground supply	41	TxOUT0-	O	Negative LVDS data output 0
18	TxIN15	I	Data Input 15	42	LVDS GND	P	LVDS ground supply
19	TxIN16	I	Data Input 16	43	NC		No connection
20	TxIN17	I	Data Input 17	44	TxIN0	I	Data Input 0
21	VDD	P	Digital power supply	45	TxIN1	I	Data Input 1
22	TxIN18	I	Data Input 18	46	GND	P	Digital ground supply
23	TxIN19	I	Data Input 19	47	TxIN2	I	Data Input 2
24	GND	P	Digital ground	48	TxIN3	I	Data Input 3

6. Detailed Description

6.1 Storage Condition

Packaged product should be stored in the ventilate warehouse with ambient temperature 15℃～25℃ and relative humidity less than 65%. There should be no acid , alkali or other radiant gas in the environment.

6.2 Absolute Maximum Ratings

a) Supply voltage range to ground potential（V_{DD}）： -0.3V ～4.0V

b) DC input voltage range（V_{in}）： -0.3V ～（V_{DD}+0.3V）

c) Storage temperature（T_{stg}）： -65℃～ 150℃

d) Power dissipation（P_D）： 2W

e) Lead temperature（T_h, 10s）：260℃

f) Thermal resistance（$R_{th(J-C)}$）：10℃/W

g) Junction temperature（T_J）：+150℃

h) DC input current（ I_I）：±10mA

NOTES: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.

6.3 Recommended Operation Conditions

a) Supply voltage relative to ground(VDD)：3.0 V to 3.6 V

b) DC input voltage, VIN and PDN： 0 to VDD

c) Case temperature range ：-55℃ to +125℃

7. Specifications

All electrical characteristics are shown in table 3.

Table3 B54LVDS217ARH electrical characteristics

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION (VDD = 3.0V±0.3V; -55℃< TC < +125℃)	LIMITS		UNIT
			MIN	MAX	
VIH	High level input voltage		2.0	VDD	V
VIL	Low level input voltage		GND	0.8	V
IIH	High-level input current	VIN = 3.6V; VDD = 3.6V	-10	+10	μA
IIL	Low-level input current	VIN = 0V; VDD = 3.6V	-10	+10	μA
VCL	Input clamp voltage	ICL = -18mA		-1.5	V
ICS	Cold Spare Leakage current	VIN = 3.6V; VDD = VSS	-20	+20	μA
VOD	Differential Output Voltage	RL = 100Ω	250	400	mV

ΔVOD	Change in VOD between complimentary output states	RL = 100Ω		35	mV
VOS	Offset Voltage	RL = 100Ω	1.120	1.410	V
ΔVOS	Change in VOS between complimentary output states	RL = 100Ω		35	mV
IOZ	Output Three-State Current	PWR DWN = 0V VOUT = 0V or VDD	-10	+10	μA
ICSOUT	Cold Spare Leakage Current	VIN=3.6V, VDD = VSS	-20	+20	μA
IOS	Output Short Circuit Current	VOUT+ or VOUT- = 0V		5mA	mA
ICCL	Transmitter supply current with loads	RL = 100Ω,CL = 5pF, f = 50MHz		65.0	mA
ICCZ	Power down current	DIN = VSS ,PDN = 0V, f = 0Hz		60.0	μA

AC SWITCHING CHARACTERISTICS

SYMBOL	**PARAMETER**	**CONDITION** (V_{DD} = 3.0V±0.3V, T_A = -55℃to +125℃)	MIN	MAX	**UNIT**
LLHT	LVDS Low-to-High Transition Time	Figure 3		1.5	ns
LHLT	LVDS High-to-Low Transition Time	Figure 3		1.5	ns
TPPos0[a]	Transmitter Output Pulse Position for Bit 0	V_{DD} =3.0V ,f=75MHz Figure9	-0.22	0.23	ns
TPPos1[a]	Transmitter Output Pulse Position for Bit 1		1.68	2.13	ns
TPPos2[a]	Transmitter Output Pulse Position for Bit 2		3.59	4.04	ns
TPPos3[a]	Transmitter Output Pulse Position for Bit3		5.49	5.94	ns
TPPos4[a]	Transmitter Output Pulse Position for Bit 4		7.40	7.85	ns
TPPos5[a]	Transmitter Output Pulse Position for Bit 5		9.30	9.75	ns

TPPos6 [a]	Transmitter Output Pulse Position for Bit 6		11.21	11.66	ns
TCCS	Channel to Channel skew	V_{DD} =3.0V, Figure10		0.45	ns
TCIP[b]	TxCLK IN Period	Figure5	13.3	66.7	ns
TCIH[b]	TxCLK IN High Time	Figure5	0.35 t_{CIP}	0.65 t_{CIP}	ns
TCIL[b]	TxCLK IN Low Time	Figure5	0.35 t_{CIP}	0.65 t_{CIP}	ns
TSTC[b]	TxIN Setup to TxCLK IN	f =15MHz ,Figure5	1.0		ns
		f =75MHz ,Figure5	0.5		
THTC[b]	TxIN Hold to TxCLK IN	f =15MHz ,Figure5	0.7		ns
		f =75MHz ,Figure5	0.5		
TCCD	TxCLK IN to TxCLK OUT Delay	V_{DD} =3.0V, Figure6	0.5	2.5	ns
TPLLS	Transmitter Phase Lock Loop Set	V_{DD} =3.0V, Figure7		10	ms
TPDD	Transmitter Powerdown Delay	V_{DD} =3.0V, Figure8		100	ns

a：Guaranteed by design.

b：Guaranteed by characterization..

AC Timing Diagrams

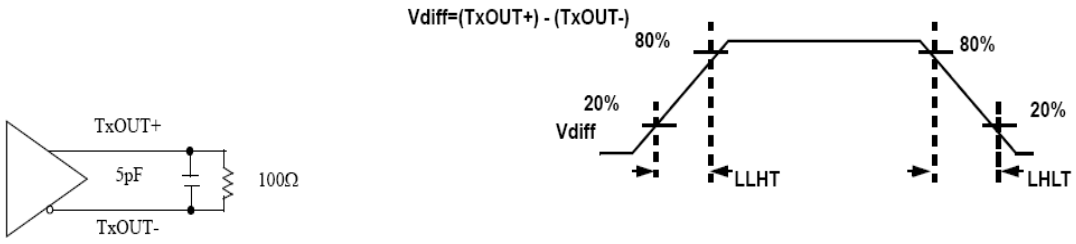


Figure3. B54LVDS217ARH Output Load and Transition Times

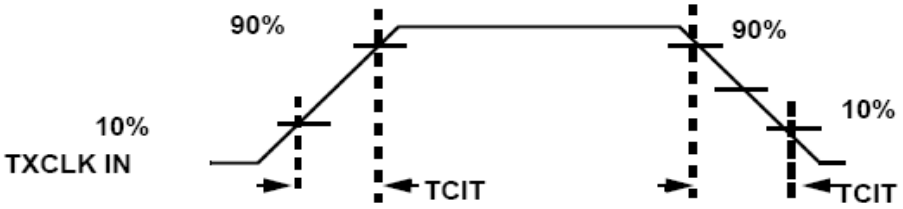


Figure4. B54LVDS217ARH Input Clock Transition Time

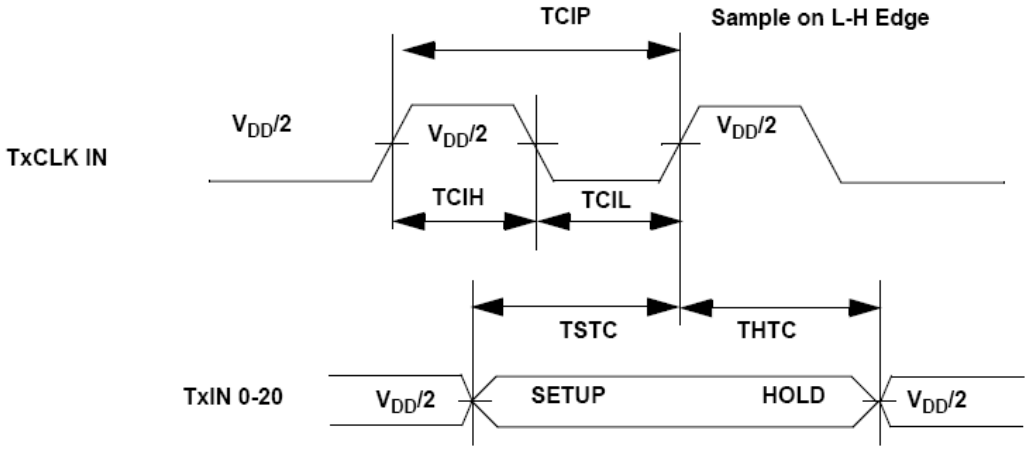


Figure5. B54LVDS217ARH Setup/Hold and High/Low Times

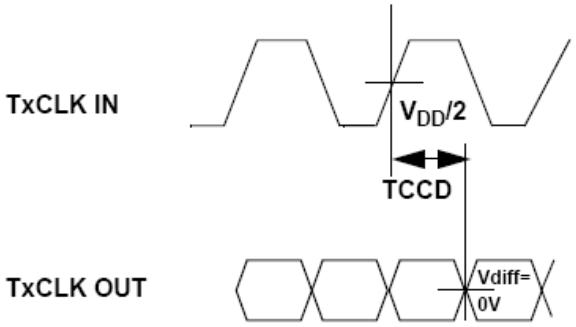


Figure6. B54LVDS217ARH Clock-to-Clock Out Delay

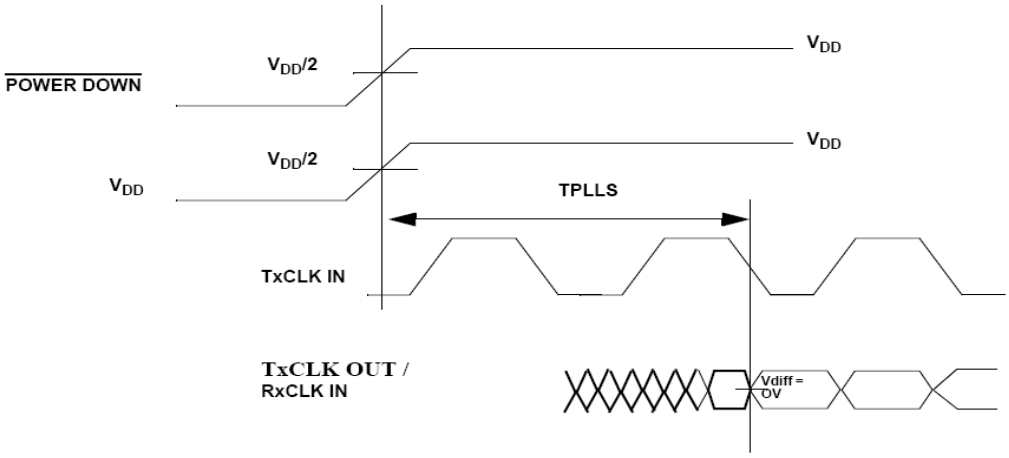


Figure7. B54LVDS217ARH Phase Lock Loop Set Time

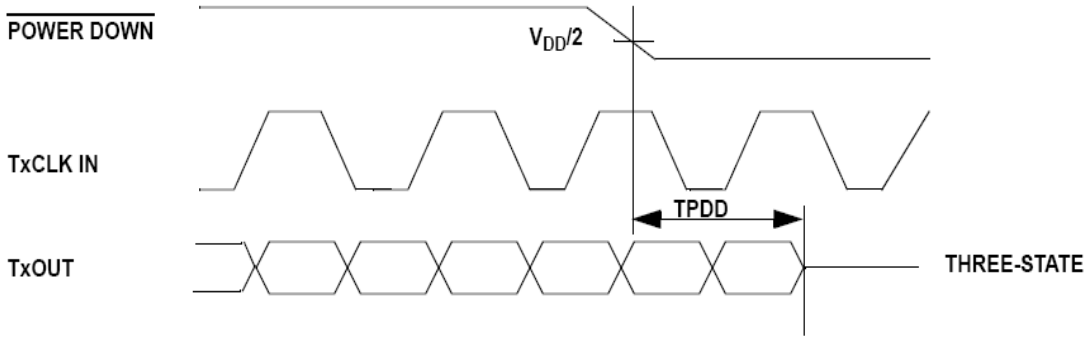


Figure8. B54LVDS217ARH Transmitter Powerdown Delay

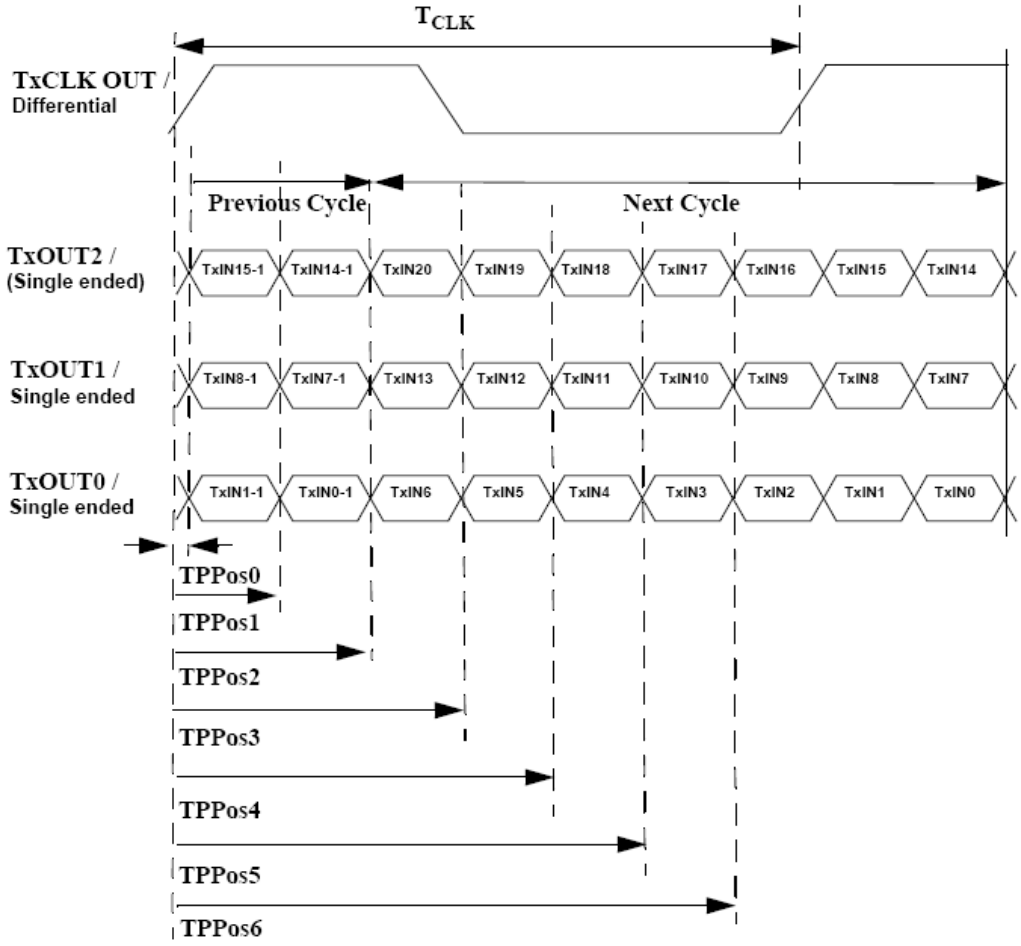


Figure9. B54LVDS217ARH Output Pulse Position Measurement

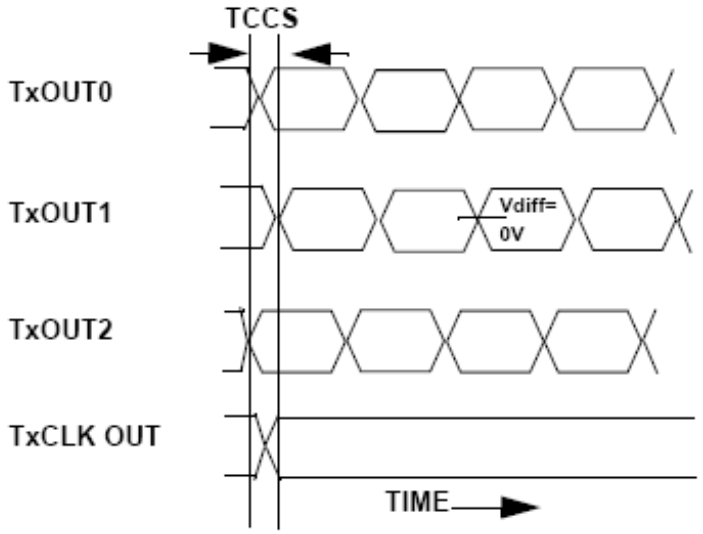


Figure10. B54LVDS217ARH Channel-to-Channel Skew

8. Package Specifications

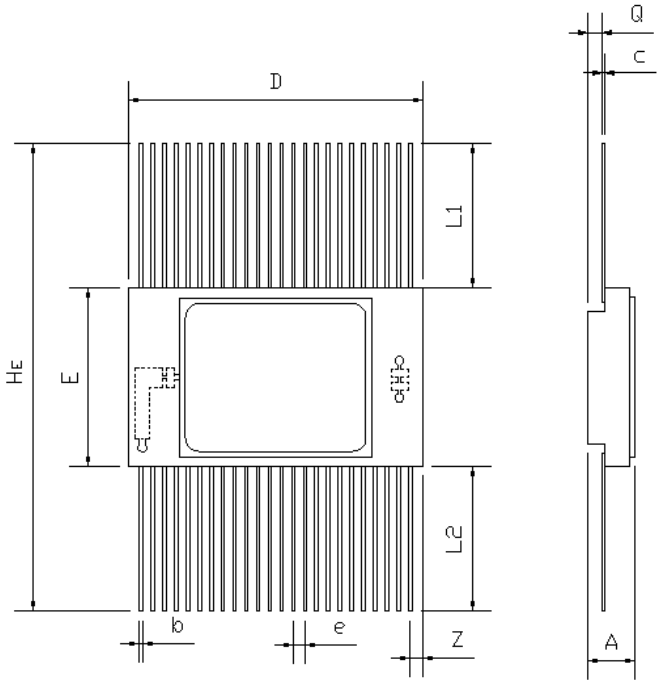


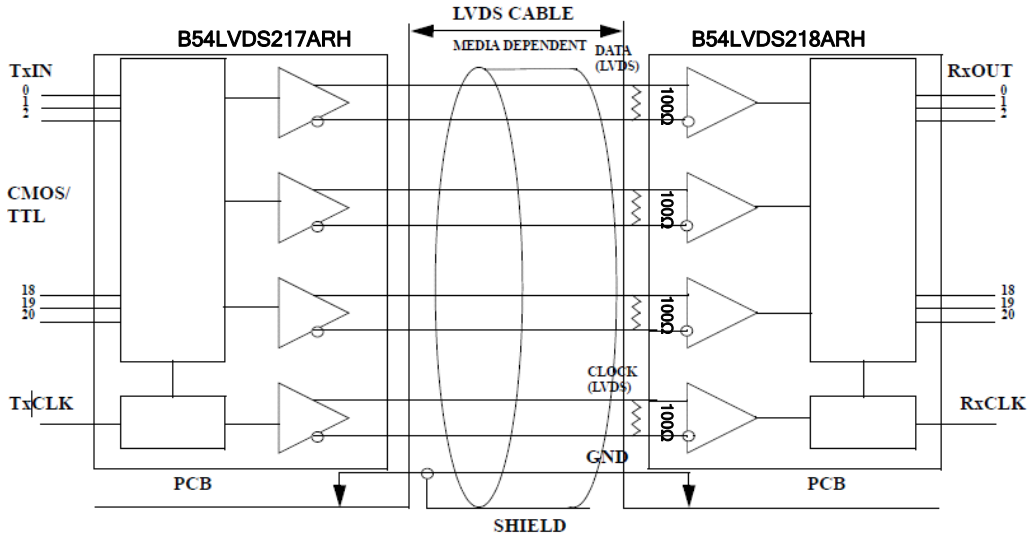
Figure11. 48-pin Ceramic Flatpack

Table 4 Package Size

Symbol	Value（unit：mm）		
	Min	Normal	Max
A	——	——	3.40
b	0.20	——	0.51
c	0.07	——	0.22
e	——	0.635	——
D	15.675	——	16.075
E	9.452	——	9.852
L1	1.924	——	8.024
L2	1.924	——	8.024
H_E	13.70	——	25.50
Q	0.13	——	0.55
Z	——	——	1.27

9. Appendix I Application Information

Typical Application



Appendix figure I-1. Typical Application

The CHANNEL LINK devices (B54LVDS217ARH and B54LVDS218ARH) are intended to be used in a wide variety of data transmission applications. The use of serialized LVDS data lines in these applications allows for efficient signal transmission over a narrow bus width, thereby reducing cost, power, and space. Depending upon the application the interconnecting media may vary. For example, for lower data rate (clock rate) and shorter cable lengths (< 2m), the media electrical performance is less critical. For higher speed/long distance applications the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). Additional applications information can be found in the following Interface Application Notes:

- **Cables**

A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is also recommended that cable skew remain below 100ps (@ ≥60 MHz clock rate) to maintain a sufficient data

sampling window at the receiver. Some of the more commonly used cable types for point-to-point applications include flat ribbon, flex, twisted pair and Twin-Coax.

All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair.

- **Termination**

Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single 100Ω resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance (90Ω to 120Ω typical) of the cable. Figure I-1 shows an example. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

- **Unused inputs**

All unused inputs at the TxIN inputs of the driver must then be tied to VSS.

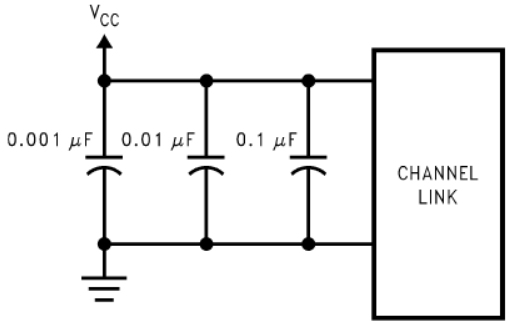
- **Cold Spare**

All pins have Cold Spare buffers. These buffers will be high impedance when VDD is tied to VSS. But the CMOS outputs (pin 3,5,11,and 14) should not be used as cold spared pins when VDD is not tied to VSS.

- **Bypassing capacitor**

Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each V_{DD} and the ground plane(s) are recommended. The three capacitor values are 0.1 μF, 0.01 μF and 0.001 μF. An example is shown in Figure I-2. The designer should employ wide traces for power and ground and ensure each

capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL V_{CC} should receive the most filtering/bypassing. Next would be the LVDS V_{CC} pins and finally the logic V_{CC} pins



Appendix figure I-2. B54LVDS217ARH Decoupling Configuration

- **Clock jitter**

The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 75 MHz clock has a period of 13.33 ns which results in a data bit width of 1.90 ns. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal, especially low frequency component less than 1MHz. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel to channel skew and interconnect skew as a part of the overall jitter/skew budget.

10. Appendix II Replaced Product

Appendix table. II -1

Device Type	Substituted Device Type
B54LVDS217ARH	Aeroflex UT54LVDS217

Service & Support：

Address:No.2 Siyingmen N. Road. Donggaodi. Fengtai District. Beijing,China.

Department：Department of international cooperation

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Zip code：100076