Ver 1.0

1553B BUS CONTROLLER

Datasheet

Part Number：B61580RH

中国航天 CASC
北京微电子技术研究所
Beijing Microelectronics Technology Institute

Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	2018.3		Initial release.	

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TABLE OF CONTENTS

1. Features

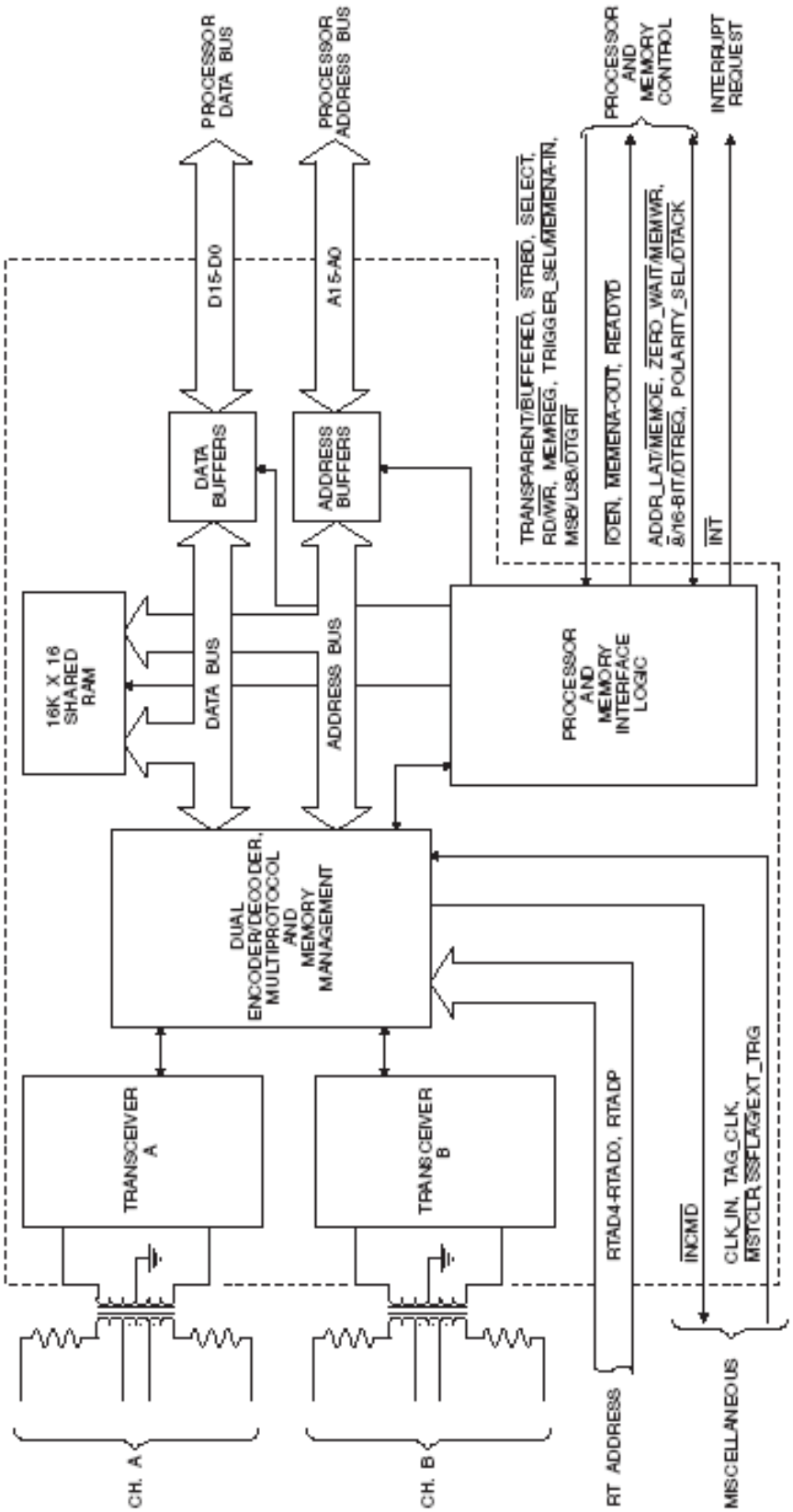
- Radiation Tolerant & Radiation
- Hardened Versions
- Fully Integrated 1553 Terminal
- Flexible Processor Interface
- 4K x 16 Internal RAM
- Automatic BC Retries
- Programmable BC Gap Times
- BC Frame Auto-Repeat
- Intelligent RT Data Buffering
- Ceramic Package
- Multiple Ordering Options;
- +5V (Only)
- +5V(Only,with Transmit Inhibits)

2. General Description

BMTI's B61580RH provides a complete integrated BC/RT/MT interface between a host processor and a MIL-STD-1553 bus. BMTI can supply the B61580RH with space level screening. This entails enhancements in the areas of element evaluation and screening procedures for active and passive elements, as well as the manufacturing and screening processes used in producing the terminals.

The B61580RH integrates dual transceiver, protocol, memory management and processor interface logic, and 4K words of RAM in the choice of 70-pin DIP packages. Transceiverless versions may be used with an external electrical or fiber optic transceiver.

3. Block Diagram


PROCESSOR DATA BUS
PROCESSOR ADDRESS BUS
PROCESSOR AND MEMORY CONTROL
INTERRUPT REQUEST
D15-D0
A15-A0
TRANSPARENT/BUFFERED, STRBD, SELECT, RD/WR, MEMREG, TRIGGER_SEL/MEMENA-IN, MSB/LSB/DTGRT
DATA BUFFERS
ADDRESS BUFFERS
IOEN, MEMENA-OUT, READYD
ADDR_LAT/MEMOE, ZERO_WAIT/MEMWR, 8/16-BIT/DTREQ, POLARITY_SEL/DTACK
INT
16K X 16 SHARED RAM
DATA BUS
ADDRESS BUS
PROCESSOR AND MEMORY INTERFACE LOGIC
DUAL ENCODER/DECODER, MULTIPROTOCOL AND MEMORY MANAGEMENT
TRANSCEIVER A
TRANSCEIVER B
RTAD4-RTAD0, RTADP
INCMD
CLK_IN, TAG_CLK, MSTCLR, SSFLAG/EXT_TRIG
CH. A
CH. B
RT ADDRESS
MISCELLANEOUS

4. Pin Description

B61580RH PIN DESCRIPTION			
PIN	**NAME**	**PIN**	**NAME**
1	*TX / RX – A*	36	TX_INH_B
2	$\overline{TX / RX - A}$	37	GNDB
3	$\overline{\text{SELECT}}$	38	+5VB
4	$\overline{STRBD}$	39	RTAD0
5	MEM / $\overline{\text{REG}}$	40	RTAD1
6	RD / $\overline{\text{WR}}$	41	RTAD2
7	$\overline{MSTCLR}$	42	RTAD3
8	A15	43	RTAD4
9	A14	44	RTADP
10	A13	45	$\overline{INCMD}$
11	A12	46	D0
12	A11	47	D1
13	A10	48	D2
14	A9	49	D3
15	A8	50	D4
16	A7	51	D5
17	A6	52	D6
18	GND	53	D7
19	CLOCK	54	+5V Logic
20	A5	55	D8
21	A4	56	D9
22	A3	57	D10
23	A2	58	D11
24	A1	59	D12
25	A0	60	D13
26	$\overline{\text{DTGRT}}$ / MSB / $\overline{\text{LSB}}$	61	D14
27	$\overline{SSFLAG}$ / *EXT _ TRIG*	62	D15
28	$\overline{MEMENA\_OUT}$	63	TAG _ CLK
29	$\overline{\text{MEMOE}}$/ADDR _ LAT	64	*TRANSPARENT* / $\overline{BUFFERED}$
30	$\overline{MEMWR}$ / $\overline{ZERO\_WAIT}$	65	$\overline{INT}$
31	$\overline{DTREQ}$ / 16 / $\overline{8}$	66	$\overline{\text{READYD}}$
32	$\overline{\text{DTACK}}$ / POLARITY _ SEL	67	$\overline{IOEN}$
33	$\overline{\text{MEMENA}}$ / TRIGGER _ SEL	68	+5VA
34	*TX / RX – B*	69	GNDA

35	$\overline{TX}$ / $\overline{RX}$ – B	70	TX_INH_A

5. Pin Configurations

See Appendix 1.

6. Product Description

BMTI's Sp'ACE II series of integrated BC/RT/MT hybrids provide a complete, flexible interface between a microprocessor and a MIL-STD-1553A, B Notice 2, McAir, or STANAG 3838 bus, implementing Bus Controller, Remote Terminal (RT) and Monitor Terminal (MT) modes. Packaged in a single 1.9 square inch 70-pin DIP, surface mountable Flat Pack or Gull Lead, the Sp'ACE II series contains dual low-power transceivers and encoder/decoders, complete BC/RT/MT multiprotocol logic, memory management and interrupt logic, 4K X 16 of shared static RAM and a direct, buffered interface to a host processor bus.

The B61580RH contains internal address latches and bidirectional data buffers to provide a direct interface to a host processor bus. The B61580RH may be interfaced directly to both 16-bit and 8-bit microprocessors (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode) in a buffered shared RAM configuration. In addition, the Sp'ACE II may connect to a 16-bit processor bus via a Direct Memory Access (DMA) interface. The B61580RH includes 4K words of buffered RAM. Alternatively, the Sp'ACE II may be interfaced to as much as 64k words of external RAM in either the shared RAM or DMA configurations.

The Sp'ACE II RT mode is multiprotocol, supporting MIL-STD-1553A, MIL-STD-1553B Notice 2, and STANAG 3838 (including EFAbus).

The memory management scheme for RT mode provides an option for separation of broadcast data, in compliance with 1553B Notice 2. Both double buffer and circular buffer options are programmable by subaddress. These features serve to ensure data consistency and to off-load the host processor for bulk data transfer applications.

The Sp'ACE II series implements three monitor modes: a word monitor, a selective message monitor, and a combined RT/selective monitor.

Other features include options for automatic retries and programmable intermessage gap for BC mode, an internal Time Tag Register, an Interrupt Status Register and internal command illegalization for RT mode.

FUNCTIONAL OVERVIEW

TRANSCEIVERS

For the +5 V front end, the B61580RH uses low-power bipolar analog monolithic and thin-film hybrid technology. The transceiver requires +5 V only and includes voltage source transmitters. The B61580RH utilizes low-power CMOS analog monolithic and thin film hybrid technology as well but requires +5V only. The voltage source transmitters provide superior line driving capability for long cables and heavy amounts of bus loading.

The receiver sections of the B61580RH are fully compliant with MIL-STD-1553B in terms of front end overvoltage protection, threshold, common mode rejection, and word error rate. In addition, the receiver filters have been designed for optimal operation with the M-Rad chip's Manchester II decoders.

M-RAD DIGITAL MONOLITHIC

The M-Rad digital monolithic represents the cornerstone element of the B61580RH Sp'ACE II family of terminals. The M-Rad chip is actually a radiation hardened version of DDC's M' (M-prime) monolithic which is the key building block behind BMTI's non-radiation hardened B61580 ACE series of terminals. As such, the M-Rad possesses all the enhanced hardware and software features which have made the B61580 ACE the industry standard 1553 interface component.

The M-Rad chip consists of a dual encoder/decoder; complete protocol for Bus Controller (BC), 1553A/B/McAir Remote Terminal (RT), and Monitor (MT) modes; memory management and interrupt logic; a flexible, buffered interface to a host processor bus and optional external RAM. Reference the region within the dotted line of FIGURE 1. Besides realizing all the protocol, memory management, and interface functions of the earlier AIM-HY series, the M-Rad chip includes a large number of enhancements to facilitate hardware and software design, and to further off-load the 1553 terminal's host processor.

DECODERS

The default mode of operation for the B61580RH BC/RT/MT requires a 16 MHz clock input. If needed, a software programmable option allows the device to be

operated from a 12 MHz clock input. Most current 1553 decoders sample using a 10 MHz or 12 MHz clock. In the 16 MHz mode (or 12 MHz), the decoders sample using both clock edges; this provides a sampling rate of 32 MHz or 24 MHz. The faster sampling rate for the M-Rad's Manchester II decoders provides superior performance in terms of bit error rate and zero-crossing distortion tolerance.

For interfacing to fiber optic transceivers for MIL-STD-1773 applications, a transceiverless version of the Sp'ACE II can be used. These versions provide a register programmable option for a direct interface to the single-ended outputs of a fiber optic receiver. No external logic is needed.

TIME TAGGING

The Sp'ACE II includes an internal read/writable Time Tag Register. This register is a CPU read/writable 16-bit counter with a programmable resolution of either 2, 4, 8, 16, 32, or 64 μs per LSB. Also, the Time Tag Register may be clocked from an external oscillator. Another option allows software controlled incrementing of the Time Tag Register. This supports self-test for the Time Tag Register. For each message processed, the value of the Time Tag register is loaded into the second location of the respective descriptor stack entry ("TIME TAG WORD") for both BC and RT modes.

Additional provided options will: clear the Time Tag Register following a Synchronize (without data) mode command or load the Time Tag Register following a Synchronize (with data) mode command; enable an interrupt request and a bit setting in the Interrupt Status Register when the Time Tag Register rolls over from FFFF to 0000. Assuming the Time Tag Register is not loaded or reset, this will occur at approximately 4 second time intervals, for 64 μs/LSB resolution, down to 131 ms intervals, for 2 μs/LSB resolution.

Another programmable option for RT mode is the automatic clearing of the Service Request Status Word bit following the B61580RH's response to a Transmit Vector Word mode command.

INTERRUPTS

The Sp'ACE II series components provide many programmable options for interrupt generation and handling. The interrupt output pin INT has three software programmable modes of operation: a pulse, a level output cleared under software control, or a level output automatically cleared following a read of the Interrupt Status Register. Individual interrupts are enabled by the Interrupt Mask Register. The host

processor may easily determine the cause of the interrupt by using the Interrupt Status Register. The Interrupt Status Register provides the current state of the interrupt conditions. The Interrupt Status Register may be updated in two ways. In the standard interrupt handling mode, a particular bit in the Interrupt Status Register will be updated only if the condition exists and the corresponding bit in the Interrupt Mask Register is enabled. In the enhanced interrupt handling mode, a particular bit in the Interrupt Status Register will be updated if the condition exists regardless of the contents of the corresponding Interrupt Mask Register bit. In any case, the respective Interrupt Mask Register bit enables an interrupt for a particular condition.

RADIATION TOLERANCE

The B61580RH combines analog bipolar/BiCMOS transceivers with logic and RAM fabricated to provide radiation survivability.

To summarize,

B61580RH has a total gamma dose immunity of 100-K Rad and providing a soft error rate of 1.91 x 10-6 errors/device-day on geosychronous orbit(GEO).The hybrids has a Latchup immunity of a LET threshold of 91.9 MeV-cm2/mg.

TABLE 1 B61580RH RADIATION SPECIFICATIONS

	TOTAL DOSE	SINGLE EVENT UPSET	SINGLE EVENT LATCHUP
B61580RH	>100Rad	1.91 x 10^{-6} errors/device-day (GEO)	>91.9 MeV-cm^2/mg

HIGH-REL SCREENING

DDC is committed to the design and manufacture of hybrids and transformers with enhanced processing and screening for spaceborne applications and other systems requiring the highest levels of reliability. These platforms include launch vehicles, satellites .

DDC has tailored its design methodologies to optimize the fabrication of space level hybrids. The intent of the design guidelines is to minimize the number of die and wirebonds, minimize the number of substrate layers, and maximize the space between components. BMTI's space grade products combine analog CMOS and radiation hardened technology to provide various levels of radiation tolerance.

The B61580RH is packaged in a 70-pin ceramic package. In contrast to Kovar (metal) packages, the use of ceramic eliminates the hermeticity problems associated

with the glass beads used in the metal packages. In addition, ceramic packages provide more rigid leads, better thermal properties, easier wirebonding, and lower weight.

The production of the space level hybrids can entail enhanced screening steps beyond BMTI's standard flow. This includes Condition A visual inspection, SEM analysis, and element evaluation for all integrated circuit die. For the hybrids, additional screening includes Particle Impact Noise Detection (PIND), 320-hour burn-in (standard on this device), 100% non-destructive wirebond pull (standard on this device), X-ray analysis, as well as Destructive Physical Analysis (DPA) testing, extended temperature cycling for QCI testing, and a moisture content limit of 5000 PPM.

ADDRESSING, INTERNAL REGISTERS, AND MEMORY MANAGEMENT

The software interface of the B61580RH to the host processor consists of 17 internal operational registers for normal operation, an additional 8 test registers, plus 64K X 16 of shared memory address space. The B61580RH's 4K X 16 of internal RAM resides in this address space. Reference TABLE 2 .

Definition of the address mapping and accessibility for the Sp'ACE II's 17 nontest registers, and the test registers, is as follows:

Interrupt Mask Register:

Used to enable and disable interrupt requests for various conditions.

Configuration Registers #1 and #2:

Used to select the B61580RH's mode of operation, and for software control of RT Status Word bits, Active Memory Area, BC Stop-on-Error, RT Memory Management mode selection, and control of the Time Tag operation.

Start/Reset Register:

Used for "command" type functions, such as software reset, BC/MT Start, Interrupt Reset, Time Tag Reset, and Time Tag Register Test. The Start/Reset Register includes provisions for stopping the BC in its auto-repeat mode, either at the end of the current message or at the end of the current BC frame.

BC/RT Command Stack Pointer Register:

Allows the host CPU to determine the pointer location for the current or most recent message when the B61580RH is in BC or RT modes.

BC Control Word/RT Subaddress Control Word Register:

In BC mode, allows host access to the current or most recent BC Control Word. The BC Control Word contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. In RT mode, this register allows host access to the current or most recent Subaddress Control Word. The Subaddress Control Word is used to select the memory management scheme and enable interrupts for the current message. The read/write accessibility can be used as an aid for testing the Sp'ACE II hybrid.

Time Tag Register:

Maintains the value of a real-time clock.The resolution of this register is programmable from among 2, 4, 8, 16, 32, and 64 μs/LSB. The TAG_CLK input signal also may cause an external oscillator to clock the Time Tag Register. Start-of-Message (SOM) and End-of-Message (EOM) sequences in BC, RT, and Message Monitor modes cause a write of the current value of the Time Tag Register to the stack area of RAM.

Interrupt Status Register:

Mirrors the Interrupt Mask Register and contains a Master Interrupt bit. It allows the host processor to determine the cause of an interrupt request by means of a single READ operation.

Configuration Registers #3, #4, and #5:

Used to enable many of the B61580RH's advanced features. These include all the enhanced mode features; that is, all the functionality beyond that of the previous generation product. For BC mode, the enhanced mode features include the expanded BC Control Word and BC Block Status Word, additional Stop-On-Error and Stop-On-Status Set functions, frame auto-repeat, programmable intermessage gap times, automatic retries, expanded Status Word Masking, and the capability to generate interrupts following the completion of any selected message. For RT mode, the enhanced mode features include the expanded RT Block Status Word, the combined RT/Selective Message Monitor mode, internal wrapping of the RTFAIL output signal (from the M-Rad chip) to the RTFLAG RT Status Word bit, the double buffering scheme for individual receive (broadcast) subaddresses, and the alternate (fully software programmable) RT Status Word. For MT mode, use of the enhanced mode enables use of the Selective Message Monitor, the combined RT/Selective Monitor

modes, and the monitor triggering capability.

Data Stack Address Register:

Used to point to the current address location in shared RAM used for storing message words (second Command Words, Data Words, RT Status Words) in the Selective Word Monitor mode.

Frame Time Remaining Register:

Provides a read only indication of the time remaining in the current BC frame. The resolution of this register is 100μs/LSB.

Message Time Remaining Register:

Provides a read only indication of the time remaining before the start of the next message in a BC frame. The resolution of this register is 1 μs/LSB.

BC Frame/RT Last Command/MT Trigger Word Register:

In BC mode, it programs the BC frame time, for use in the frame auto-repeat mode. The resolution of this register is 100 μs/LSB, with a range of 6.55 seconds; in RT mode, this register stores the current (or most previous) 1553 Command Word processed by the Sp'ACE II RT; in the Word Monitor mode, this register specifies a 16-bit Trigger (Command) Word. The Trigger Word may be used to start or stop the monitor, or to generate interrupts.

Status Word Register and BIT Word Registers:

Provide read-only indications of the B61580RH's RT Status and BIT Words.

Test Mode Registers 0-7:

These registers may be used to facilitate production or maintenance testing of the Sp'ACE II and systems incorporating the Sp'ACE II hybrid.

TABLE 2 ADDRESS MAPPING

ADDRESS LINES						REGISTER DESCRIPRION
HEX	A4	A3	A2	A1	A0	
00	0	0	0	0	0	Interrupt Mask Register (RD/WR)
01	0	0	0	0	1	Configuration Register #1 (RD/WR)
02	0	0	0	1	0	Configuration Register #2 (RD/WR)
03	0	0	0	1	1	Start/Reset Register (WR)
03	0	0	0	1	1	BC/RT Command Stack Pointer Register (RD)
04	0	0	1	0	0	BC Control Word/RT Subaddress Control Word Register (RD/WR)

05	0	0	1	0	1	Time Tag Register (RD/WR)
06	0	0	1	1	0	Interrupt Status Register (RD)
07	0	0	1	1	1	Configuration Register #3 (RD/WR)
08	0	1	0	0	0	Configuration Register #4 (RD/WR)
09	0	1	0	0	1	Configuration Register #5 (RD/WR)
0A	0	1	0	1	0	Data Stack Address Register (RD/WR)
0B	0	1	0	1	1	BC Frame Time Remaining Register (RD/WR)
0C	0	1	1	0	0	BC Time Remaining to Next Message Register (RD/WR)
0D	0	1	1	0	1	BC Frame Time/RT Last Command/MT Trigger Word Register (RD/WR)
0E	0	1	1	1	0	RT Status Word Register (RD)
0F	0	1	1	1	1	RT BIT Word Register (RD)
10	1	0	0	0	0	Test Mode Register 0
•						
•						
17	1	0	1	1	1	Test Mode Register 7
18	1	1	0	0	0	reserved
•						
•						
1F	1	1	1	1	1	reserved

TABLE 3 Interrupt Mask Register (RD/WR 00H)

BIT	DESCRIPTION
15（MSB）	RESERVED
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HS FAIL
8	BC RETRY
7	RT ADDRESS PARITY ERROR

6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC/RT SELECTED MESSAGE
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0（LSB）	END OF MESSAGE

TABLE 4 Configuration Register #1 (RD/WR 01H)

BIT	BC FUNCTION (BITs11-0 ENHANCED MODE ONLY)	RT WITHOUT ALTERNATE STATUS	RT WITHALTERNATE STATUS	MONITOR FUNCTION
15	RT/BC-MT(logic 0)	(logic 1)	(logic 1)	(logic 0)
14	MT/BC-RT(logic 0)	(logic 0)	(logic 0)	(logic 1)
13	CURRENT AREA B/A	CURRENT AREA B/A	CURRENT AREA B/A	CURRENT AREA B/A
12	MESSAGE STOP-ON-ERROR	MESSAGE MONITOR ENABLED (MMT)	MESSAGEMONITOR ENABLED (MMT)	MESSAGE MONITOR ENABLED (MMT)
11	FRAME STOP-ON-ERROR	DYNAMIC BUS CONTROLACCEPTANCE	S10	TRIGGER ENABLED WORD
10	STATUS SET STOP-ON-MESSAGE	BUSY	S09	START-ON-TRIGGER
9	STATUS SET STOP-ON-FRAME	SERVICE REQUEST	S08	STOP-ON-TRIGGER
8	FRAME AUTO-REPEAT	SUBSYSTEM FLAG	S07	NOT USED
7	EXTERNAL TRIGGER ENABLED	RTFLAG	S06	EXTERNAL TRIGGER

				ENABLED
6	INTERNAL TRIGGER ENABLED	NOT USED	S05	NOT USED
5	INTERMESSAGE GAP TIMER ENABLED	NOT USED	S04	NOT USED
4	RETRY ENABLED	NOT USED	S03	NOT USED
3	DOUBLED/SINGLE RETRY	NOT USED	S02	NOT USED
2	BC ENABLED (Read Only)	NOT USED	S01	MONITOR ENABLED (Read Only)
1	BC FRAME IN PROGRESS (Read Only)	NOT USED	S00	MONITOR TRIGGERED(Read Only)
0	BC MESSAGE IN PROGRESS(Read Only)	RT MESSAGE IN PROGRESS (Read Only)	RT MESSAGE IN PROGRESS (Read Only)	MONITOR ACTIVE (Read Only)

TABLE 5 Configuration Register #2 (RD/WR 02H)

BIT	DESCRIPTION
15（MSB）	ENHANCED INTERRUPTS
14	LOGIC “0”
13	BUSY LOOKUP TABLE ENABLE
12	RX SA DOUBLE BUFFER ENABLE
11	OVERWRIT EINVALID DATA
10	256-WORD BOUNDARY DISABLE
9	TIME TAG RESOLUTION 2 (TTR2)
8	TIME TAG RESOLUTION 1 (TTR1)
7	TIME TAG RESOLUTION 0 (TTR0)
6	CLEAR TIME TAG ON SYNCHRONIZE

TABLE 6

Start/Reset Register (WR 03H)

BIT	DESCRIPTION
15	RESERVED
•	•
•	•
•	•
7	RESERVED
6	BC/MT STOP-ON-MESSAGE
5	BC STOP-ON-FRAME
4	TIME TAG TEST CLOCK
3	TIME TAG RESET
2	INTERRUPT RESET
1	BC/MT START
0	RESET

5	LOAD TIME TAG ON SYNCHRONIZE
4	INTERRUPT STATUS AUTO CLEAR
3	LEVEL/PULSE INTERRUPT REQUEST
2	CLEAR SERVICE REQUEST
1	ENHANCED RT MEMORY MANAGEMENT
0（LSB）	SEPARATE BROADCAST DATA

TABLE 7 BC/RT Command Stack Pointer Register (RD 03H)

BIT	DESCRIPTION
15（MSB）	COMMAND STACK POINTER 15
•	•
•	•
•	•
0（LSB）	COMMAND STACK POINTER 15

TABLE 8 BC Control Word Register (RD/WR 04H)

BIT	DESCRIPTION
15（MSB）	RESERVED
14	MESSAGE ERROR MASK
13	SERVICE REQUESTBIT MASK
12	SUBSYS BUSY BIT MASK
11	SUBSYS FLAG BIT MASK
10	TERMINAL FLAG BIT MASK
9	RESERVED BITS MASK
8	RETRY ENABLED
7	BUS CHANNEL A/B
6	OFF LINE SELF TEST
5	MASK BROADCAST BIT
4	EOM INTERRUPT ENABLE
3	1553A/B SELECT
2	MODE CODE FORMAT
1	BROADCAST FORMAT
0（LSB）	RT-RT FORMAT

TABLE 9 RT Subaddress Control Word Register (RD/WR 04H)

BIT	DESCRIPTION
15（MSB）	RX: DOUBLE BUFFER ENABLE
14	TX: EOM INT
13	TX: CIRC BUF INT
12	TX: MEMORY MANAGEMENT 2 (MM2)
11	TX: MEMORY MANAGEMENT 1 (MM1)
10	TX: MEMORY MANAGEMENT 0 (MM0)
9	RX: EOM INT
8	RX: CIRC BUF INT
7	RX: MEMORY MANAGEMENT 2 (MM2)
6	RX: MEMORY MANAGEMENT 1 (MM1)

TABLE 10Time Tag Register (RD/WR 05H)

BIT	DESCRIPTION
15（MSB）	TIME TAG 15
•	•
•	••
•	•
0（LSB）	TIME TAG 15

5	RX: MEMORY MANAGEMENT 0 (MM0)
4	BCST: EOM INT
3	BCST: CIRC BUF INT
2	BCST: MEMORY MANAGEMENT 2 (MM2)
1	BCST: MEMORY MANAGEMENT 1 (MM1)
0（LSB）	BCST: MEMORY MANAGEMENT 0 (MM0)

TABLE 11 INTERRUPTTATUS REGISTER
(READ 06H)

BIT	DESCRIPTION
15（MSB）	MASTER INTERRUPT
14	RAM PARITY ERROR
13	BC/RT TRANSMITTER TIMEOUT
12	BC/RT COMMAND STACK ROLLOVER
11	MT COMMAND STACK ROLLOVER
10	MT DATA STACK ROLLOVER
9	HS FAIL
8	BC RETRY
7	RT ADDRESS PARITY ERROR
6	TIME TAG ROLLOVER
5	RT CIRCULAR BUFFER ROLLOVER
4	BC/RT SELECTIVE MESSAGE
3	BC END OF FRAME
2	FORMAT ERROR
1	BC STATUS SET/RT MODE CODE/MT PATTERN TRIGGER
0（LSB）	END OF MESSAGE

TABLE 12 CONFIGURATION REGISTER #3 (RD/WR 07H)	
BIT	DESCRIPTION
15（MSB）	ENHANCED MODE ENABLE
14	BC/RT COMMAND STACK SIZE 1
13	BC/RT COMMAND STACK SIZE 0
12	MT COMMAND STACK SIZE 1
11	MT COMMAND STACK SIZE 0
10	MT DATA STACK SIZE 2
9	MT DATA STACK SIZE 1
8	MT DATA STACK SIZE 0
7	ILLEGALIZATION DISABLED
6	OVERRIDE MODE T/R ERROR
5	ALTERNATE STATUS WORD ENABLE
4	ILLEGAL RX TRANSFER DISABLE
3	BUSY RX TRANSFER DISABLE
2	RTFAIL-FLAG WRAP ENABLE
1	1553A MODE CODES ENABLE
0（LSB）	ENHANCED MODE CODE HANDLING

TABLE 13 CONFIGURATION REGISTER #4 (RD/WR 08H)	
BIT	DESCRIPTION
15（MSB）	EXTERNAL BIT WORD ENABLE
14	INHIBIT BIT WORD IF BUSY
13	MODE COMMAND OVERRIDE BUSY
12	EXPANDED BC CONTROL WORD ENABLE
11	BROADCAST MASK ENABLE/XOR
10	RETRY IF -A AND M.E.
9	RETRY IF STATUS SET
8	1ST RETRY ALT/SAME BUS
7	2ND RETRY ALT/SAME BUS
6	VALID M.E./NO DATA
5	VALID BUSY/NO DATA
4	MT TAG GAP OPTION
3	LATCH RT ADDRESS WITH CONFIG #5
2	TEST MODE 2
1	TEST MODE 1
0（LSB）	TEST MODE 0

TABLE 14 CONFIGURATION REGISTER #5 (RD/WR 09H)	
BIT	DESCRIPTION
15（MSB）	12MHZ CLOCK SELECT
14	SINGLE ENDED SELECT
13	EXTERNAL TX INHIBIT A, read only

12	EXTERNAL TX INHIBIT B, read only
11	EXPANDED CROSSING ENABLED
10	RESPONSE TIMEOUT SELECT 1
9	RESPONSE TIMEOUT SELECT 0
8	GAP CHECK ENABLED
7	BROADCAST DISABLED
6	RT ADDRESS LATCH/TRANSPARENT
5	RT ADDRESS 4
4	RT ADDRESS 3
3	RT ADDRESS 2
2	RT ADDRESS 1
1	RT ADDRESS 0
0（LSB）	RT ADDRESS PARITY

TABLE 16 BC FRAME TIMEREMAINING REGISTER (RD/WR 0BH)

BIT	DESCRIPTION
15（MSB）	BC FRAME TIME REMAINING 15
•	••
•	•
••	•
0（LSB）	BC FRAME TIME REMAINING 15

TABLE 15 MONITOR DATATACK ADDRESS REGISTER (RD/WR 0AH)

BIT	DESCRIPTION
15（MSB）	MONITOR DATASTACK ADDRESS 15
•	••
•	•
••	•
0（LSB）	MONITOR DATASTACK ADDRESS 0

TABLE 18 BC FRAME TIME/RT LAST COMMAND/ TRIGGER REGISTER (RD/WR 0DH)

BIT	DESCRIPTION
15（MSB）	BIT 15
•	••
•	•
••	•
0（LSB）	BIT 0

TABLE 19 RT STATUS WORD REGISTER (RD/WR 0EH)

BIT	DESCRIPTION
15（MSB）	LOGIC “0”
14	LOGIC “0”
13	LOGIC “0”
12	LOGIC “0”
11	LOGIC “0”
10	MESSAGE ERROR
9	INSTRUMENTATION
8	SERVICE REQUEST
7	RESERVED
6	RESERVED
5	RESERVED
4	BROADCAST COMMAND RECEIVED
3	BUSY
2	SUBSYSTEM FLAG
1	DYNAMIC BUS CONTROL ACCEPT
0（LSB）	TERMINAL FLAG

TABLE 20 RT BIT WORD REGISTER (WRITE 0FH)	
BIT	DESCRIPTION
15（MSB）	TRANSMITTER TIMEOUT
14	LOOP TEST FAILURE B
13	LOOP TEST FAILURE A
12	HANDSHAKE FAILURE
11	TRANSMITTER SHUTDOWN B
10	TRANSMITTER SHUTDOWN A
9	TERMINAL FLAG INHIBITED
8	CHANNEL B/A
7	HIGH WORD COUNT
6	LOW WORD COUNT
5	INCORRECT SYNC RECEIVED

4	PARITY/MANCHESTER ERROR RECEIVED
3	RT-RT GAP/SYNC/ADDRESS ERROR
2	RT-RT NO RESPONSE ERROR
1	RT-RT 2ND COMMAND WORD ERROR
0（LSB）	COMMAND WORD CONTENTS ERROR

TABLE 17 BC MESSAGE TIME REMAINING REGISTER (RD/WR 0CH)

BIT	DESCRIPTION
15（MSB）	BC MESSAGE TIME REMAINING 15
•	••
•	•
••	•
0（LSB）	BC MESSAGE TIME REMAINING 0

CONTROLLER (BC) ARCHITECTURE

The BC protocol of the B61580RH implements all MIL-STD-1553B message formats. Message format is programmable on a message-by-message basis by means of bits in the BC Control Word and the T/R bit of the Command Word for the respective message. The BC Control Word allows 1553 message format, 1553A/B type RT, bus channel, self-test, and Status Word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status Word RT Address field, and various RT-to-RT transfer errors. The B61580RH's BC response timeout value is programmable with choices of 18, 22, 50, and 130 μs. The longer response timeout values allow for operation over long buses and/or the use of repeaters.

FIGURE 2 illustrates BC intermessage gap and frame timing.The B61580RH may be programmed to process BC frames of up to 512 messages with no processor intervention. It is possible to program for either single frame or frame auto-repeat operation. In the auto-repeat mode, the frame repetition rate may be controlled either

internally, using a programmable BC frame timer, or from an external trigger input. The internal BC frame time is programmable up to 6.55 seconds in increments of 100 μs. In addition to BC frame time, intermessage gap time, defined as the start of the current message to the start of the subsequent message, is programmable on an individual message basis. The time between individual successive messages is programmable up to 65.5 ms, in increments of 1 μs.

BC MEMORY ORGANIZATION

TABLE 21 illustrates a typical memory map for BC mode. It is important to note that the only fixed locations for the B61580RH in the Standard BC mode are for the two Stack Pointers (address locations 0100 (hex) and 0104) and for the two Message Count locations (0101 and 0105). Enabling the Frame Auto-Repeat mode will reserve four more memory locations for use in the Enhanced BC mode; these locations are for the two Initial Stack Pointers (address locations 102 (hex) and 106) and for the Initial Message Count locations (103 and 107). The user is free to locate the Stack and BC Message Blocks anywhere else within the 64K (4K internal) shared RAM address space.

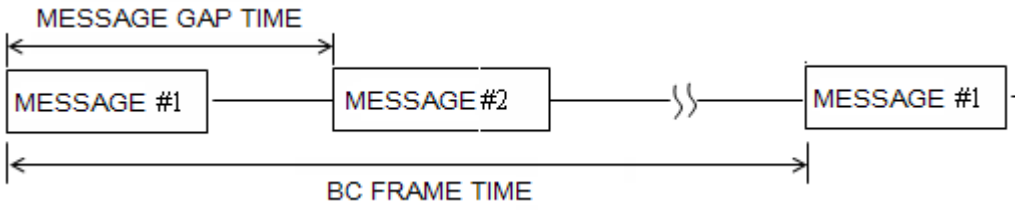


FIGURE 2 BC MESSAGE GAP AND FRAME TIMING

For simplicity of illustration, assume the allocation of the maximum length of a BC message for each message block in the typical BC memory map of TABLE 21. The maximum size of a BC message block is 38 words, for an RT-to-RT transfer of 32 Data Words (Control + 2 Commands + Loopback + 2 Status Words + 32 Data Words). Note, however, that this example assumes the disabling of the 256-word boundaries.

TABLE 21 TYPICAL BC MEMORY ORGANIZATION(SHOWN FOR 4K RAM)

ADDRESS (HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101	Message Count A (fixed location)

0102	Initial Stack Pointer A (see note) (Auto-Frame Repeat Mode)
0103	Initial Message Count A (see note) (Auto-Frame Repeat Mode)
0104	Stack Pointer B
0105	Message Count B
0106	Initial Stack Pointer B (see note) (Auto-Frame Repeat Mode)
0107	Initial Message CountB (see note) (Auto-Frame Repeat Mode)
0108-012D	Message Block 0
012E-0153	Message Block 1
0154-0179	Message Block 2
•	•
•	•
•	•
0ED6-0EFB	Message Block 93
0EFC-0EFF	Not Used
0F00-0FFF	Stack B
Note: Used only in the Enhanced BC mode with Frame Auto-Repeat enabled.	

BC MEMORY MANAGEMENT

FIGURE 3 illustrates the B61580RH's BC memory management scheme. One of the BC memory management features is the global double buffering mechanism. This provides for two sets of the various BC mode data structures: Stack Pointer and Message Counter locations, Descriptor Stack areas, and BC message blocks. Bit 13 of Configuration Register #1 selects the current active area. At any point in time, the B61580RH's internal 1553 memory management logic may access only the various data structures within the "active" area. FIGURE 3 delineates the "active" and "inactive" areas by the nonshaded and shaded areas, respectively; however, at any point in time, both the "active" and "nonactive" areas are accessible by the host processor. In most applications, the host processor will access the "nonactive" area, while the 1553 bus processes the "active" area messages.

The BC may be programmed to transmit multimessage frames of up to 512 messages. The number of messages to be processed is programmable by the Active Area Message Count location in the shared RAM, initialized by the host processor. In addition, the host processor must initialize another location, the Active Area Stack Pointer. The Stack Pointer references the four-word message block descriptor in the Stack area of shared RAM for each message to be processed. The BC Stack size is programmable with choices of 256, 512, 1024, and 2048 words.

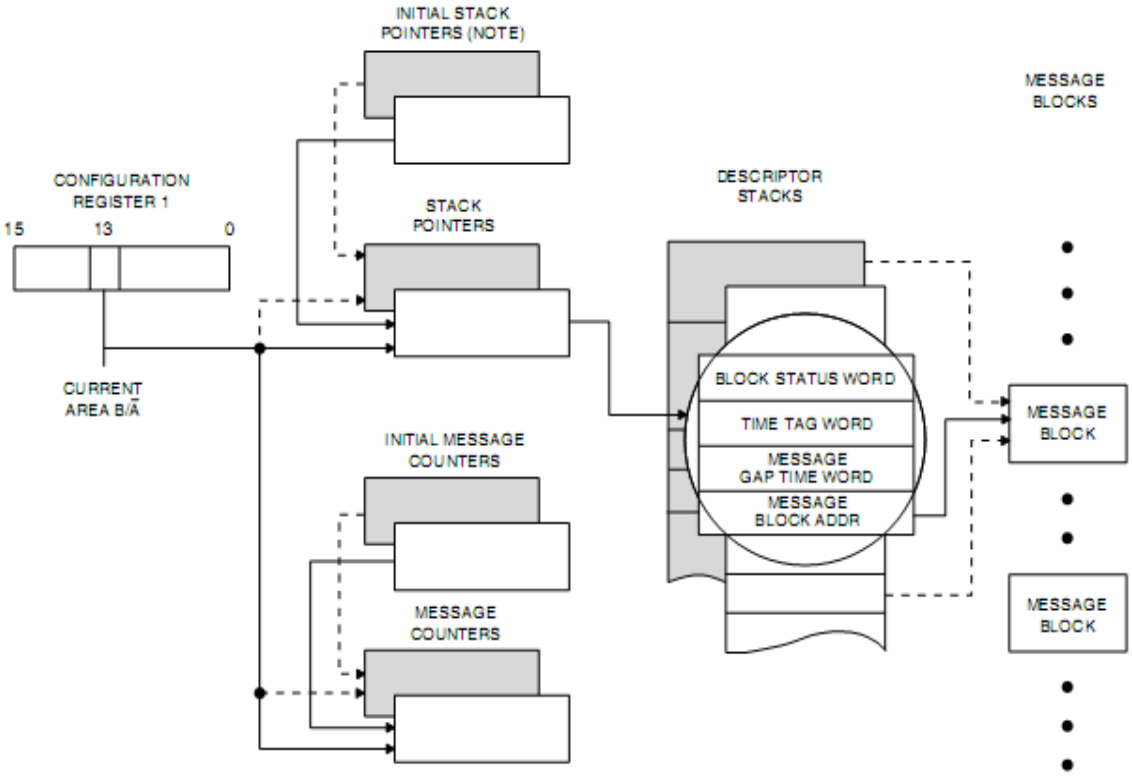
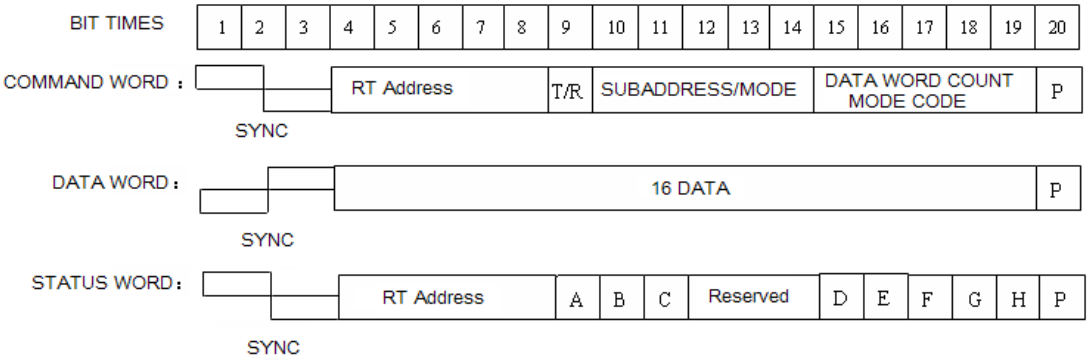


FIGURE 3 BC MODE MEMORY MANAGEMENT

BC MESSAGE BLOCK FORMATS AND BC CONTROL WORD

In BC mode, the B61580RH supports all MIL-STD-1553 message formats. For each 1553 message format, the B61580RH mandates a specific sequence of words within the BC Message Block. This includes locations for the Control, Command and (transmitted) Data Words that are to be read from RAM by the BC protocol logic. In addition, subsequent contiguous locations must be allocated for storage of received Loopback, RT Status and Data Words. FIGURE 4 illustrates the organization of the BC message blocks for the various MIL-STD-1553 message formats. Note that for all of the message formats, the BC Control Word is located in the first location of the message

block.



A: MESSAGE ERROR

B: INSTRUMENTION

C: SERVICE REQUEST

D: BROADCAST COMMAND RECEIVED

E: BUSY

F: SUBSYSTEM FLAG

G:DYNAMIC BUS CONTROL ACCEPTANCE

H:TERMINAL FLAG

The BC Control Word is not transmitted on the 1553 bus. Instead, it contains bits that select the active bus and message format, enable off-line self-test, masking of Status Word bits, enable retries and interrupts, and specify MIL-STD-1553A or -1553B error handling. The bit mapping and definitions of the BC Control Word are illustrated in TABLE 8.

The BC Control Word is followed by the Command Word to be transmitted, and subsequently by a second Command Word (for an RT-to-RT transfer), followed by Data Words to be transmitted (for Receive commands). The location after the last word to be transmitted is reserved for the Loopback Word. The loopback Word is an on-line self-test feature. The subsequent locations after the Loopback Word are reserved for received Status Words and Data Words (for Transmit commands).

AUTOMATIC RETRIES

The B61580RH BC implements automatic message retries. When enabled, retries will occur, following response timeout or format error conditions. As additional options,

retries may be enabled when the Message Error Status Word bit is set by a 1553A RT or following a “Status Set” condition. For a failed message, either one or two message retries will occur, and the bus channel (same or alternate) is independently programmable for the first and second retry attempts. Retries may be enabled or disabled on an individual message basis.

BC INTERRUPTS

BC interrupts may be enabled by the Interrupt Mask Register for Stack Rollover, Retry, End-of-Message (global), End-of-Message (in conjunction with the BC Control Word for individual messages), response timeout, message error, end of BC frame, and Status Set conditions. The definition of “Status Set” is programmable on an individual message basis by means of the BC Control Word. This allows for masking (“care/don’t care”) for the individual RT Status Word bits

BC MODE BLOCK STATUS WORD		
BIT	DESCRIPTION	
15（MSB）	EOM	
14	SOM	
13	CHANNEL B/A	
12	ERROR FLAG	
11	STATUS SET	RT-to-RT Transfer
10	FORMAT ERROR	Control Word
9	NO RESPONSE TIMEOUT	
8	LOOP TEST FAIL	
7	MASKED STATUS SET	
6	RETRY COUNT 1	
5	RETRY COUNT 0	
4	GOOD DATA BLOCK TRANSFER	
3	WRONG STATUS ADDRESS/NO GAP	
2	WORD COUNT ERROR	
1	INCORRECT SYNC TYPE	
0（LSB）	INVALID WORD	

BC-to-RT Transfer	RT-to-BC Transfer
Control Word	Control Word
Receive Command Word	Transmit Command Word
Data Word #1	Transmit Command Looped Back
Data Word #2	Status Received
••••	Data Word #1
•	Data Word #2
•	•
Last Data Word	•
Last Data Word Looped Back	•
Status Received	Last Data Word

Receive Command
Transmit Command
Transmit Command Looped Back
Tx RT Status Word
Data #1
Data #2
•
•
•
Last Data
Rx RT Status Word

RT-to-RTs (Broadcast) Transfer
Control Word
Rx Broadcast Command
Tx Command
Tx Command Looped Back
Tx RT Status Word
Data #1
Data #2
•
•
•
Last Data

Broadcast
Control Word
Broadcast Command
Data #1
Data #2
•
•
•
Last Data
Last Data Status Word

Mode Code;No Data
Control Word
Mode Command
Mode Command Looped Back
Status Received

Tx Mode Code;With Data
Control Word
Tx Mode Command
Mode Command Looped Back
Status Received
Data Word

Rx Mode Code;With Data
Control Word
Rx Mode Command
Data Word
Data Word Looped Back
Status Received

Broadcast Mode Code;No Data
Control Word
Broadcast Mode Command
Broadcast Mode Command Looped Back

Broadcast Mode Code;With Data
Control Word
Broadcast Mode Command
Data Word
Data Word Looped Back

FIGURE 4 BC MESSAGE BLOCK FORMATS

REMOTE TERMINAL (RT) ARCHITECTURE

The RT protocol design of the B61580RH represents BMTI's fifth generation implementation of a 1553 RT. One of the salient features of the Sp'ACE II's RT architecture is its true multiprotocol functionality. This includes programmable options for support of MIL-STD-1553A, the various McAir protocols, and MIL-STD-1553B Notice 2. The BU-61580 RT response time is 2 to 5 μs dead time (4 to 7 μs per 1553B), providing compliance to all the 1553 protocols. Additional multiprotocol features of the B61580RH include options for full software control of RT Status and Built-in-Test (BIT) words. Alternatively, for 1553B applications, these words may be formulated in real time by the B61580RH protocol logic.

The B61580RH RT protocol design implements all the MIL-STD-1553B message formats and dual redundant mode codes. This design is based largely on previous generation products that have passed SEAFAC testing for MIL-STD-1553B

compliance.

The Sp'ACE II RT performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. Other key features of the B61580RH RT include a set of interrupt conditions, internal command illegalization, and programmable busy by subaddress.

RT MEMORY ORGANIZATION

TABLE 22 illustrates a typical memory map for the Sp'ACE II in RT mode. As in BC mode, the two Stack Pointers reside in fixed locations in the shared RAM address space: address 0100 (hex) for the Area A Stack Pointer and address 0104 for the Area B Stack Pointer. Besides the Stack Pointer, for RT mode there are several other areas of the B61580RH address space designated as fixed locations. All RT modes of operation require the Area A and Area B Lookup Tables. Also allocated, are several fixed locations for optional features: Command Illegalization Lookup Table, Mode Code Selective Interrupt Table, Mode Code Data Table, and Busy Bit Lookup Table. It should be noted that any unenabled optional fixed locations may be used for general purpose storage (data blocks).

The RT Lookup tables, which provide a mechanism for mapping data blocks for individual Tx/Rx/Bcst-subaddresses to areas in the RAM, occupy address range locations 0140 to 01BF for Area A and 01C0 to 023F for Area B. The RT lookup tables include Subaddress Control Words and the individual Data Block Pointers. If used, address range 0300-03FF will be dedicated as the illegalizing section of RAM. The actual Stack RAM area and the individual data blocks may be located in any of the nonfixed areas in the shared RAM address space.

RT MEMORY MANAGEMENT

Another salient feature of the Sp'ACE II series products is the flexibility of its RT memory management architecture. The RT architecture allows the memory management scheme for each transmit, receive, or broadcast subaddress to be programmable on a subaddress basis. Also, in compliance with MIL-STD-1553B Notice 2, the B61580RH provides an option to separate data received from broadcast messages from nonbroadcast received data.Besides supporting a global double buffering scheme (as in BC mode), the Sp'ACE II RT provides a pair of 128-word Lookup Tables for memory management control, programmable on a subaddress basis (refer to TABLE 23). The 128-word tables include 32-word tables for transmit message

pointers and receive message pointers. There is also a third, optional Lookup Table for broadcast message pointers, providing Notice 2 compliance, if necessary.

The fourth section of each of the RT Lookup Tables stores the 32 subaddress Control Words (refer to TABLE 9 and TABLE 24). The individual Subaddress Control Words may be used to select the RT memory management option and interrupt scheme for each transmit, receive, and (optionally) broadcast subaddress.

For each transmit subaddress, there are two possible memory management schemes: (1) single message; and (2) circular buffer. For each receive (and optionally broadcast) subaddress, there are three possible memory management schemes: (1) single message; (2) double buffered; and (3) circular buffer. For each transmit, receive and broadcast subaddress, there are two interrupt conditions programmable by the respective Subaddress Control Word: (1) after every message to the subaddress; (2) after a circular buffer rollover. An additional table in RAM may be used to enable interrupts following selected mode code messages.When using the circular buffer scheme for a given subaddress, the size of the circular buffer is programmable by three bits of the Subaddress Control Word (see TABLE 24). The options for circular buffer size are 128, 256, 512, 1024, 2048, 4096, and 8192 Data Words.

TABLE 22 TYPICAL RT MEMORY MA P(SHOWN FOR 4K RAM)

ADDRESS(HEX)	DESCRIPTION
0000-00FF	Stack A
0100	Stack Pointer A (fixed location)
0101-0103	RESERVED
0104	Stack Pointer B (fixed location)
0105-0107	RESERVED
0108-010F	Mode Code Selective Interrupt Table (fixed area)
0110-013F	Mode Code Data (fixed area)
0140-01BF	Lookup Table A (fixed area)
01C0-023F	Lookup Table B (fixed area)
0240-0247	Busy Bit Lookup Table (fixed area)
0248-025F	(not used)
0260-027F	Data Block 0
0280-02FF	Data Block 1-4

0300-03FF	Command Illegalizing Table (fixed area)
0400-041F	Data Block 5
0420-043F	Data Block 6
••	•
•	•
•	•
0FE0-0FFF	Data Block 100

TABLE 23 LOOKUP TABLES

AREA A	AREA B	DESCRIPTION	COMMENT
0140-015F	01C0-01DF	Rx(/Bcst)_SA0 - Rx(/Bcst)_SA31	Receive(/Broadcast) Lookup Table
0160-017F	01E0-01FF	Tx_SA0 - Tx_SA31	Transmit Lookup Table
0180-019F	0200-021F	Bcst_SA0 - Bcst_SA31	Broadcast Lookup Table Optional
01A0-01BF	0220-023F	SACW_SA0 - SACW_SA31	Subaddress Control Word Lookup Table (Optional)

TABLE 24 SUBADDRESS CONTROL Word MEMORY MANAGEMENT SUBADDRESS BUFFER SCHEME				
MM2	**MM1**	**MM0**	**DESCRIPTION**	**COMMENT**
0	0	0	Single Message or Double Buffered	
0	0	1	128-Word	Circular Buffer of Specified Size
0	1	0	256-Word	
0	1	1	512-Word	
1	0	0	1024-Word	
1	0	1	2048-Word	
1	1	0	4096-Word	
1	1	1	8192-Word	

SINGLE MESSAGE MODE

FIGURE 5 illustrates the RT Single Message memory management scheme. When operating the B61580RH in its “AIM-HY” (default) mode, the Single Message scheme is implemented for all transmit, receive, and broadcast subaddresses. In the Single Message mode (also in the Double Buffer and Circular Buffer modes), there is a global double buffering scheme, controlled by bit 13 of Configuration Register #1. This selects from between the two sets of the various data structures shown in the figure: the Stack Pointers (fixed addresses), Descriptor Stacks (user defined addresses), RT Lookup Tables (fixed addresses), and RT Data Word blocks (user defined addresses). FIGURES 5, 6, and 7 delineate the “active” and ”nonactive” areas by the nonshaded and shaded areas, respectively.

As shown, the Sp’ACE II stores the Command Word from each message received, in the fourth location within the message descriptor (in the stack) for the respective message. The T/R bit, subaddress field, and (optionally) broadcast/own address, index into the active area Lookup Table, to locate the data block pointer for the current message. The B61580RH RT memory management logic then accesses the data block pointer to locate the starting address for the Data Word block for the current message. The maximum size for an RT Data Word block is 32 words.

For a particular subaddress in the Single Message mode, there is overwriting of the contents of the data blocks for receive/broadcast subaddresses – or overreading, for

transmit subaddresses. In the single message mode, it is possible to access multiple data blocks for the same subaddress. This, however, requires the intervention of the host processor to update the respective Lookup Table pointer. To implement a data wraparound subaddress, as required by Notice 2 of MIL-STD-1553B, the Single Message scheme should be used for the wraparound subaddress. Notice 2 recommends subaddress 30 as the wraparound subaddress.

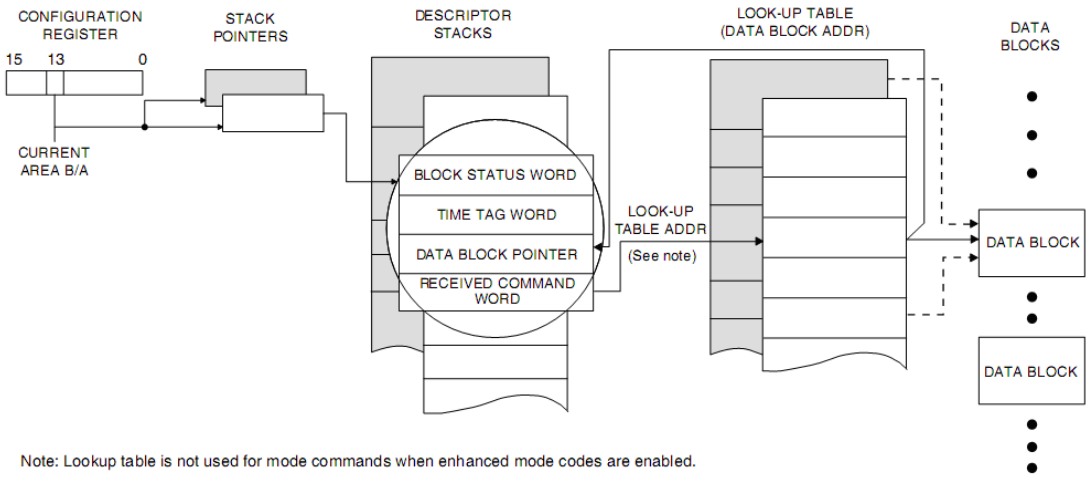


FIGURE 5 RT MEMORY MANAGEMENT:SINGLE MEMSSAGE MODE

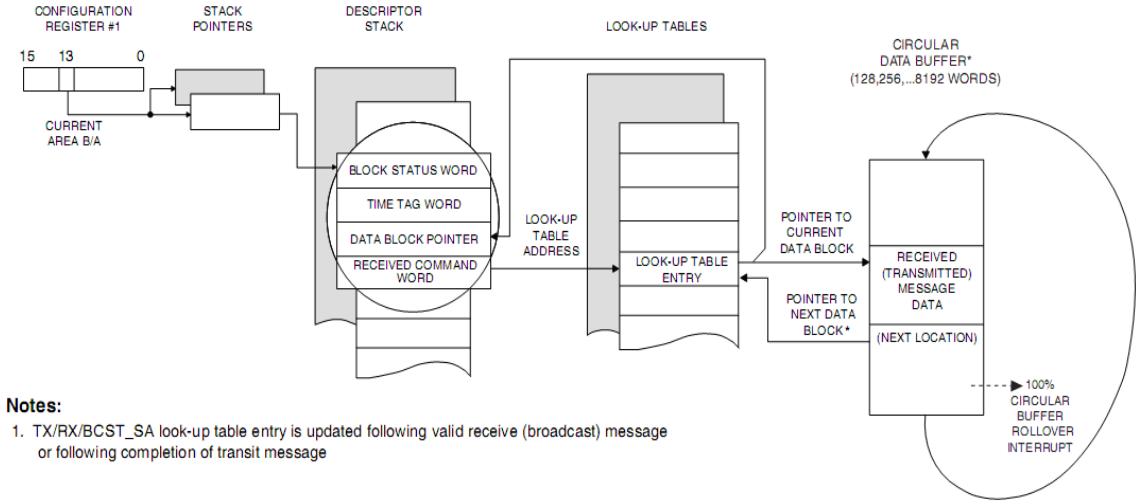


FIGURE 6 RT MEMORY MANAGEMENT:CIRCULAR BUFFER MODE

CIRCULAR BUFFER MODE

FIGURE 6 illustrates the RT circular buffer memory management scheme. The circular buffer mode facilitates bulk data transfers. The size of the RT circular buffer, shown on the right side of the figure, is programmable from 128 to 8192 words (in even

powers of 2) by the respective Subaddress Control Word.

As in the single message mode, the host processor initially loads the individual Lookup Table entries. At the start of each message, the Sp'ACE II stores the Lookup Table entry in the third position of the respective message block descriptor in the stack area of RAM, as in the Single Message mode. The Sp'ACE II transfers Receive or Transmit Data Words to (from) the circular buffer, starting at the location referenced by the Lookup Table pointer.

At the end of a valid (or, optionally, invalid) message, the value of the Lookup Table entry updates to the next location after the last address accessed for the current message. As a result, Data Words for the next message directed to the same Tx/Rx(/Bcst) subaddress will be accessed from the next contiguous block of address locations within the circular buffer. As a recommended option, the Lookup Table pointers may be programmed to not update following an invalid receive (or broadcast) message. This allows the 1553 bus controller to retry the failed message, resulting in the valid (retried) data overwriting the invalid data. This eliminates overhead for the RT's host processor. When the pointer reaches the lower boundary of the circular buffer (located at 128, 256, . . . 8192-word boundaries in the B61580RH address space), the pointer moves to the top boundary of the circular buffer, as FIGURE 6 shows.

IMPLEMENTING BULk DATA TRANSFERS

The use of the Circular Buffer scheme is ideal for bulk data transfers; that is, multiple messages to/from the same subaddress.

The recommendation for such applications is to enable the circular buffer interrupt request. By so doing, the routine transfer of multiple messages to the selected subaddress, including errors and retries, is transparent to the RT's host processor. By strategically initializing the subaddress's Lookup Table pointer prior to the start of the bulk transfer, the B61580RH may be configured to issue an interrupt request only after it has received the anticipated number of valid Data Words to the designated subaddress.

SUBADDRESS DOUBLE BUFFERING MODE

For receive (and broadcast) subaddresses, the B61580RH RT offers a third memory management option, Subaddress Double Buffering. Subaddress double buffering provides a means of ensuring data consistency. FIGURE 7 illustrates the RT Subaddress Double Buffering scheme. Like the Single Message and Circular Buffer

modes, the Double Buffering mode may be selected on a subaddress basis by means of the Subaddress Control Word. The purpose of the Double Buffering mode is to provide the host processor a convenient means of accessing the most recent, valid data received to a given subaddress. This serves to ensure the highest possible degree of data consistency by allocating two 32-bit Data Word blocks for each individual receive (and/or broadcast) subaddress.At a given point in time, one of the two blocks will be designated as the "active" 1553 data block while the other will be designated as the "inactive" block. The Data Words from the next receive message to that subaddress will be stored in the "active" block.

Upon completion of the message, provided that the message was valid and Subaddress Double Buffering is enabled, the B61580RH will automatically switch the "active" and "inactive" blocks for the respective subaddress. The Sp'ACE II accomplishes this by toggling bit 5 of the subaddress's Lookup Table Pointer and rewriting the pointer. As a result, the most recent valid block of received Data Words will always be readily accessible to the host processor.

As a means of ensuring data consistency, the host processor is able to reliably access the most recent valid, received Data Word block by performing the following sequence:

(1) Disable the double buffering for the respective subaddress by the Subaddress Control Word. That is, temporarily switch the subaddress's memory management scheme to the Single Message mode.

(2) Read the current value of the receive (or broadcast) subaddress's Lookup Table pointer. This points to the current "active" Data Word block. By inverting bit 5 of this pointer value, it is possible to locate the start of the "inactive" Data Word block. This block will contain the Data Words received during the most recent valid message to the subaddress.

(3) Read out the words from the "inactive" (most recent) Data Word Block.

(4) Re-enable the Double Buffering mode for the respective subaddress by the Subaddress Control Word.

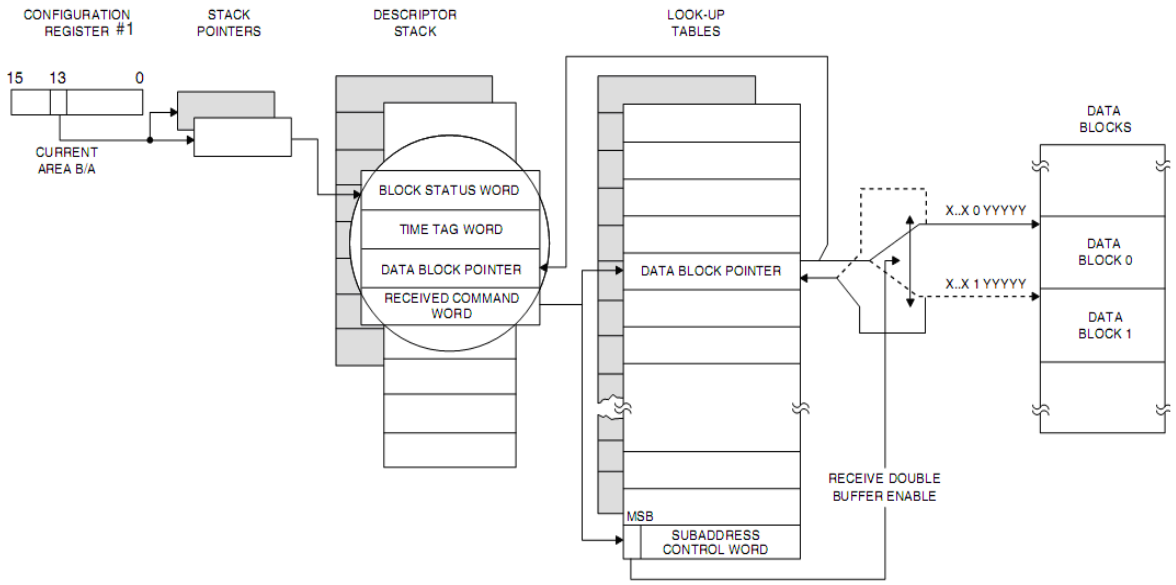


FIGURE 7 RT MEMORY MANAGEMENT :SUBADDRESS DOUBLE BUFFERING MODE

RT INTERRUPTS

As in BC mode, the B61580RH RT provides many maskable interrupts. RT interrupt conditions include End of (every) Message, Message Error, Selected Subaddress (Subaddress Control Word) Interrupt, Circular Buffer Rollover, Selected Mode Code Interrupt, and Stack Rollover.

DESCRIPTOR STACK

At the beginning and end of each message, the B61580RH RT stores a four-word message descriptor in the active area stack.

The RT stack size is programmable, with choices of 256, 512, 1024, and 2048 words. FIGURES 5, 6, and 7 show the four words: Block Status Word, Time Tag Word, Data Block Pointer, and the 1553 received Command Word. The RT Block Status Word includes indications of message in-progress or message complete, bus channel, RT-to-RT transfer and RT-to-RT transfer errors, message format error, loop test (self-test) failure, circular buffer rollover, illegal command, and other error conditions.

TABLE 25 shows the bit mapping of the RT Block Status Word.As in BC mode, the Time Tag Word stores the current contents of the B61580RH's read/writable Time Tag Register. The resolution of the Time Tag Register is programmable from among 2,

4, 8, 16, 32, and 64 μs/LSB. Also, incrementing of the Time Tag counter may be from an external clock source or via software command.

The Sp'ACE II stores the contents of the accessed Lookup Table location for the current message, indicating the starting location of the Data Word block, as the Data Block Pointer. This serves as a convenience in locating stored message data blocks.

The Sp'ACE II stores the full 16-bit 1553 Command Word in the fourth location of the RT message descriptor.

TABLE 25 RT MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15（MSB）	EOM
14	SOM
13	CHANNEL B/A
12	ERROR FLAG
11	RT-RT FORMAT
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	LOOP TEST FAIL
7	DATA STACK ROLLOVER
6	ILLEGAL COMMAND WORD
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0（LSB）	COMMAND WORD CONTENTS ERROR

RT COMMAND ILLEGALIZATION

The B61580RH provides an internal mechanism for RT command illegalization. In addition, there is a means for allowing the setting of the Busy Status Word bit to be only for a programmed subset of the transmit/receive/broadcast subaddresses.

The illegalization scheme uses a 256-word area in the B61580RH's address space. A benefit of this feature is the reduction of printed circuit board requirements, by eliminating the need for an external PROM, PLD, or RAM device that does the

illegalizing function. The B61580RH's illegalization scheme provides maximum flexibility, allowing any subset of the 4096 possible combinations of broadcast/own address, T/R bit, subaddress, and word count/mode code to be illegalized. Another advantage of the RAM-based illegalization technique is that it provides for a high degree of self-testability.

ADDRESSING THE ILLEGALIzATION TABLE

TABLE 26 illustrates the addressing scheme of the illegalization RAM. As shown, the base address of the illegalizing RAM is 0300 (hex). The Sp'ACE II formulates the index into the Illegalizing Table based on the values of BROADCAST/OWNADDRESS ADDRESS, T/R bit, Subaddress, and the MSB of the Word Count/Mode Code field (WC/MC4) of the current Command Word.

The internal RAM has 256 words reserved for command illegalization. Broadcast commands may be illegalized separately from nonbroadcast receive commands and mode commands.Commands may be illegalized down to the word count level. For example, a one-word receive command to subaddress 1 may be legal, while a two-word receive command to subaddress 1 may be illegalized.

The first 64 words of the Illegalization Table refer to broadcast receive commands (two words per subaddress). The next 64 words refer to broadcast transmit commands. Since nonmode code broadcast transmit commands are by definition invalid, this section of the table (except for subaddresses 0 and 31) does not need to be initialized by the user. The next 64 words correspond to nonbroadcast receive commands. The final 64 words refer to nonbroadcast transmit commands. Messages with Word Count/ Mode Code (WC/MC) fields between 0 and 15 may be illegalized by setting the corresponding data bits for the respective even-numbered address locations in the illegalization table. Likewise, messages with WC/MC fields between 16 and 31 may be illegalized by setting the corresponding data bits for the respective odd-numbered address locations in the illegalization table.

The following should be noted with regards to command illegalization:

(1) To illegalize a particular word count for a given broadcast/own address-T/R subaddress, the appropriate bit position in the respective illegalization word should be set to logic 1. A bit value of logic 0 designates the respective Command Word as a legal command. The B61580RH will respond to an illegalized nonbroadcast command with the Message Error bit set in its RT Status Word.

(2) For subaddresses 00001 through 11110, the “WC/MC” field specifies the Word Count field of the respective Command Word. For subaddresses 00000 and 11111, the “WC/MC” field specifies the Mode Code field of the respective Command Word.

(3) Since nonmode code broadcast transmit messages are not defined by MIL-STD-1553B, the sixty (60) words in the illegalization RAM, addresses 0342 through 037D, corresponding to these commands do not need to be initialized. The B61580RH will not respond to a nonmode code broadcast transmit command, but will automatically set the Message Error bit in its internal Status Register, regardless of whether or not the corresponding bit in the illegalization RAM has been set. If the next message is a Transmit Status or Transmit Last Command mode code, the BU-61580 will respond with its Message Error bit set.

TABLE 26 ILLEGALIZATION RAM ADDRESS DEFINITION

BIT	DESCRIPTION
15（MSB）	0
14	0
13	0
12	0
11	0
10	0
9	1
8	1
7	BROADCAST/OWN_ADDRESS
6	T/R
5	SUBADDRESS 4
4	SUBADDRESS 3
3	SUBADDRESS 2
2	SUBADDRESS 1
1	SUBADDRESS 0
0（LSB）	WC4/MC4

Mode Codes

The basic philosophy of the information transfer system is that it operates as a transparent communication link."Transparent" means that an application's function does not need to be involved with the management of communication.Obviously, the

information transfer system requires management that introduces overhead in the data bus system.

The command words, status words, status word response gaps, and intermessage gaps are the overhead.Within the command word the mode codes provide data bus management capability.

The mode codes have been divided into two groups;mode codes without a data word (00000-01111) and mode codes with a data word(10000-11111).The use of bit 15 in the command word to identify the two types was provided to aid in the decoding process.Also, the use of a single data word instead of multiple data words was adopted to simplify the mode circuitry.

Generally,with these two types of mode commands,all data bus system management requirements can be met.

Additional overhead is required by the system to maintain RT health, system time control (synchronization), subaddress message mapping, aperiodic message control, initialization/shutdown messages, etc.The determination of whether the command word contains a mode code is accomplished by decoding the subaddress/mode field (bit times 10-14).This field being either all zero's [00000] or all one's [11111] indicates that the command is a mode code and that the word count/mode code field (bit times 1519) contain the mode code type.Notice 2 requires that terminals must decode both indicators and that they must not convey different information.(Some earlier designs had used the [00000] indicator for the terminal hardware and the [11111] indicator for subsystem hardware.

TABLE 27 Assigned Mode Codes

Transmit-receive bit	Mode code	Function	Associated data word	Broadcast command allowed
1	00000	Dynamic bus control	NO	NO
1	00001	Synchronize	NO	YES
1	00010	Transmit status word	NO	NO
1	00011	Initiate self-test	NO	YES
1	00100	Transmitter shutdown	NO	YES
1	00101	Override transmitter shutdown	NO	YES
1	00110	Inhibit terminal flag bit	NO	YES

1	00111	Override inhibit terminal flag bit	NO	YES
1	01000	Reset remote terminal	NO	YES
1	01001	Reserved	NO	TBD
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1	01111	Reserved	NO	TBD
1	10000	Transmit vector word	YES	NO
0	10001	Synchronize	YES	YES
1	10010	Transmit last command	YES	NO
1	10011	Transmit bit word	YES	NO
0	10100	Selected transmitter shutdown	YES	YES
0	10101	Override selected transmitter shutdown	YES	YES
1或0	10110	Reserved	YES	TBD
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1或0	11111	Reserved	YES	TBD

PROGRAMMABLE BUSY

As a means of providing compliance with Notice 2 of MIL-STD-1553B, the B61580RH RT provides a software controllable means for setting the Busy Status Word bit as a function of subaddress.By a Busy Lookup Table in the B61580RH address space, it is possible to set the Busy bit based on command broadcast/own address, T/R bit, and subaddress.Another programmable option allows received Data Words to be either stored or not stored for messages when the Busy bit is set.

OTHER RT FUNCTIONS

The B61580RH allows the hardwired RT Address to be read by the host processor.Also, there are options for the RT FLAG Status Word bit to be set under software control and/or automatically following a failure of the loopback self-test.Other software controllable RT options include software programmable RT Status and RT BIT words, automatic clearing of the Service Request Status Word bit

following a Transmit Vector Word mode command, capabilities to clear and/or load the Time Tag Register following receipt of Synchronize mode commands, options regarding Data Word transfers for the Busy and/or Message Error (Illegal) Status Word bits, and for handling of 1553A and reserved mode codes.

MONITOR (MT) ARCHITECTURE

The B61580RH provides three bus monitor (MT) modes:

(1) The "AIM-HY"(default) or "AIM-HY'er"Word Monitor mode.

(2) A Selective Message Monitor mode.

(3) A Simultaneous Remote Terminal/Selective Message Monitor mode.

The strong recommendation for new applications is the use of the Selective Message Monitor, rather than the Word Monitor.

Besides providing monitor filtering based on RT Address,T/R bit, and Subaddress, the Message Monitor eliminates the need to determine the start and end of messages by software.The development of such software tends to be a tedious task.Moreover, at run time, it tends to entail a high degree of CPU overhead.

WORD MONITOR

In the Word Monitor mode, the B61580RH monitors both 1553 buses.After initializing the Word Monitor and putting it on-line the B61580RH stores all Command, Status, and Data Words received from both buses.For each word received from either bus, the B61580RH stores a pair of words in RAM.The first word is the 16 bits of data from the received word.The second word is the Monitor Identification (ID), or "Tag"word.The ID Word contains information relating to bus channel, sync type, word validity, and interword time gaps.The B61580RH stores data and ID words in a circular buffer in the shared RAM address space.

MONITOR TRIGGER WORD

There is a Trigger Word Register that provides additional flexibility for the Word Monitor mode.The B61580RH stores the value of the 16-bit Trigger Word in the MT Trigger Word Register.The contents of this register represent the value of the Trigger Command Word.The B61580RH has programmable options to start or stop the Word Monitor, and/or to issue an interrupt request following receipt of the Trigger Command Word from the 1553 bus.

SELECTIVE MESSAGE MONITOR MODE

The B61580RH Selective Message Monitor provides features to greatly reduce the

software and processing burden of the host CPU.The Selective Message Monitor implements selective monitoring of messages from a dual 1553 bus, with the monitor filtering based on the RT Address, T/R bit, and Subaddress fields of received 1553 Command Words.The Selective Message Monitor mode greatly simplifies the host processor software by distinguishing between Command and Status Words.The Selective Message Monitor maintains two stacks in the B61580RH RAM:a Command Stack and a Data Stack.

SIMULTANEOUS RT/MESSAGE MONITOR MODE

The Selective Message Monitor may function as a purely passive monitor or may be programmed to function as a simultaneous RT/Monitor.The RT/Monitor mode provides complete Remote Terminal (RT) operation for the B61580RH's strapped RT address and bus monitor capability for the other 30 non-broadcast RT addresses.This allows the B61580RH to simultaneously operate as a full function RT and "snoop"on all or a subset of the bus activity involving the other RTs on a bus.This type of operation is sometimes needed to implement a backup bus controller.The combined RT/Selective Monitor maintains three stack areas in the B61580RH address space:an RT Command Stack, a Monitor Command Stack, and a Monitor Data Stack.The pointers for the various stacks have fixed locations in the B61580RH address space.

SELECTIVE MESSAGE MONITOR MEMORY ORGANIZATION

TABLE 28 illustrates a typical memory map for the SP'ACE in the Selective Message Monitor mode.This mode of operation defines several fixed locations in the RAM.These locations allocate in a manner that is compatible with the combined RT/Selective Message Monitor mode.The fixed memory map consists of two Monitor Command Stack Pointers (location 102h and 106h), two Monitor Data Stack Pointers (locations 103h and 107h), and a Selective Message Monitor Lookup Table (0280-02FFh) based on RT Address T/R, and subaddress.Assume a Monitor Command Stack size of 1K words, and a Monitor Data Stack size of 4K words.

TABLE 28 TYPICAL SELECTIVE MESSAGE MONITOR MEMORY MA P(SHOWN FOR 4K RAM)

ADDRESS(HEX)	DESCRIPTION
0000-0101	Not Used
0102	Monitor Command Stack Pointer A (fixed location)
0103	Monitor Data Stack Pointer A (fixed location)

0104-0105	Not Used
0106	Monitor Command Stack Pointer B (fixed location)
0107	Monitor Data Stack Pointer B (fixed location)
0108-027F	Not Used
0280-02FF	Selective Monitor Lookup Table (fixed area)
0300-03FF	Not Used
0400-07FF	Monitor Command Stack A
0800-0FFF	Monitor Data Stack A

Refer to FIGURE 8 for an illustration of the Selective Message Monitor operation.Upon receipt of a valid Command Word, the B61580RH will reference the Selective Monitor Lookup Table (a fixed block of addresses) to check for the condition (disabled/enabled) of the current command.If disabled, the B61580RH will ignore (and not store) the current message;if enabled,the B61580RH will create an entry in the Monitor Command Stack at the address location referenced by the Monitor CommandStack Pointer.

Similar to RT mode, The SP'ACE stores a Block Status Word,16-bit Time Tag Word, and Data Block Pointer in the Message Descriptor, along with the received 1553 Command Word following reception of the Command Word.The SP'ACE writes the Block Status and Time Tag Words at both the start and end of the message.The Monitor Block Status Word contains indications of message in-progress or message complete, bus channel, Monitor Data Stack Rollover, RT-to-RT transfer and RT-to-RT transfer errors, message format error, and other error conditions.

TABLE 30 shows the Message Monitor Block Status Word.The Data Block Pointer references the first word stored in the Monitor Data Stack (the first word following the Command Word) for the current message.The B61580RH will then proceed to store the subsequent words from the message [possible second Command Word, Data Word(s), Status Word(s)] into consecutive locations in the Monitor Data Stack.

TABLE 29 WORD MONITOR IDENTIFICATION WORD	
BIT	**DESCRIPTION**
15(MSB)	GAP TIME
.	.

•	•
•	•
8	GAP TIME
7	WORD FLAG
6	THIS RT
5	BROADCAST
4	ERROR
3	COMMAND/DATA
2	CHANNEL B/A
1	CONTIGUOUS DATA/GAP
0(LSB)	MODE CODE

TABLE 30 MESSAGE MONITOR MODE BLOCK STATUS WORD

BIT	DESCRIPTION
15(MSB)	EOM
14	SOM
13	CHANNEL B/A
12	ERROR FLAG
11	RT-RT TRANSFER
10	FORMAT ERROR
9	NO RESPONSE TIMEOUT
8	GOOD DATA BLOCK TRANSFER
7	DATA STACK ROLLOVER
6	RESERVED
5	WORD COUNT ERROR
4	INCORRECT SYNC
3	INVALID WORD
2	RT-RT GAP/SYNC/ADDRESS ERROR
1	RT-RT 2ND COMMAND ERROR
0(LSB)	COMMAND WORD CONTENTS ERROR

The size of the Monitor Command Stack is programmable to 256, 1K, 4K, or 16K

words.The Monitor Data Stack size is programmable to 512, 1K, 2K, 4K, 8K, 16K, 32K, or 64K words.

Monitor interrupts may be enabled for Monitor Command Stack Rollover, Monitor Data Stack Rollover, and/or End-of-Message conditions.In addition, in the Word Monitor mode there may be an interrupt enabled for a Monitor Trigger condition.

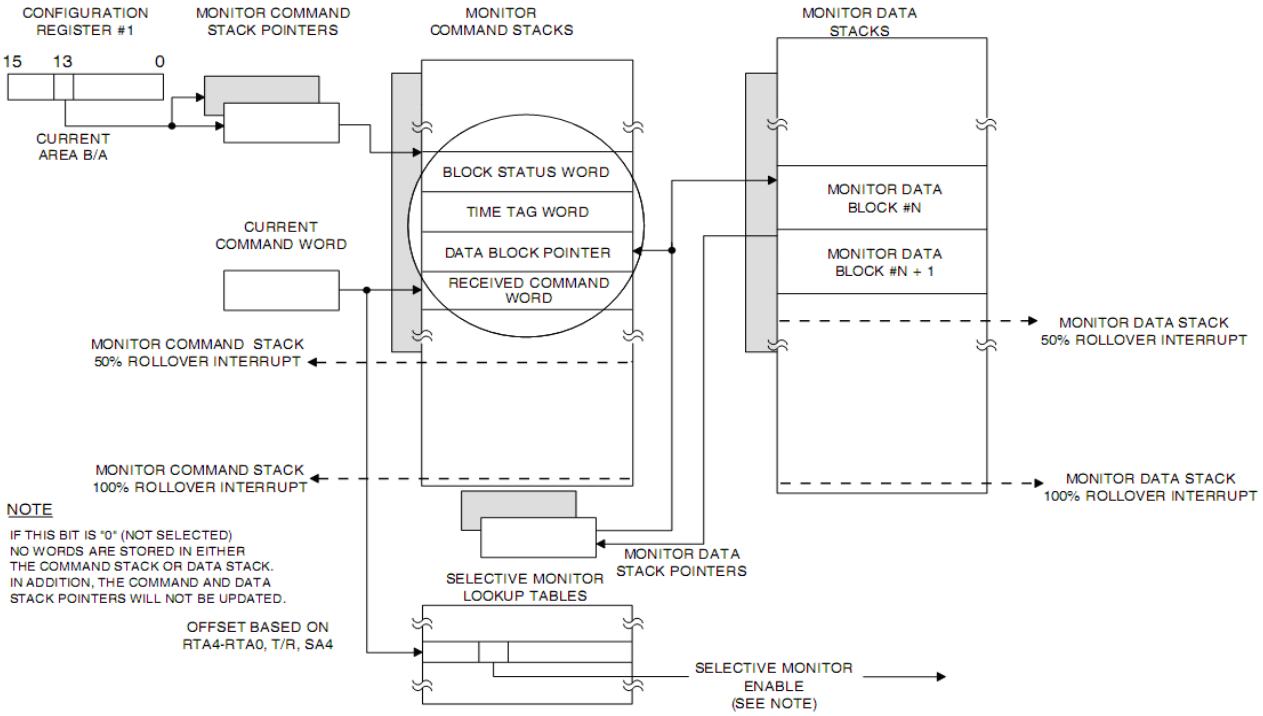


FIGURE 8 SELECTIVE MESSAGE MONITOR MEMORY MANAGEMENT

PROCESSOR AND MEMORY INTERFACE

The SP'ACE terminals provide much flexibility for interfacing to a host processor and optional external memory.FIGURE 1 shows that there are 14 control signals, 6 of which are dual purpose, for the processor/memory interface.FIGURES 9 through 14 illustrate six of the configurations that may be used for interfacing the B61580RH to a host processor bus.The various possible configurations serve to reduce to an absolute minimum the amount of glue logic required to interface to 8-, 16-, and 32-bit processor buses.Also included are features to facilitate interfacing to processors that do not have a "wait state"type of handshake acknowledgment.Finally, the SP'ACE supports a reliable interface to an external dual port RAM.This type of interface minimizes the portion of the available processor bandwidth required to access the 1553 RAM.

The 16-bit buffered mode (FIGURE 9) is the most common configuration used.It provides a direct, shared RAM interface to a 16-bit or 32-bit microprocessor.In this

mode, the SP'ACE's internal address and data buffers provide the necessary isolation between the host processor's address and data buses and the corresponding internal memory buses.In the buffered mode, the 1553 shared RAM address space limit is the B61580RH's 4K words of internal RAM.The 16-bit buffered mode provides a pair of pin-programmable options:

(1) The logic sense of the RD/WR control input is selectable by the POLARITY_SEL input;for example, write when RD/WR is low for Motorola 680X0 processors;write when RD/WR is high

for the Intel i960 series microprocessors.

(2) By strapping the input signal ZERO WAITto logic "1", the SP'ACE terminals may interface to processors that have an acknowledge type of handshake input to accommodate hardware controlled wait states;most current processor chips have such an input.In this case, the B61580RH will assert its READY output low only after it has latched WRITE data internally or has presented READ data on D15-D0.

By strapping ZERO WAIT to logic "0", it is possible to easily interface the B61580RH to processors that do not have an acknowledge type of handshake input.An example of such a processor is Analog Device's ADSP2101 DSP chip.In this configuration,the processor can clear its strobe output before the completion of access to the B61580RH internal RAM or register.In this case,READY goes high following the rising edge of STRBD and will stay high until completion of the transfer.READY will normally be low when ZERO WAITis low.

Similar to the 16-bit buffered mode, the 16-bit transparent mode (FIGURE 10) supports a shared RAM interface to a host CPU.The transparent mode offers the advantage of allowing the buffer RAM size to be expanded to up to 64K words, using external RAM.A disadvantage of the transparent mode is that it requires external address and data buffers to isolate the processor buses from the memory/ B61580RH buses.

A modified version of the transparent mode involves the use of dual port RAM, rather than conventional static RAM.Refer to FIGURE 11.This allows the host to access RAM very quickly, the only limitation being the access time of the dual port RAM.This configuration eliminates the B61580RH arbitration delays for memory accesses.The worst case delay time occurs only during a simultaneous access by the host and the B61580RH 1553 logic to the same memory address.In general, this will

occur very rarely and the SP'ACE limits the delay to approximately 250 ns.

FIGURE 12 illustrates the connections for the 16-bit Direct Memory Access (DMA) mode.In this configuration the host processor, rather than the SP'ACE terminal, arbitrates the use of the address and data buses.The arbitration involves the two DMA output signals Request (DTREQ) , Acknowledge (DTACK),and the input signal Grant (DTGRT).The DMA interface allows the SP'ACE components to interface to large amounts of system RAM while eliminating the need for external buffers.For system address spaces larger than 64K words, it is necessary for the host processor to provide a page register for the upper address bits (above A15) when the B61580RH accesses the RAM (while asserting (DTACK)low).

The internal RAM is accessible through the standard SP'ACE interface (SELECT, STRBD, READYD, etc).The host CPU may access external RAM by the SP'ACE's arbitration logic and output control signals, as illustrated in FIGURE 12.Alternatively,control of the RAM may be shared by both the host processor and the SP'ACE, as illustrated in FIGURE 13.The latter requires the use of external logic, but allows the processor to access the RAM directly at the full access speed of the RAM, rather than waiting for the SP'ACE handshake acknowledge output READY.

FIGURE 14 illustrates the 8-bit buffered mode.This interface allows a direct connection to 8-bit microprocessors and 8-bit microcontrollers.As in the 16-bit buffered configuration, the buffer RAM limit is the B61580RH's 4K words of internal RAM.

In the 8-bit mode, the host CPU accesses the B61580RH's internal registers and RAM by a pair of 8-bit registers embedded in the SP'ACE interface.The 8-bit interface may be further configured by three strappable inputs:ZEROWAIT, POLARITY_SEL,and TRIGGER_SEL.By connecting ZEROWAIT to logic "0", the B61580RH may be interfaced with minimal "glue"logic to 8-bit microcontrollers, such as the Intel 8051 series, that do not have an Acknowledge type of handshake input.The programmable inputs POLARITY_SEL and TRIGGER_SEL allow the B61580RH to accommodate the different byte ordering conventions and "A0"logic sense utilized by different 8-bit processor families.

PROCESSOR INTERFACE TIMING

FIGURES 16 and 17 illustrate the timing for the host processor to access the SP'ACE's internal RAM or registers in the 16-bit,nonzero wait buffered

mode.FIGURE 16 illustrates the 16-bit,buffered, nonzero wait state mode read cycle timing while FIGURE 17 shows the 16-bit, buffered, nonzero wait state modewrite cycle timing.

During a CPU transfer cycle, the signals STRB and SELECT must be sampled low on the rising edge of the system clock to request access to the B61580RH's internal shared RAM.The transfer will begin on the first rising system clock edge when SELECT and STRBD are low and the 1553 protocol/memory management unit is not accessing the internal RAM.The falling edge of the output signal IOEN indicates the start of the transfer.

The SP'ACE latches the signals MEM/REG and RD/WR internally on the first falling clock edge after the start of the transfer cycle.The address inputs latch internally on the first rising clock edge after the signal IOEN goes low.Note that the address lines may be latched at any time using the ADDR_LAT input signal.

The output signal READYD will be asserted low on the third (or 7th if it's an internal read) rising system clock edge after IOEN goes low.The assertion of READYD low indicates to the host processor that read data is available on the parallel data bus, or that write data has been stored.At this time, the CPU should bring the signal STRBD high, completing the transfer cycle.

ADDRESS LATCH TIMING

FIGURE 15 illustrates the operation and timing of the address input latches for the buffered interface mode.In the transparent mode, the address buffers are always transparent.Since the transparent mode requires the use of external buffers, external address latches would be required to demultiplex a multiplexed address bus.In the buffered mode however, the SP'ACE's internal address latches may be used to perform the demultiplexing function.

The ADDR_LAT input signal controls address latch operation. When ADDR_LAT is high, the outputs of the latch (which drive the SP'ACE's internal memory bus) track the state of address inputs A15 - A00.When low, the internal memory bus remains latched at the state of A15 - A00 just prior to the falling edge of ADDR_LAT.

MISCELLANEOUS SELF-TEST

The B61580RH products incorporate several self-test features.These features include an on-line wraparound self-test for all messages in BC and RT modes, an

off-line wraparound self-test for BC mode, and several other internal self-test features.

The BC/RT on-line loop test involves a wraparound test of the encoder/decoder and transceiver.The BC off-line self-test involves the encoder/decoder, but not the transceiver.These tests entail checking the received version of every transmitted word for validity (sync, encoding, bit count, parity) and checking the received version of the last transmitted word for a bit-by-bit comparison with the encoded word.The loopback test also fails if there is a timeout of the internal transmitter watchdog timer.A failure of the loop test results in setting a bit in the message's Block Status Word and, if enabled, will result in an interrupt request.With appropriate host processor software, the BC offline test is able to exercise the parallel and serial data paths,encoder, decoder, and a substantial portion of the BC protocol and memory management logic.

There are additional built-in self-test features, involving the use of three configuration register bits and the eight test registers. This allows a test of approximately 99% of the J-Rad chip's internal logic.These tests include an encoder test, a decoder test, a register test, a protocol test, and a test of the fail-safe (transmitter timeout) timer.

There is also a test mode.In the test mode, the host processor can emulate arbitrary activity on the 1553 buses by writing to a pair of test registers.The test mode can be operated in conjunction with the Word Monitor mode to facilitate end-to-end selftests.

Electrical Characteristic

See Appendix 2.

Typical Application

See Appendix 3.

Package

See Appendix 4.

Appendix 1

PIN	SIGNAL NAME	PORT	DESCRIPTION
1	TX/RX-A	I/O	Analog Transmit/Receive Input/Outputs. Connect directly to 1553 isolation transformers.
2	$\overline{\text{TX/RX-A}}$	I/O	
34	TX/RX-B	I/O	
35	$\overline{\text{TX/RX-B}}$	I/O	
3	$\overline{\text{SELECT}}$	I	Generally connected to a CPU address decoder output to select the B61580RH for a transfer to/from either RAM or register. May be tied to STRBD
4	$\overline{\text{STRBD}}$	I	Strobe Data. Used with SELECT to initiate and control the data transfer cycle between the host processor .
5	MEM/ $\overline{\text{REG}}$	I	Memory/Register. Generally connected to either a CPU address line or address decoder output. Selects between memory access MEM/REG = 1 (or register access MEM/REG = 0).
6	RD/$\overline{\text{WR}}$	I	Read/Write. For host processor access, selects either reading or writing. In the 16-bit buffered mode, if polarity select is logic (0), then RD/WR is low (logic 0) for read accesses and high (logic 1) for write accesses. If polarity select is logic 1 or the configuration of the interface is a mode other than 16-bit buffered mode, then RD/WR is high (logic 1) for read accesses and low (logic 0) for write accesses.
7	$\overline{\text{MSTCLR}}$	I	Master Clear. Negative true Reset input, normally asserted low following power turn-on. Requires a minimum 100ns negative pulse to reset all internal logic to its “power turn-on” state.
8	A15	I/O	16-bit bidirectional address bus. In both the buffered and transparent modes, the host CPU accesses the B61580RH registers and 64K words of internal RAM by A15 through A0. The host CPU performs register selection by A4 through A0. In the buffered mode, A15-A0 are inputs only. In the transparent mode, A15-A0 are inputs during CPU accesses and drive outward
9	A14	I/O	
10	A13	I/O	
11	A12	I/O	
12	A11	I/O	
13	A10	I/O	

14	A9	I/O	(towards the CPU) when the 1553 protocol/memory management logic accesses up to 64K x 16 of external RAM. The address bus drives outward only in the transparent mode when the signal DTACK is low (indicating that theB 63825RH has control of the processor interface bus) and IOEN is high (indicating that this is not a CPU access). Most of the time, including immediately after power turn-on RESET, the A15-A0 outputs will be in their disabled (high impedance) state.
15	A8	I/O	
16	A7	I/O	
17	A6	I/O	
20	A5	I/O	
21	A4	I/O	
22	A3	I/O	
23	A2	I/O	
24	A1	I/O	
25	A0	I/O	
18	GND	I	Ground
19	CLOCK	I	16MHz (or 12MHz) clock input.
26	$\overline{\text{DTGRT}}$ (I) /MSB/ $\overline{\text{LSB}}$(I)	I	Data Transfer Grant or Most Significant Byte/Least Significant Byte. In transparent mode, active low input signal asserted, in response to the DTREQ output, to indicate that access to the processor buses has been granted to the B61580RH. In 8-bit buffered mode, input signal used to indicate which byte is being transferred (MSB or LSB). The POLARITY_SEL input controls the logic sense of MSB/LSB. (Note: only the 8-bit buffered mode uses MSB/LSB.) See description of POLARITY_SEL signal.
27	$\overline{\text{SSFLAG}}$/EXT_TRIG	I	Subsystem Flag or External Trigger input. In the Remote Terminal mode, asserting this input will set the Subsystem Flag bit in the B61580RH's RT Status Word. A low on the SSFLAG input overrides a logic "1" of the respective bit (bit 8) of Configuration Register #1. In the Bus Controller mode, an enabled external BC Start option (bit 7 of Configuration Register #1) and a low-to-high transition on this input will issue a BC Start command, starting execution of the current BC frame. In the Word Monitor mode, an enabled external trigger (bit 7 of Configuration Register #1) and a low-to-high transition on this input will issue a monitor trigger.
28	$\overline{\text{MEMENA\_}}$	O	Memory Enable Output. Asserted low during both host processor and 1553 protocol/memory management memory transfer cycles.

			Used as a memory chip select (CS) signal for external RAM in the transparent mode.
29	$\overline{\text{MEMOE}}$ (O)/ADDR_LAT(I)	I/O	Memory Output Enable or Address Latch. In transparent mode, MEMOE output will be used to enable data outputs for external RAM read cycles (normally connected to the OE signal on external RAM chips). In buffered mode, ADDR_LAT input will be used to configure the internal address latches in latched mode (when low) or transparent mode (when high).
30	$\overline{\text{MEMWR}}$(O)/ $\overline{\text{ZERO\_WAIT}}$ (I)	I/O	Memory Write or Zero Wait State. In transparent mode, active low output signal (MEMWR) will be asserted low during memory write transfers to strobe data into internal or external RAM (normally connected to the WR signal on external RAM chips). In buffered mode, input signal (ZERO WAIT) will be used to select between the zero wait mode (ZERO WAIT= logic 0) and the nonzero wait mode (ZERO WAIT = logic 1). (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACEII operating in 8-bit Buffered Non-Zero Wait Mode)
31	$\overline{\text{DTREQ}}$ /16/$\overline{8}$(I)	I/O	Data Transfer Request or 16-bit/8-bit Transfer Mode Select. In transparent mode, active low output signal used to request access to the processor interface bus (address, data, and control buses). In buffered mode, input signal used to select between the 16-bit data transfer mode (16/ = logic 1) and the 8 bit data transfer mode (16/8 = logic 0). (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACE and SP'ACEII operating in 8-bit Buffered Non-Zero Wait Mode)
32	$\overline{\text{DTACK}}$(O)/POLARITY_SEL (I)	I/O	Data Transfer Acknowledge or Polarity Select. In transparent mode, active low output signal used to indicate acceptance of the processor interface bus in response to a data transfer grant (DTGR). In 16-bit buffered mode (TRANSPARENT/BUFFERED = logic 0 and 16/8= logic 1), input signal used to control the logic sense of the RD/WR signal.

			When POLARITY_SEL is logic 1, RD/WR must be asserted high (logic 1) for a read operation and low (logic 0) for a write operation. When POLARITY_SEL is logic 0, RD/WR must be asserted low (logic 0) for a read operation and high (logic 1) for a write operation. In 8-bit buffered mode (TRANSPARENT/BUFFERED = logic 0 and 16/8 = logic 0), input signal used to control the logic sense of the MSB/LSB signal. When POLARITY_SEL is logic 0, MSB/LSB must be asserted low (logic 0) to indicate the transfer of the least significant byte and high (logic 1) to indicate the transfer of the most significant byte. When POLARITY_SEL is logic 1, MSB/LSB must be asserted high (logic 1) to indicate the transfer of the least significant byte and low (logic 0) to indicate the transfer of the most significant byte.
33	$\overline{\text{MEMENA}}$ (I)/TRIGGER_SEL (I)	I	Memory Enable Input or Trigger Select. In transparent mode, MEMENA_IN is an active low Chip Select (CS) input to the 4K x 16 of internal shared RAM. When only using internal RAM, connect directly to MEMENA_OUT or ground. In 8-bit buffered mode, the input signal (TRIGGER_SEL) indicates the order of byte pairs transferred to or from the B61580RH by the host processor. This signal has no operation (can be N/C) in the 16-bit buffered mode. In the 8-bit buffered mode, TRIGGER_SEL should be asserted high (logic 1) if the byte order for both read operations and write operations is MSB followed by LSB. TRIGGER_SEL should be asserted low (logic 0) if the byte order for both read operations and write operations is LSB followed by MSB.
36		I	Transmitter inhibit inputs for the Channel B MIL-STD-1553 transmitters. For normal operation, these inputs should be connected to logic "0". To force a shutdown of Channel B, a value of logic "1" should be applied to the respective TX_INH input.
37	GNDB	I	Ground
38	+5VB	I	CH. B +5V Supply

39	RTAD0	I	Remote Terminal Address Inputs
40	RTAD1	I	
41	RTAD2	I	
42	RTAD3	I	
43	RTAD4	I	
44	RTADP	I	Remote Terminal Address Parity. Must provide odd parity sum with RTAD4-RTAD0 in order for the RT to respond to non-broadcast commands.
45	$\overline{\text{INCMD}}$	O	In Command. In BC mode, asserted low throughout processing cycle for each message. In RT mode or Message Monitor mode, asserted low following receipt of Command Word and kept low until completion of current message sequence. In Word Monitor mode, goes low following MONITOR START command, kept low while monitor is on-line, goes high following RESET command.
46	D0	I/O	16-bit bidirectional data bus. This bus interfaces the host processor to the internal registers and 4K words of RAM. In addition, in the transparent mode, this bus allows data transfers to take place between the internal protocol/memory management logic and up to 64K x 16 of external RAM. Most of the time, the outputs for D15 through D0 are in their high impedance state. They drive outward in the buffered or transparent mode when the host CPU reads the internal RAM or registers. Or, in the transparent mode, when the protocol/memory management logic is accessing (either reading or writing) internal RAM or writing to external RAM.
47	D1	I/O	
48	D2	I/O	
49	D3	I/O	
50	D4	I/O	
51	D5	I/O	
52	D6	I/O	
53	D7	I/O	
55	D8	I/O	
56	D9	I/O	
57	D10	I/O	
58	D11	I/O	
59	D12	I/O	
60	D13	I/O	
61	D14	I/O	
62	D15	I/O	
54	+5V	I	Logic +5V Supply

63	TAG_CLK	I	External Time Tag Clock input. Use may be designated by bits 7, 8, and 9 of Configuration Register #2. When used it increments the internal Time Tag Register/Counter. If not used, should be connected to +5V or ground.
64	TRANSPARENT/ $\overline{\text{BUFFERED}}$	I	Used to select between the Transparent/ DMA mode (when strapped to logic 1) and the Buffered mode (when strapped to logic 0) for the host processor interface. (Please see Appendix G in the ACE User's Guide for Product Advisory regarding SP'ACEand SP'ACE II operating in 8-bit Buffered Non-Zero Wait Mode)
65	$\overline{\text{INT}}$	O	Interrupt request output. If the LEVEL/PULSE interrupt bit (bit 3) of Configuration Register #2 is low, a negative pulse of approximately 500 ns in width is output on INT. If bit 3 is high, a low level interrupt request output will be asserted on INT.
66	$\overline{\text{READYD}}$	O	Handshake output to host processor. For a nonzero wait state read access, signals that data is available to be read on D15 through D0. For a nonzero wait state write cycle, signals the completion of data transfer to a register or RAM location. In the buffered zero wait state mode, active high output signal (following the rising edge of STRBD used to indicate the latching of address and data (write only) and that an internal transfer between the address/data latches and the RAM/registers is on-going.
67	$\overline{\text{IOEN}}$	O	Tri-state control for external address and data buffers. Generally not needed in the buffered mode. When low, external buffers should be enabled to allow the host processor access to the B61580RH's RAM and registers.
68	+5VA	I	CH. A +5V Supply
69	GNDA	I	Ground
70	$\overline{\text{TX\_INH\_A}}$	I	Transmitter inhibit inputs for the Channel A MIL-STD-1553 transmitters. For normal operation, these inputs should be connected to logic "0". To force a shutdown of Channel A, a value of logic "1" should be applied to the respective TX_INH input.

Appendix 2

B61580RH SPECIFICATIONS				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
ABSOLUTEMAXIMUMRATING				
Supply Voltage				
Logic +5V	-0.3		7.0	V
Transceiver +5V	-0.3		7.0	V
Logic				
Voltage Input Range	-0.3		Vcc+0.5	V
RECEIVER				
Differential Input Resistance	2.5			kΩ
Differential Input Capacitance			5	pF
Threshold Voltage, TransformerCoupled, Measured on Stub	0.20		0.860	Vp-p
Common Mode Voltage	0		10	Vpeak
TRANSMITTER				
Differential Output Voltage				
Direct Coupled Across 35 Ω Measured on Bus	6	7	9	V
Transformer Coupled Across70 Ω, Measured on Bus	18		27	V
Output Noise, Differential (Direct Coupled)			10	mV
Output Offset Voltage, Transformer Coupled Across 70 ohms	-250		250	mV
Rise/Fall Time	100	150	300	ns
LOGIC				
V_{IH}	2.4			V
V_{IL}			0.8	V
I_{IH} (V_{CC}=5.5V, V_{IN}=5.5V)	-10		10	uA
I_{IH} (V_{CC}=5.5V, V_{IN}=2.7V)				
SSFLAG/EXT_TRIG	-692		-84	uA
All Other Inputs	-346		-42	uA
I_{IL} (V_{CC}=5.5V, V_{IN}=0.4V)				
SSFLAG/EXT_TRIG	-794		-100	uA
All Other Inputs	-397		-50	uA

V_{OH} (V_{CC}=4.5V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OH}=max)	2.4			V
V_{OL} (V_{CC}=4.5V, V_{IH}=2.7V, V_{IL}=0.2V, I_{OL}=max)			0.4	V
I_{OL}				mA
D15-D0，V_{CC}=5.0V	6.4			mA
INCMD,INT,MEMENA_OUT,READYD,IOEN,TXA,TXA_,TXB,TXB_ ，				
V_{cc}=5.0V	3.2			mA
I_{OH}				
D15-D0，V_{CC}=5.0V			-6.4	mA
INCMD,INT,MEMENA_OUT,READYD,IOEN,TXA,TXA_,TXB,TXB_ ，				
V_{cc}=5.0V			-3.2	mA
POWER SUPPLY REQUIREMENTS				
Voltages/Tolerances				
+5V (Logic)	4.5	5.0	5.5	V
+5V (Ch.A, Ch.B)	4.75	5.0	5.25	V
Current Drain (Total Hybrid)				
Idle		95	200	mA
25% Transmitter Duty Cycle		175	350	mA
50% Transmitter Duty Cycle		260	500	mA
100% Transmitter Duty Cycle		470	800	mA
reliability parameter				
ESD	1000			V
LATCH UP	200			mA
CLOCK INPUT				
Frequency				
Nominal Value (programmable)				
Default Mode		16.0		MHz
Option		12.0		MHz
Long Term Tolerance				
1553A Compliance			0.01	%
1553B Compliance			0.1	%
Short Term Tolerance,1 second				
1553A Compliance			0.001	%
1553B Compliance			0.01	%

Duty Cycle				
16 MHz	33		67	%
12 MHz	40		60	%
1553 MESSAGETIMING				
Completion of CPU Write (BC Start-to-Start of Next Message)		2.5		us
BC Intermessage Gap		9.5		us
BC/RT/MT Response Timeout				
18.5 nominal	17.5	18.5	19.5	us
22.5 nominal	21.5	22.5	23.5	us
50.5 nominal	49.5	50.5	51.5	us
128.0 nominal	127.	128.	131.0	us
Transmitter Watchdog Timeout	0	0	7	us
RT Response Timeout	4			us
		668		
THERMAL				
Thermal Resistance, Junction-to-Case,Hottest Die			6.8	℃/W
Operating Junction Temperature	-55		150	℃
Storage Temperature	-65		150	℃
Lead Temperature (soldering, 10 sec.)			300	℃
PHYSICAL CHARACTERISTICS				
Size	1.9×1.0×0.165			in.
	48.3×25.4×4.19			mm
Weight	18.5			g

Appendix 3

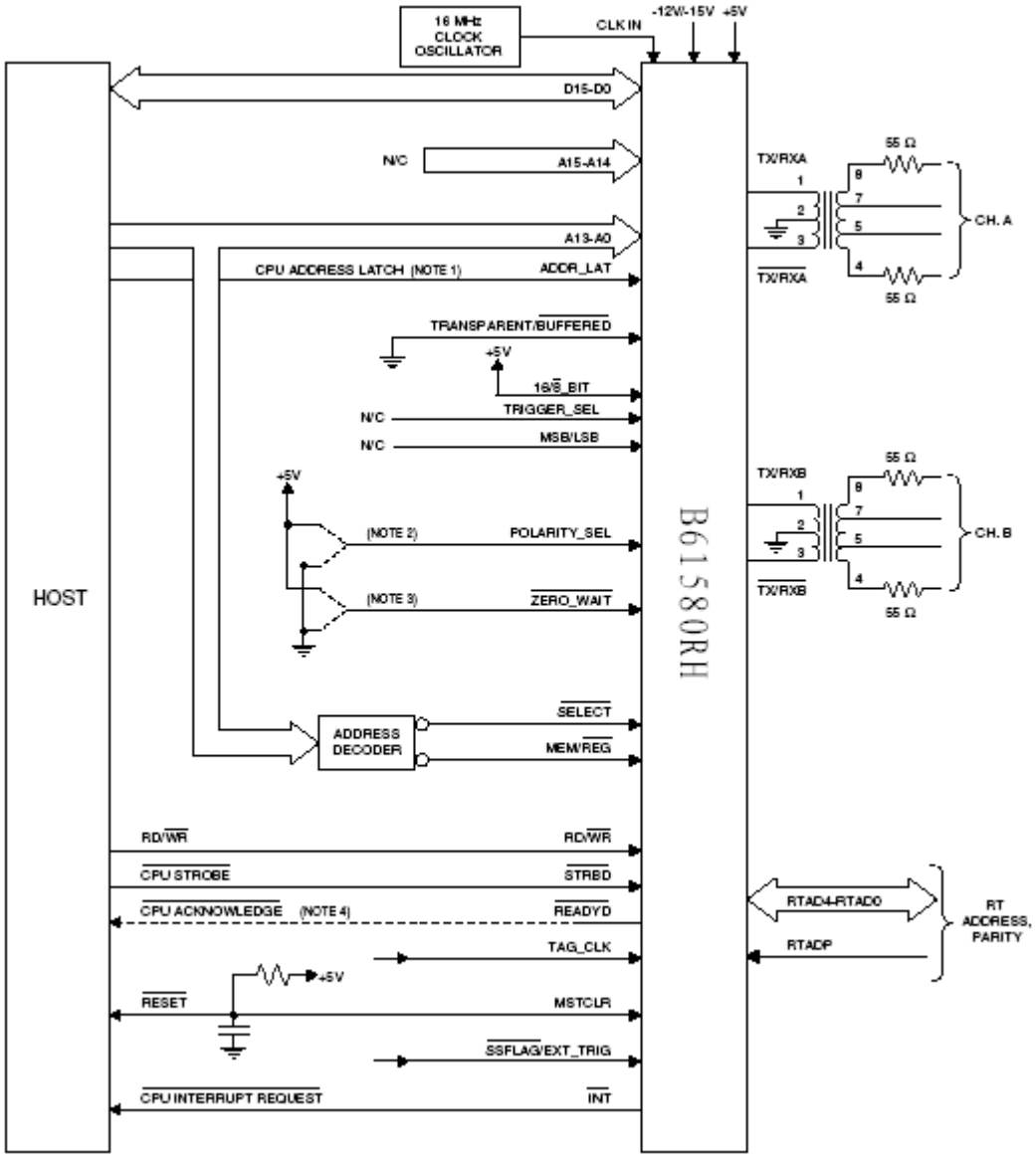


FIGURE 9 16-BIT BUFFERED MODE

NOTES:

1. CPU ADDRESS LATCH SIGNAL PROVIDED BY PROCESSORS WITH MULTIPLEXED ADDRESS/DATA BUSES.

2. IF POLARITY_SEL = "1", RD/WR IS HIGH TO READ, LOW TO WRITE.IF POLARITY_SEL = "0", RD/WR IS LOW TO READ,HIGH TO WRITE.

3. ZERO_WAIT SHOULD BE STRAPPED TO LOGIC "1" FOR NON-ZERO WAIT INTERFACE AND TO LOGIC "0" FOR ZERO WAIT INTERFACE.

4. CPU ACKNOWLEDGE PROCESSOR INPUT ONLY FOR NON-ZERO WAIT TYPE OF INTERFACE.

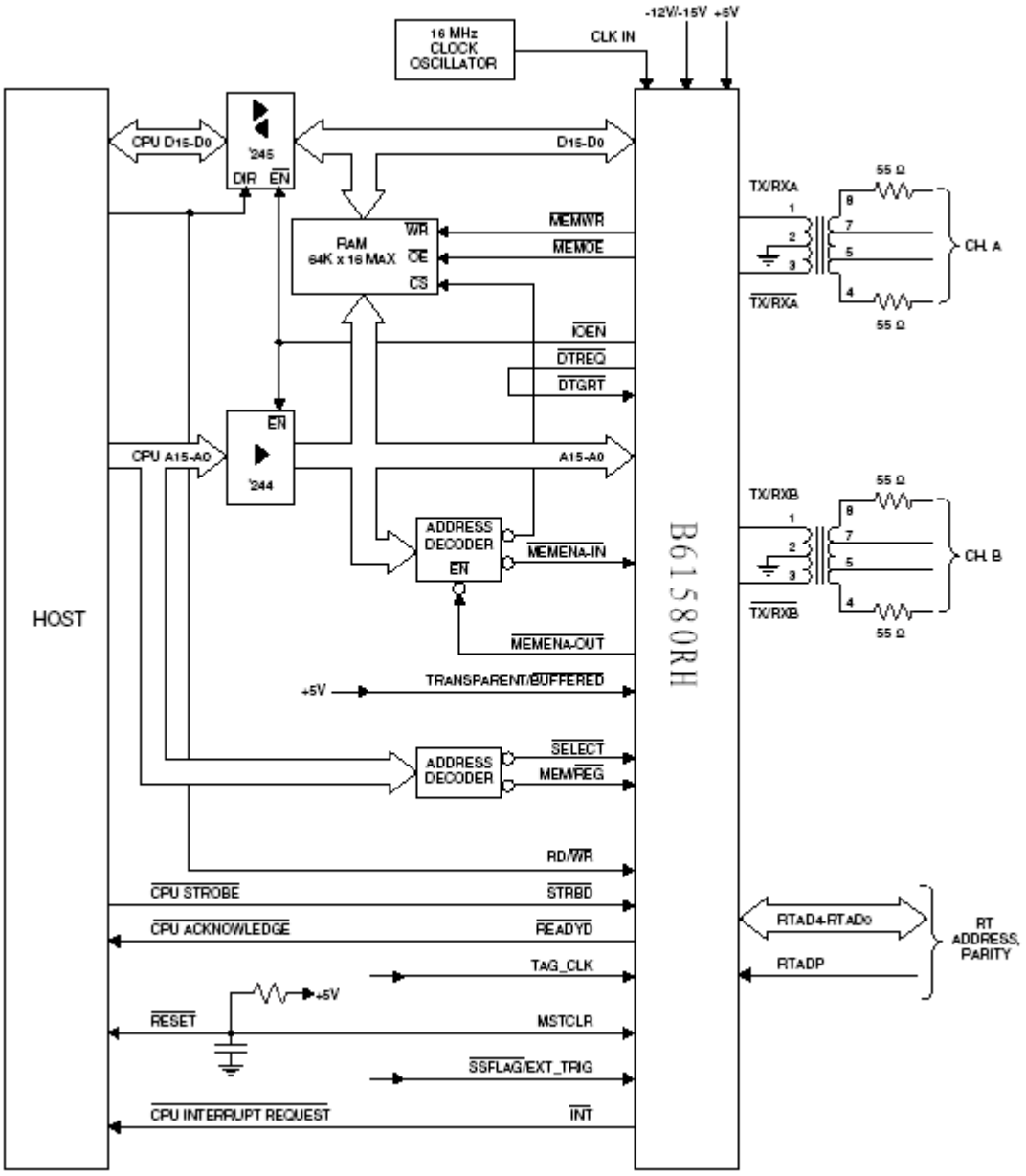


FIGURE 10 16-BIT TRANSPARENT MODE

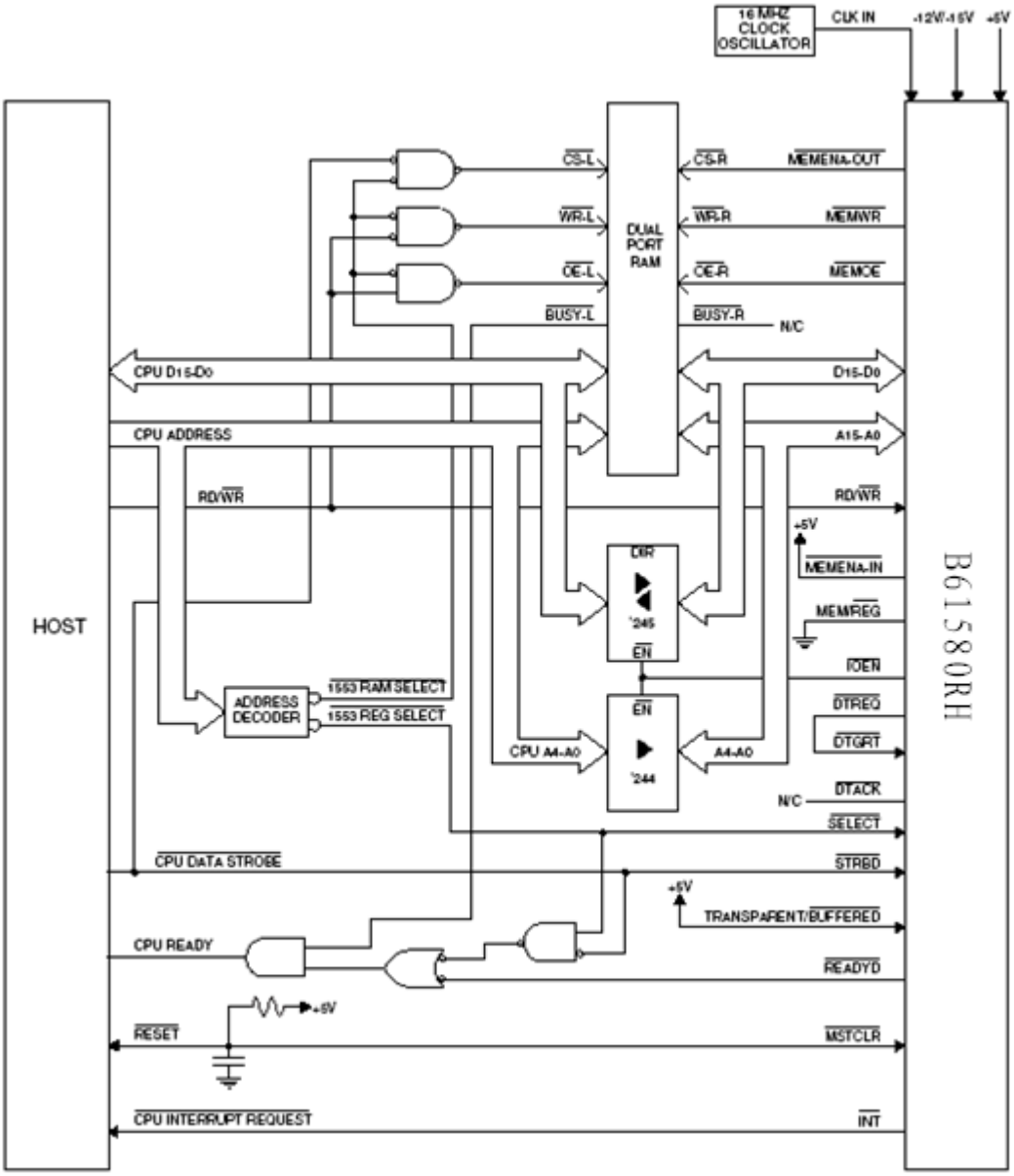


FIGURE 11 16-BIT TRANSPARENT MODE USING DUAL PORT RAM

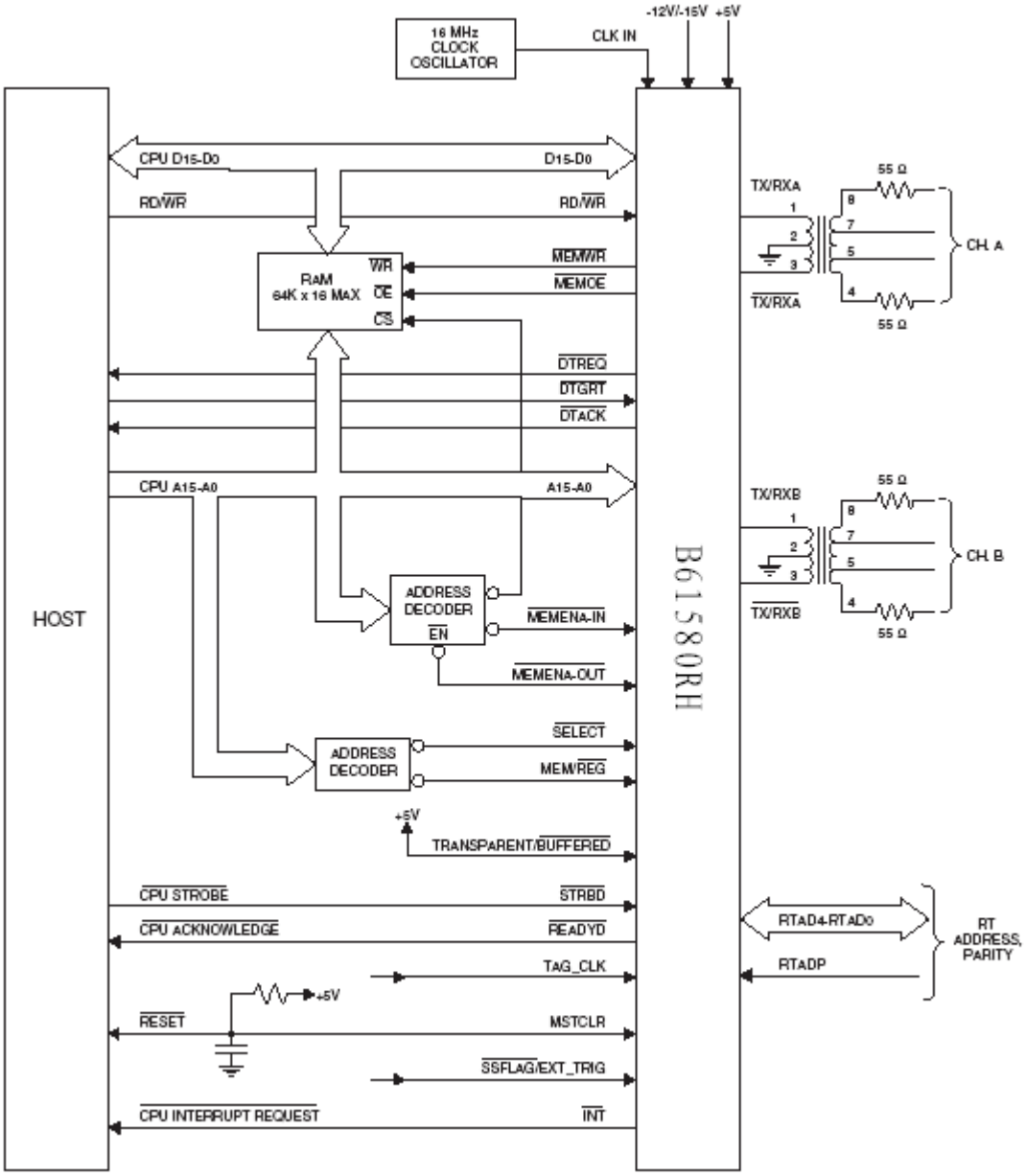


FIGURE 12 16-BIT DIRECT MEMORY ACCESS(DMA) MODE

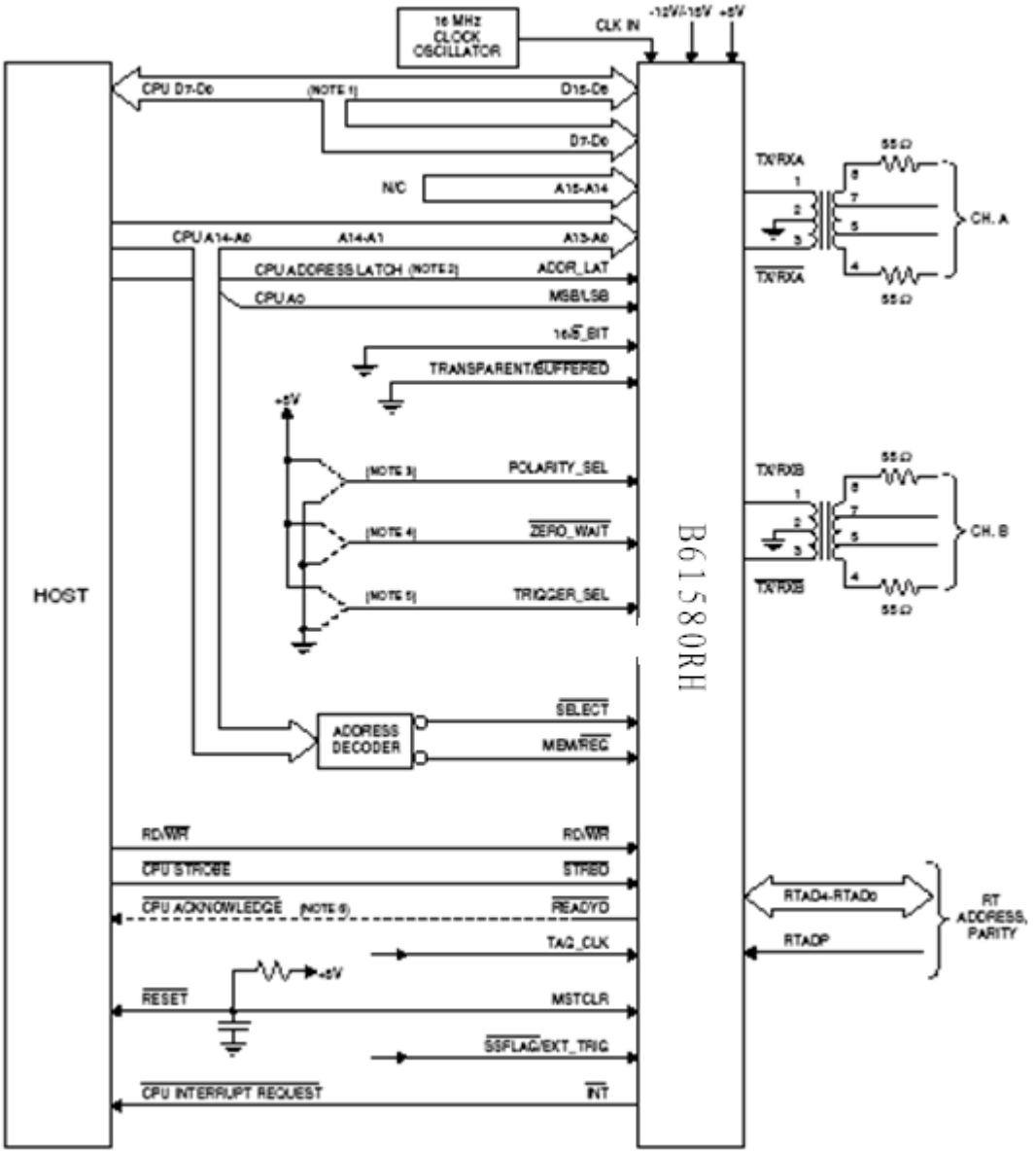
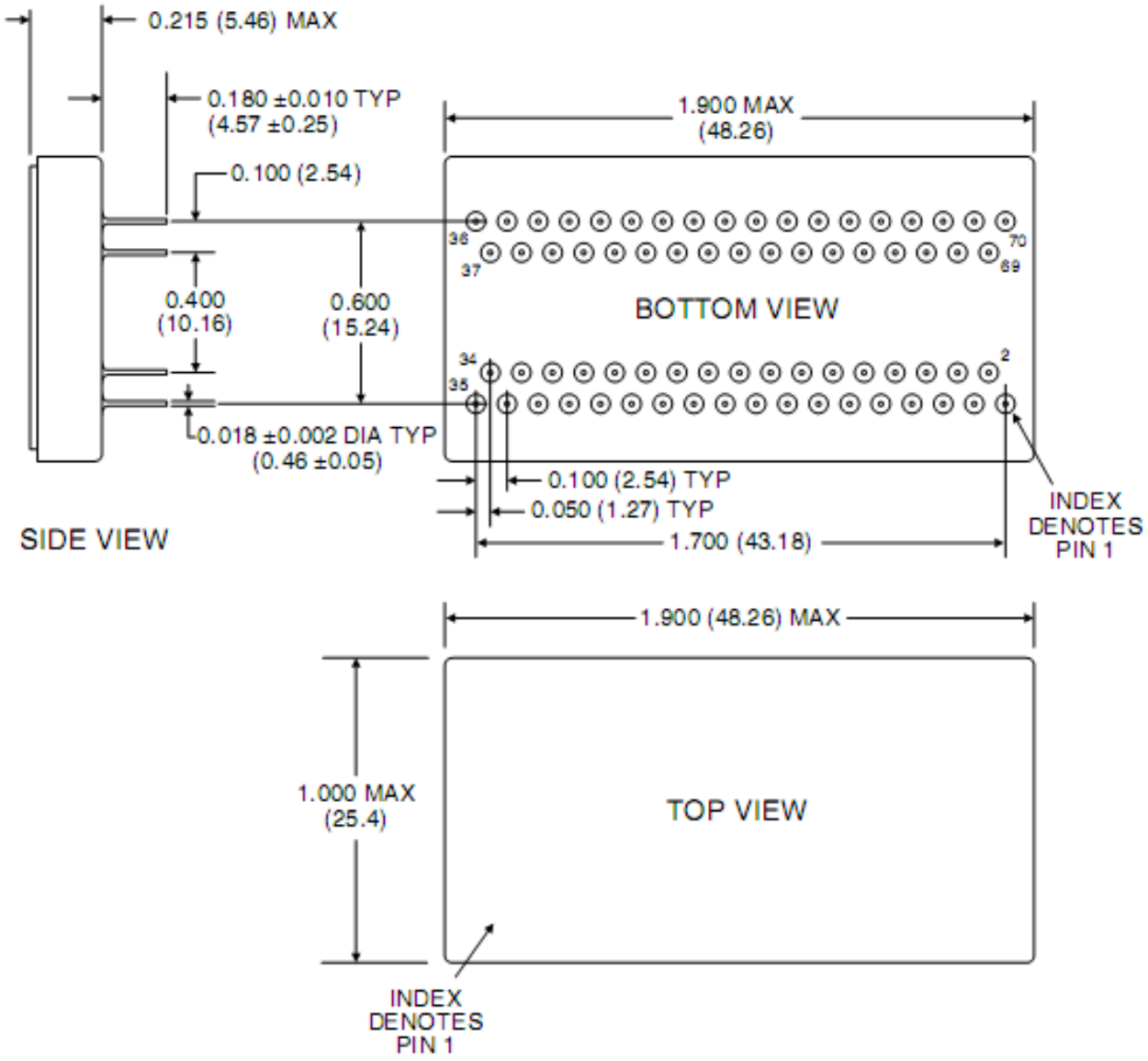


FIGURE 13 8-BIT BUFFERED MODE

Appendix 4


0.215 (5.46) MAX
0.180 ±0.010 TYP
(4.57 ±0.25)
0.100 (2.54)
0.400
(10.16)
0.600
(15.24)
0.018 ±0.002 DIA TYP
(0.46 ±0.05)
SIDE VIEW
1.900 MAX
(48.26)
36
37
70
69
BOTTOM VIEW
34
35
2
0.100 (2.54) TYP
0.050 (1.27) TYP
1.700 (43.18)
INDEX
DENOTES
PIN 1
1.900 (48.26) MAX
1.000 MAX
(25.4)
TOP VIEW
INDEX
DENOTES
PIN 1

Appendix 5

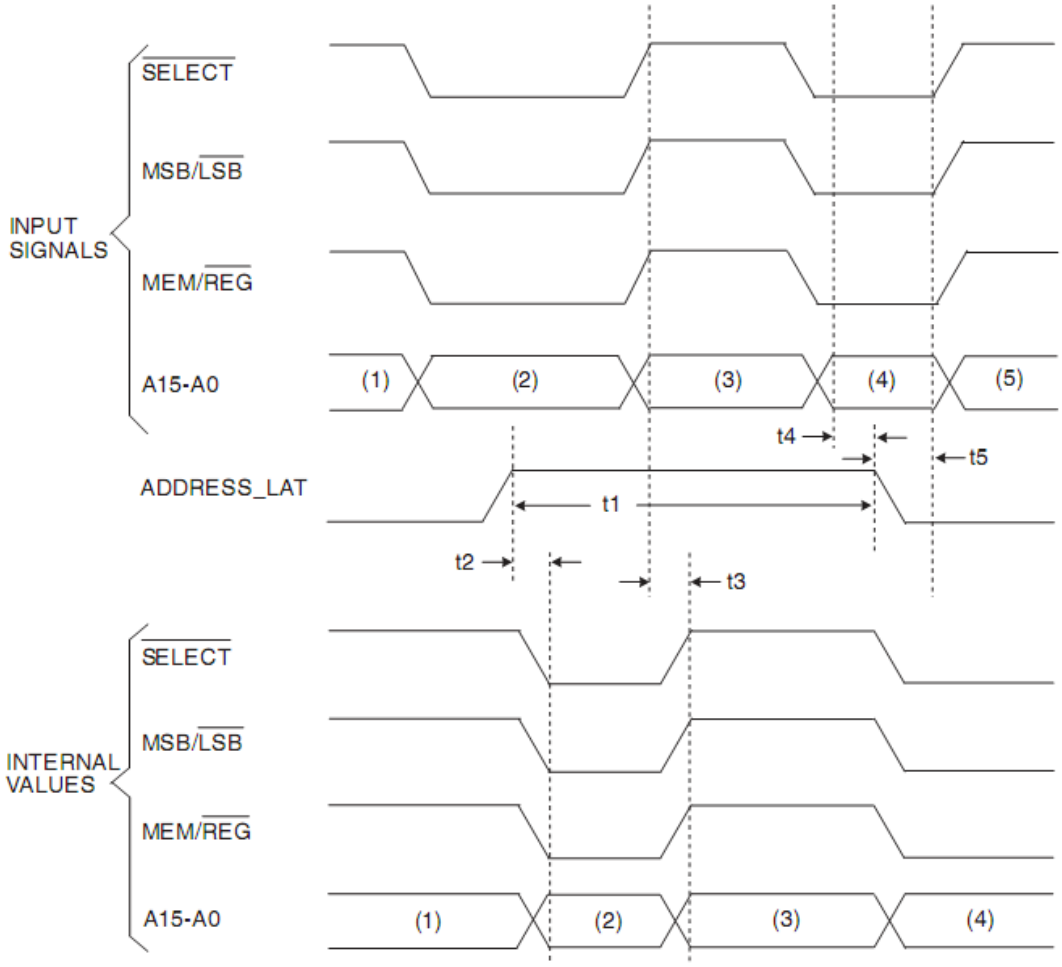


FIGURE 14 ADDRESS LATCH TIMING

Notes for FIGURE 14 and associated table.

1.Applicable to buffered mode only.Address SELECTAND MEM/REG latches are always transparent in the transparent mode of operation.

2.Latches are transparent when ADDR_LAT is high.Internal values do not update when ADDR_LAT is low.

3.MSB/LSB input signal is applicable to 8-bit mode only (16/8 input = logic “0”).MSB/LSB input is a “don’t care”for 16-bit operation.

TABLE FOR FIGURE 14.ADDRESS LATCH TIMING					
REF	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1	ADDR_LAT pulse width	20	—	—	ns
t	ADDR_LAT high delay to internal signals valid	—	—	10	ns
t3	Propagation delay from external input signals to internal signals valid	—	—	10	ns
t4	Input setup time prior to falling edge of ADDR_LAT	10	—	—	ns
t5	Input hold time following falling edge of ADDR_LAT	20	—	—	ns

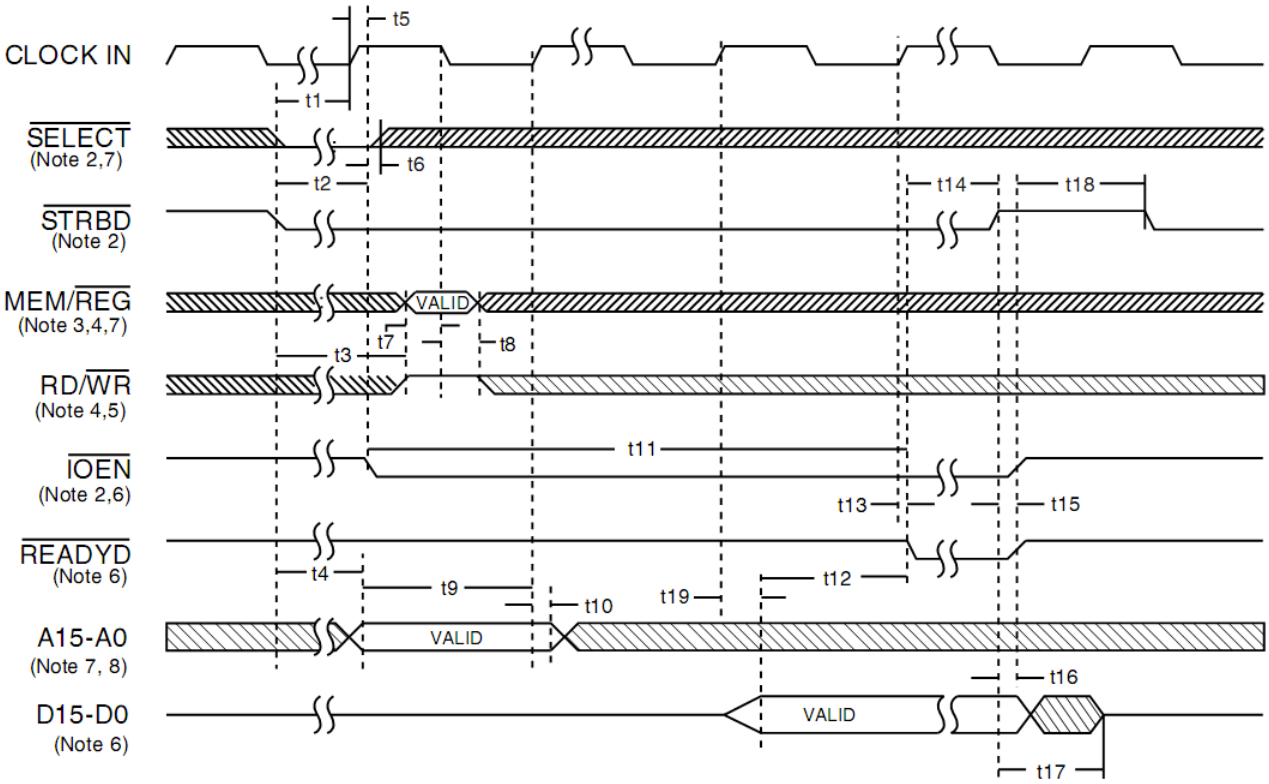


FIGURE 15 CPU READING RAM (SHOWN FOR 16-BIT,BUFFERED,NONZERO WAIT MODE)

CPU READING RAM OR REGISTERS (SHOWN FOR 16-BIT,BUFFERED,NONZERO WAIT MODE)					
REF	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge	10			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access @ 16 MHz)			107.5	ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (contended access @ 12 MHz)			128.3	μs

t3	MEM/ $\overline{\text{REG}}$, RD/WR setup time following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low(@ 16 MHz)			10	ns
t3	MEM/ $\overline{\text{REG}}$, RD/WR setup time following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low(@ 12 MHz)			20	ns
t4	Address valid setup time following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 16 MHz)			30	ns
t4	Address valid setup time following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 12 MHz)			50	ns
t5	CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge			35	ns
t6	$\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling	0			ns
t7	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge	10			ns
t8	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ hold time prior to CLOCK IN falling edge	30			ns
t9	Address valid setup time prior to CLOCK IN rising edge	30			ns
t10	Address hold time following CLOCK IN rising edge	30			ns
t11	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (reading RAM @ 16 MHz)	170	187.5	205	ns
t11	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (reading RAM @ 12 MHz)	235	250	265	ns
t11	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (reading registers @ 16 MHz)	170	187.5	205	ns
t11	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (reading registers @ 12 MHz)	235	250	265	ns
t12	Output Data valid prior to $\overline{\text{READYD}}$ falling (@ 16 MHz)	33			ns
t12	Output Data valid prior to $\overline{\text{READYD}}$ falling (@ 12 MHz)	54			ns
t13	CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling			35	ns
t14	$\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time			∞	ns
t15	$\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ rising edge and $\overline{\text{READYD}}$ rising edge			30	ns
t16	Output Data hold time following $\overline{\text{STRBD}}$ rising edge	0			ns
t17	$\overline{\text{STRBD}}$ rising delay to output Data tri-state			40	ns
t18	$\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising	0			ns
t19	CLOCK IN rising edge delay to Output Data valid			60	ns

Notes for FIGURE 15 and associated table.

1.For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5 V or GND.For the nonzero wait interface ZEROWAIT, must be connected to logic "1".

2.SELECT and STRBD may be tied together.IOEN goes low on the first rising CLK edge when SELECT and STRBD is sampled low(satisfying t2) and the B61580RH's protocol/memory management logic is not accessing the internal RAM.When this occurs, IOEN goes low, starting the transfer cycle.After IOEN goes low,SELECT may be released high.

3.MEM/REG must be presented high for memory access, low for register access.

4.MEM/REG and RD/WR are buffered transparently until the first falling edge of CLK after IOEN goes low.After this CLK edge,MEM/REG and RD/WR become latched internally.

5.The logic sense for RD/WR in the diagram assumes that POLARITY_SEL is connected to

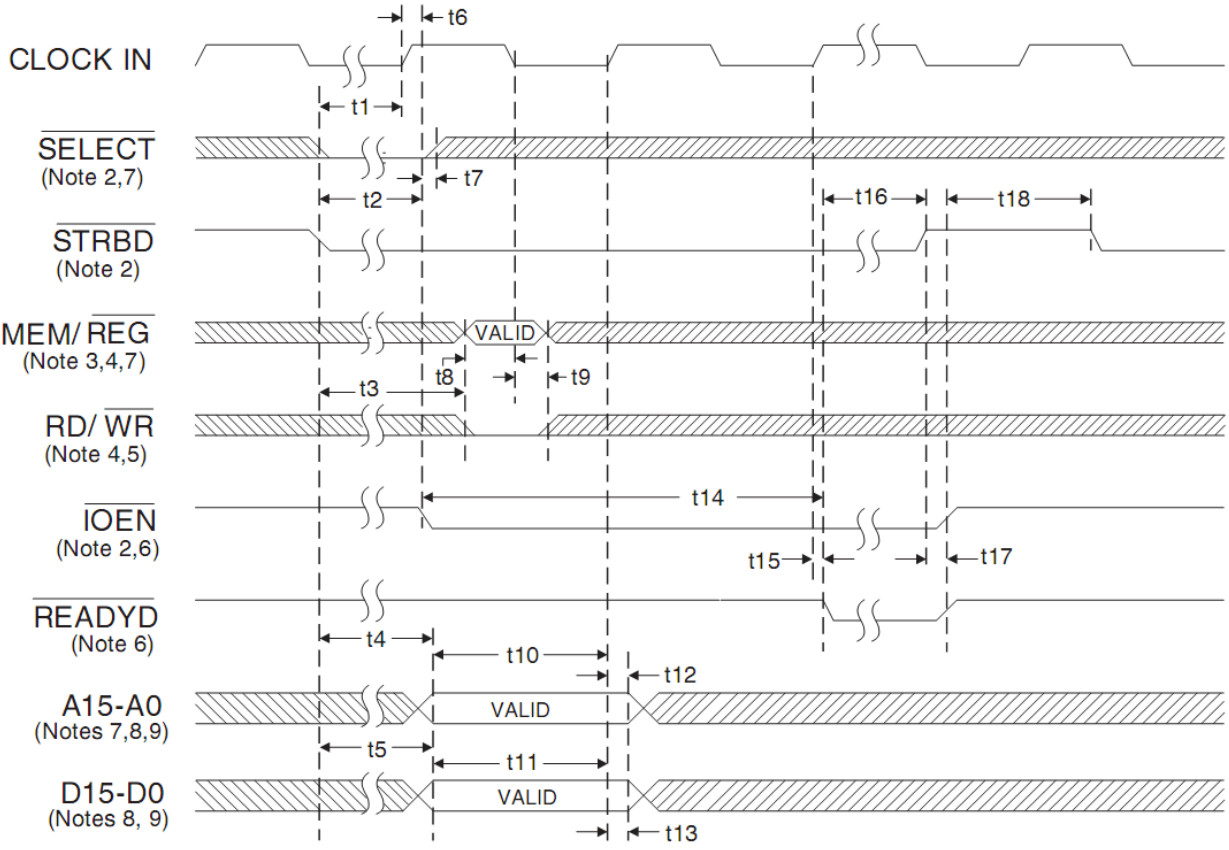


FIGURE 16 CPU WRITING RAM (SHOWN FOR 16-BIT,BUFFERED,NONZERO WAIT MODE)

CPU WRITING RAM OR REGISTERS (SHOWN FOR 16-BIT,BUFFERED,NONZERO WAIT MODE)					
REF	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNITS**
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time prior to clock rising edge	10			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (uncontended access @ 16 MHz)			107.5	ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low delay to $\overline{\text{IOEN}}$ low (contended access @ 12 MHz)			128.3	μs
t3	MEM/ $\overline{\text{REG}}$, RD/ $\overline{\text{WR}}$ setup time following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low(@ 16 MHz)			10	ns
t3	MEM/ $\overline{\text{REG}}$, RD/ $\overline{\text{WR}}$ setup time following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low(@ 12 MHz)			20	ns
t4	Address valid setup time following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 16 MHz)			30	ns
t4	Address valid setup time following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 12 MHz)			50	ns
t5	Input Data valid setup following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 16 MHz)			50	
t5	Input Data valid setup following $\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low (@ 12 MHz)			70	ns
t6	CLOCK IN rising edge delay to $\overline{\text{IOEN}}$ falling edge			35	ns
t7	$\overline{\text{SELECT}}$ hold time following $\overline{\text{IOEN}}$ falling	0			ns
t8	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ setup time prior to CLOCK IN falling edge	10			ns
t9	MEM/$\overline{\text{REG}}$, RD/$\overline{\text{WR}}$ hold time prior to CLOCK IN falling edge	30			ns
t10	Address valid setup time prior to CLOCK IN rising edge	30			ns
t11	Input Data valid setup prior to CLOCK IN rising edge	10			ns
t12	Address hold time following CLOCK IN rising edge	30			ns
t13	Input Data valid hold time following CLOCK IN rising edge	30			ns
t14	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 16 MHz)	170	187.5	205	ns
t14	$\overline{\text{IOEN}}$ falling delay to $\overline{\text{READYD}}$ falling (@ 12 MHz)	235	250	265	ns
t15	CLOCK IN rising edge delay to $\overline{\text{READYD}}$ falling edge			35	ns
t16	$\overline{\text{READYD}}$ falling to $\overline{\text{STRBD}}$ rising release time			∞	ns
t17	$\overline{\text{STRBD}}$ rising delay to $\overline{\text{IOEN}}$ rising, $\overline{\text{READYD}}$ rising			30	ns

t18	$\overline{\text{STRBD}}$ high hold time following $\overline{\text{READYD}}$ rising	0			ns

Notes for FIGURE 16 and associated table.

1.For the 16-bit buffered configuration, the inputs TRIGGER_SEL and MSB/LSB may be connected to +5 V or GND.For the nonzero wait interface,ZEROWAIT must be connected to logic “1.”

2.SELECT and STRBD may be tied together.IOEN goes low on the first rising CLK edge when SELECT

and STRBD is sampled low (satisfying t2) and the B61580RH’s protocol/memory management logic is not accessing the internal RAM.When this occurs, IOEN goes low, starting the transfer cycle.After IOEN goes low, SELECT may be released high.

3.MEM/REG must be presented high for memory access, low for register access.

4.MEM/REG and RD/WR are buffered transparently until the first falling edge of CLK after IOEN goes low.After this CLK edge,MEM/REG and RD/WR become latched internally.

5.The logic sense for RD/WR in the diagram assumes that POLARITY_SEL is connected to logic “1”.If POLARITY_SEL is connected to logic "0", RD/WR must be asserted high to read.

6.The timing for the IOEN and READYD outputs assumes a 50 pf load.For loading above 50 pf, the validity of IOEN and READYD is delayed by an additional 0.14 ns/pf typ, 0.28 ns/pf max.

7.Timing for A15-A0 assumes ADDR-LAT is connected to logic “1”.Refer to Address Latch timing for additional details.

8.Internal RAM is accessed by A13 through A0.Registers are accessed by A4 through A0.

9.The address bus A15-A0 and data bus D15-D0 are internally buffered transparently until the first rising edge of CLK after IOEN goes low.After this CLK edge, A15-A0 become latched internally.

Service and Support：

Service and Support：

Address： No.2 Siyingmen N. Road. Donggaodi. Fengtai District.Beijing.China.

Department： Department of international cooperation

Telephone：+86(0)10-67968115-6751

Email：gjhz@mxtronics.com

Fax：+86(0)10-68757706

Zip code：100076