

Ver 1.3

## Radiation-Hardened SRAM

# Datasheet

**Part Number: B8CR1M39RH**



**北京微电子技术研究所**

Beijing Microelectronics Technology Institute

## Page of Revise Control

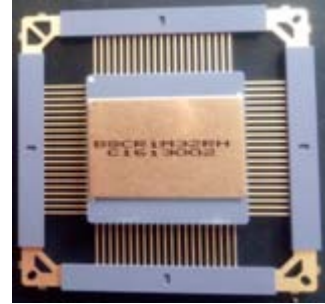
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## 1. Features

- 20 ns maximum read time
- 10 ns minimum write time
- Asynchronous operation
- CMOS compatible inputs and output levels,  
three-state bidirectional data bus
- I/O Voltage 3.3 V, 1.2 V core
- ESD better than 2000 V
- Operational environment:
  - Total-dose: 100 K Rad (Si)
  - SEL Immune: > 75 MeV·cm<sup>2</sup>/mg
  - SEU Error Rate=1E-10errors/bit-day in Geosynchronous Orbit
- Packaging options
  - 84-lead ceramic quad flatpack (CQFP84)



## 2. General Description

The B8CR1M39RH is a high-performance radiation-hardened CMOS static SRAM organized as 1024K words by 40 bits. Fabricated with industry-standard CMOS technology, the device works in asynchronous mode and requires no external clocks. The combination of radiation-hardness, fast access time, and low power consumption makes the B8CR1M39RH ideal for high speed system designed for operation in radiation environments.

### 3. Block Diagram

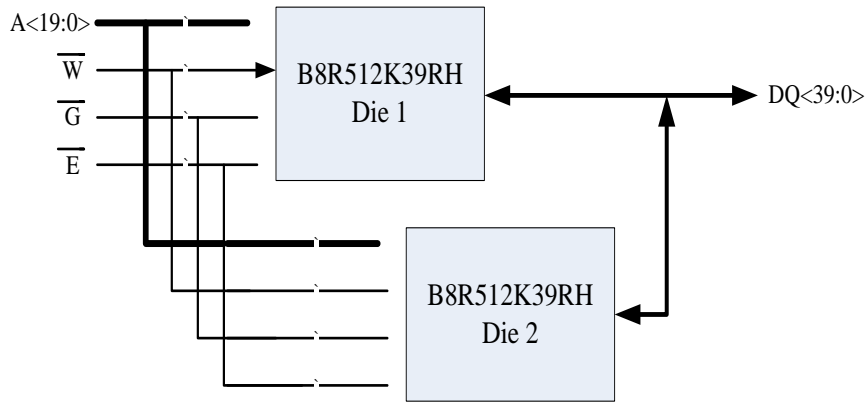


Figure 1. B8CR1M39RH Block Diagram

### 4. Pin Description

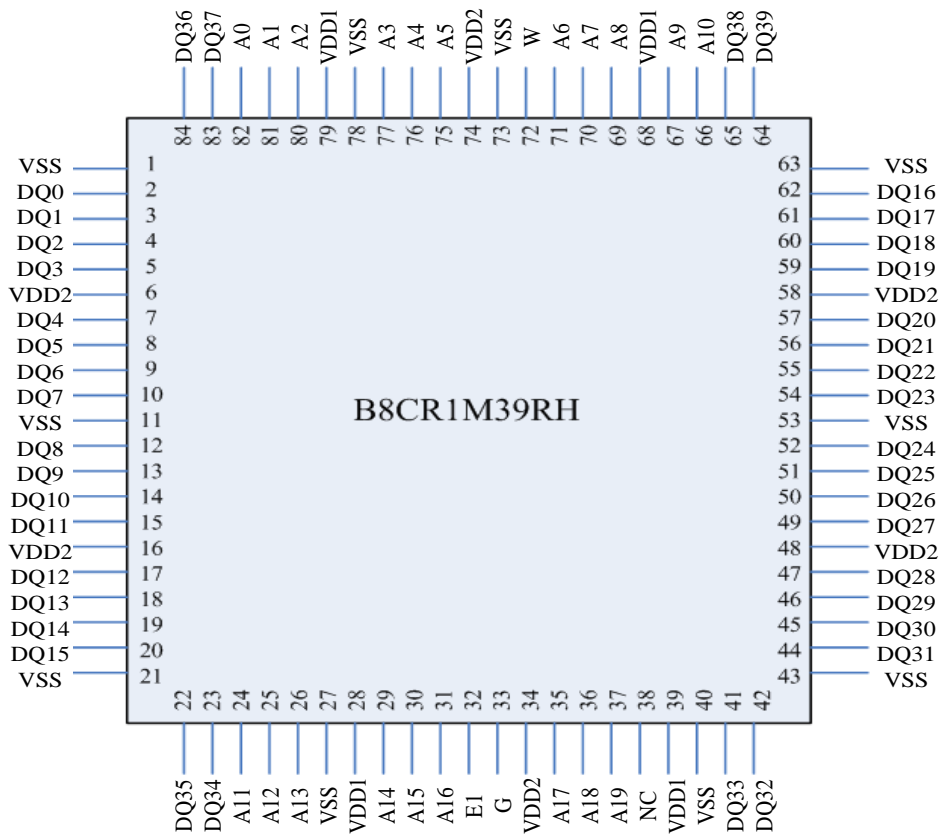


Figure 2. B8CR1M39RH SRAM Pinout

Table 1. Pin Name

Pin Names	Functions
A0~A19	Address
DQ0~DQ39	Data Input / Output
$\bar{E}$	Chip Enable (Active Low)
$\bar{W}$	Write Enable (Low Write Enable, and High Read Enable)
$\bar{G}$	Output Enable (Active Low)
V <sub>DD1</sub>	Power (1.2 V)
V <sub>DD2</sub>	Power (3.3 V)
V <sub>SS</sub>	Ground
NC	No Connect

## 5. Pin Configurations (Appendix 1)

## 6. Product Description

### 6.1 Quality Grade and Production Standard

The quality grade of the radiation-hardened SRAM B8CR1M39RH is GJB597A-1996 B. And B8CR1M39RH is up to the HX 64082A-2017 space application semiconductor IC standard.

### 6.2 Function Description

The B8CR1M39RH has three control inputs, Chip Enable  $\bar{E}$ , Write Enable  $\bar{W}$ , and Output Enable ( $\bar{G}$ ), 20 address inputs A (19:0), and 40 data lines, DQ0~DQ39.

Table 2. Device Operation Truth Table

Inputs			Outputs	
$\overline{G}$	$\overline{W}$	$\overline{E}$	I/O Mode	Mode
X	X	1	DQ(39:0) 3-State	Standby
X	0	0	DQ(39:0) Data in	Write
0	1	0	DQ(39:0) Data out	Read
1	1	0	DQ(39:0) 3-State	Read DQ 3-State
Notes: 1. X = Don't care				

◆ **Read Cycle**

A combination of  $\overline{W}$  greater than  $V_{IH}(\min)$  and  $\overline{E}$  less than  $V_{IL}(\max)$  defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 4, is initiated by a change in address inputs while the chip is enabled with  $\overline{G}=0$ ,  $\overline{W}=1$ . Valid data appears on data outputs DQ(39:0) after the specified  $t_{AVQV}$  is satisfied. Outputs remain active throughout the entire cycle. As long as chip enables and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time ( $t_{AVAV}$ ).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 5, is initiated by  $\overline{G}=0$ ,  $\overline{W}=1$ , and the addresses remain stable for the entire cycle. After the specified  $t_{ETQV}$  is satisfied, the word addressed by A(19:0) is accessed and appears at the data outputs DQ(39:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 6, is initiated by  $\overline{E}=0$ ,  $\overline{W}=1$ , and the addresses are stable. Read access time is  $t_{GLQV}$  unless  $t_{AVQV}$  or  $t_{ETQV}$  have not been satisfied.

◆ **Write Cycle**

A combination of  $\overline{W}$  and  $\overline{E}$  less than  $V_{IL}(\max)$  defines a write cycle. The state of  $\overline{G}$  is a “don't care” for a write cycle. The outputs are placed in the high-impedance state when either  $\overline{G}$  is greater than  $V_{IH}(\min)$ , or when  $\overline{W}$  is less than  $V_{IL}(\max)$ .

Write Cycle 1, the Write Enable-controlled Access in Figure 7, is defined by a write terminated by  $\overline{W}$  going high, with  $\overline{E}=0$ . The write pulse width is defined by  $t_{WLWH}$  when the write is initiated by  $\overline{W}$ , and by  $t_{ETWH}$  when the write is initiated by  $\overline{E}$ . Unless the outputs have been previously placed in the high-impedance state by  $\overline{G}$ , the

user must wait  $t_{WLQZ}$  before applying data to the pins DQ(39:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 8, is defined by a write terminated by  $\overline{E}$  going inactive. The write pulse width is defined by  $t_{WLEF}$  when the write is initiated by  $\overline{W}$ , and by  $t_{ETEF}$  when the write is initiated by  $\overline{E}$  going active. For the  $\overline{W}$  initiated write, unless the outputs have been previously placed in the high-impedance state by  $\overline{G}$ , the user must wait  $t_{WLQZ}$  before applying data to the pins DQ(39:0) to avoid bus contention.

### 6.3 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Limits
$V_{DD1}$	Core supply voltage	-0.3V ~ +1.35 V
$V_{DD2}$	I/O supply voltage	-0.3V ~ +3.8 V
$V_{IO}$	Voltage on any pin	-0.3V ~ +3.8 V
$T_{STG}$	Storage Temperature	-65°C ~ 150°C
$P_D$	Maximum power dissipation	2W
$T_J$	Maximum junction temperature	+175°C
$R_{th(J-C)}$	Thermal resistance, junction-to-case	5°C/W

### 6.4 Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Limits
$V_{DD1}$	Core supply voltage	1.08 V ~ 1.32V
$V_{DD2}$	I/O supply voltage	2.97 V ~ 3.63 V
$T_C$	Case temperature range	-55°C ~ +125°C
$V_I$	DC input voltage	0 V ~ $V_{DD2}$

Notes: The correct power-up sequence should be  $V_{DD1} \rightarrow V_{DD2}$ .



## 7. Electrical Characteristics

### 7.1 DC Electrical Characteristics (Pre and Post-Radiation)

Table 5. DC Parameter Table ( I )

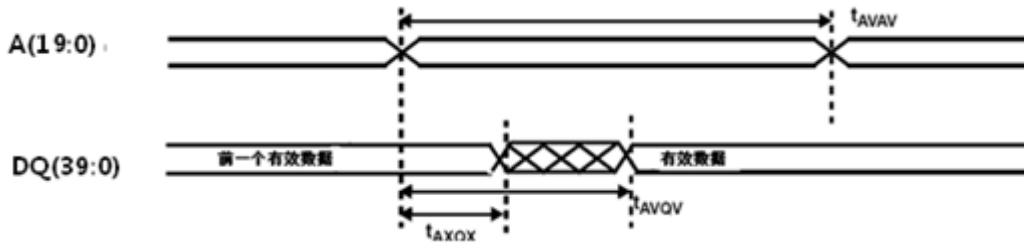
Parameter	Symbol	Condition (GND=0V, $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ) $1.7\text{V} \leq V_{DD1} \leq 1.9\text{V}$ 、 $3.0\text{V} \leq V_{DD2} \leq 3.6\text{V}$	Limits		UNIT	
			MIN	MAX		
High-level input voltage	$V_{IH}$		$.7 * V_{DD2}$ 2	—	V	
Low-level input voltage	$V_{IL}$		—	$.3 * V_{DD2}$ D2	V	
High-level output voltage	$V_{OH}$	$V_{DD2}=3\text{V}$ , $I_{OH}=-4\text{ mA}$ , all outputs needed are tested	$.8 * V_{DD2}$ 2	—	V	
Low-level output voltage	$V_{OL}$	$V_{DD2}=3\text{V}$ , $I_{OL}=8\text{ mA}$ , all outputs needed are tested	—	$.2 * V_{DD2}$ D2	V	
High-level input leakage current	$I_{IH}$	$V_{DD2}=3.6\text{V}$ , $V_{DD1}=1.9\text{V}$ , $V_I=3.6\text{V}$ , all inputs are tested	-2	2	$\mu\text{A}$	
Low-level input leakage current	$ I_{IL} $	$V_{DD2}=3.6\text{V}$ , $V_{DD1}=1.9\text{V}$ , $V_I=0\text{V}$ , all inputs are tested	-2	2	$\mu\text{A}$	
Three-state (high-level) output leakage current	$I_{OZH}$	$V_{DD2}=3.6\text{V}$ , $V_{DD1}=1.9\text{V}$ , $V_O=V_{DD2}$ , all bidirectional I/O are tested	-2	2	$\mu\text{A}$	
Three-state (low-level) output leakage current	$ I_{OZL} $	$V_{DD2}=3.6\text{V}$ , $V_{DD1}=1.9\text{V}$ , $V_O=0$ , all bidirectional I/O are tested	-2	2	$\mu\text{A}$	
VDD1 Supply current read operation @ 1MHz	$I_{DD1(OP1)}$	CMOS inputs :	$V_{DD1}=1.32\text{V}$	—	90	mA
		$V_{IL}=V_{SS}+0.2\text{V}$ , $V_{IH}=V_{DD2}-0.2\text{V}$ , $I_{OUT}=0$ $V_{DD2}=V_{DD2}(\text{max})$	$V_{DD1}=1.2\text{V}$	—	80	mA

VDD1 Supply current read operation @ 50MHz	$I_{DD1(OP2)}$	CMOS inputs : $V_{IL}=V_{SS}+0.2V$ $V_{IH}=V_{DD2}-0.2V, I_{OUT}=0,$ $V_{DD2}= V_{DD2}(max)$	$V_{DD1}=1.32V$	—	110	mA
			$V_{DD1}=1.2V$	—	100	mA
VDD2 Supply current read operation @ 1MHz	$I_{DD2(OP1)}$	CMOS inputs: $V_{IL}=V_{SS}+0.2V$ $V_{IH}=V_{DD2}-0.2V, I_{OUT}=0,$ $V_{DD2}= V_{DD2}(max), V_{DD1}= V_{DD1}(max)$		—	5	mA
VDD2 Supply current read operation @ 50MHz	$I_{DD2(OP2)}$	CMOS inputs: $V_{IL}=V_{SS}+0.2V$ $V_{IH}=V_{DD2}-0.2V, I_{OUT}=0$ $V_{DD2}= V_{DD2}(max), V_{DD1}= V_{DD1}(max)$		—	5	mA
Supply current standby @0Hz	$I_{DD1(SB)}$	CMOS inputs $I_{OUT}=0 \bar{E} = V_{DD} -0.2V$ $V_{DD2}= V_{DD2}(max), V_{DD1}= V_{DD1}(max)$		—	90	mA
Supply current standby@0Hz	$I_{DD2(SB)}$	CMOS inputs $I_{OUT}=0 \bar{E} = V_{DD} -0.2V$ $V_{DD2}= V_{DD2}(max), V_{DD1}= V_{DD1}(max)$		—	3	mA
Supply current standby A<19:0>@50MHz	$I_{DD1(SB)}$	CMOS inputs $I_{OUT}=0 \bar{E} = V_{DD} -0.2V$ $V_{DD2}= V_{DD2}(max), V_{DD1}= V_{DD1}(max)$		—	90	mA
Supply current standby A<19:0>@50MHz	$I_{DD2(SB)}$	CMOS inputs $I_{OUT}=0 \bar{E} = V_{DD} -0.2V$ $V_{DD2}= V_{DD2}(max), V_{DD1}= V_{DD1}(max)$		—	3	mA
Note: * the post-irradiation performance is guaranteed at 25°C $V_{IH}=V_{DD2},$						

## 7.2 Read Cycle AC Electrical Characteristics (Pre and Post-Radiation)

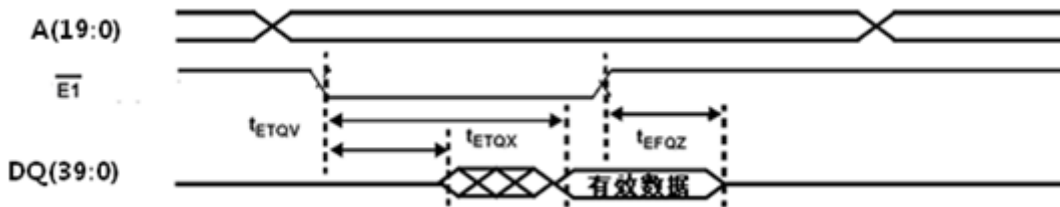
Table 6. Read Cycle AC Parameters

Parameter	Symbol	Condition ( $V_{DD1}=V_{DD1}(\min)$ , $V_{DD2}=V_{DD2}(\min)$ , $-55^{\circ}\text{C}\leq T_A\leq 125^{\circ}\text{C}$ )	Limits		UNIT
			MIN	MAX	
Read cycle time	$t_{AVAV}^1$	Figure 4	20	—	ns
Address to data valid	$t_{AVQV}$		—	20	ns
Output hold time from address change	$t_{AXQX}^2$		3	—	ns
$\overline{G}$ -controlled output enable time	$t_{GLQX}^{2,1}$	Figure 6	2	—	ns
$\overline{G}$ -controlled output data valid	$t_{GLQV}$		—	10	ns
$\overline{G}$ -controlled output three-state time	$t_{GHQZ}^2$		2	8	ns
$\overline{E}$ -controlled output enable time	$t_{ETQX}^{2,3}$	Figure 5	5	—	ns
$\overline{E}$ -controlled access time	$t_{ETQV}^3$		—	20	ns
$\overline{E}$ -controlled output three-state time	$t_{EFQZ}^{2,4}$		2	9	ns
Notes: * the post-irradiation performance is guaranteed at 25°C 1. Guaranteed but not tested. 2. Three-state is defined as a 200mV change from steady-state output voltage. 3. The ET (chip enable true) notation refers to the latter falling edge of $\overline{E}$ . 4. The EF (chip enable false) notation refers to the latter rising edge of $\overline{E}$ .					



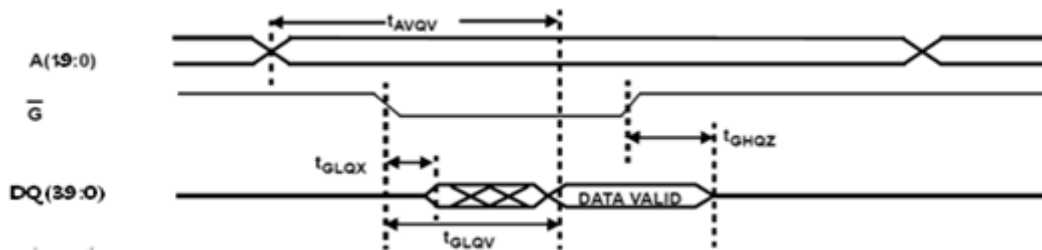
Assumptions:  $\overline{E} \leq V_{IL}(\max)$ ,  $\overline{G} \leq V_{IL}(\max)$ ,  $\overline{W} \geq V_{IH}(\min)$

Figure 4. SRAM Read Cycle 1: Address Access



Assumptions:  $\overline{G} \leq V_{IL}(\max)$ ,  $\overline{W} \geq V_{IH}(\min)$

Figure 5. SRAM Read Cycle 2: Chip Enable Access



Assumptions:  $\overline{E} \leq V_{IL}(\max)$ ,  $\overline{W} \geq V_{IH}(\min)$

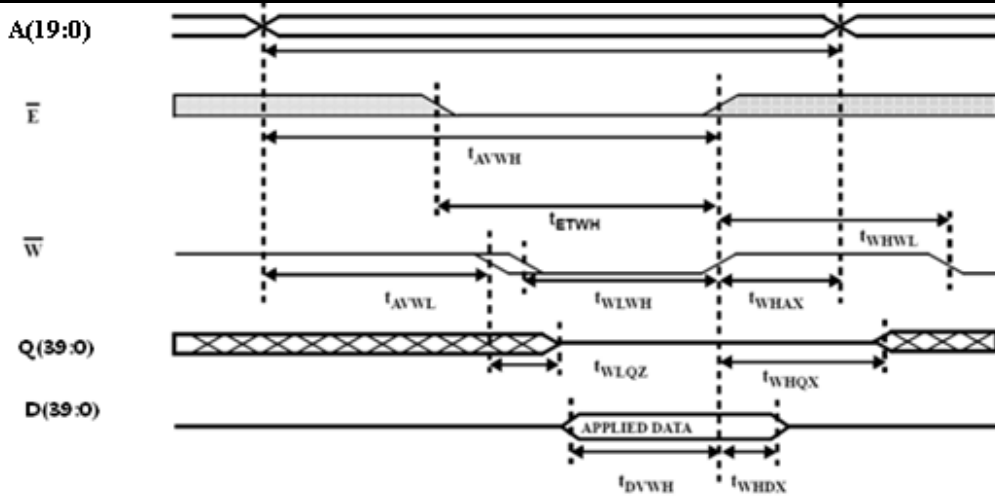
Figure 6. SRAM Read Cycle 3: Output Enable Access

### 7.3 Write Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 7. Write Cycle AC Parameter ( I )

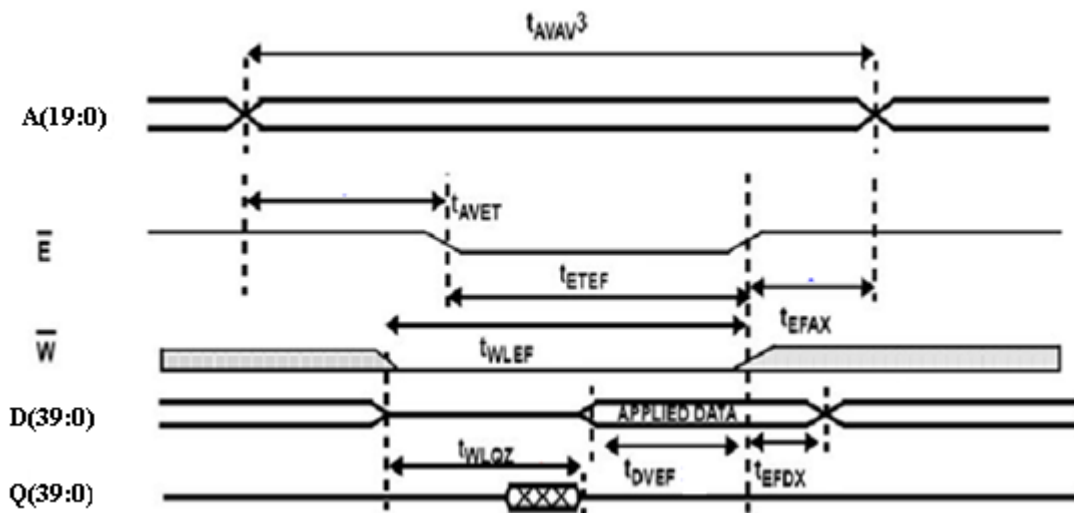
Parameter	Symbol	Condition ( $V_{DD1}=V_{DD1}(\min)$ , $V_{DD2}=V_{DD2}(\min)$ , $-55^{\circ}\text{C}\leq T_A\leq 125^{\circ}\text{C}$ )	Limits		UNIT
			MIN	MAX	
Write cycle time	$t_{AVAV}^1$	Figure 7 & Figure 8	10		ns
Chip enable to end of write	$t_{ETWH}$	Figure 7	6	—	ns
Address setup time for write ( $\overline{E}$ controlled)	$t_{AVET}$		0	—	ns
Address setup time for write ( $\overline{W}$ -controlled)	$t_{AVWL}$	Figure 7	0	—	ns
Write pulse width	$t_{WLWH}$	Figure 7	6	—	ns
Address hold time for write ( $\overline{W}$ -controlled)	$t_{WHAX}$	Figure 7	2	—	ns
Address hold time for chip enable ( $\overline{E}$ -controlled)	$t_{EFAX}$	Figure 8	2	—	ns
$\overline{W}$ -controlled three-state time	$t_{WLQZ}^2$	Figure 7	—	9	ns
$\overline{W}$ -controlled output enable time	$t_{WHQX}^2$	Figure 7	2	—	ns
Chip enable pulse width ( $\overline{E}$ -controlled)	$t_{ETEF}$	Figure 8	6	—	ns
Data setup time	$t_{DVWH}$	Figure 7	2	—	ns
Data hold time	$t_{WHDX}$	Figure 7	2	—	ns
Chip enable controlled write pulse width	$t_{WLEF}$	Figure 8	6	—	ns
Data setup time	$t_{DVEF}$	Figure 8	2	—	ns
Data hold time	$t_{EFDX}$	Figure 8	2	—	ns

Address valid to end of write	$t_{AVWH}$	Figure 7	6	—	ns
Write disable time	$t_{WHWL}^1$	Figure 7	2	—	ns
Notes:					
* the post-irradiation performance is guaranteed at 25°C					
1. Tested with $\overline{G}$ high.					
2. Three-state is defined as 200mV change from steady-state output voltage.					



Assumptions:  $\overline{G} \leq V_{IL(max)}$

Figure 7. SRAM Write Cycle 1:  $\overline{W}$ -controlled Access



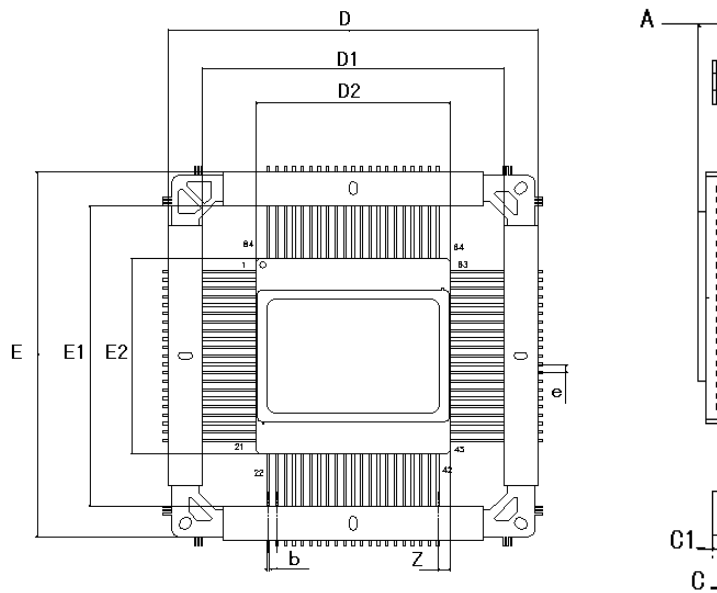
Assumption:  $\overline{G} \leq V_{IL(max)}$

Figure 8. SRAM Write Cycle 2: Enable-chip Controlled Access

## 8. Typical Application (Appendix 2)

## 9. Packaging

The SRAM B8CR1M39RH utilizes 84-Lead Ceramic Quad Flatpack as shown in Figure 9 and the corresponding dimensions are listed in Table 8, which is accordance with GB/T7092.



Notes:

1. The lid is electrically connected to VSS.

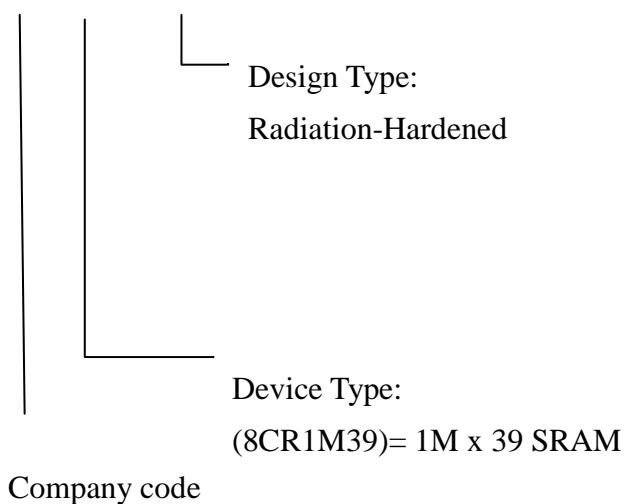
Figure 9. Package Outline

Table 8. Package Dimensions

Symbol	Min	Normal	Max
A	1.83	—	2.93
b	0.20	—	0.55
C	0.10	—	0.20
C1	0.5	—	1.28
D/E	54.07	—	56.67
D1/E1	44.46	—	45.96
D2/E2	28.62	—	29.80
e	—	1.27	—
z	1.13	—	2.31

## 10. Naming Rule

B8CR1M39RH



## 11. Replaced Product

Device Type	Substituted Device Type
B8CR1M39RH	Aeroflex UT8R1M39

B8CR1M39RH



Comparison	Device Type	Substituted Device Type	Differences and compatibility
	B8CR1M39RH	Aeroflex UT8R1M39	
Storage capacity	1Mx39bit	1Mx39bit	Identical
Read access time	$\leq 20\text{ns}$	$\leq 20\text{ns}$	Identical
Write access time	$\leq 10\text{ns}$	$\leq 10\text{ns}$	Identical
$V_{IH}$	$\geq 0.7 \times V_{DD2}$	$\geq 0.7 \times V_{DD2}$	Identical
$V_{IL}$	$\leq 0.3 \times V_{DD2}$	$\leq 0.3 \times V_{DD2}$	Identical
$V_{OH}$	$\geq 0.8 \times V_{DD2}$	$\geq 0.8 \times V_{DD2}$	Identical
$V_{OL}$	$\leq 0.2 \times V_{DD2}$	$\leq 0.2 \times V_{DD2}$	Identical
$I_{DD1(OP2)}$	$\leq 110\text{mA}$	$\leq 225\text{mA}$	Inconformity (B8CR1M39RH is better than UT8R1M39 in $I_{DD1(OP2)}$ )
ESD	2000V	2000V	Identical
Total-dose	300Krad (Si)	100Krad (Si)	Inconformity (B8CR1M39RH is better than UT8R1M39 in Total-dose)
SEL Immune	$\geq 99.8\text{MeV} \cdot \text{cm}^2/\text{mg}$	$\geq 110\text{MeV} \cdot \text{cm}^2/\text{mg}$	Inconformity (Limited to domestic SEL test conditions)
SEU Soft error rate	$\leq 3.73 \times 10^{-13}$ upsets/bit-day in Geosynchronous Orbit	$\leq 6.3 \times 10^{-7}$ upsets/bit-day	Inconformity (B8CR1M39RH is better than UT8R1M39 in SEU Soft error rate)

## Appendix 1

Pin Descriptions are listed in Table 9:

Table 9. Pin Symbols and Functions

Pin NO.	Symbol	Functions	Pin NO.	Symbol	Functions
1	V <sub>SS</sub>	Ground	43	V <sub>SS</sub>	Ground
2	DQ0	I/O	44	DQ31	I/O
3	DQ1	I/O	45	DQ30	I/O
4	DQ2	I/O	46	DQ29	I/O
5	DQ3	I/O	47	DQ28	I/O
6	V <sub>DD2</sub>	Power(3.3V)	48	V <sub>DD2</sub>	Power(3.3V)
7	DQ4	I/O	49	DQ27	I/O
8	DQ5	I/O	50	DQ26	I/O
9	DQ6	I/O	51	DQ25	I/O
10	DQ7	I/O	52	DQ24	I/O
11	V <sub>SS</sub>	Ground	53	V <sub>SS</sub>	Ground
12	DQ8	I/O	54	DQ23	I/O
13	DQ9	I/O	55	DQ22	I/O
14	DQ10	I/O	56	DQ21	I/O
15	DQ11	I/O	57	DQ20	I/O
16	V <sub>DD2</sub>	Power(3.3V)	58	V <sub>DD2</sub>	Power(3.3V)
17	DQ12	I/O	59	DQ19	I/O
18	DQ13	I/O	60	DQ18	I/O
19	DQ14	I/O	61	DQ17	I/O
20	DQ15	I/O	62	DQ16	I/O
21	V <sub>SS</sub>	Ground	63	V <sub>SS</sub>	Ground
22	DQ35	I/O	64	DQ39	I/O
23	DQ34	I/O	65	DQ38	I/O
24	A11	Address	66	A10	Address
25	A12	Address	67	A9	Address
26	A13	Address	68	V <sub>DD1</sub>	Power(1.2V)

27	V <sub>SS</sub>	Ground	69	A8	Address
28	V <sub>DD1</sub>	Power(1.2V)	70	A7	Address
29	A14	Address	71	A6	Address
30	A15	Address	72	$\overline{W}$	Write Enable
31	A16	Address	73	V <sub>SS</sub>	Ground
32	$\overline{E}$	Chip Enable	74	V <sub>DD2</sub>	Power(3.3V)
33	$\overline{G}$	Output Enable	75	A5	Address
34	V <sub>DD2</sub>	Power(3.3V)	76	A4	Address
35	A17	Address	77	A3	Address
36	A18	Address	78	V <sub>SS</sub>	Ground
37	A19	Address	79	V <sub>DD1</sub>	Power(1.2V)
38	NC	No connect	80	A2	Address
39	V <sub>DD1</sub>	Power(1.2V)	81	A1	Address
40	V <sub>SS</sub>	Ground	82	A0	Address
41	DQ33	I/O	83	DQ37	I/O
42	DQ32	I/O	84	DQ36	I/O

## Appendix 2

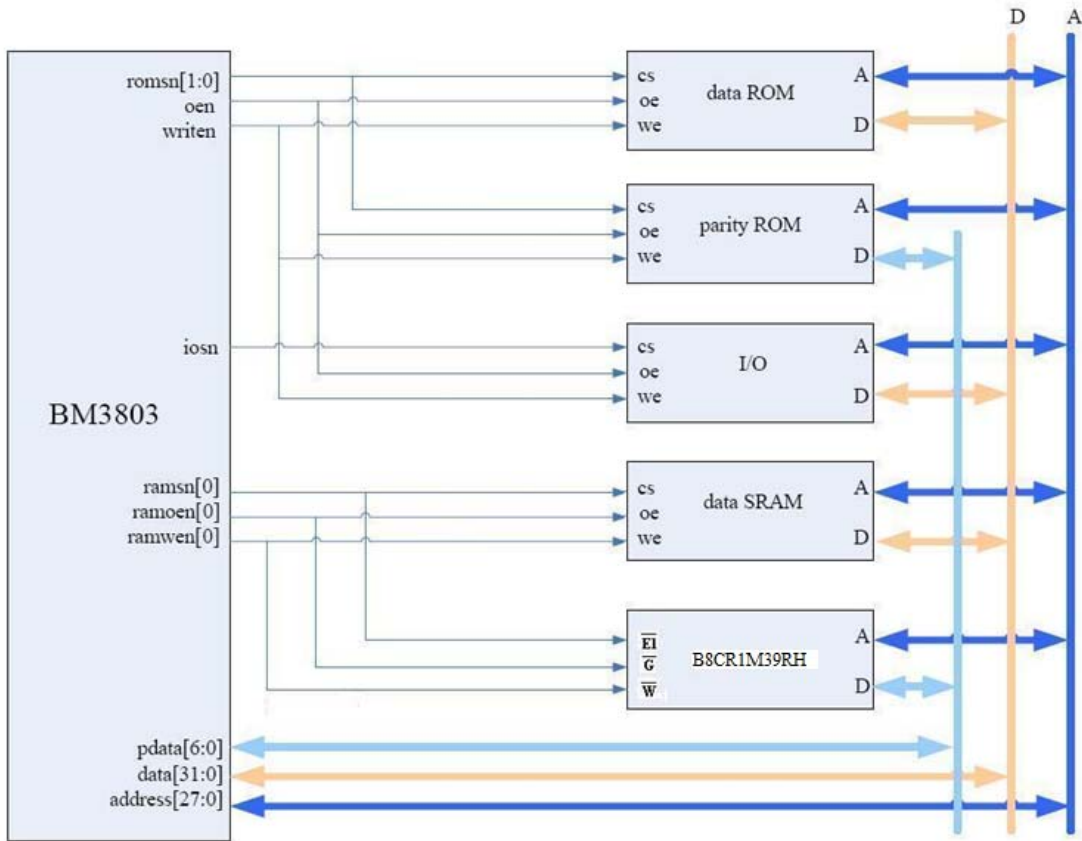


Figure 10. Typical Application

Figure 10 illustrates a typical application system, which consists of a CPU and an SRAM (B8CR1M39RH) chip. The B8CR1M39RH serves as data storage for the CPU, while the CPU controls the SRAM operation properly.

For starting up normally, both 3.3 and 1.2 V power supply should be applied to the SRAM correctly, then it will operate according to the control signals sent by the CPU. Normally the CPU will write some data into the SRAM in the first place. For this operation,  $\overline{wn}$  and  $\overline{En}$  should be set lower than  $V_{IH}(\max)$ , and either of two different write cycles described in Section 7.3 can be used to realize the writing, as long as the signals generated by the CPU satisfy the relevant timing sequence requirements.

The read operation can be implemented similarly. For this operation,  $\overline{w_n}$  should be set higher than  $V_{IH}(\min)$  and  $\overline{E_n}$  should be set lower than  $V_{IH}(\max)$ . The B8CR1M39RH offers three different kinds of read cycles, the selection of which can be decided according to the demand of whole system. Also, proper signal sequence is required for successful read operation.

Notes:

1. Supply voltage sequencing is recommended to be  $V_{DD2}$  prior to  $V_{DD1}$ .
2. Supply voltage is required to be as stable as possible.
3. The input should not be suspend in midair.
4. The output should not be connected to supply voltage or  $V_{SS}$ .
5. The lid is electrically connected to  $V_{SS}$ .

## Service & Supply

Address: No.2. Siyingmen N.Rd. Donggaodi Fengtai District,BeiJing,China

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