Ver 1.2

Radiation-Hardened SRAM

Datasheet

Part Number：B8CR512K32RH

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Page of Revise Control

Version No.	Publish Time	Revised Chapter	Revise Introduction	Note
1.0	1.20.2015		Document creation	
1.1	07.22.2015	Appendix 2	Advance typical application	
1.2	03.06.2018		Text and wording modifications	

TABLE OF CONTENTS

1. Features

- 17 ns maximum access time
- Asynchronous operation, functionally compatible with Aeroflex UT8CR512K32 SRAM
- CMOS compatible inputs and output levels, three-state bidirectional data bus
- I/O Voltage 3.3 V，1.8 V core
- ESD better than 2000 V
- Operational environment:
  - Total-dose: 100 K Rad (Si)
  - SEL Immune: > 75 MeV cm^2/mg
  - SEU Error Rate=1E-10errors/bit-day in Geosynchronous Orbit
- Packaging options
  - 68-lead ceramic quad flatpack （QFP68）

2. General Description

The B8CR512K32RH is a high-performance radiation-hardened CMOS static SRAM organized as 524,288 words by 32 bits. Fabricated with industry-standard CMOS technology, the device works in asynchronous mode . The combination of radiation-hardness, fast access time, and low power consumption makes the B8CR256K32RH ideal for high speed system designed for operation in radiation environments.

3. Block Diagram

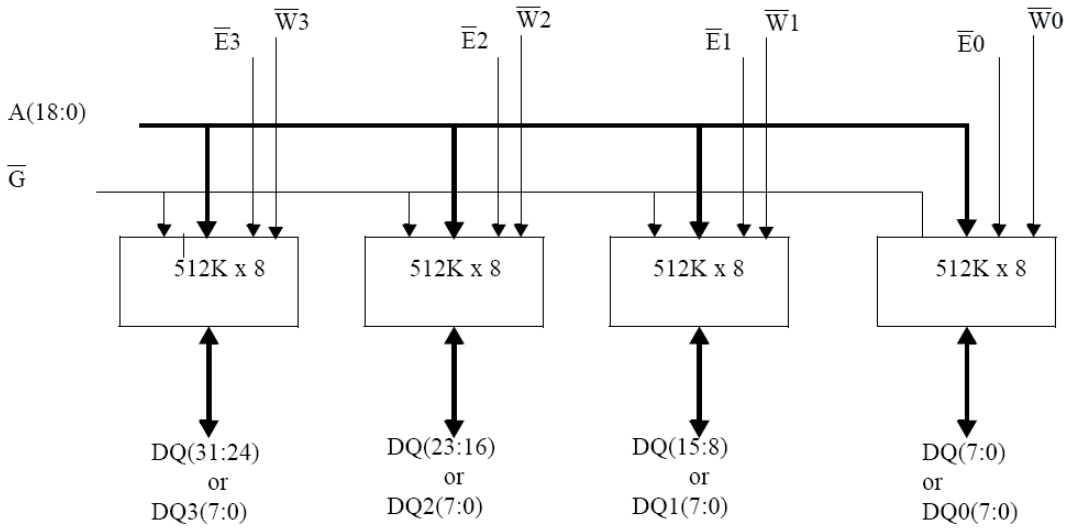


Figure 1. B8CR512K32RH Block Diagram

4. Pin Description

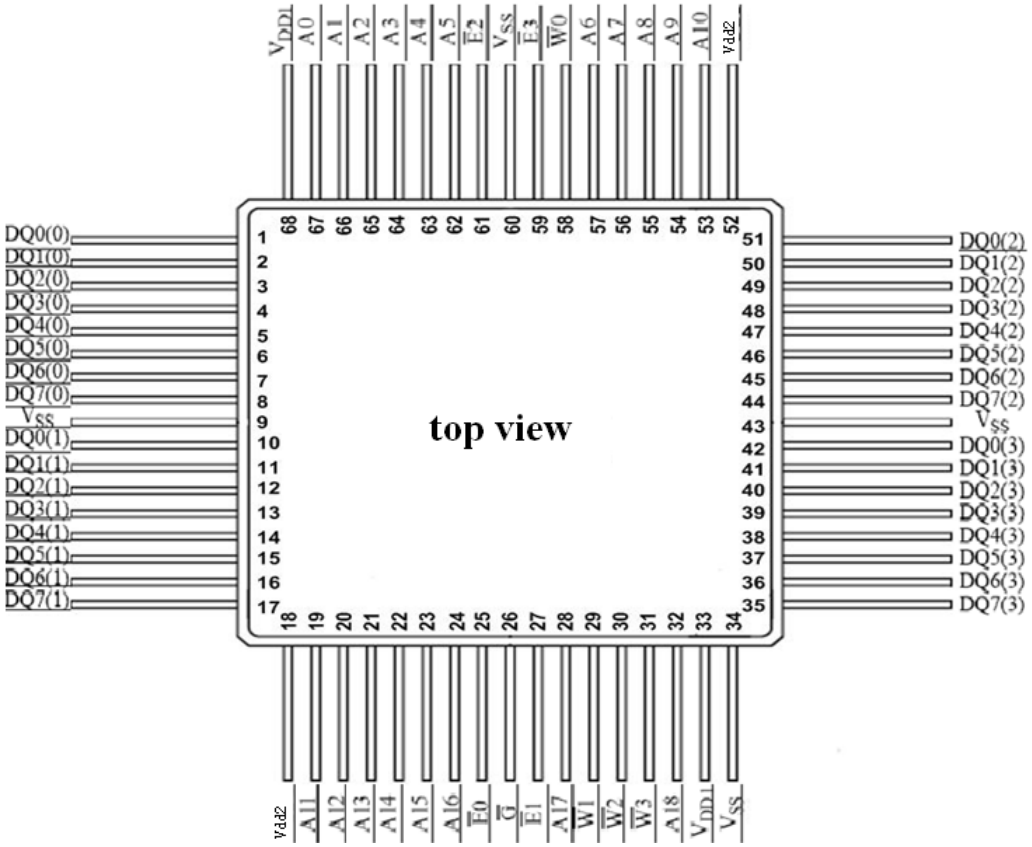


Figure 2. B8CR512K32RH SRAM Pinout

Table 1. Pin Name

Pin Names	Functions
A0~A18	Address
DQ0~3(7:0)	Data Input / Output
$\overline{E}0$~$\overline{E}3$	Chip Enable (Active Low)
$\overline{W}0$~$\overline{W}3$	Write Enable (Low Write Enable, and High Read Enable)
$\overline{G}$	Output Enable (Active Low)
V_{DD1}	Power (1.8 V)
V_{DD2}	Power (3.3 V)
V_{SS}	Ground

5. Pin Configurations（Appendix 1）

6. Product Description

6.1 Quality Grade and Production Standard

The quality grade of the radiation-hardened SRAM B8CR512K32RH is GJB597A-1996 B. And B8CR512K32RH is up to the Q/Zt 20413-2015 semiconductor IC standard.

6.2 Function Description

The B8CR512K32RH has nine control inputs, Chip Enable $\overline{E0}$~$\overline{E3}$, Write Enable $\overline{W0}$~$\overline{W3}$, and Output Enable ($\overline{G}$), 19 address inputs A (18:0), and 32 data lines, DQ0~3(7:0).

Table 2. Device Operation Truth Table

Inputs	Outputs

$\overline{G}$	$\overline{Wn}$	$\overline{En}$	I/O Mode	Mode
X	X	1	DQn(7:0) 3-State	Standby
X	0	0	DQn(7:0) Data in	Write
0	1	0	DQn(7:0) Data out	Read
1	1	0	DQn(7:0) 3-State	Read DQ 3-State
Notes: 1. X = Don't care				

◆ **Read Cycle**

A combination of $\overline{Wn}$ greater than V_{IH}(min) and $\overline{En}$ less than V_{IL}(max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

SRAM Read Cycle 1, the Address Access in Figure 4, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$=0，$\overline{Wn}$ =1. Valid data appears on data outputs DQn(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enables and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 5, is initiated by $\overline{G}$=0，$\overline{Wn}$ =1, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the word addressed by A(18:0) is accessed and appears at the data outputs DQn(7:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 6, is initiated by $\overline{En}$ =0, $\overline{Wn}$ =1, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

◆ **Write Cycle**

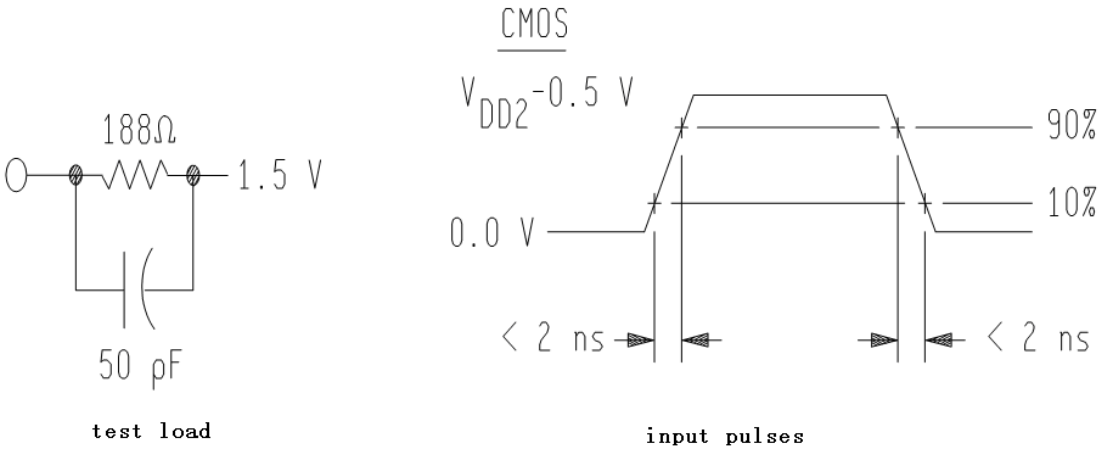
A combination of $\overline{Wn}$ and $\overline{En}$ less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 7, is defined by a write terminated by $\overline{W}$ going high, with $\overline{En}$ =0. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{En}$. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins

DQn(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 8, is defined by a write terminated by $\overline{En}$ going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{Wn}$, and by t_{ETEF} when the write is initiated by $\overline{En}$ going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQn(7:0) to avoid bus contention.

6.3 AC Test Load and Input Waveforms



Notes: 1. 50pF includes scope probe and test socket capacitance.

2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = V_{DD2}/ 2).

Figure 3. AC Test Load and Input Waveforms

6.4 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD1}	Core supply voltage	1.7 V ~ 1.9 V
V_{DD2}	I/O supply voltage	3.0 V ~ 3.6 V

T_C	Case temperature range	-55℃ ~ +125℃
V_I	DC input voltage	0 V ~ V_{DD2}
Notes: The correct power-up sequence should be V_{DD1}--> V_{DD2}.		

7. Electrical Characteristics

7.1 DC Electrical Characteristics (Pre and Post-Radiation)

Table 4. DC Parameter Table (Ⅰ)

Parameter	Symbol	Condition (GND=0V，-55℃≤T_A≤125℃) 1.7V≤V_{DD1}≤1.9V、3.0V≤V_{DD2}≤3.6V	Limits		UNIT
			MIN	MAX	
High-level input voltage	V_{IH}		.7*V_{DD2}	—	V
Low-level input voltage	V_{IL}		—	.3*V_{DD2}	V
High-level output voltage	V_{OH}	V_{DD2}=3V, I_{OH}=-4 mA, all outputs needed are tested	.8*V_{DD2}	—	V
Low-level output voltage	V_{OL}	V_{DD2}=3V, I_{OL}=8 mA, all outputs needed are tested	—	.2*V_{DD2}	V
Input capacitance	C_{IN}	f=1MHz@0V, T_C=25℃		50	pF
Bidirectional I/O Capacitance	C_{IO}	f=1MHz@0V, T_C=25℃		18	pF
High-level input leakage current	I_{IH}	V_{DD2}=3.6V, V_{DD1}=1.9V, V_I=3.6V, all inputs are tested	-2	2	μA
Low-level input leakage current	$\|I_{IL}\|$	V_{DD2}= 3.6V, V_{DD1}=1.9V, V_I= 0V, all inputs are tested	-2	2	μA
Three-state (high-level) output leakage current	I_{OZH}	V_{DD2}= 3.6V, V_{DD1}=1.9V, V_O=V_{DD2}, all bidirectional I/O are tested	-2	2	μA

Three-state (low-level) output leakage current	$\|I_{OZL}\|$	V_{DD2}= 3.6V, V_{DD1}=1.9V, V_O=0, all bidirectional I/O are tested	-2	2	μA
Core Supply current operating @1MHz	$I_{DD1}(OP_1)$	V_{IL}=0.2V, V_{IH} =3.4V, I_{DD1} current is tested V_{DD1}=1.9V		70	mA
Core Supply current operating @66MHz	$I_{DD1}(OP_2)$	V_{IL}=0.2V, V_{IH} =3.4V, I_{DD1} current is tested V_{DD1}=1.9V		220	mA
I/O Supply current operating @1 MHz	$I_{DD2}(OP_1)$	V_{IL}=0.2V, V_{IH} =3.4V, V_{DD1}=1.9V, V_{DD2}=3.6V, I_{DD2} current is tested		0.35	mA
I/O Supply current operating @66 MHz	$I_{DD2}(OP_2)$	V_{IL}=0.2V, V_{IH} =3.4V, V_{DD1}=1.9V, V_{DD2}=3.6V, I_{DD2} current is tested		11	mA
Supply current standby @0 Hz	I_{DD1}(SB)	CMOS inputs, I_{OUT}=0，$\overline{E1}$=V_{DD2}-0.2, E2=GND， V_{DD2}= 3.6V, V_{DD1}=1.9V		65	mA
Supply current standby @0 Hz	I_{DD2}(SB)	CMOS inputs, I_{OUT}=0，$\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}=3.6V, V_{DD1}=1.9V		400	μA
Supply current standby A (16:0) @66M Hz	I_{DD1}(SB)	CMOS inputs,I_{OUT}=0，$\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}= 3.6V, V_{DD1}=1.9V		65	mA
Supply current standby A (16:0) @66M Hz	I_{DD2}(SB)	CMOS inputs,I_{OUT}=0，$\overline{E1}$ =V_{DD2}-0.2,E2=GND， V_{DD2}= 3.6V, V_{DD1}=1.9V		2	mA

Notes:

* For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.

2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. $V_{IH}=V_{DD2.}$

7.2 Read Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 5. Read Cycle AC Parameters

Parameter	Symbol	Condition ($V_{DD1}=V_{DD1}$(min), $V_{DD2}=V_{DD2}$(min), -55℃≤ T_A ≤125℃)	Limits		UNIT
			MIN	MAX	
Read cycle time	t_{AVAV}[1]	Figure 4	17	—	ns
Address to data valid	t_{AVQV}		—	17	ns
Output hold time from address change	t_{AXQX}[2]		3	—	ns
$\overline{G}$-controlled output enable time	t_{GLQX}[2,1]	Figure 6	0	—	ns
$\overline{G}$-controlled output data valid	t_{GLQV}		—	7	ns
$\overline{G}$-controlled output three-state time	t_{GHQZ}[2]		—	7	ns
$\overline{E\ 1}$-controlled output enable time	t_{ETQX}[2,3]	Figure 5	5	—	ns
$\overline{E\ 1}$-controlled access time	t_{ETQV}[3]		—	17	ns

$\overline{E}$ 1-controlled output three-state time	t_{EFQZ} [2,4]		—	10	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1. Guaranteed but not tested.
2. Three-state is defined as a 200mV change from steady-state output voltage.
3. The ET (chip enable true) notation refers to the latter falling edge of $\overline{E}$ 1 or rising edge of E2.
4. The EF (chip enable false) notation refers to the latter rising edge of $\overline{E}$ 1 or falling edge of E2.

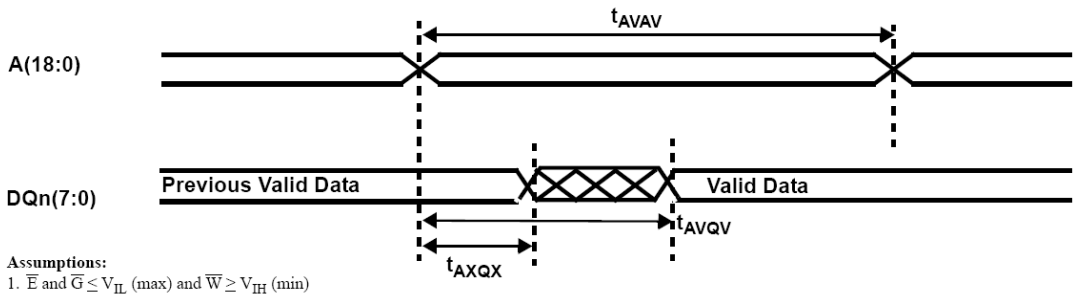
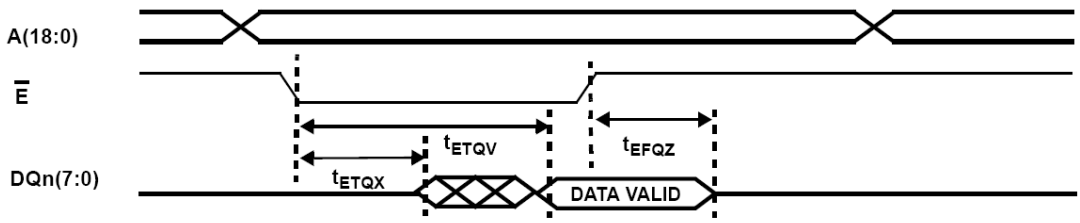
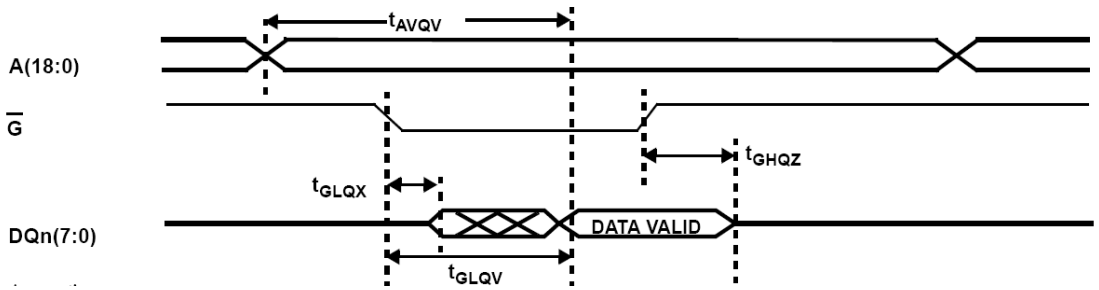


Figure 4. SRAM Read Cycle 1: Address Access



Assumptions： $\overline{G}$, $\overline{W}$≥V_{IH}(min)

Figure 5. SRAM Read Cycle 2: Chip Enable Access



Assumptions: $\overline{En}$ ≤V_{IL}(max), $\overline{W}$≥V_{IH}(min)

Figure 6. SRAM Read Cycle 3: Output Enable Access

7.3 Write Cycle AC Electrical Characteristics (Pre and Post-Radiation)

Table 6. Write Cycle AC Parameter (Ⅰ)

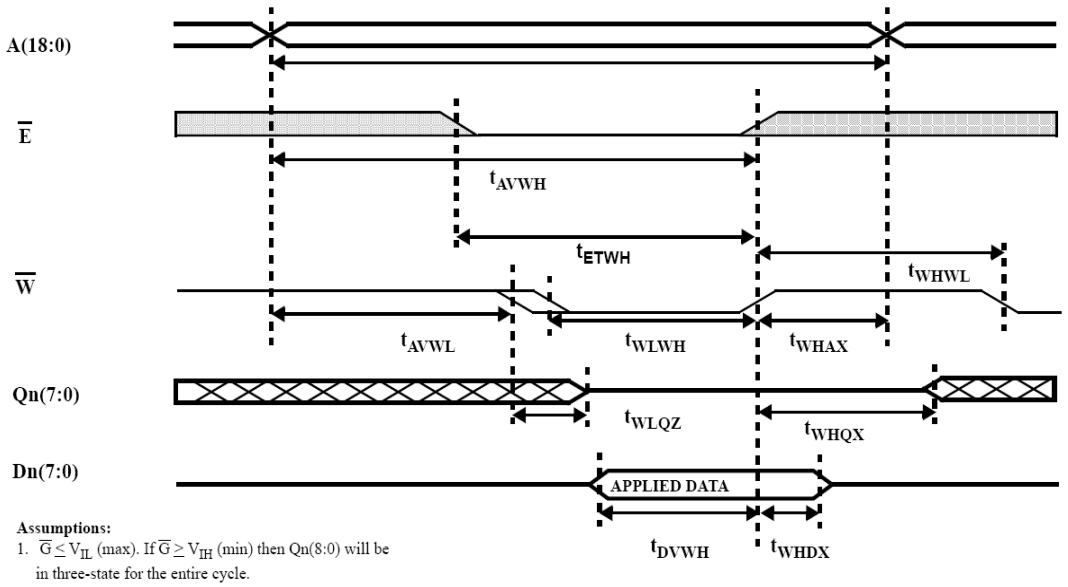
Parameter	Symbol	Condition (V_{DD1}=V_{DD1}(min), V_{DD2}=V_{DD2}(min), -55℃≤T_A≤125℃)	Limits		UNIT
			MIN	MAX	
Write cycle time	t_{AVAV}[1]	Figure 7 & Figure 8	17		ns
Chip enable to end of write	t_{ETWH}	Figure 7	12	—	ns
Address setup time for write ($\overline{E}$1 /E2-controlled)	t_{AVET}		0	—	ns
Address setup time for write ($\overline{W}$ -controlled)	t_{AVWL}	Figure 7	0	—	ns
Write pulse width	t_{WLWH}	Figure 7	12	—	ns
Address hold time for write ($\overline{W}$ -controlled)	t_{WHAX}	Figure 7	2	—	ns

Address hold time for chip enable ($\overline{E}$1/E2-controlled)	t_{EFAX}	Figure 8	0	—	ns
$\overline{W}$-controlled three-state time	t_{WLQZ}[2]	Figure 7	—	6	ns
$\overline{W}$-controlled output enable time	t_{WHQX}[2]	Figure 7	4	—	ns
Chip enable pulse width ($\overline{E}$1 /E2-controlled)	t_{ETEF}	Figure 8	12	—	ns
Data setup time	t_{DVWH}	Figure 7	7	—	ns
Data hold time	t_{WHDX}	Figure 7	2	—	ns
Chip enable controlled write pulse width	t_{WLEF}	Figure 8	12	—	ns
Data setup time	t_{DVEF}	Figure 8	7	—	ns
Data hold time	t_{EFDX}	Figure 8	0	—	ns
Address valid to end of write	t_{AVWH}	Figure 7	12	—	ns
Write disable time	t_{WHWL}[1]	Figure 7	3	—	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25×C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

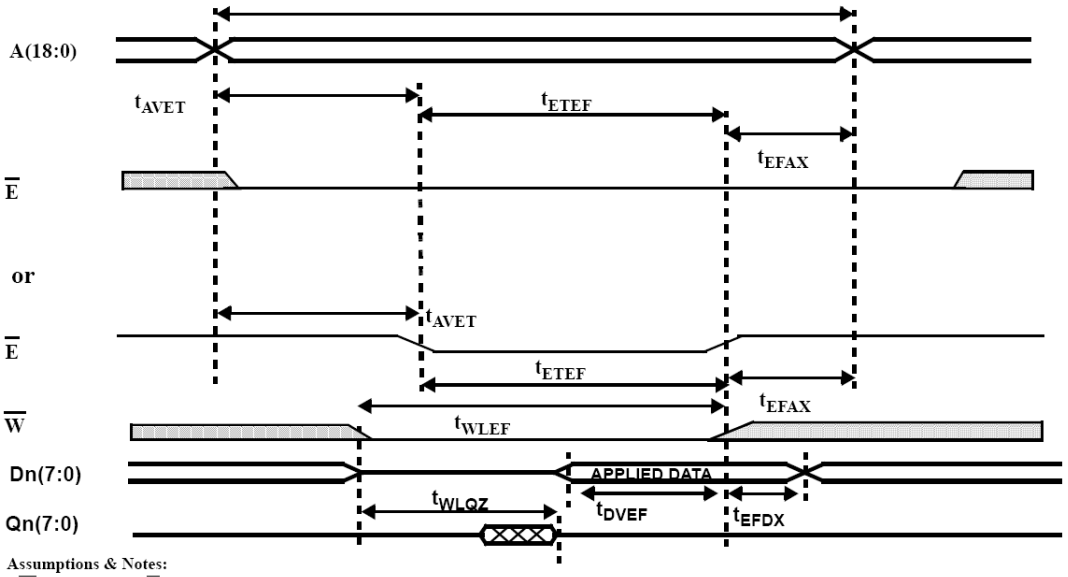
1. Tested with $\overline{G}$ high.
2. Three-state is defined as 200mV change from steady-state output voltage.



Assumptions:

1. $\overline{G} \leq V_{IL}$(max). If $\overline{G} \geq V_{IH}$(min) then Q(8:0) will be in three-state for the entire cycle.
2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 7. SRAM Write Cycle 1: $\overline{W}$-controlled Access



Assumption:

1. $\overline{G} \leq V_{IL}$(max). If $\overline{G} \geq V_{IH}$(min) then Q(8:0) will be in three-state for the entire cycle.

2. t_{AVET}: Address setup time for device enable, minimum 5ns is recommended for normal operation.

Figure 8. SRAM Write Cycle 2: Enable-chip Controlled Access

7.4 Absolute Maximum Ratings

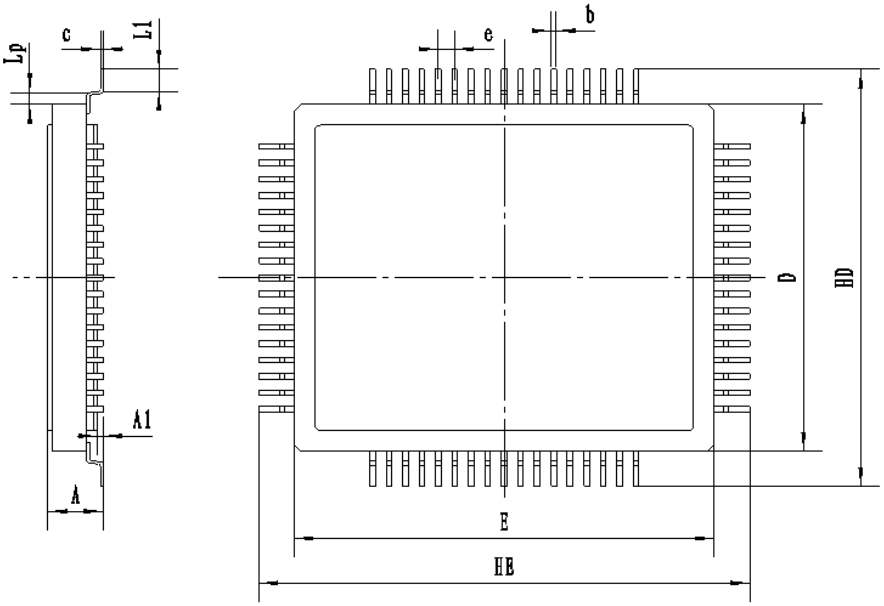
Table 7. Absolute Maximum Ratings

Symbol	Parameter	Limits
V_{DD1}	Core supply voltage	-0.3V ~ +2.1 V
V_{DD2}	I/O supply voltage	-0.3V ~ +3.8 V
$V_{I/O}$	Voltage on any pin	-0.3V ~ +3.8 V
T_{STG}	Storage Temperature	-65℃ ~ 150℃
P_D	Maximum power dissipation	1.2W
T_J	Maximum junction temperature	+175℃
$R_{th(J-C)}$	Thermal resistance, junction-to-case	5℃/W

8. Typical Application（Appendix 2）

9. Packaging

The SRAM B8CR512K32RH utilizes 68-Lead Quad Ceramic Flatpack as shown in Figure 9 and the corresponding dimensions are listed in Table 8, which is accordance with GB/T7092.



Notes:

1. The lid is electrically connected to V_{SS}.

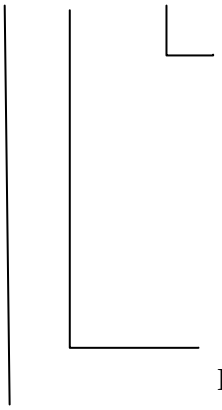
Figure 9. Package Outline

Table 8. Package Dimensions

Symbol	Value (Unit: mm)		
	Min	Normal	Max
A	3.9	—	5.4
A1	0.51	0.70	1.01
b	—	0.43	—
c	—	0.2	—
e	—	1.27	—
D	26.53	26.8	27.07
HD	30.63	31.8	32.67
E	32.08	32.4	32.72
HE	36.18	37.4	38.32
L1	1.25	1.5	1.75
Lp	1.0	1.0	1.15

10. Naming Rule

B8CR512K32RH



Design Type:
Radiation-Hardened

Device Type:
(8CR512K32)=512K x 32 SRAM
Company code

11. Replaced Product

Device Type	Substituted Device Type
B8CR512K32RH	Aeroflex UT8CR512K32

Appendix 1

Pin Descriptions are listed in Table 9：

Table 9. Pin Symbols and Functions

Pin NO.	Symbol	Functions	Pin NO.	Symbol	Functions
1	DQ0(0)	I/O	35	DQ7(3)	I/O
2	DQ1(0)	I/O	36	DQ6(3)	I/O
3	DQ2(0)	I/O	37	DQ5(3)	I/O
4	DQ3(0)	I/O	38	DQ4(3)	I/O
5	DQ4(0)	I/O	39	DQ3(3)	I/O
6	DQ5(0)	I/O	40	DQ2(3)	I/O
7	DQ6(0)	I/O	41	DQ1(3)	I/O
8	DQ7(0)	I/O	42	DQ0(3)	I/O
9	V_{SS}	Ground	43	V_{SS}	Ground
10	DQ0(1)	I/O	44	DQ7(2)	I/O
11	DQ1(1)	I/O	45	DQ6(2)	I/O
12	DQ2(1)	I/O	46	DQ5(2)	I/O
13	DQ3(1)	I/O	47	DQ4(2)	I/O
14	DQ4(1)	I/O	48	DQ3(2)	I/O
15	DQ5(1)	I/O	49	DQ2(2)	I/O
16	DQ6(1)	I/O	50	DQ1(2)	I/O
17	DQ7(1)	I/O	51	DQ0(2)	I/O
18	V_{DD2}	Power(3.3V)	52	V_{DD2}	Power(3.3V)
19	A11	Address	53	A10	Address
20	A12	Address	54	A9	Address
21	A13	Address	55	A8	Address
22	A14	Address	56	A7	Address
23	A15	Address	57	A6	Address
24	A16	Address	58	$\overline{W}0$	Write Enable 0

25	$\overline{E}0$	Chip Enable 0	59	$\overline{E}3$	Chip Enable3
26	$\overline{G}$	Output Enable	60	V_{SS}	Ground
27	$\overline{E}1$	Chip Enable 1	61	$\overline{E}2$	Chip Enable 2
28	A17	Address	62	A5	Address
29	$\overline{W}1$	Write Enable 1	63	A4	Address
30	$\overline{W}2$	Write Enable 2	64	A3	Address

Appendix 2

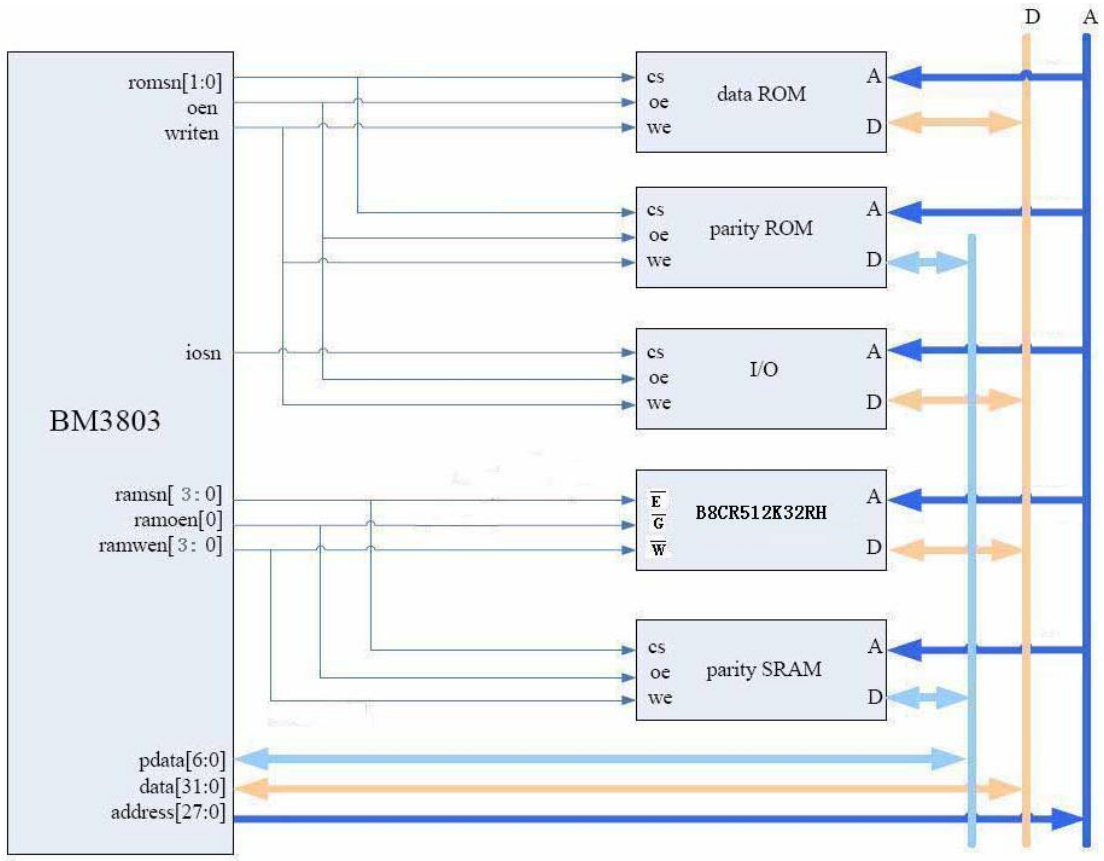


Figure 10. Typical Application

Figure 10 illustrates a typical application system, which consists of a CPU and an SRAM (B8CR512K32RH) chip. The B8CR512K32RH serves as data storage for the

CPU, while the CPU controls the SRAM operation properly.

For starting up normally, both 3.3 and 1.8 V power supply should be applied to the SRAM correctly, then it will operate according to the control signals sent by the CPU. Normally the CPU will write some data into the SRAM in the first place. For this operation, $\overline{Wn}$ should be set lower than V_{IH}, and either of two different write cycles described in Section 7.3 can be used to realize the writing, as long as the signals generated by the CPU satisfy the relevant timing sequence requirements.

The read operation can be implemented similarly, except that $\overline{Wn}$ should be deasserted primarily. The B8R512K8RH offers three different kinds of read cycles, the selection of which can be decided according to the demand of whole system. Also, proper signal sequence is required for successful read operation.

Notes:

1. Supply voltage sequencing is recommended to be V_{DD2} prior to V_{DD1}.
2. Supply voltage is required to be as stable as possible.
3. The input should not be suspend in midair. The transition of the input signal should be less than 10ns ,voltage from Vil to Vih.
4. The output should not be connected to supply voltage or V_{SS}.

The lid is electrically connected to V_{SS}.

Service & Supply

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