Ver 1.1

8-Bit 100MSPS Analog to Digital Converter

Datasheet

Part Number：B9288ARH

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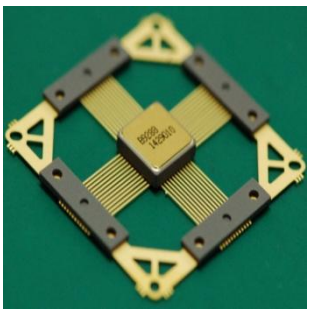
1. Features



- Dual 8-Bit, 100 MSPS ADC
- Low Power: 90 mW at 100 MSPS per Channel
- On-Chip Reference and Track/Holds
- 475 MHz Analog Bandwidth Each Channel
- 1 V p-p Analog Input Range Each Channel
- Single +3.0 V Supply Operation (2.7 V–3.6 V)
- Standby Mode for Single Channel Operation
- Twos Complement or Offset Binary Output Mode
- Output Data Alignment Mode
- Total Ionizing Dose ≥100 Krad(Si)
- The Single Event Latch-up robust ability≥37 Mev/mg/cm^2

2. General description

The B9288ARH is a radiation hardened, dual 8-bit monolithic sampling analog to digital converter with on-chip track-and-hold circuits and is optimized for low cost, low power, small size and ease of use. The product operates at a 100 MSPS conversion rate with outstanding dynamic performance over its full operating range. Each channel can be operated independently. The ADC requires only a single 3.0 V (2.7 V to 3.6 V) power supply and an encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3 V or 2.5 V logic. The encode input is TTL/CMOS

compatible and the 8-bit digital outputs can be operated from +3.0 V (2.5 V to 3.6 V) supplies. User selectable options are available to offer a combination of standby modes, digital data formats and digital data timing schemes. In standby mode, the digital outputs are driven to a high impedance state. Fabricated on an advanced CMOS process, the B9288ARH is available in a 48-lead surface mount ceramic package (CQFP) specified over the temperature range (–55 ℃ to +125 ℃).

3. Functional block diagram

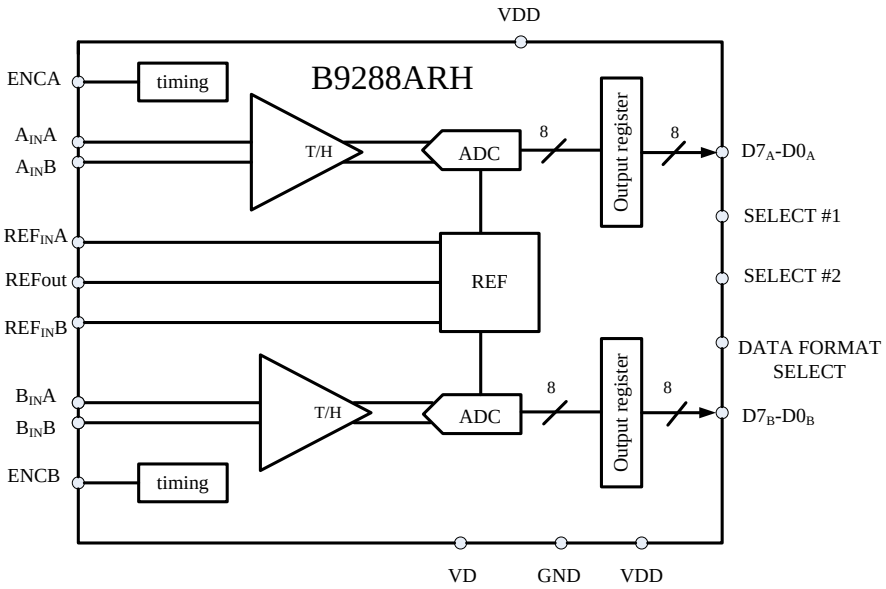


Figure 3-1. Functional block diagram

4. Pin configuration

The pins outlines of the device are shown in figure:

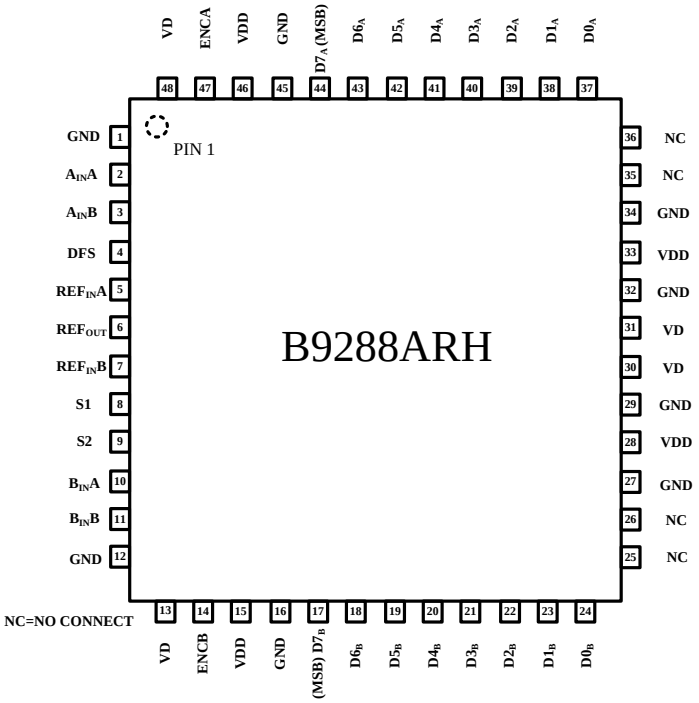


Figure 4-1 Pin Description

The pin description is shown in this table.

Table 4-1 B9288ARH Pin Description

Pin No.	Symbol	Description
1,12,16,27,29 32,34,45	GND	Ground
2	$A_{IN}A$	Analog Input for Channel A.
3	$A_{IN}B$	Analog Input for Channel A (Complementary).
4	DFS	Data Format Select: (Offset binary output available if set low. Twos complement output available if set high).
5	$REF_{IN}A$	Reference Voltage Input for Channel A.
6	REF_{OUT}	Internal Reference Voltage
7	$REF_{IN}B$	Reference Voltage Input for Channel B
8	S1	User Select 1,Tied with Respect to VD
9	S2	User Select 2
10	$B_{IN}B$	Analog Input for Channel B (Complementary).
11	$B_{IN}A$	Analog Input for Channel B
13,30,31,48	V_D	Analog Supply (3 V)
14	ENC_B	Clock Input for Channel B.
15,28,33,46	V_{DD}	Digital Supply (3 V).

17-24	$D7_B$-$D0_B$	Digital Output for Channel B.
25,26,35,36	NC	Do Not Connect
37-44	$D0_A$-$D7_A$	Digital Output for Channel A
47	ENC_A	Clock Input for Channel A

5. Pin Description

Table 5-1. Pin Definition

Pin No.	Symbol	Attribute	Pin No.	Symbol	Attribute
1	GND	Ground	**25**	NC	NC
2	$A_{IN}A$	Input	**26**	NC	NC
3	$A_{IN}B$	Input	**27**	GND	Ground
4	DFS	In put	**28**	V_{DD}	Supply Power
5	$REF_{IN}A$	In put	**29**	GND	Ground
6	REF_{OUT}	Output	**30**	V_D	Supply Power
7	$REF_{IN}B$	Input	**31**	V_D	Supply Power
8	S1	Input	**32**	GND	Ground
9	S2	Input	**33**	V_{DD}	Supply Power
10	$B_{IN}B$	Input	**34**	GND	Ground
11	$B_{IN}A$	Input	**35**	NC	NC
12	GND	Ground	**36**	NC	NC
13	V_D	Supply Power	**37**	$D0_A$	Output
14	ENC_B	Input	**38**	$D1_A$	Output
15	V_{DD}	Supply Power	**39**	$D2_A$	Output
16	GND	Ground	**40**	$D3_A$	Output
17	$D7_B$	Output	**41**	$D4_A$	Output
18	$D6_B$	Output	**42**	$D5_A$	Output
19	$D5_B$	Output	**43**	$D6_A$	Output
20	$D4_B$	Output	**44**	$D7_A$	Output
21	$D3_B$	Output	**45**	GND	Ground
22	$D2_B$	Output	**46**	V_{DD}	Supply Power
23	$D1_B$	Output	**47**	ENC_A	Input
24	$D0_B$	Output	**48**	VD	Supply Power

6. Product description

6.1 Function Description

The B9288ARH ADC architecture is a bit-per-stage pipeline-type converter utilizing switch capacitor techniques. These stages determine the 5 MSBs and drive a 3-bit flash. Each stage provides sufficient overlap and error correction allowing optimization of comparator accuracy. The input buffers are differential and both sets of inputs are internally biased. This allows the most flexible use of ac or dc and differential or single-ended input modes. The output staging block aligns the data, carries out the error correction and feeds the data to output buffers. The set of output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. There is no discernible difference in performance between the two channels.

Good high speed design practices must be followed when using the B9288ARH. To obtain maximum benefit, decoupling capacitors should be physically as close to the chip as possible, minimizing trace and via inductance between chip pins and capacitor. It is recommended to place a 0.1 uF capacitor at each power ground pin pair for high frequency decoupling, and include one 10 uF capacitor for local low frequency decoupling. The $V_{REF\ IN}$ pin should also be decoupled by a 0.1 uF capacitor. It is also recommended to use a split power plane and contiguous ground plane. Data output traces should be short (<1 inch), minimizing on-chip noise at switching.

1. Clock Input

Any high speed AD converter is extremely sensitive to the quality of the sampling clock provided by the user. A track hold circuit is essentially a mixer. Any noise, distortion or timing jitter on the clock will be combined with the desired signal at the AD output. For that reason, considerable care has been taken in the design of the Clock input of the B9288ARH, and the user is advised to give commensurate thought to the clock source. The Clock input is fully TTL CMOS compatible.

2. Digital Outputs

The digital outputs are TTL CMOS compatible for lower power consumption. During standby, the output buffers transition to a high impedance state. A data format selection option supports either twos complement (set high) or offset binary output (set low) formats.

3. Analog Input

The analog input to the B9288ARH is a differential buffer. For best dynamic

performance, impedance at two input should match. Special care was taken in the design of the analog input stage of the B9288ARH to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1 V p-p centered at VD * 0.3

4. Voltage Reference

A stable and accurate 1.18 V voltage reference is built into the B9288ARH. In normal operation, the internal reference is used by strapping Pins 5 and 7 to Pin 6, The input range can be adjusted by varying the reference voltage applied to the B9288ARH. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage, which changes linearly.

5. Timing

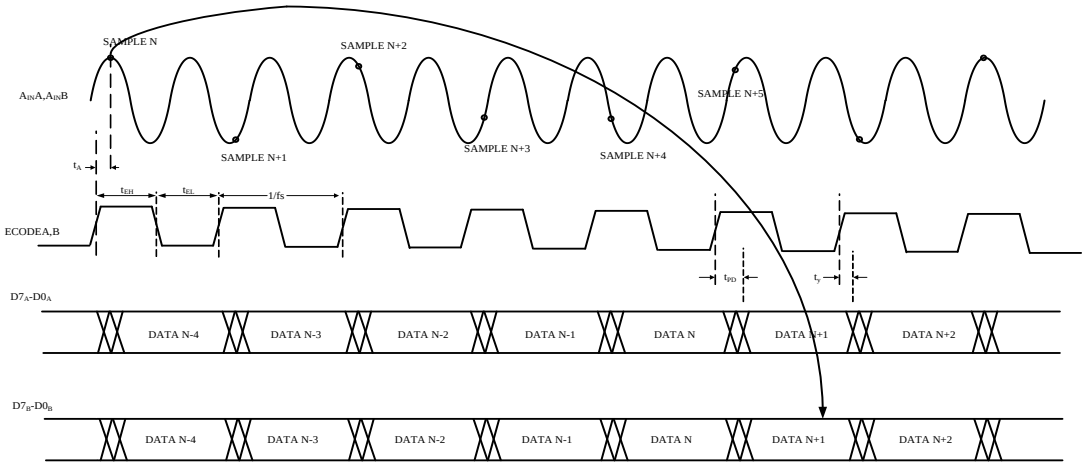


Figure 6-1. Normal Operation, Same Clock (S1 = 1, S2 = 0) Channel Timing

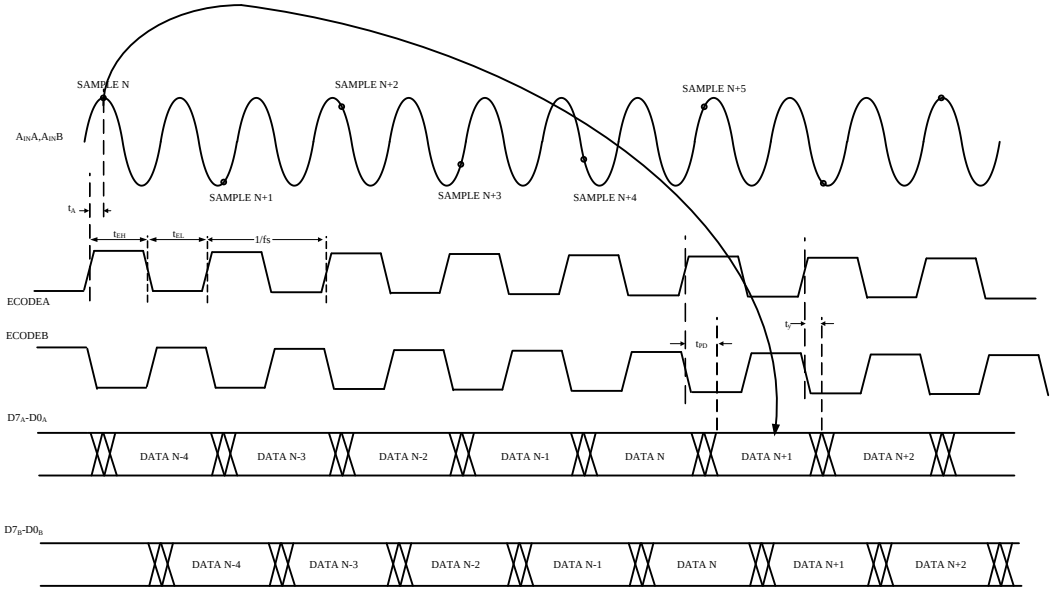


Figure 6-2. Normal Operation with Two Clock Sources (S1 = 1, S2 = 0) Channel Timing

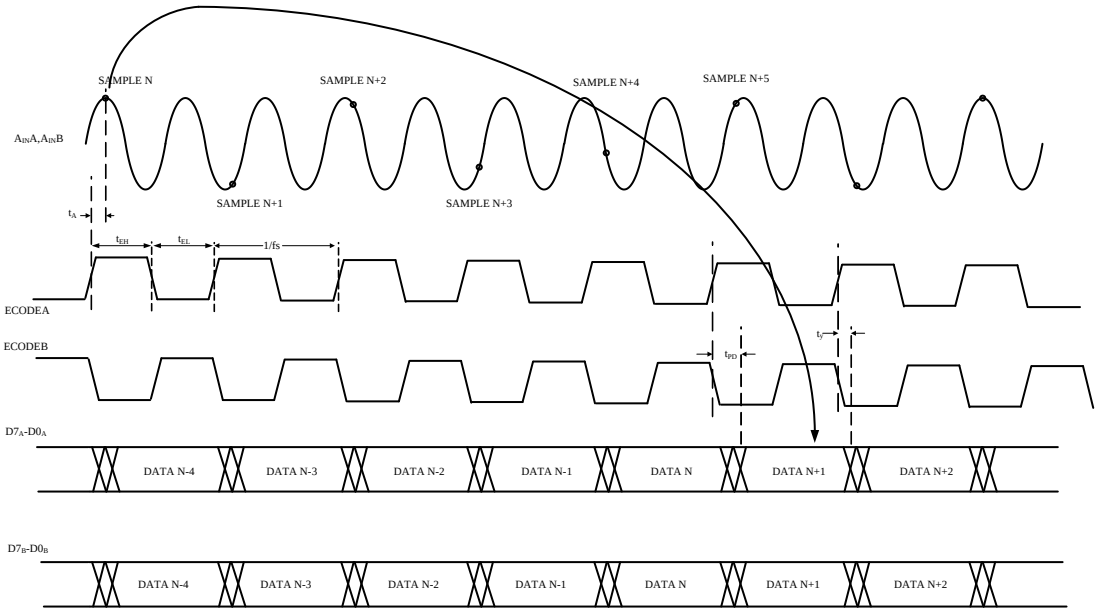


Figure 6-3. Data Align with Two Clock Sources (S1 = 1, S2 = 1) Channel Timing

The B9288ARH provides latched data outputs, with four pipeline delays. Data outputs are available one propagation delay after the rising edge of the encode command (see up Figures 6-1, 6-2, 6-3). The length of the output data lines and loads placed on them should be minimized to reduce transients within the B9288ARH.

These transients can detract from the converter's dynamic performance. The minimum guaranteed conversion rate of the B9288ARH is 1 MSPS. At clock rates below 1 MSPS, dynamic performance will degrade. Typical power up recovery time after standby mode is 15 clock cycles.

6. User Select Options

Two pins are available for a combination of operational modes. These options allow the user to place both channels in standby, excluding the reference, or just the B channel. Both modes place the output buffers and clock inputs in high impedance states.

The other option allows the user to skew the B channel output data by 1/2 a clock cycle. In other words, if two clocks are fed to the B9288ARH and are 180 °out of phase, enabling the data align will allow Channel B output data to be available at the rising edge of Clock A. If the same encode clock is provided to both channels and the data align pin is enabled, then output data from Channel B will be 180 °out of phase with respect to Channel A. If the same encode clock is provided to both channels and the data align pin is disabled, then both outputs are delivered on the same rising edge of the clock.

Table 6-1 User Select Function

S1	S2	User Select Options
0	0	Standby Both Channels A and B.
0	1	Standby Channel B Only.
1	0	Normal Operation (Data Align Disabled).
1	1	Data align enabled (data from both channels available on rising edge of Clock A. Channel B data is delayed a 1/2 clock cycle)

6.2 Storage Condition

The warehouse environment of B9288ARH should be consistent with requirements of the Ⅰ class warehouse, and comply with the requirements of 4.1.1 of "The Space Component's effective storage period and extended retest requirements":

- The device must be stored in a warehouse with good ventilation and no acid, alkaline, or other corrosive gas around. The temperature and humidity should be

controlled within a certain range as follow:

The Class of Storage Environment

Symbol	Temperature(℃)	Relative Humidity (%)
Ⅰ	10~25	25~70
Ⅱ	-5~30	20~75
Ⅲ	-10~40	20~85

6.3 Absolute Maximum Ratings

1) Power Voltage（V_D）…… -0.3V～4.0V

2) Storage temperature (T_{STG})：…… -65℃~+ 150℃

3)Thermal Resistance（$R_{th\ (jc)}$） …… 5℃/W

4)Weld Temperature（T_H,10s）……260℃(Mac.)；300℃（Manual）

5)Junction Temperature（T_J） …… 150℃

6.4 Recommended Operating Conditions

a) Supply power voltage（V_D）……3V

b) Input voltage reference （V_{REF}）……1.2V

c) Temperature for operating（T_A）……-55℃ ～ 125℃

6.5 Radiation Hardened Performance

a） Total Ionizing Dose：≥100K Rad(Si)

b） The Single Event Latch-up threshold：≥37MeV cm^2/mg

7. Electrical Characteristics

The testing temperature of the device is 25℃, and the result listed in the table.

Parameter	Symbol	condition （-55℃≤ TA ≤ 125℃ VDD=VD=+3V，GND=0V.）	min	typ	max	units
Resolution	*RES*			8		bit
Integral Nonlinearity	E_L		-1.5	±1.0	1.5	LSB
Differential Nonlinearity	E_{DL}		-1.0	±0.5	1.0	LSB
Gain Error	E_G		-8	±4	8	%FS
Input Voltage	V_{ins}		—	1.0	1.0	Vpp

Parameter	Symbol	condition （-55℃≤ TA ≤ 125℃ VDD=VD=+3V，GND=0V.）	min	typ	max	units
Range						
Output Reference Voltage	V_{REF}		1.14	1.18	1.24	V
High level output voltage	V_{OH}		2.4	2.95	—	V
Low level output voltage	V_{OL}		—	0.04	0.2	V
Power dissipation	P_W	Double Channel mode，f_{SAMPLE}=100MSPS	—	180	220	mW
		Single Channel mode，f_{SAMPLE}=100MSPS	—	100	120	mW
		Standby mode，f_{SAMPLE}=100MSPS	—	6	15	mW
Input common voltage	$V_{in\cdot\ cm}$		0.7	0.9	1.1	V
Input resistance	R_{IN}		7	10	13	kΩ
Input capacitance	C_{IN}		—	7	10	pF
Analog Bandwidth Full Power	BW_p		475	475	—	MHz
Signal to Noise Ratio	*SNR*	f_{in}=10MHz，differential Input，-0.7dBFS，f_{SAMPLE}=100MSPS	43	45	—	dB
Signal to Noise and Distortion	*SINAD*		42.5	44	—	dB
Spurious Free Dynamic Range	*SFDR*		50	60	—	dB
Channel insulate ratio	*CIR*		55	60	—	dB
Effective number of bits	*ENOB*		6.8	7.0	—	Bit
Conversion frequency	f_s		100	100	—	MHz

8. Typical application（Appendix Ⅰ）

9. Package Outline Dimension

CQFP48 packaging.

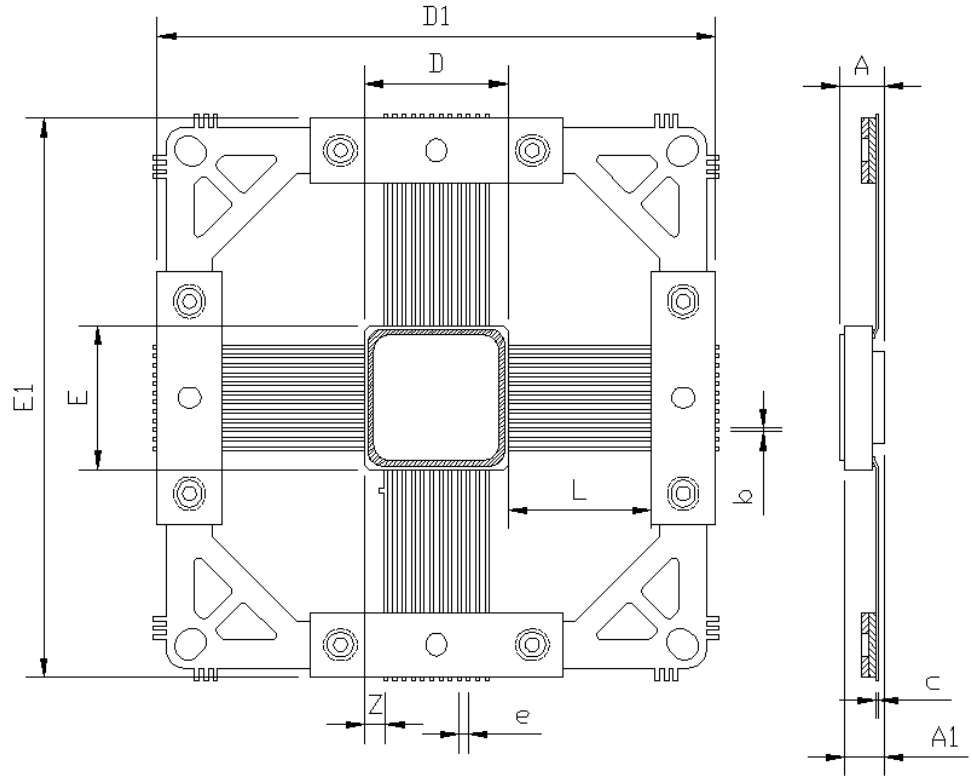


Figure 9-1. Outline dimension before cut

Symbol	Value（Units:mm）		
	Min.	Typ.	Max.
A	1.9	–	2.8
A1	1.8	–	2.5
b	0.15	–	0.25
c	–	0.15	–
e	–	0.5	–
Z	–	1.15	–
D/E	7.3	7.8	8.3
D1/E1	29.0	–	31.6
L	–	7.75	–

B9288ARH should be cut to suitable size before used. The last dimension is shown in:

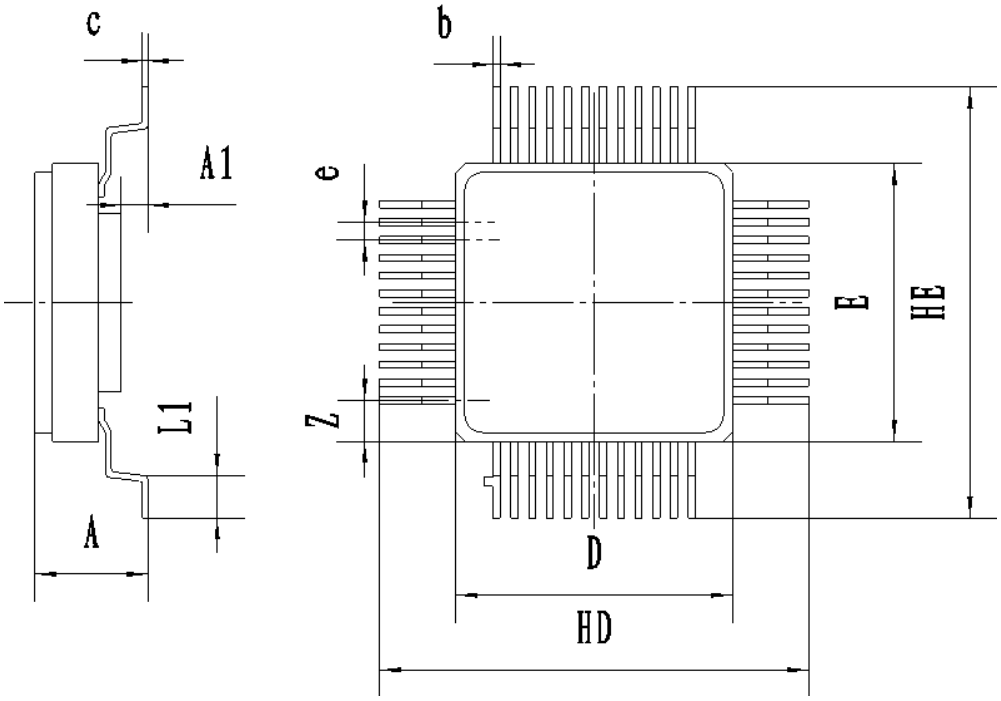
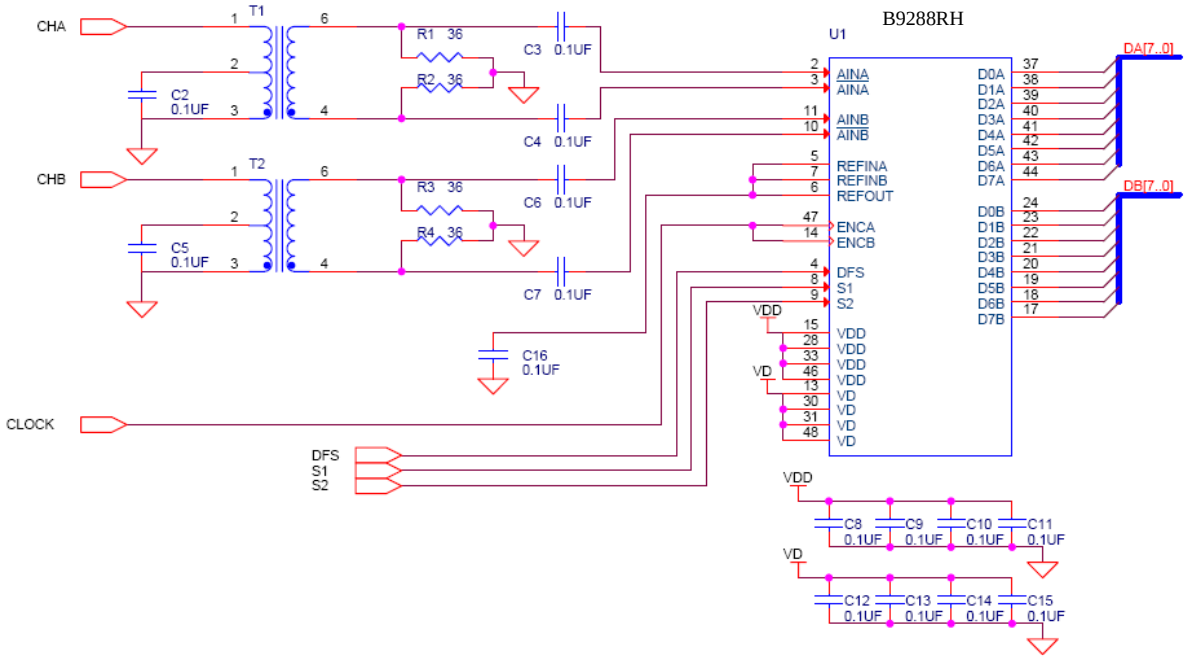


Figure 9-2. Outline dimension after cut

Symbol	Value（Units:mm）		
	Min.	Typ	Max.
A	2.6	–	3.6
A1	0.5	0.75	1.01
b	–	0.2	–
c	–	0.152	–
e	–	0.5	–
Z	–	1.15	–
D/E	7.6	7.8	8.0
HD/HE	12.1	12.8	13.5
L1	1.25	1.5	1.75

Appendix Ⅰ: Typical application



The figure is shown the typical application of B9288ARH, with ac coupled input.

In order to get the best performance of B9288ARH, recommend to change the single-ended to differential input which is used a balun. If absolutely to use a single ended input, the minus input of A_{IN} or B_{IN} must be connected a 0.1uF capacitance before connect to GND, which to assure the input common voltage is 1V.

The clock input should adopt a stable clock resource with the minimum jitter.

In the PCB design, the coupling capacitance should be considered carefully, every power source input should coupled a 0.1uF capacitance nearly.

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