Ver 1.1

# 14-Bit 2GSPS Digital to Analog Converter

# Datasheet

**Part Number：B9739RB**

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# Page of Revise Control

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| 1.0 | 2017.12 | - | - | |
| 1.1 | 2018.3 | - | Changed the template, corrected parameter | |
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# 1. Unique features


- Industry leading single/multicarrier IF or RF synthesis
- Dual-port LVDS data interface Up to 1 GSPS operation
  Source synchronous DDR clocking
- Programmable output current: 9mA to 30 mA
- Low power: 0.9 W at 2.0 GSPS
- Total Ionizing Dose ≥ 100 Krad(Si)
- SEL threshold ≥ 75 MeV $cm^2/mg$

# 2. General Description

The B9739RB is a 14-bit, 2.0 GSPS high performance RF digital-to-analog converter (DAC). Its DAC core features a quad-switch architecture that provides exceptionally low distortion performance with an industry-leading direct RF synthesis capability. This feature enables multicarrier generation up to the Nyquist frequency in baseband mode as well as second and third Nyquist zones in mix mode. The output current can be programmed over the 9 mA to 30 mA range.

The inclusion of on-chip controllers simplifies system integration. A dual-port, source synchronous, LVDS interface simplifies the digital interface with existing FGPA/ASIC technology. On-chip controllers are used to manage external and internal clock domain variations over temperature to ensure reliable data transfer from the host to the DAC core. Multichip synchronization is possible with an on-chip synchronization controller. A serial peripheral interface (SPI) is used for device configuration as well as readback of status registers.

The B9739RB is manufactured on a 0.18 μm CMOS process and operates from 1.8V and 3.3V supplies. It is supplied in a 160-ball chip scale ball grid array for reduced package parasitics.

# 3. Block Diagram

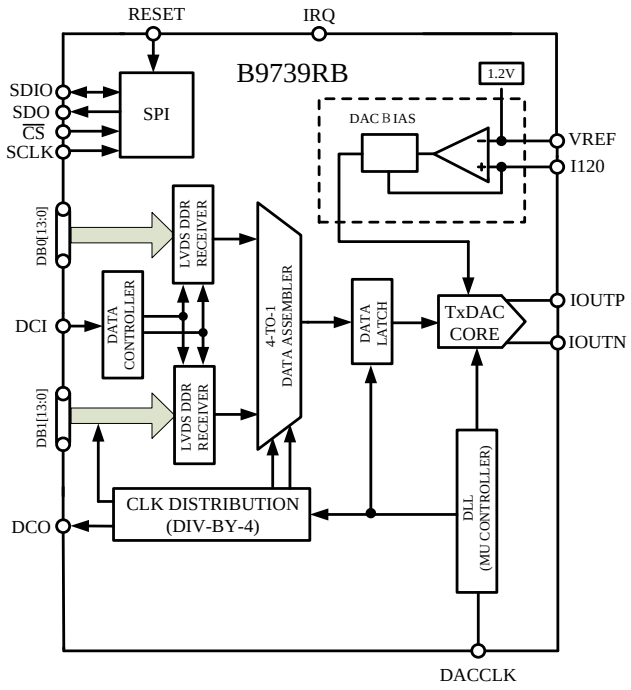



**Figure 3-1. Block Diagram**

**PRODUCT HIGHLIGHTS**

- Ability to synthesize high quality wideband signals with bandwidths of up to 1 GHz in the first or second Nyquist zone.
- A proprietary quad-switch DAC architecture provides exceptional ac linearity performance while enabling mix mode operation.
- A dual-port, double data rate, LVDS interface supports the maximum conversion rate of 2000 MSPS.
- On-chip controllers manage external and internal clock domain skews.
- Programmable differential current output with a 9 mA to 30 mA range.

# 4. Pin Description

The B9739RB is packaged in CBGA160. The pins description are shown in figure 4-1.

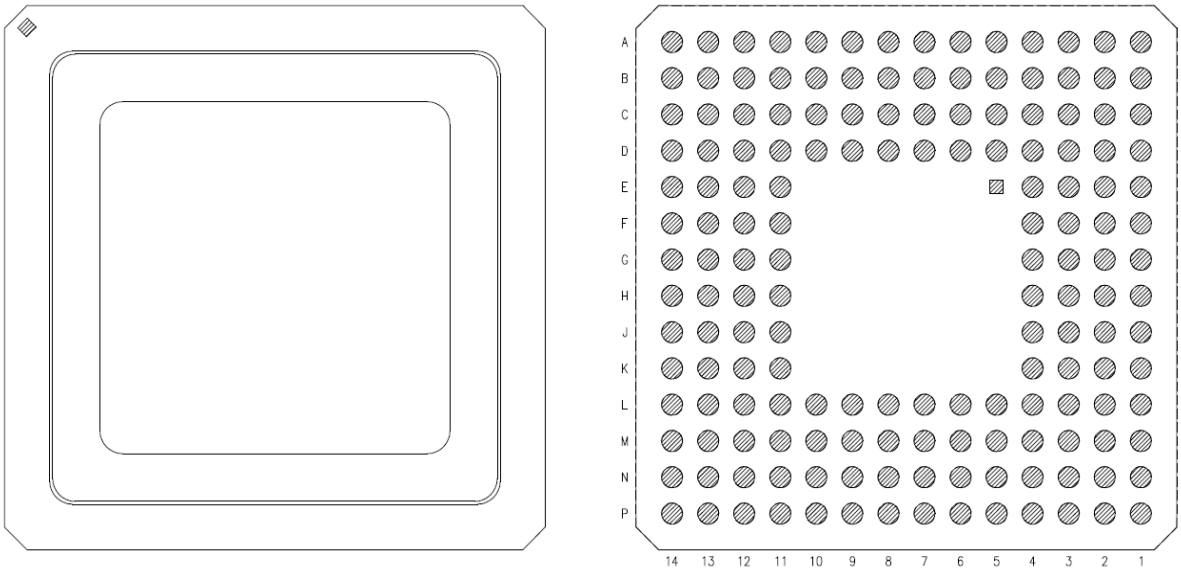



**Figure 4-1. Pin configuration**

# 5. Electrical Characteristic

| Parameter | Symbol | Condition（Unless other notes，$V_{DDA}$=$V_{DD33}$=3.3V，$V_{DD}$=$V_{DDC}$=1.8V $I_{OFS}$=20mA，-55℃ ≤ $T_A$≤ 125℃） | Min. | Max. | Units |
|---|---|---|---|---|---|
| RESOLUTION | *RES* | — | 14 | — | Bits |
| Differential Nonlinearity (DNL) | $E_{DL}$ | — | -3.0 | +3.0 | LSB |
| Integral Nonlinearity (INL) | $E_L$ | — | -5.0 | +5.0 | LSB |
| Gain Error | $E_G$ | — | -5.5 | +5.5 | %FS |
| Full-Scale Output Minimum Current | $I_{FS\_min}$ | — | — | 9 | mA |
| Full-Scale Output Maximum Current | $I_{FS\_max}$ | — | 30 | — | mA |
| Output Compliance Range | $V_{OC}$ | — | -1 | +1 | V |
| Internal Reference Voltage | $V_{REF}$ | — | 1.15 | 1.30 | V |
| Analog Power Supply Current | $I_{VDDA}$ | $f_{DAC}$=2.0GSPS | — | 57 | mA |
| 3.3V Digital Power Supply Current | $I_{VDD33}$ | $f_{DAC}$ =2.0GSPS | — | 56 | mA |
| 1.8V Digital Power Supply Current | $I_{VDD}$ | $f_{DAC}$ =2.0GSPS | — | 357 | mA |
| Clock Power Supply Current | $I_{VDDC}$ | $f_{DAC}$ =2.0GSPS | — | 249 | mA |
| Power Dissipation | $P_w$ | $f_{DAC}$ =2.0GSPS | — | 1.6 | W |

| | | | | | |
|---|---|---|---|---|---|
| LVDS Input Common-Mode Voltage Range | $V_{COM}$ | — | 1000 | 1400 | mV |
| LVDS Differential Input Threshold | $\|V_{IDTH}\|$ | — | 200 | — | mV |
| LVDS Differential Output Resistance | $Z_T$ | — | 75 | 135 | Ω |
| LVDS（DB）Input Rate | $f_{DB}$ | $f_{DAC}$=2.0GSPS | 1000 | — | MSPS |
| LVDS（DCI）Input Rate | $f_{DCI}$ | $f_{DAC}$=2.0GSPS | 500 | — | MSPS |
| Digital Input High Voltage | $V_{IH}$ | Logical Control Interface | 2.4 | — | V |
| Digital Input Low Voltage | $V_{IL}$ | Logical Control Interface | — | 0.4 | V |
| Digital Input High Current | $I_{IH}$ | Logical Control Interface | -10 | +10 | μA |
| Digital Input Low Current | $I_{IL}$ | Logical Control Interface | -10 | +10 | μA |
| Digital Output High Voltage | $V_{OH}$ | $I_{OH}$=4mA | 2.4 | 3.5 | V |
| Digital Output Low Voltage | $V_{OL}$ | $I_{OL}$=4mA | 0 | 0.5 | V |
| Maximum Update Rate | $f_{DAC}$ | — | 2.0 | — | GSPS |
| Spurious-Free Dynamic Range | *SFDR* | $f_{DAC}$=2GSPS，$f_O$=20MHz | 50 | — | dBc |
| | | $f_{DAC}$ =2GSPS，$f_O$=100MHz | | | |
| | | $f_{DAC}$ =2GSPS，$f_O$=550MHz | | | |
| Two-Tone Intermodulation Distortion | *TTIMD* | $f_{DAC}$ =2GSPS，$f_{out1}$=20MHz，$f_{out2}$=21.25MHz | 60 | — | dBc |
| | | $f_{DAC}$ =2GSPS，$f_{out1}$=100MHz，$f_{out2}$=101.25MHz | | | |
| | | $f_{DAC}$ =2GSPS，$f_{out1}$=550MHz，$f_{out2}$=551.25MHz | | | |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | With Respect To | Rating |
|---|---|---|
| $V_{DDA}$ | $V_{SSA}$ | -0.3V~+3.6V |
| $V_{DD33}$ | $V_{SSA}$ | -0.3V~+3.6V |
| $V_{DD}$ | $V_{SS}$ | -0.3V~+1.98V |
| $V_{DDC}$ | $V_{SSC}$ | -0.3V~+1.98V |
| $V_{SSA}$ | $V_{SS}$ | -0.3V~+0.3V |
| $V_{SSA}$ | $V_{SSC}$ | -0.3V~+0.3V |
| $V_{SS}$ | $V_{SSC}$ | -0.3V~+0.3V |
| DACCLK_P,DACCLK_N | $V_{SSC}$ | -0.3V~VDDC+0.18V |
| DCI,DCO,SYNC_IN,SYNC_OUT | $V_{SS}$ | -0.3V~VDD33+0.3V |
| LVDS Data Inputs | $V_{SS}$ | -0.3V~VDD33+0.3V |
| IOUTP,IOUTN | $V_{SSA}$ | -1.0V~VDDA+0.3V |

| | | |
|---|---|---|
| I120,VREF | $V_{SSA}$ | -0.3V~VDDA+0.3V |
| IRQ, $\overline{CS}$, SCLK,SDO,SDIO,RESET | $V_{SS}$ | -0.3V~VDD33+0.3V |
| Junction Temperature | | 175℃ |
| Storage Temperature | | -65℃~150℃ |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# 6. Product Description

## 6.1 Function Description

The B9739RB contains a set of programmable registers described in Table 6-3 that are used to configure and monitor various internal parameters. Note the following points when programming the B9739RB SPI registers:

• Registers pertaining to similar functions are grouped together and assigned adjacent addresses.

• Bits that are undefined within a register should be assigned a 0 when writing to that register.

• Registers that are undefined should not be written to.

• A hardware or software reset is recommended upon power-up to place SPI registers in a known state.

• A SPI initialization routine is required as part of the boot process.

### 6.1.1 Reset

Issuing a hardware or software reset places the B9739RB SPI registers in a known state. All SPI registers (excluding 0x00) are set to their default states as described in Table 6-3 upon issuing a reset. After issuing a reset, the SPI initialization process need only write to registers that are required for the boot process as well as any other register settings that must be modified, depending on the target application.

Although the B9739RB does feature an internal power-on-reset (POR), it is still recommended that a software or hardware reset be implemented shortly after power-up. The internal reset signal is derived from a logical OR operation from the internal POR signal, the RESET pin, and the software reset state. A software reset can be issued via the reset bit (Register 0x00, Bit 5) by toggling the bit high then low.

Note that, because the MSB/LSB format may still be unknown upon initial power-up (that is, internal POR is unsuccessful), it is also recommended that the bit settings for Bits[7:5] be mirrored onto Bits[2:0] for the instruction cycle that issues a software reset. A hardware reset can be issued from a host or external supervisory IC by applying a high pulse with a minimum width of 40 ns to the RESET pin (that is, Pin F14). RESET should be tied to VSS if unused

**Table 6-1 SPI Registers Pertaining to SPI Options**

| Address(Hex) | Bit | Description |
|---|---|---|
| 0x00 | 7 | Enable 3-wire SPI |
| | 6 | Enable SPI LSB first |
| | 5 | Software reset |

### 6.1.2 SPI Operation

The serial port of the B9739RB shown in Figure 6-1 has a 3- or 4-wire SPI capability, allowing read/write access to all registers that configure the device's internal parameters. It provides a flexible, synchronous serial communications port, allowing easy interface to many industry- standard microcontrollers and microprocessors. The 3.3 V serial I/O is compatible with most synchronous transfer formats, including the Motorola SPI and the Intel SSR protocols.

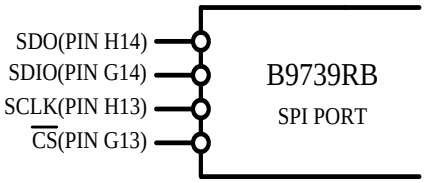



**Figure 6-1 B9739RB SPI Port**

#### 6.1.2.1 Instruction Header Information

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 |
| R/W | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

An 8-bit instruction header must accompany each read and write operation. The MSB is a R/indicator bit with logic high indicating a read operation. The remaining seven bits specify the address bits to be accessed during the data transfer portion. The eight data bits immediately follow the instruction header for both read and write operations. For write operations, registers change immediately upon writing to the last bit of each transfer byte. $\overline{CS}$ can be raised after each sequence of eight bits (except the last byte) to stall the bus. The serial transfer resumes when $\overline{CS}$ is lowered. Stalling on nonbyte boundaries resets the SPI.

The B9739RB serial port can support both most significant bit (MSB) first and

least significant bit (LSB) first data formats. Figure 6-2 illustrates how the serial port words are formed for the MSB first and LSB first modes. The bit order is controlled by the SDIO_DIR bit (Register 0x00, Bit 7). The default value is 0, MSB first. When the LSB first bit is set high, the serial port interprets both instruction and data bytes LSB first.

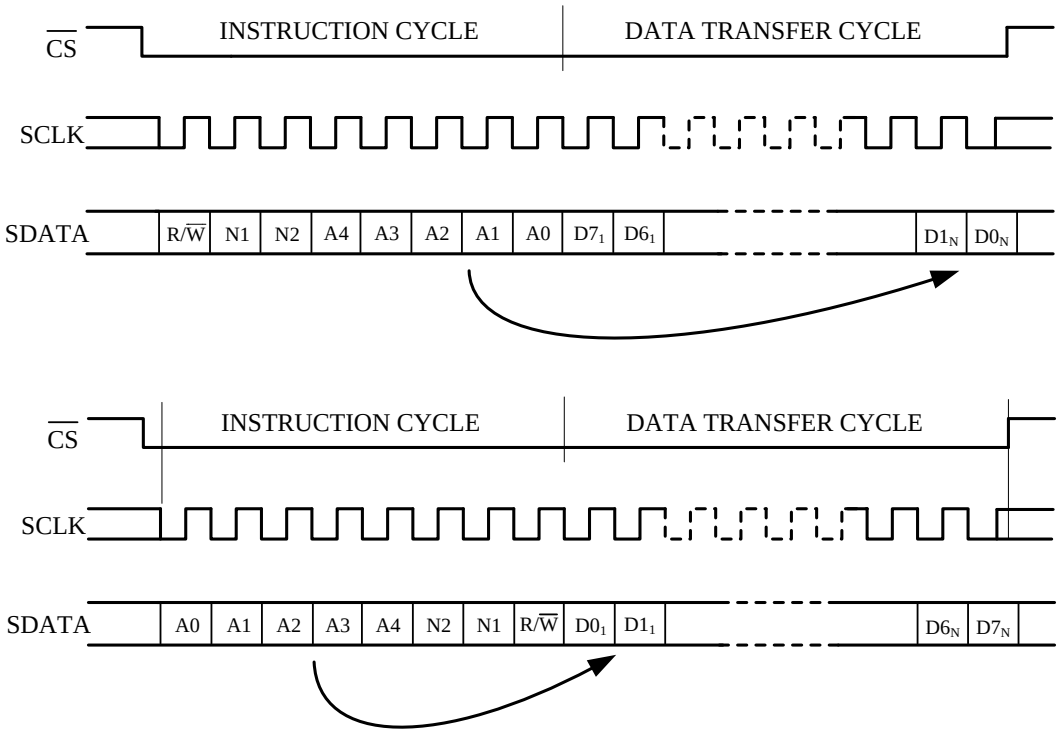



**Figure 6-2 SPI Timing, MSB First(Upper) and LSB First(Lower)**

Figure 6-3 illustrates the timing requirements for a write operation to the SPI port. After the serial port enable ($\overline{CS}$) signal goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of the clock (SCLK). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the SDIO pin on the rising edge of the next eight clock cycles.

Figure 6-4 illustrates the timing for a 3-wire read operation to the SPI port. After $\overline{CS}$ goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of SCLK. A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the SDIO pin on the falling edges of the next eight clock cycles.

Figure 6-5 illustrates the timing for a 4-wire read operation to the SPI port. The timing is similar to the 3-wire read operation with the exception that data appears at

the SDO pin only, while the SDIO pin remains at high impedance throughout the operation. The SDO pin is an active output only during the data transfer phase and remains three-stated at all other times.

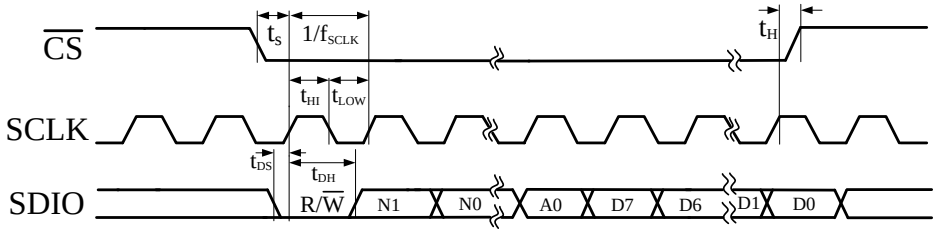



**Figure 6-3 SPI Write Operation Timing**

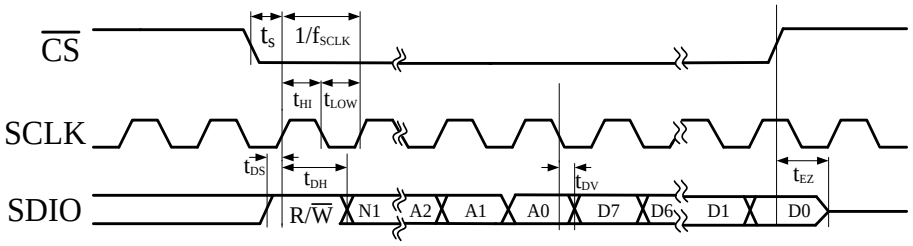



**Figure 6-4 SPI 3-Wire Read Operation Timing**

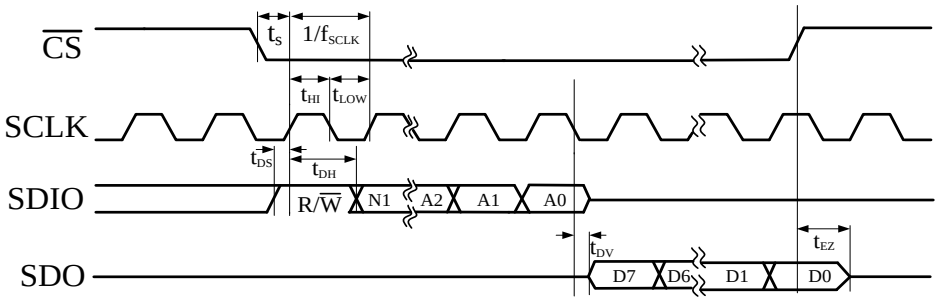



**Figure 6-5 SPI 4-Wire Read Operation Timing**

## 6.2 SPI Register Map

**Table 6-2 Full Register Map（ = Not Applicable）**

| Name | Hex Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bi t2 | Bit 1 | Bit 0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| Mode | 00 | SDIO_DIR | LSB/MSB | Reset | | | | | | 0x00 |
| Power-Down | 01 | | | LVDS_ DRVR_PD | LVDS_ DCVR_PD | | | CLK_ RCVR_PD | DAC_ BIAS_PD | 0x00 |
| CNT_ CLK_DIS | 02 | | | | | CLKGEN_PD | | REC_CNT_ CLK | MU_CNT_ CLK | 0x03 |
| IRQ_EN | 03 | | | | | MU_LST_EN | MU_LCK_EN | RCV_ LST_EN | RCV_ LCK_EN | 0x00 |
| IRQ_REQ | 04 | | | | | MU_LST_ IRQ | MU_LCK_ IRQ | RCVLST_ IRQ | RCVLCK_ IRQ | 0x00 |

| Name | Hex Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bi t2 | Bit 1 | Bit 0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| RSVD | 05 | | | | | | | | | |
| FSC_1 | 06 | FSC[7] | FSC[6] | FSC[5] | FSC[4] | FSC[3] | FSC[2] | FSC[1] | FSC[0] | 0x00 |
| FSC_2 | 07 | Sleep | | | | | | FSC[9] | FSC[8] | 0x02 |
| DEC_ CNT | 08 | | | | | | | DAC_DEC[1] | DAC_DEC[0] | 0x00 |
| LVDS_ CNT | 0A | | | | | HNDOFF_ CHK_RST | | LVDS_ Bias[1] | LVDS_ Bias[0] | 0x00 |
| DIG_ STAT | 0B | HNDOFF_ Fall[3] | HNDOFF_ Fall[2] | HNDOFF_ Fall[1] | HNDOFF_ Fall[0] | HNDOFF_ Rise[3] | HNDOFF_ Rise[2] | HNDOFF_ Rise[1] | HNDOFF_ Rise[0] | RNDM |
| LVDS_ STAT1 | 0C | SUP/HLD_ Edge1 | | DCI_ PHS3 | DCI_ PHS1 | DCI_PRE_ PH2 | DCI_PRE_ PH0 | DCI_PST_ PH2 | DCI_PST_ PH0 | RNDM |
| LVDS_ STAT2 | 0D | | SUP/HLD_ Edge0 | | | LVDS1_HI | LVDS1_LO | LVDS0_HI | LVDS0_LO | RNDM/0 |
| LVDS_ REC_ CNT1 | 10 | | | | | | RCVR_ FLG_RST | RCVR_ LOOP_ON | RCVR_ CNT_ENA | 0x42 |
| LVDS_ REC_ CNT2 | 11 | SMP_DEL[1] | SMP_DEL[0] | FINE_DEL_M ID[3] | FINE_DEL_M ID[2] | FINE_DEL_M ID[1] | FINE_DEL_M ID[0] | RCVR_ GAIN[1] | RCVR_ GAIN[0] | 0xDD |
| LVDS_ REC_ CNT3 | 12 | SMP_DEL[9] | SMP_DEL[8] | SMP_DEL[7] | SMP_DEL[6] | SMP_DEL[5] | SMP_DEL[4] | SMP_DEL[3] | SMP_DEL[2] | 0x29 |
| LVDS_ REC_ CNT4 | 13 | DCI_DEL[3] | DCI_DEL[2] | DCI_DEL[1] | DCI_DEL[0] | FINE_DEL_ SKW[3] | FINE_DEL_ SKW[2] | FINE_DEL_ SKW[1] | FINE_DEL_ SKW[0] | 0x71 |
| LVDS_ REC_ CNT5 | 14 | CLKDIVPH[1] | CLKDIVPH[0] | DCI_DEL[9] | DCI_DEL[8] | DCI_DEL[7] | DCI_DEL[6] | DCI_DEL[5] | DCI_DEL[4] | 0x0A |
| LVDS_ REC_ CNT6 | 15 | | | | | LCKTHR[3] | LCKTHR[2] | LCKTHR[1] | LCKTHR[0] | 0x42 |
| LVDS_ REC_ STAT1 | 19 | SMP_DEL[1] | SMP_DEL[0] | | | SMP_FINE_ DEL[3] | SMP_FINE_ DEL[2] | SMP_FINE_ DEL[1] | SMP_FINE_ DEL[0] | 0xC7 |
| LVDS_ REC_ STAT2 | 1A | SMP_DEL[9] | SMP_DEL[8] | SMP_DEL[7] | SMP_DEL[6] | SMP_DEL[5] | SMP_DEL[4] | SMP_DEL[3] | SMP_DEL[2] | 0x29 |
| LVDS_ REC_ STAT3 | 1B | DCI_DEL[1] | DCI_DEL[0] | | | | | CLKDIV PH[1] | CLKDIV PH[0] | 0xC0 |
| LVDS_ | 1C | DCI_DEL[9] | DCI_DEL[8] | DCI_DEL[7] | DCI_DEL[6] | DCI_DEL[5] | DCI_DEL[4] | DCI_DEL[3] | DCI_DEL[2] | 0x29 |

| Name | Hex Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bi t2 | Bit 1 | Bit 0 | Default |
|---|---|---|---|---|---|---|---|---|---|---|
| REC_ STAT4 | | | | | | | | | | |
| LVDS_ REC_ STAT5 | 1D | FINE_DEL_ PST[3] | FINE_DEL_ PST[2] | FINE_DEL_ PST[1] | FINE_DEL_ PST[0] | FINE_DEL_ PRE[3] | FINE_DEL_ PRE[2] | FINE_DEL_ PRE[1] | FINE_DEL_ PRE[0] | 0x86 |
| LVDS_ REC_ STAT9 | 21 | | | | | RCVR_ TRK_ON | RCVR_ FE_ON | RCVR_LST | RCVR_LCK | 0x00 |
| CROSS_ CNT1 | 22 | | | | DIR_P | CLKP_ OFFSET[3] | CLKP_ OFFSET[2] | CLKP_ OFFSET[1] | CLKP_ OFFSET[0] | 0x00 |
| CROSS_ CNT2 | 23 | | | | DIR_N | CLKN_ OFFSET[3] | CLKN_ OFFSET[2] | CLKN_ OFFSET[1] | CLKN_ OFFSET[0] | 0x00 |
| PHS_ DET | 24 | | | CMP_BST | PHS_DET AUTO_EN | Bias[3] | Bias[2] | Bias[1] | Bias[0] | 0x00 |
| MU_ DUTY | 25 | MU- DUTYAUTO_E N | POS/NEG | ADJ[5] | ADJ[4] | ADJ[3] | ADJ[2] | ADJ[1] | ADJ[0] | 0x00 |
| MU_ CNT1 | 26 | | Slope | Mode[1] | Mode[0] | Read | Gain[1] | Gain[0] | Enable | 0x42 |
| MU_ CNT2 | 27 | MUDEL[0] | SRCH_ MODE[1] | SRCH_ MODE[0] | SET_PHS[4] | SET_PHS[3] | SET_PHS[2] | SET_PHS[1] | SET_PHS[0] | 0x40 |
| MU_ CNT3 | 28 | MUDEL[8] | MUDEL[7] | MUDEL[6] | MUDEL[5] | MUDEL[4] | MUDEL[3] | MUDEL[2] | MUDEL[1] | 0x00 |
| MU_ CNT4 | 29 | SEARCH_TOL | Retry | CONTRST | Guard[4] | Guard[3] | Guard[2] | Guard[1] | Guard[0] | 0x0B |
| MU_ STAT1 | 2A | | | | | | | MU_LOST | MU_LKD | 0x00 |
| ANA_ CNT1 | 32 | HDRM[7] | HDRM[6] | HDRM[5] | HDRM[4] | HDRM[3] | HDRM[2] | HDRM[1] | HDRM[0] | 0xCA |
| ANA_ CNT2 | 33 | | | | | | | MSEL[1] | MSEL[1] | 0x03 |
| PARTID | 35 | ID[7] | ID[6] | ID[5] | ID[4] | ID[3] | ID[2] | ID[1] | ID[0] | 0x20 |

**Table 6-3 SPI Port Configuration and Software Reset Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x00 | SDIO_DI R | 7 | R/W | 0 | 0=4-wire SPI，1=3-wire SPI |
| | LSB/MSB | 6 | R/W | 0 | 0=MSB first，1=LSB first |
| | Reset | 5 | R/W | 0 | Software reset is recommended before modification of other SPI registers from the |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | default setting. Setting the bit to 1 causes all registers (except 0x00) to be set to the default setting. Setting the bit to 0 corresponds to the inactive state, allowing the user to modify registers from the default setting |

**Table 6-4 POWER-DOWN LVDS Interface and TXDAC Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x01 | LVDS_DRVR_PD | 5 | R/W | 0 | Power-down of the LVDS drivers/receivers and TxDAC. 0 = enable, 1 = disable. |
| | LVDS_RCVR_PD | 4 | R/W | 0 | |
| | CLK_RCVR_PD | 1 | R/W | 0 | |
| | DAC_BIAS_PD | 0 | R/W | 0 | |

**Table 6-5 Control Clock Disable Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x02 | CLKGEN_PD | 3 | R/W | 0 | Internal CLK distribution enable: 0 = enable, 1 = disable. |
| | REC_CNT_CLK | 1 | R/W | 1 | LVDS receiver and Mu controller clock disable. 0 = disable, 1 = enable. |
| | REC_CNT_CLK | 0 | R/W | 1 | |

**Table 6-6 Interrupt Request(ipq) Enable/Status Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x03 | MU_LST_EN | 3 | W | 0 | This register enables the sync, mu, and LVDS Rx controllers to update their corresponding IRQ status bits in Register 0x04, which defines whether the controller is locked (LCK) or unlocked (LST).<br>0 = disable (resets the status bit).<br>1 = enable. |
| | MU_LCK_EN | 2 | W | 0 | |
| | RCV_LST_EN | 1 | W | 0 | |
| | RCV_LCK_EN | 0 | W | 0 | |
| 0x04 | MU_LST_IRQ | 3 | R | 0 | This register indicates the status of the controllers. For LCK_IQR bits: 0 = lost locked, 1 = locked. For LST_IQR bits: 0 = not lost locked, 1 = unlocked. Note that, if the controller IRQ is serviced, the relevant bits in Register 0x03 should be reset by writing 0, followed by another write of 1 to enable. |
| | MU_LCK_IRQ | 2 | R | 0 | |
| | RCV_LST_IRQ | 1 | R | 0 | |
| | RCV_LCK_IRQ | 0 | R | 0 | |

**Table 6-7 TxDAC Full-Scale Current Setting(ioutfs) and Sleep Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x06 | FSC_1 | [7:0] | R/W | 0x00 | Sets the TxDAC IOUTFS current between 8 mA and 31 mA (default = 20 mA). IOUTFS = 0.0226 × FSC[9:0] + 8.58, where FSC = 0 to 1023. |
| 0x07 | FSC_2 | [1:0] | R/W | 0x02 | |
| | Sleep | 7 | R/W | | 0 = enable DAC output, 1 = disable DAC output (sleep). |

**Table 6-8 TxDAC Quad-Switch Mode Of Operation Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x08 | DAC_DEC | [1:0] | R/W | 0x00 | 0x00 = normal baseband mode.<br>0x01 = return-to-zero mode.<br>0x02 = mix mode. |

**Table 6-9 DCI Phase Alignment Status Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x0C | DCI_PRE_PH0 | 2 | R | 0 | 0 = DCI rising edge is after the PRE delayed version of the Phase 0 sampling edge.<br>1 = DCI rising edge is before the PRE delayed version of the Phase 0 sampling edge. |
| | DCI_PST_PH0 | 0 | R | 0 | 0 = DCI rising edge is after the POST delayed version of the Phase 0 sampling edge.<br>1 = DCI rising edge is before the POST delayed version of the Phase 0 sampling edge. |

**Table 6-10 Data Receiver Controller_Data Sample Delay Value Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x11 | SMP_DEL[1:0] | [7:6] | R/W | 11 | Controller enabled: the 10-bit value (with a maximum of 332) represents the start value for the delay line used by the state machine to sample data. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Leave at the default setting of 167, which represents the midpoint of the delay line. Controller disabled: the value sets the actual value of the delay line. |

**Table 6-11 Data and Sync Receiver Controller_DCI Delay Value/Window and Phase Rotation Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x13 | DCI_DEL[3:0] | [7:4] | R/W | 0111 | Refer to the DCI_DEL description in Register 0x14. |
| | FINE_DEL_SKEW | [3:0] | R/W | 0001 | A 4-bit value sets the difference (that is, window) for the DCI PRE and POST sampling clocks. Leave at the default value of 1 for a narrow window. |
| 0x14 | CLKDIVPH[1:0] | [7:6] | R/W | 00 | Relative phase of internal div-by-4 circuit. This feature allows phase rotation in 90 ° increments (that is, 1 count) to extend Rx controllers locking range for clock rates between 0.8 GSPS to 1.6 GSPS (only valid with sync controller disabled). |
| | DCI_DEL[9:4] | [5:0] | R/W | 001010 | Controller enabled: the 10-bit value (with a maximum of 332) represents the start value for the delay line used by the state machine to sample the DCI input. Leave at the default setting of 167, which represents the midpoint of the delay line. Controller disabled: the value sets the actual value of the delay line. |

**Table 6-12 CLK Input Common Mode Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x22 | DIR_P | 4 | R/W | 0 | DIR_P and DIR_N: 0 = VCM at the DACCLK_P input decreases with the offset value. 1 = VCM at the DACCLK_P input increases with the offset value. CLKx_OFFSET sets the magnitude of the offset for the DACCLK_P and DACCLK_N inputs. For optimum performance, set to 1111. |

**Table 6-13 Mu Controller Configuration and Status Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 0x24 | CMP_BST | 5 | R/W | 0 | Phase detector enable and boost bias bits. Note that both bits should always be set to 1 to enable these functions. |
| | PHS_DET AUTO_EN | 4 | R/W | 0 | |
| 0x25 | MU_DUTY AUTO_EN | 7 | R/W | 0 | Mu controller duty cycle enable. Note that this bit should always be set to 1 to enable. |
| 0x26 | Slope | 6 | R/W | 1 | Mu controller phase slope lock. 0 = negative slope, 1 = positive slope. Refer to Table 6-17 for optimum setting. |
| | Mode[1:0] | [5:4] | R/W | 00 | Sets the mu controller mode of operation.<br>00 = search and track (recommended).<br>01 = search only.<br>10 = track. |
| | Read | 3 | R/W | 0 | Set to 1 to read the current value of the Mu delay line in. |
| | Gain[1:0] | [2:1] | R/W | 01 | Sets the mu controller tracking gain. Recommended to leave at the default 01 setting. |
| | Enable | 0 | R/W | 0 | 1 = enable the mu controller.<br>0 = disable the mu controller. |
| 0x27 | MUDEL[0] | 7 | R/W | 0 | The LSB of the 9-bit MUDEL setting. |
| | SRCH_MODE[1:0] | [6:5] | R/W | 0 | Sets the direction in which the mu controller searches (from its initial MUDEL setting) for the optimum mu delay line setting that corresponds to the desired phase/slope setting (that is, SET_PHS and slope ).<br>00 = down.<br>01 = up.<br>10 = down/up (recommended). |
| | SET_PHS[4:0] | [4:0] | R/W | 0 | Sets the target phase that the mu controller locks to with a maximum setting of 16. Refer to Table 6-17 for optimum setting. |
| 0x28 | MUDEL[8:1] | [7:0] | W | 0x00 | With enable（Bit 0, Register 0x26）setto0,this 9-bit value represents the value that the mu delay is set to. Note that the maximum value is 432.<br>With enable set to 1, this value represent the mu delayvalue at which the controller begins its seatch. Setting this value to the delay line midpoint of 216 is recommended. |
| | | | R | 0x00 | When read (Bit 3, Register 0x26) is set to 1, the value read back is equal to the value |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | written into the register when enable = 0 or the value that the mu controller locks to when enable = 1. |
| 0x29 | SEARCH_TOL | 7 | R/W | 0 | 0 = not exact (can find a phase within two values of the desired phase). 1 = finds the exact phase that is targeted (optimal setting). |
| | Retry | 6 | R/W | 0 | 0 = stop the search if the correct value is not found.<br>1 = retry the search if the correct value is not found. |
| | CONTRST | 5 | R/W | 0 | Controls whether the controller resets or continues when it does not find the desired phase.<br>0 = continue (optimal setting).<br>1 = reset. |
| | Guard[4:0] | 4 | R/W | 01011 | Sets a guard band from the beginning and end of the mu delay line which the mu controller does not enter into unless it does not find a valid phase outside the guard band (optimal value is Decimal 11 or 0x0B). |
| 0x2A | MU_LST | 1 | R | 0 | 0 = mu controller has not lost lock.<br>1 = mu controller has lost lock. |
| | MU_LKD | 0 | R | 0 | 0 = mu controller is not locked.<br>1= mu controller is locked. |

**Table 6-14 Part ID Register**

| Address(Hex) | Name | Bit | R/W | Default Setting | Comments |
|---|---|---|---|---|---|
| 0x35 | PART_ID | [7:0] | R | 0x20 | Part ID number |

## 6.3 Theory Of Operation

Figure 6-6 shows a top-level functional diagram of the B9739RB. A high performance TxDAC core delivers a signal dependent, differential current (nominal ±10 mA) to a balanced load referenced to ground. The frequency of the clock signal appearing at the B9739RB differential clock receiver, DACCLK, sets the TxDAC's update rate. This clock signal, which serves as the master clock, is routed directly to the TxDAC as well as to a clock distribution block that generates all critical internal and external clocks.

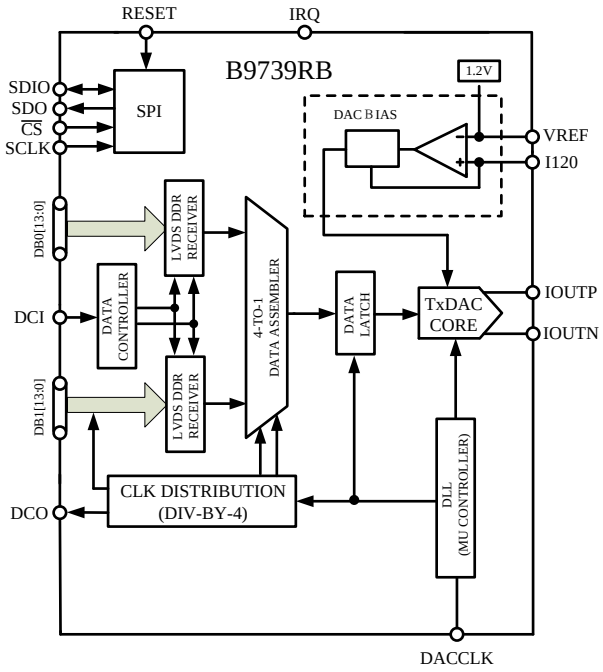



**Figure 6-6 Function Block Diagram of the B9739RB**

The B9739RB includes two 14-bit LVDS data ports (DB0 and DB1) to reduce the data interface rate to ½ the TxDAC update rate. The host processor drives deinterleaved data with offset binary format onto the DB0 and DB1 ports, along with an embedded DCI clock that is synchronous with the data. Because the interface is double data rate (DDR), the DCI clock is essentially an alternating 010101……01010 bit pattern with a frequency equal to ¼ the TxDAC update rate ($f_{DAC}$). To simplify synchronization with the host processor, the B9739RB passes an LVDS clock output (DCO) that is also equal to the DCI frequency.

The B9739RB data receiver controller generates an internal sampling clock offset by 90° from the DCI to sample the input data on the DB0 and DB1 ports. When enabled and configured properly for track mode, it ensures proper data recovery between the host and the B9739RB clock domains. The data receiver controller has the ability to track several hundreds of ps of drift between these clock domains, typically caused by supply and temperature variation.

As mentioned, the host processor provides the B9739RB with a deinterleaved data stream such that the DB0 and DB1 data ports receive alternating samples (that is, odd/even data streams). The B9739RB data assembler is used to reassemble (that is, multiplex) the odd/even data streams into their original order before delivery into the TxDAC for signal reconstruction. The pipeline delay from a sample being latched into the data port to when it appears at the DAC output is on the order of 78 (±)

DACCLK cycles. Applications that require matching pipeline delays (that is, synchronization) between multiple B9739RBs can use the SYNC controller. The SYNC controller phase aligns the outputs of one or more B9739RB devices (that is,. slaves) to a master B9739RB device.

The B9739RB includes a delay lock loop (DLL) circuit controlled via a mu controller to optimize the timing hand-off between the B9739RB digital clock domain and TxDAC core. Besides ensuring proper data reconstruction, the TxDAC's ac performance is also dependent on this critical hand-off between these clock domains with speeds of up to 2.0 GSPS. Once properly initialized and configured for track mode, the DLL maintains optimum timing alignment over temperature, time, and power supply variation.

A SPI interface is used to configure the various functional blocks as well as monitor their status for debug purposes. Proper operation of the B9739RB requires that controller blocks be initialized upon power-up. A simple SPI initialization routine is used to configure the controller blocks (see Figure 6-18 and Figure 6-19). An IRQ output signal is available to alert the host should any of the controllers fall out of lock during normal operation.

The following sections discuss the various functional blocks in more detail as well as their implications when interfacing to external ICs and circuitry. While a detailed description of the various controllers (and associated SPI registers used to configure and monitor) is also included for completeness, the recommended SPI boot procedure can be used to ensure reliable operation.

### 6.3.1 LVDS Data Port Interface

The B9739RB supports input data rates from 1.6 GSPS to 2.0 GSPS using dual LVDS data ports. The interface is source synchronous and double data rate (DDR) where the host provides an embedded data clock input (DCI) at $f_{DAC}/4$ with its rising and falling edges aligned with the data transitions. The data format is offset binary; however, twos complement format can be realized by reversing the polarity of the MSB differential trace. As shown in Figure 6-7, the host feeds the B9739RB with deinterleaved input data into two 14-bit LVDS data ports (DB0 and DB1) at ½ the DAC clock rate (that is, $f_{DAC}/2$). The B9739RB internal data receiver controller then generates a phase shifted version of DCI to register the input data on both the rising and falling edges.

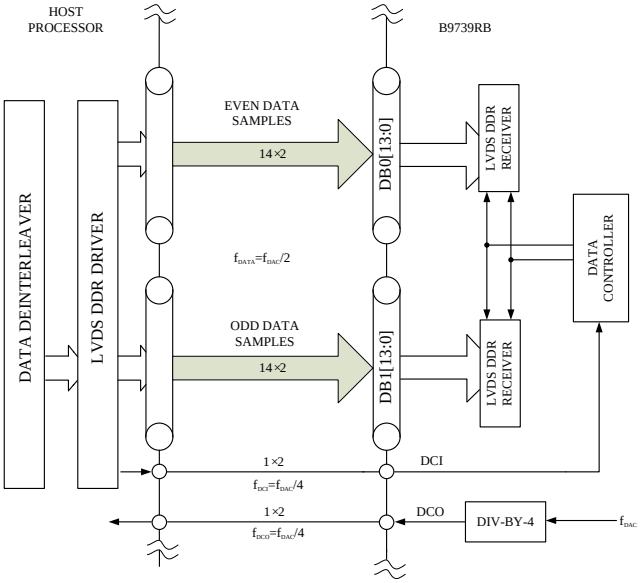



**Figure 6-7 Recommended Digital Interface Between the B9739RB Host Processor**

As shown in Figure 6-8, the DCI clocks edges must be coincident with the data bit transitions with minimum skew, jitter, and intersymbol interference. To ensure coincident transitions with the data bits, the DCI signal should be implemented as an additional data line with an alternating (010101…) bit sequence from the same output drivers used for the data. Maximizing the opening of the eye in both the DCI and data signals improves the reliability of the data port interface. Differential controlled impedance traces of equal length (that is, delay) should also be used between the host processor and B9739RB input to limit bit-to-bit skew.

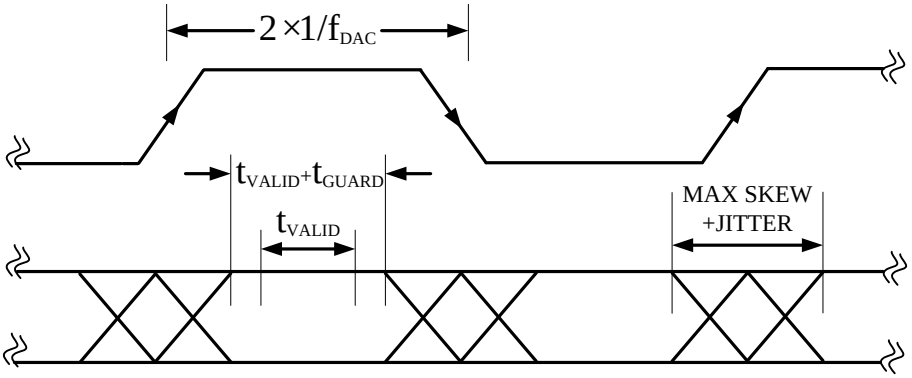



**Figure 6-8 LVDS Data Port Timing Requirements**

The maximum allowable skew and jitter out of the host processor with respect to the DCI clock edge on each LVDS port is calculated as

MaxSkew + Jitter = Period(ns) – ValidWindow(ps) - Guard

Where ValidWindow(ps) is represented by $t_{VALID}$, Guard is represented $t_{GUARD}$ in figure 6-8.

For synchronous operation, the B9739RB provides a data clock output, DCO, to the host at the same rate as DCI (that is, $f_{DAC}/4$) to maintain the lowest skew variation between these clock domains. Since the DCO signal is generated from a separate clock divider, its phase relationship relative to the $f_{DAC}/4$ clocks used by the data receiver controller will vary upon each power-up. Applications sensitive to this phase ambiguity (resulting in a ±2 DACCLK pipeline variation) should consider using the sync controller.

The host processor has a worst-case skew between DCO and DCI that is both implementation and process dependent. This worst-case skew can also vary an additional 30% over temperature and supply corners. The delay line within the data receiver controller can track a ±1.5 ns skew variation after initial lock. While it is possible for the host to have an internal PLL that generates a synchronous $f_{DAC}/4$ from which the DCI signal is derived, digital implementations that result in the shortest propagation delays result in the lowest skew variation.

The data receiver controller is used to ensure proper data hand-off between the host and B9739RB internal digital clock domains. The circuit shown in Figure 6-9 functions as a delay lock loop in which a 90o phase shifted version of the DCI clock input is used to sample the input data into the DDR receiver registers. This ensures that the sampling instance occurs in the middle of the data pattern eyes (assuming matched DCI and DBx[13:0] delays). Note that, because the DCI delay and sample delay clocks are derived from the div-by-4 circuitry, this 90° phase relationship holds as long as the delay settings (that is, DCI_DEL, SMP_DEL) are also matched.

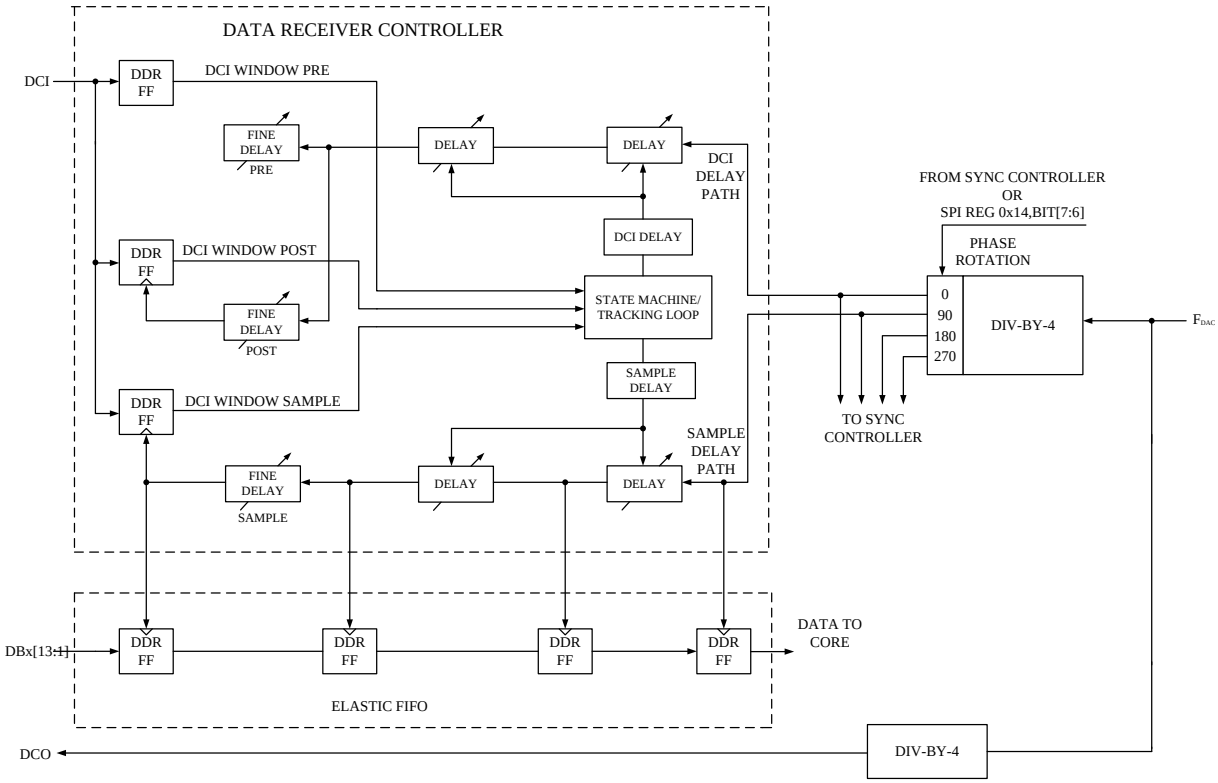



**Figure 6-9 Top Level Diagram of the Data Receiver Controller**

The div-by-4 circuit generates four clock phases that serve as inputs to the data receiver controller. All of the DDR registers in the data and DCI paths operate on both clock edges; however, for clarity purposes, only the phases (that is, 0o and 90o) corresponding to the positive edge of each path are shown. One of the div-by-4 phases is used to generate the DCO signal; therefore, the phase relationship between DCO and clocks fed into the controller remains fixed. Note that it is this attribute that allows possible factory calibration of images and clock spurs attributed to $f_{DAC}/4$ modulation of the critical DAC clock.

Once this data has been successively sampled into the first set of registers, an elastic FIFO is used to transfer the data into the B9739RB clock domain. To continuously track any phase variation between the two clock domains, the data receiver controller should always be enabled and placed into track mode (Register 0x10, Bit 1 and Bit 0). Tracking mode operates continuously in the background to track delay variations between the host and B9739RB clock domains. It does so by ensuring that the DCI signal is sampled within a very narrow window defined by two internally generated clocks (that is, PRE and PST), as shown in Figure 6-10.

Proper sampling of the DCI signal can also be confirmed by monitoring the status of DCI_PRE_PH0 (Register 0x0C, Bit 2) and DCI_PST_PH0 (Register 0x0C, Bit 0). If the delay settings are correct, the state of DCI_ PRE_PH0 should be 0, and the state

of DCI_PST_PH0 should be 1. Note that the states of these status bits may toggle occasionally due to cycle-to cycle jitter exceeding the window width. However, the controller averages these status bits over multiple clock cycles to ensure that the DCI signal falls within a programmable window.

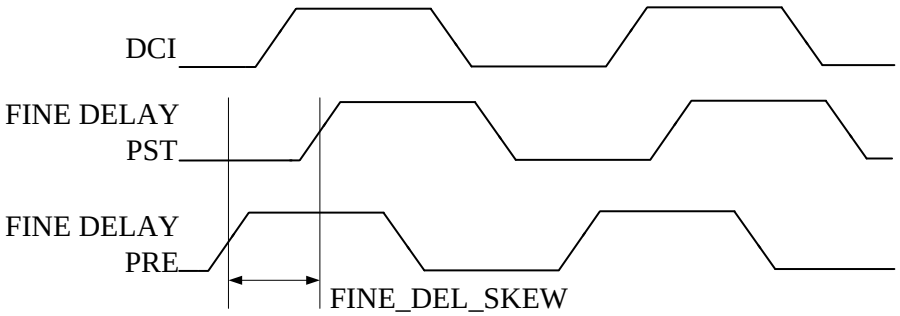



**Figure 6-10 Pre and Post-Delay Sampling Diagram**

The skew or window width (FINE_DEL_SKEW) is set via Register 0x13, Bits[3:0], with a maximum skew of approximately 180 ps and resolution of 12 ps. It is recommended that the skew be set to 36 ps (that is, Register 0x13 = 0x72) during initialization. The skew setting also affects the speed of the controller loop, with tighter skew settings corresponding to longer response time.

### 6.3.1.1 Data Receiver Controller Initialization Description

The data controller should be initialized and placed into track mode as the second step in the SPI boot sequence. The following steps are recommended for the initialization of the data receiver controller:

1. Set FINE_DEL_SKEW to 2 for a larger DCI sampling window (Register 0x13 = 0x72). Note that the default DCI_DEL and SMP_DEL settings of 167 are optimum
2. Disable the controller before enabling (that is, Register 0x10 = 0x00).
3. Enable the Rx controller in two steps: Register 0x10 = 0x02 followed by Register 0x10 = 0x03.
4. Wait 135K clock cycles.
5. Read back Register 0x21 and confirm that it is equal to 0x05 to ensure that the DLL loop is locked and tracking.
6. Include this step for operation <1.6 GSPS. Read back the DCI_DEL value to determine whether the value falls within a user-defined tracking guard band. If it does not, rotate CLKDIVPH by 1 (Register 0x14, Bits[7:6] and go back to Step 2.

Once the controller is enabled during the initial SPI boot process (see Table 6-19),

the controller enters a search mode where it seeks to find the closest rising edge of the DCI clock (relative to a delayed version of an internal $f_{DAC}/4$ clock) by simultaneously adjusting the delays in the clocks used to register the DCI and data inputs. A state machine searches above and below the initial DCI_DEL value. The state machine first searches for the first rising edge above the DCI_DEL and then searches for the first rising edge below the DCI_DEL value. The state machine selects the closest rising edge and then enters track mode. It is recommended that the default midscale delay setting (that is, Decimal 167) for the DCI_DEL and SMP_DEL bits be kept to ensure that the selected edge remains closest to the delay line midpoint, thus providing the greatest range for tracking timing variations and preventing the controller from falling out of lock.

The adjustable delay span for these internal clocks (that is, DCI and sample delay) is nominally 4 ns. The 10-bit delay value is user programmable from the decimal equivalent code (0 to 384) with approximately 12 ps/LSB resolution via the DCI_DEL and SMP_DEL registers (via Register 0x11 thru Register 0x14). When the controller is enabled, it overwrites these registers with the delay value it converges upon. The minimum difference between this delay value and the minimum/maximum values (that is, 0 and 334) represents the guard band for tracking. Therefore, if the controller initially converges upon a DCI_DEL and SMP_DEL value between 80 and 304, the controller has a guard band of at least 80 code (approximately 1 ns) to track phase variations between the clock domains.

Upon initialization of the B9739RB, a certain period of time is required for the data receiver controller to lock onto the DCI clock signal. Note that, due to its dependency on the mu controller and synchronization controller (optional), the data receiver controller should be enabled only after these other controllers have been enabled and established locked. All of the internal controllers operate at submultiples of the DAC update rate. The number of fDAC clock cycles required to lock onto the DCI clock is dependent on whether the synchronization controller is enabled as shown in Table 6-15.

**Table 6-15 Typical/Worst-Case Lock Times for LVDS Controller(Relative to $1/f_{DAC}$)**

| Synchronization Controller | Typical | Worst Case |
|---|---|---|
| Off | 70K | 135K |
| Slave | 70K | 135K |
| Master | 300K | 560K |

During the SPI initialization process, the user has the option of polling Register

0x21 (Bit 0, Bit 1, and Bit 3) to determine if the data receiver controller is locked, has lost lock, or has entered into track mode before completing the boot sequence. Alternatively, the appropriate IRQ bit (Register 0x03 and Register 0x04) can be enabled such that an IRQ output signal is generated upon the controller establishing lock (see the Interrupt Requests section).

The data receiver controller can also be configured to generate an interrupt request (IRQ) upon losing lock. Losing lock can be caused by excessive jitter on the DCI input signal, disruption of the main DAC clock input, or loss of a power supply rail. To service the interrupt, the host can poll the RCVR_LCK bit (Register 0x21, Bit 0) to determine the current state of the controller. If this bit is cleared, the search/track procedure can be restarted by setting the RCVR_LOOP_ON bit in Register 0x10, Bit 1. After waiting the required lock time, the host can poll the RCVR_LCK bit to see if it has been set. Before leaving the interrupt routine, the RCVR_FLG_RST bit (Register 0x10, Bit 2) should be reset by writing a high followed by a low.

### 6.3.1.2 Data Receiver Operation at Lower Clock Rates

At clock rates below 1.6 GSPS, it is recommended to include provisions to rotate the CLKDIVPH setting in the SPI boot process. As previously mentioned, the delay line can be varied over a nominal 4 ns window. If the minimum specified clock rate of 800 MSPS is considered, a DCI clock rate of 200 MSPS corresponds to a 5 ns period, thus exceeding the delay line length. Therefore, it becomes possible that the initial startup phase from the div-by-4 circuit (and DCO output) is such that the data receiver controller can never establish initial lock upon power up.

If the clock rate is increased to 1600 MSPS (that is, DCI clock period of 2.5 ns), the controller will always be able to find at least two DCI clock edges, therefore, establish lock. However, should the DCI edges fall symmetrically (equal distance) from the initial DCI_DEL midscale setting, a guard band of ±0.75 ns (that is, (4.0 − 2.5)/2) results. Rotating the CLKDIVPH can result in an improvement in this case by skewing one of the DCI edges toward the DCI_DEL midscale value.

Rotating the CLKDIVPH phase provides a means of adjusting the delay in course steps of $f_{DAC}/4$. For example, in the 800 MSPS and 1600 MSPS cases described above, rotating the CLKDIVPH setting by 1 corresponds to a delay shift of 5 ns and 2.5 ns, respectively. By adding an additional step in the SPI initialization routine for the data receiver controller, it becomes possible to increase the effective range of the delay line to ensure a DCI_DEL value that falls within a reasonable guard band.

### 6.3.1.3 LVDS Driver and Receiver Input

The B9739RB features a LVDS-compatible driver and receivers. The LVDS driver output used for the DCO and SYNC_OUT signal includes an equivalent 200 Ω source resistor that limits its nominal output voltage swing to ±200 mV when driving a 100 Ω load. The DCO output driver can be powered down via Register 0x01, Bit 5. An equivalent circuit is shown in Figure 6-11.

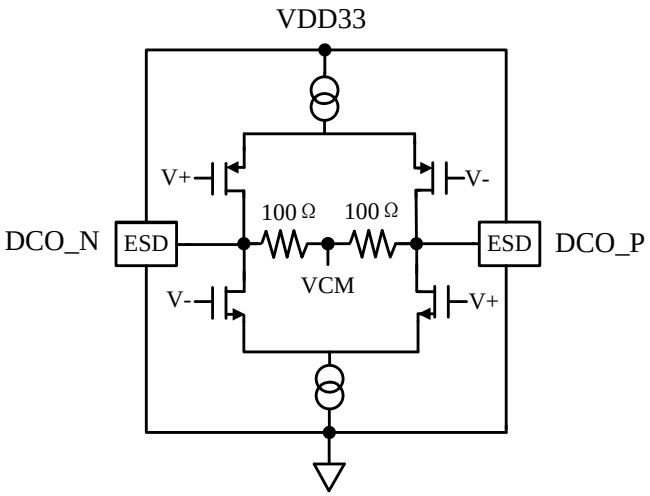



**Figure 6-11 Equivalent LVDS Output**

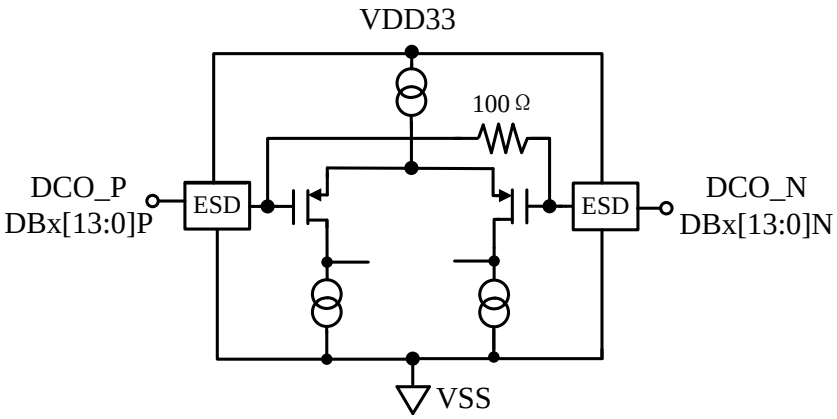



**Figure 6-12 Equivalent LVDS Input**

The LVDS receivers include 100Ω termination resistors, as shown in Figure 6-12. These receivers meet the IEEE-1596.3-1996 reduced swing specification (with the exception of input hysteresis, which cannot be guaranteed over all process corners). Figure 6-13 and Figure 6-14 show an example of nominal LVDS voltage levels seen at the input of the differential receiver with resulting common-mode voltage and equivalent logic level. The LVDS receivers can be powered down via Register 0x01,

Bit 4.

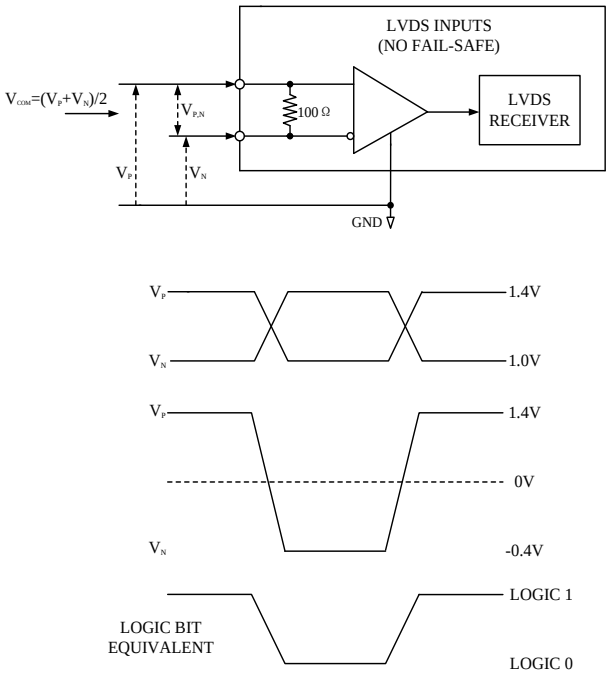



**Figure 6-13 LVDS Data Inputs Levels**

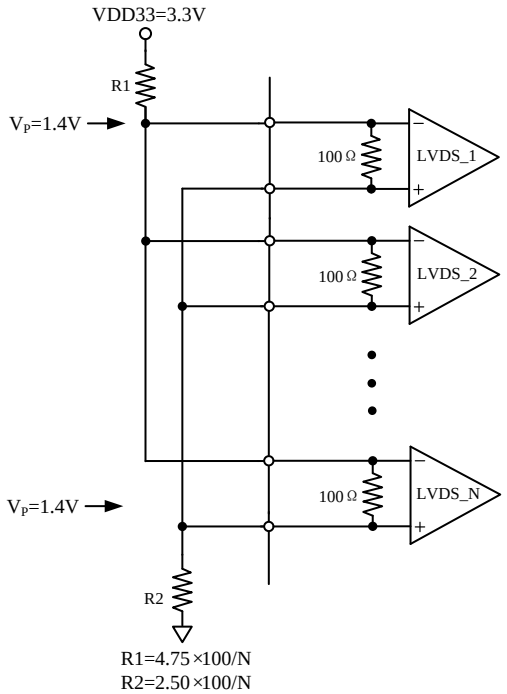



**Figure 6-14 Resistor Network to Bias Unused LVDS Data Inputs**

The B9739RB LVDS inputs do not include fail-safe capability. Any unused data input pins should be biased with an external network or static driver. Figure 6-14 shows an external biasing network that can be used to place unused data bits into a known state. The resistor values for R1 and R2 are selected to establish a $V_P$ and $V_N$

of 1.4 V and 1.0 V, respectively, depending on the number of unused digital inputs, N.

**Table 6-16 LVDS Input Levels**

| Applied Voltages | | Resulting Differential Voltage | Resulting Common-Model Voltage | Logic Bit Binary Equivalent |
|---|---|---|---|---|
| $V_P$(V) | $V_N$(V) | $V_{P,N}$ | $V_{COM}$ | |
| 1.4 | 1 | +0.4V | 1.2V | 1 |
| 1 | 1.4 | -0.4V | 1.2V | 0 |
| 1 | 0.8 | +200mV | 900mV | 1 |
| 0.8 | 1 | -200mV | 900mV | 0 |

## 6.3.2 Mu controller

A delay lock loop (DLL) is used to optimize the timing between the internal digital and analog domains of the B9739RB such that data is successfully transferred into the TxDAC core at rates of up to 2.0 GSPS. As shown in Figure 6-15, the DAC clock is split into an analog and a digital path with the critical analog path leading to the DAC core (for minimum jitter degradation) and the digital path leading to a programmable delay line. Note that the output of this delay line serves as the master internal digital clock from which all other internal and external digital clocks are derived. The amount of delay added to this path is under the control of the mu controller, which optimizes the timing between these two clock domains and continuously tracks any variation (once in track mode) to ensure proper data hand-off.

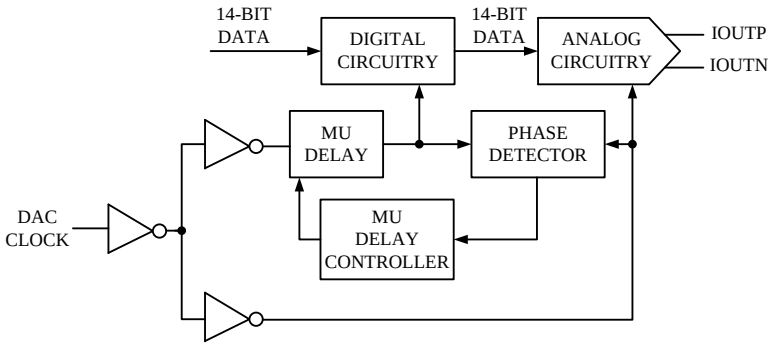



**Figure 6-15 MU Delay Controller Block Diagram**

The mu controller adjusts the timing relationship between the digital and analog domains via a tapped digital delay line having a nominal total delay of 864 ps. The delay value is programmable to a 9-bit resolution (that is, 0 to 432 decimal) via the MUDEL register, resulting in a nominal resolution of 2 ps/LSB. Because a time delay maps to a phase offset for a fixed clock frequency, the control loop essentially compares the phase relationship between the two clock domains and adjusts the phase

(that is, via a tapped delay line) of the digital clock such that it is at the desired fixed phase offset (SET_PHS) from the critical analog clock.

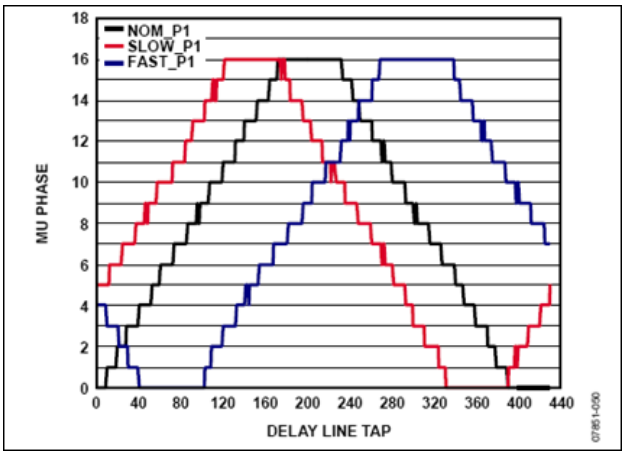



**Figure 6-16 Mu Phase Characteristic of Three Devices from Different Process Lots at 1.2GSPS**

The mu phase characteristics can vary significantly among devices due to gm variations in the digital delay line that are sensitive to process skews (along with temperature and supply). As a result, careful selection of the target phase location is required such that the mu controller can converge upon this phase location for all devices. Figure 6-16 shows that mu phase characteristics of three devices at 25° C from slow, nominal, and fast skew lots at 1.2 GSPS. Note that a －6 mu phase setting does not map to any delay line tap setting for the fast process skew case; therefore, another target mu phase is recommended at this clock rate.

Table 6-17 provides a list of recommended mu phase/slope settings over the specified clock range of the B9739RB based on the considerations previously described. These values should be used to ensure robust operation of the mu controller.

**Table 6-17 Recommended Target Mu Phase Settings vs. Clock Rate**

| Clock Rate （GSPS） | Slope | Mu Phase |
|---|---|---|
| 0.8 | - | 6 |
| 0.9 | - | 4 |
| 1 | + | 5 |
| 1.1 | + | 8 |
| 1.2 | + | 12 |
| 1.3 | - | 12 |
| 1.4 | - | 10 |
| 1.5 | - | 8 |
| 1.6 to 2.0 | - | 6 |

After the mu controller completes its search and establishes lock on the target mu

phase, it attempts to maintain a constant timing relationship between the two clock domains over the specified temperature and supply range. If the mu controller requests a mu delay setting that exceeds the tapped delay line range (that is, <0 or >432), the mu controller can lose lock, causing possible system disruption (that is, can generate IRQ or restart the search). To avoid this scenario, symmetrical guard bands are recommended at each end of the mu delay range. The guard band scaling is such that one LSB of Guard[4:0] (Register 0x29) corresponds to eight LSBs of MUDEL (Register 0x28). The recommended guard band setting of 11 (that is, Register 0x29 = 0xCB) corresponds to 88 LSBs, thus providing sufficient margin.

### 6.3.2.1 MU Controller Initialization Description

The mu controller must be initialized and placed into track mode as a first step in the SPI boot sequence. The following steps are required for initialization of the mu controller. Note that the B9739RB data sheet specifications and characterization data are based on the following mu controller settings:

1. Turn on the phase detector with boost (Register 0x24 = 0x30).
2. Enable the mu delay controller duty-cycle correction circuitry and specify the recommended slope for phase. (that is, Register 0x25 = 0x80 corresponds to a negative slope).
3. Specify search/track mode with a recommended target phase, SET_PHS, of 6 (for example) and an initial MUDEL[8:0] setting of 216 (Register 0x27 = 0x46 and Register 0x28 = 0x6C).
4. Set search tolerance to exact and retry if the search fails its initial attempt. Also, set the guard band to the recommended setting of 11 (Register 0x29 = 0xCB).
5. Set the mu controller tracking gain to the recommended setting and enable the mu controller state machine (Register 0x26 = 0x03).

Upon completion of the last step, the mu controller begins a search algorithm that starts with an initial delay setting specified by the MUDEL register (that is, 216, which corresponds to the midpoint of the delay line). The initial search algorithm works by sweeping through different mu delay values in an alternating manner until the desired phase (that is, a SET_PHS of 4) is exactly measured. When the desired phase is measured, the slope of the phase measurement is then calculated and compared against the specified slope (slope = negative).

If everything matches, the search algorithm is finished. If not, the search continues in both directions until an exact match can be found or a programmable guard band is

reached in one of the directions. When the guard band is reached, the search still continues but only in the opposite direction. If the desired phase is not found before the guard band is reached in the second direction, the search changes back to the alternating mode and continues looking within the guard band. The typical locking time for the mu controller is approximately 180K DAC cycles (at 2 GSPS ~ 75 $\mu$s).

The search fails if the mu delay controller reaches the endpoints. The mu controller can be configured to retry (Register 0x29, Bit 6) the search or stop. For applications that have a microcontroller, the preferred approach is to poll the MU_LKD status bit (Register 0x2A, Bit 0) after the typical locking time has expired. This method allows the system controller to check the status of other system parameters (that is, power supplies and clock source) before reattempting the search (by writing 0x03 to Register 0x26). For applications that do not have polling capabilities, the mu controller state machine should be reconfigured to restart the search in hopes that the system's condition that did not cause locking on the first attempt has disappeared.

Once the mu delay value is found that exactly matches the desired mu phase setting and slope (for example, 6 with a negative. slope), the mu controller goes into track mode. In this mode, the mu controller makes slight adjustments to the delay value to track any variations between the two clock paths due to temperature, time, and supply variations. Two status bits, MU_LKD (Register 0x2A, Bit 0) and MU_LST (Register 0x2A, Bit 1) are available to the user to signal the existing status control loop. If the current phase is more than four steps away from the desired phase, the MU_LKD bit is cleared, and if the lock acquired was previously set, the MU_LST bit is set. Should the phase deviation return to within three steps, the MU_LKD bit is set again while the MU_LST is cleared. Note that this sort of event may occur if the main clock input (that is, DACCLK) is disrupted or the mu controller exceeds the tapped delay line range (that is, <0 or >432).

If lock is lost, the mu controller has the option of remaining in the tracking loop or resetting and starting the search again via the CONTRST bit (Register 0x29, Bit 5). Continued tracking is the preferred state because it is the least disruptive to a system in which the B9739RB temporarily loses lock. The user can poll the mu delay and phase value by first setting the read bit high (Register 0x26, Bit 3). Once the read bit is set, the MUDEL[8:0] bits and the SET_PHS[4:0] bits (Register 0x27 and Register 0x28) that the controller is currently using can be read.

### 6.3.3 Interrupt Requests

The B9739RB can provide the host processor with an interrupt request output signal (IRQ) that indicates that one or more of the B9739RB internal controllers have achieved lock or lost lock. These controllers include the mu, data receiver, and synchronization controllers. The host can then poll the IRQ status register (Register 0x04) to determine which controller has lost lock. The IRQ output signal is an active high output signal available on Pin F13. If used, its output should be connected via a 10 kΩ pull-up resistor to VDD33.

Each IRQ is enabled by setting the enable bits in Register 0x03, which purposely has the same bit mapping as the IRQ status bits in Register 0x04. Note that these IRQ status bits are set only when the controller transitions from a false to true state. Therefore, it is possible for the x_LCK_IRQ and x_LST_IRQ status bits to be set when a controller temporarily loses lock but is able to reestablish lock before the IRQ is serviced by the host. In this case, the host should validate the present status of the suspect controller by reading back its current status bits, which are available in Register 0x21 and/or Register 0x2A. Based on the status of these bits, the host can take appropriate action, if required, to reestablish lock. To clear an IRQ after servicing, it is necessary to reset relevant bits in Register 0x03 by writing 0 followed by another write of 1 to reenable. A detailed diagram of the interrupt circuitry is shown in Figure 6-17.

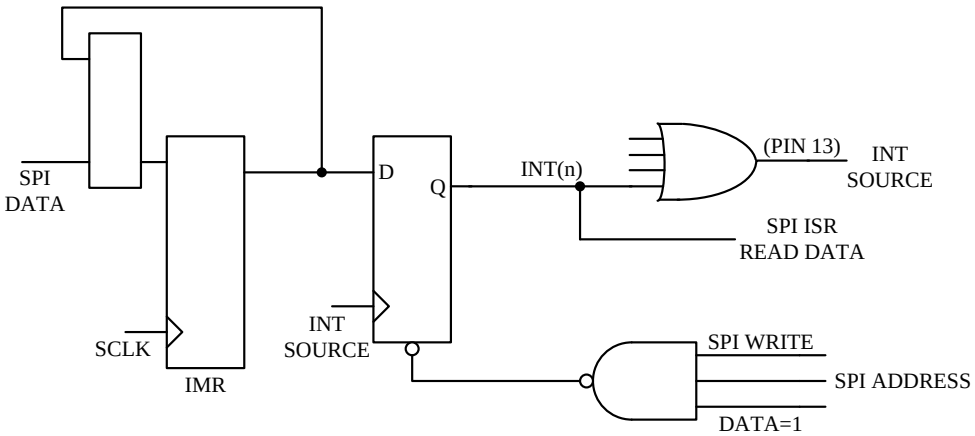



**Figure 6-17 Interrupt Request Circuitry**

It is also possible to use the IRQ during the B9739RB initialization phase after power-up to determine when the mu and data receiver controllers have achieved lock. For example, before enabling the mu controller, the MU_LCK_EN bit (Register 0x03, Bit 2) can be set and the IRQ output signal monitored to determine when lock has been established before continuing in a similar manner with the data receiver

controllers. Note that the relevant LCK bit should be cleared before continuing to the next controller. After all controllers are locked, the lost lock enable bits (that is, x_LST_EN) should be set.

**Table 6-18 Interrupt Request Registers**

| Address(Hex) | Bit | Description |
|---|---|---|
| 0x03 | 3 | MU_LST_EN |
| | 2 | MU_LCK_EN |
| | 1 | RCV_LST_EN |
| | 0 | RCV_LCK_EN |
| 0x04 | 3 | MU_LST_IRQ |
| | 2 | MU_LCK_IRQ |
| | 1 | RCV_LST_IRQ |
| | 0 | RCV_LCK_IRQ |
| 0x21 | 4 | SYNC_LCK |
| | 3 | RCVR_TRK_ON |
| | 1 | RCVR_LST |
| | 0 | RCVR_LCK |
| 0x2A | 1 | MU_LST |
| | 0 | MU_LKD |

## 6.4 Analog Interface Consideration

### 6.4.1 Analog Modes Of Operation

The B9739RB uses the quad-switch architecture shown in Figure 6-18. The quad-switch architecture masks the code-dependent glitches that occur in a conventional two-switch DAC. Figure 6-19 compares the waveforms for a conventional DAC and the quad-switch DAC. In the two-switch architecture, a code-dependent glitch occurs each time the DAC switches to a different state (that is, D1 to D2). This code-dependent glitching causes an increased amount of distortion in the DAC. In a quad-switch architecture (no matter what the codes are), there are always two switches transitioning at each half clock cycle, thus eliminating the code-dependent glitches. However, a constant glitch occurs at 2 × DACCLK because half of the internal switches change state on the rising DACCLK edge, while the other half change state on the falling DACCLK edge.

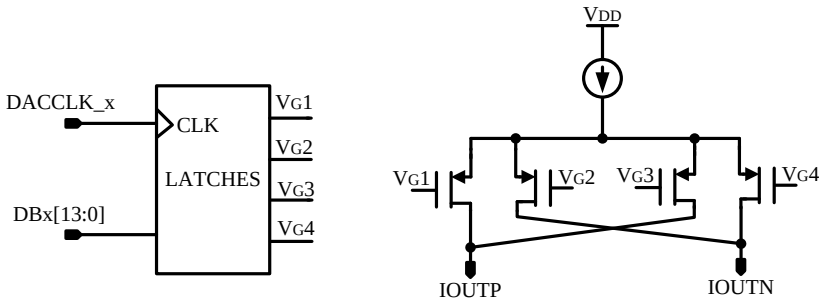



**Figure 6-18 B9739RB Quad-Switch Architecture**

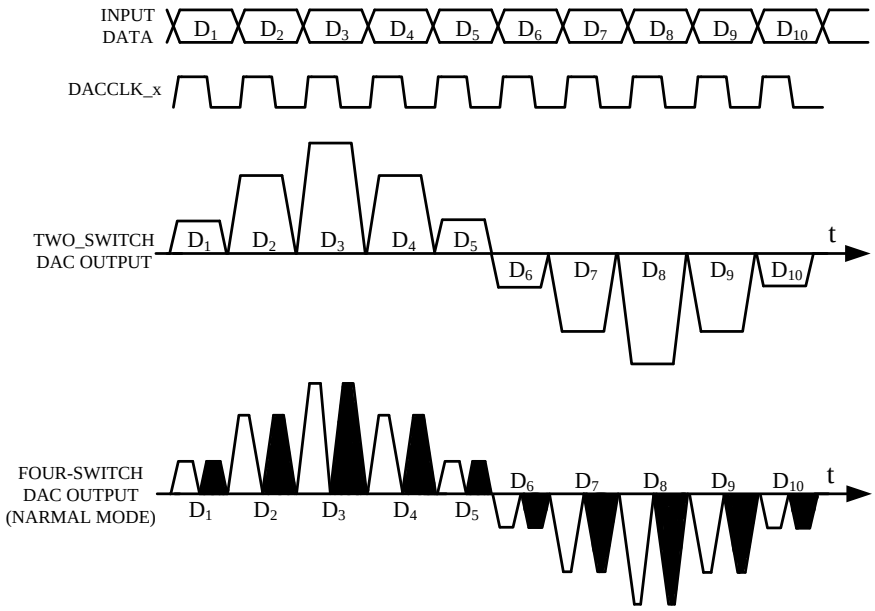



**Figure 6-19 Two-Switch and Quad-Switch DAC Waveforms**

Another attribute of the quad-switch architecture is that it also enables the DAC core to operate in one of the following three modes: normal mode, mix mode, and return-to-zero (RZ) mode. The mode is selected via SPI Register 0x08, Bits[1:0] with normal mode being the default value. In the mix mode, the output is effectively chopped at the DAC sample rate. This has the effect of reducing the power of the fundamental signal while increasing the power of the images centered around the DAC sample rate, thus improving the output power of these images. The RZ mode is similar to the analog mix mode, except that the intermediate data samples are replaced with midscale values.

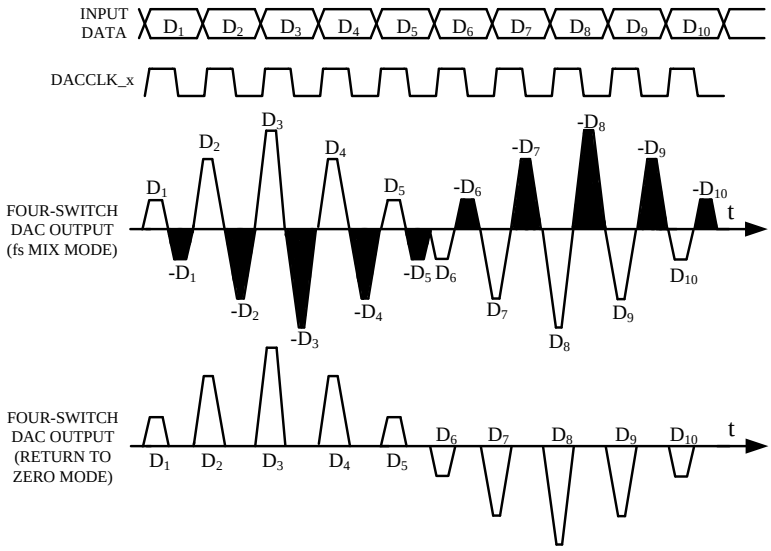



**Figure 6-20 Mix-Mode and RZ DAC Waveforms**

Figure 6-20 shows the DAC waveforms for both the mix mode and the RZ mode. Note that the disadvantage of the RZ mode is the 6 dB loss of power to the load because the DAC is only functioning for ½ the DAC update period. This ability to change modes provides the user the flexibility to place a carrier anywhere in the first three Nyquist zones, depending on the operating mode selected. Switching between the analog modes reshapes the sinc roll-off inherent at the DAC output. The maximum amplitude in all three Nyquist zones is impacted by this sinc roll-off, depending on where the carrier is placed (see Figure 6-21). As a practical matter, the usable bandwidth in the third Nyquist zone becomes limited at higher DAC clock rates (that is, >2 GSPS) when the output bandwidth of DAC core and the interface network (that is, balun) contributes to additional roll-off.

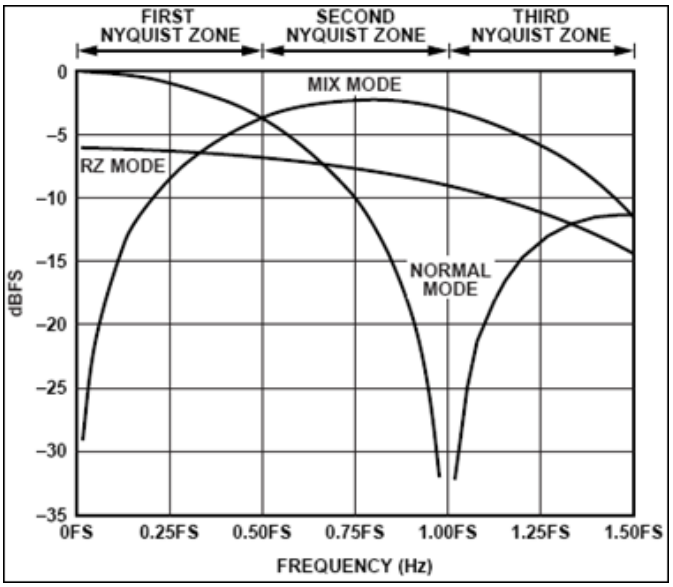



**Figure 6-21 Sinc Roll-Off for Each Analog Operating Mode**

## 6.4.2 Clock Input Considerations

The quality of the clock source and its drive strength are important considerations in maintaining the specified ac performance. The phase noise and spur characteristics of the clock source should be selected to meet the target application requirements. Phase noise and spurs at a given frequency offset on the clock source are directly translated to the output signal. It can be shown that the phase noise characteristics of a reconstructed output sine wave are related to the clock source by 20 × log10 ($f_{OUT}/f_{CLK}$) when the DAC clock path contribution, along with thermal and quantization effects, are negligible.

The B9739RB clock receiver provides optimum jitter performance when driven by a fast slew rate originating from the LVPECL or CML output drivers. For a low jitter sinusoidal clock source, the ADCLK914 can be used to square-up the signal and provide a CML input signal for the B9739RB clock receiver. Note that all specifications and characterization presented in the data sheet are with the ADCLK914 driven by a high quality RF signal generator with the clock receiver biased at a 800 mV level. A dc blocking capacitor is used between the clock driver output and clock receiver input to allow for different dc bias levels. To minimize signal loss for high clock rates, a high quality, dc blocking RF capacitor is recommended.

Figure 6-24 shows a clock source based on the ADF4350 low phase noise/jitter PLL. The ADF4350 can provide output frequencies from 140 MHz up to 4.4 GHz with jitter as low as 0.5 ps rms.

Each single-ended output can provide a squared-up output level that can be varied from －4 dBm to +5 dBm allowing for >2 V p-p output differential swings. The ADF4350 also includes an additional CML buffer that can be used to drive another AD9739 device.

The B9739RB clock receiver features the ability to independently adjust the common-mode level of its inputs over a span of ±100 mV centered about its midsupply point (that is, VDDC/2) as well as an offset for hysteresis purposes. Figure 6-22 shows the equivalent input circuit of one of the inputs. ESD diodes are not shown for clarity purposes. It has been found through characterization that the optimum setting is for both inputs to be biased at approximately 0.8 V. This can be achieved by writing a 0x0F (corresponding to a －15) setting to both cross controller registers (that is, Register 0x22 and Register 0x23).

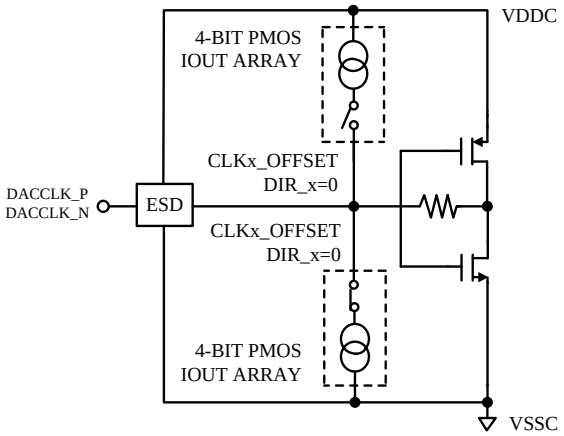



**Figure 6-22 Clock Input and Common-Mode Control**

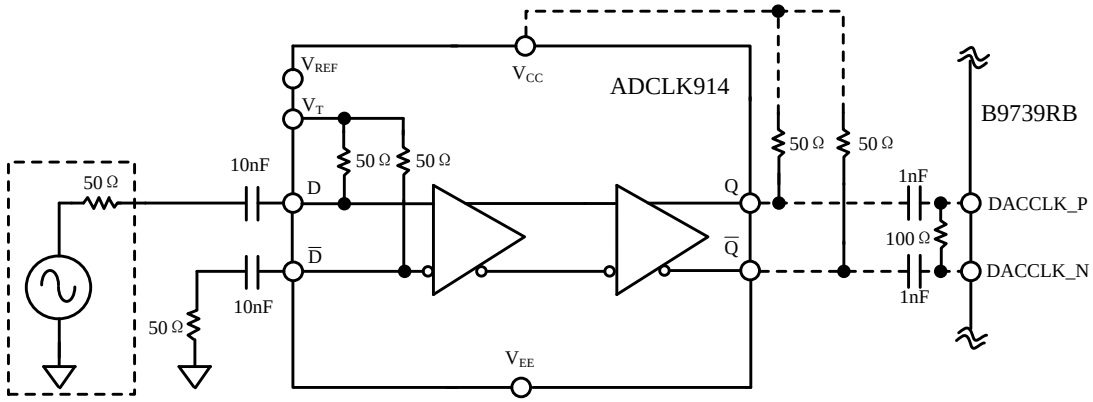



**Figure 6-23 ADCLK914 Interface to the B9739RB CLK Input**

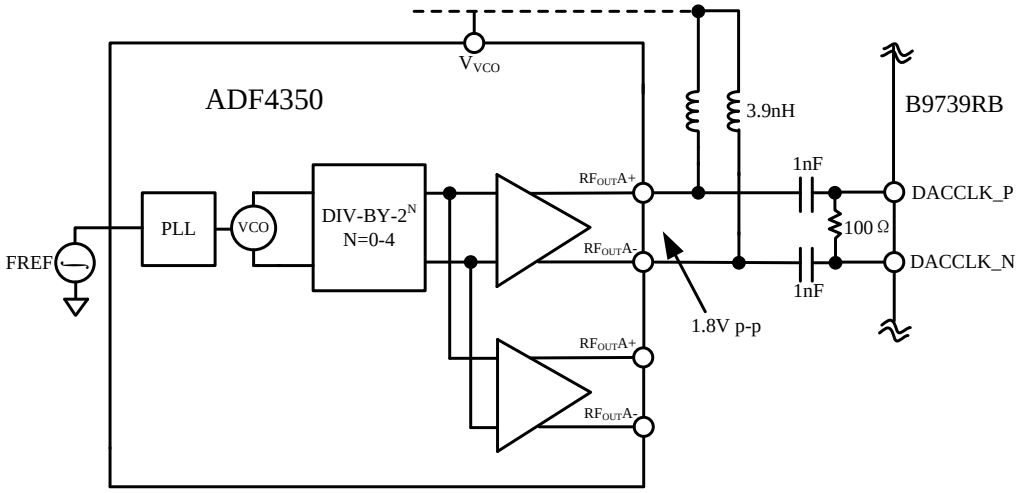



**Figure 6-24 ADF4350 Interface to the B9739RB CLK Input**

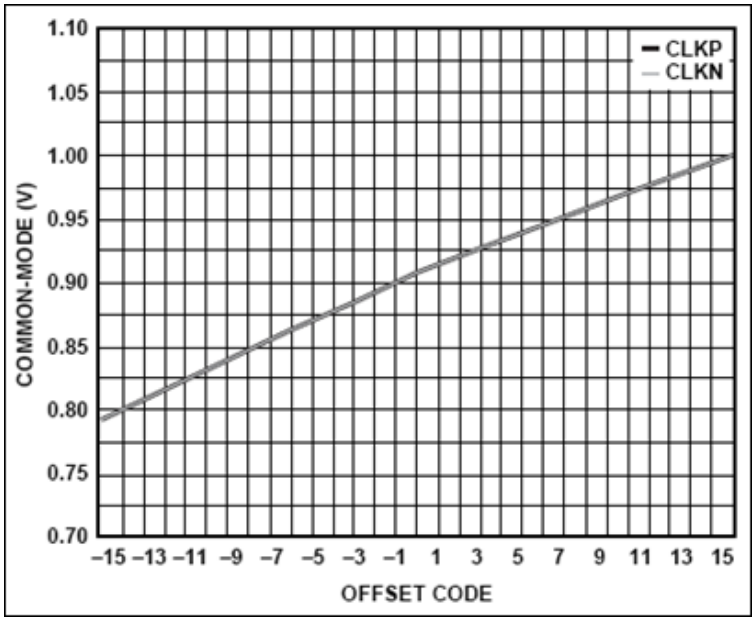



**Figure 6-25 Common-Mode Voltage with Respect to CLKP_OFFSET/CLKN_OFFSET and DIR_P/DIR_N**

## 6.4.3 Voltage Reference

The B9739RB output current is set by a combination of digital control bits and the I120 reference current, as shown in Figure 6-26.

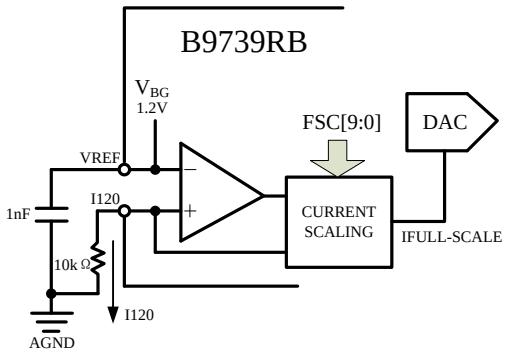



**Figure 6-26 Voltage Reference Circuit**

The reference current is obtained by forcing the band gap voltage across an external 10 kΩ resistor from I120 (Pin B14) to ground. The 1.25 V nominal band gap voltage (VREF) generates a 120 μA reference current in the 10 kΩ resistor. Note the following constraints when configuring the voltage reference circuit:

- Both the 10 kΩ resistor and 1 nF bypass capacitor are required for proper operation.
- Adjusting the output full-scale current, IOUTFS, of the DAC from its default setting of 20 mA should be performed digitally.
- The B9739RB is not a multiplying DAC. Modulating the reference current, I120, with an ac signal is not supported.

- The band gap voltage appearing at VREF (Pin C14) must be buffered for use with external circuitry because its output impedance is approximately 5 kΩ.
- An external reference can be used to overdrive the internal reference by connecting it to VREF (Pin C14).

In theory, $I_{OUTFS}$ can be adjusted digitally over 8.7 mA to 31.7 mA by using FSC[9:0] (Register 0x06 and Register 0x07).

The following equation relates IOUTFS to the FSC[9:0] register, which can be set from 0 to 1023:

$$IOUTFS = 22.6 \times FSC[9:0] / 1000 + 8.7$$

Note that a default value of 0x200 generates 20 mA full scale, which is used for most of the characterization presented in this data sheet (unless noted otherwise).

## 6.4.4 Analog Outputs

### 6.4.4.1 Equivalent DAC Output and Transfer Function

The B9739RB provides complementary current outputs, IOUTP and IOUTN, that source current into an external ground reference load. Figure 6-27 shows an equivalent output circuit for the DAC. Note that, compared to most current output DACs of this type, the B9739RB outputs exhibit a slight offset current (that is, $I_{OUTFS}/16$), and the peak differential ac current is slightly below $I_{OUTFS}/2$ (that is, $15/32 \times I_{OUTFS}$).

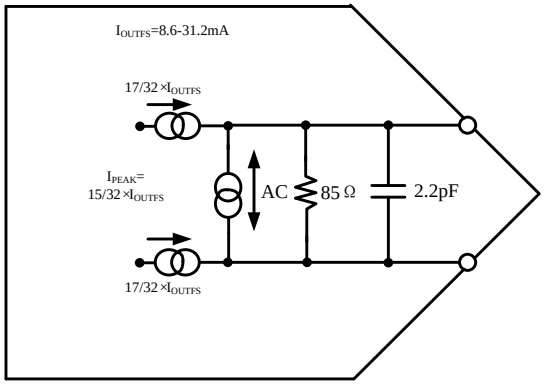



**Figure 6-27 Equivalent DAC Output Circuit**

As shown in Figure 6-27, the DAC output can be modeled as a pair of dc current sources that source a current of $17/32 \times I_{OUTFS}$ to each output. A differential ac current source, $I_{PEAK}$, is used to model the signal-dependent nature of the DAC output. The polarity and signal dependency of this ac current source are related to the digital code by the following equations:

$$F(Code) = (DACCODE - 8192)/8192$$

$-1 \le F(Code) < 1$

Where DACCODE = 0 to 16383(decimal).

Because $I_{PEAK}$ can swing $\pm(15/32) \times I_{OUTFS}$, the output currents measured at IOUTP and IOUTN can span from IOUTFS/16 to $I_{OUTFS}$. However, because the ac signal-dependent current component is complementary, the sum of the two outputs is always constant (that is, IOUTP + IOUTN = $(34/32) \times I_{OUTFS}$).

The code-dependent current measured at the IOUTP (and IOUTN) output is as follows:

$$IOUTP = 17/32 \times IOUTFS + 15/32 \times IOUTFS \times F(Code)$$

$$IOUTN = 17/32 \times IOUTFS - 15/32 \times IOUTFS \times F(Code)$$

Figure 6-28 shows the IOUTP vs. DACCODE transfer function when IOUTFS is set to 19.65 mA.

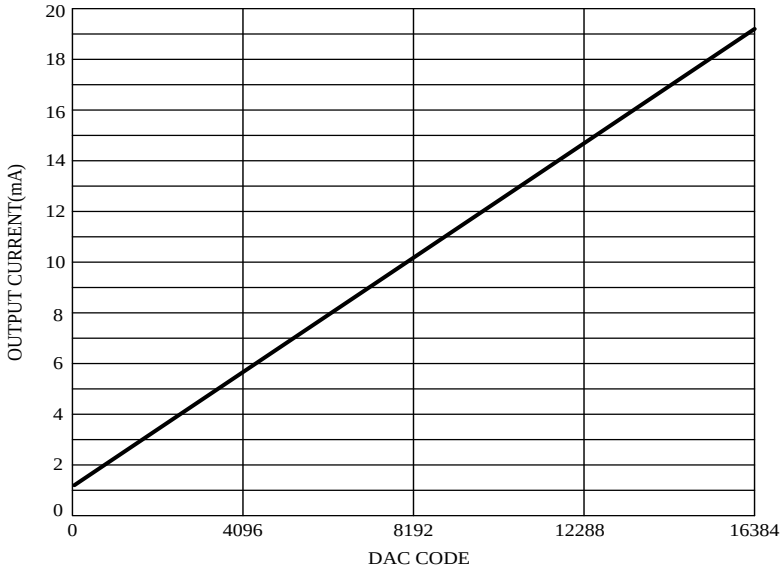



**Figure 6-28 Gain Curve for FSC[9:0] = 512, DAC Offset = 1.228 mA**

## 6.4.4.2 Peak DAC Output Power Capability

The maximum peak power capability of a differential current output DAC is dependent on its peak differential ac current, IPEAK, and the equivalent load resistance it sees. Because the B9739RB includes a differential 85 Ω resistance, it is best to use a doubly terminated external output network similar to what is shown in Figure 6-29. In this case, the equivalent load seen by the ac current source of the DAC is 25 Ω.

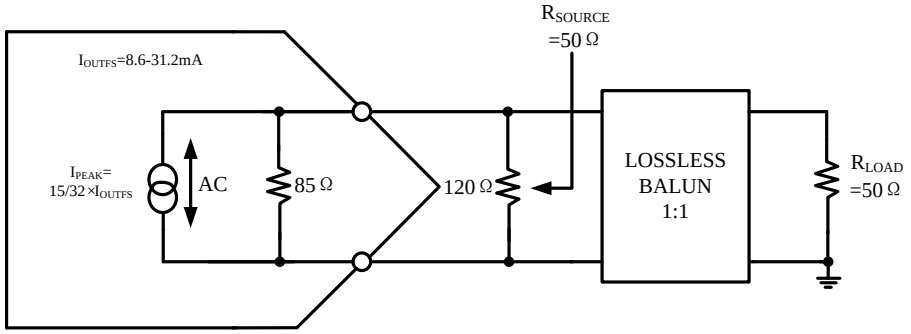



**Figure6- 29 Equivalent Circuit for Determining Maximum Peak Power to a 50 Ω Load**

If the B9739RB is programmed for IOUTFS = 20 mA, its peak ac current is 9.375 mA and its peak power delivered to the equivalent load is 2.2 mW (that is, $P = I^2R$). Because the source and load resistance seen by the 1:1 balun are equal, this power is shared equally; therefore, the output load receives 1.1 mW or 0.4 dBm.

To calculate the rms power delivered to the load, the following must be considered:

- Peak-to-rms of the digital waveform
- Any digital backoff from digital full scale
- The DAC's sinc response and nonideal losses in external network

For example, a reconstructed sine wave with no digital backoff ideally measures －2.6 dBm because it has a peak-to-rms ratio of 3 dB. If a typical balun loss of 0.4 dBm is included, －3 dBm of actual power can be expected in the region where the sinc response of the DAC has negligible influence. Increasing the output power is best accomplished by increasing IOUTFS, although any degradation in linearity performance must be considered acceptable for the target application.

### 6.4.4.3 Output Stage Configuration

The B9739RB is intended to serve high dynamic range applications that require wide signal reconstruction bandwidth (that is, DOCSIS CMTS) and/or high IF/RF signal generation. Optimum ac performance can only be realized if the DAC output is configured for differential (that is, balanced) operation with its output common-mode voltage biased to analog ground. The output network used to interface to the DAC should provide a near 0 Ω dc bias path to analog ground. Any imbalance in the output impedance between the IOUTP and IOUTN pins results in asymmetrical signal swings that degrade the distortion performance (mostly even order) and noise performance. Component selection and layout are critical in realizing the performance potential of the B9739RB.

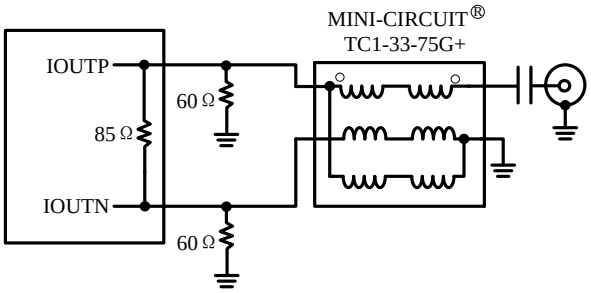



**Figure 6-30 Recommended Balun for Wideband Applications with Upper Bandwidths of up to 2.2GHz**

Most applications requiring balanced-to-unbalanced conversion can take advantage of the Ruthroff 1:1 balun configuration shown in Figure 6-30. This configuration provides excellent amplitude/phase balance over a wide frequency range while providing a 0 Ω dc bias path to each DAC output. Also, its design provides exceptional bandwidth and can be considered for applications requiring signal reconstruction of up to 2.2 GHz. The characterization plots shown in this data sheet are based on the AD9739 evaluation board, which uses this configuration. Figure 67 compares the measured frequency response for normal and mix mode using the B9739RB evaluation board vs. the ideal frequency response.

Figure 6-31 shows an interface that can be considered when interfacing the DAC output to a self-biased differential gain block. The inductors shown serve as RF chokes (L) that provide the dc bias path to analog ground. The value of the inductor, along with the dc blocking capacitors (C), determines the lower cutoff frequency of the composite pass-band response. An RF balun should also be considered before the RF differential gain stage and any filtering to ensure symmetrical common-mode impedance seen by the DAC output while suppressing any common-mode noise, harmonics, and clock spurs prior to amplification.

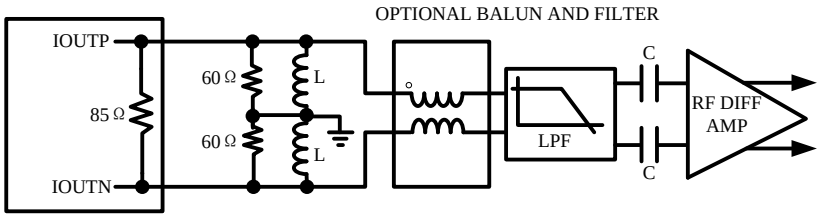



**Figure 6-31 Interfacing the DAC Output to the Self-Biased Differential Gain Stage**

For applications operating the B9739RB in mix mode with output frequencies extending beyond 2.2 GHz, the circuits shown in Figure 6-32 should be considered. The circuit in Figure 6-32 uses a wideband balun with a configuration similar to the one shown in Figure 6-31 to provide a dc bias path for the DAC outputs. The circuit

in Figure 6-33 takes advantage of ceramic chip baluns to provide a dc bias path for the DAC outputs while providing excellent amplitude/phase balance over a narrower RF band. These low cost, low insertion loss baluns are available for different popular RF bands and provide excellent amplitude/ phase balance over their specified frequency range.

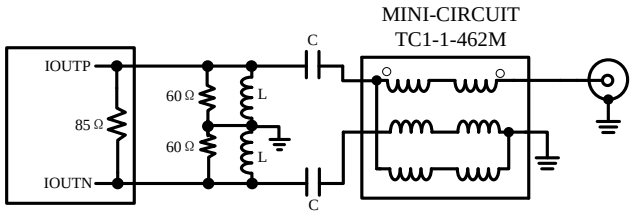



**Figure 6-32 Recommended Mix Mode Configuration Offering Extended RF Bandwidth Using a TC1-1-43A+ Balun**

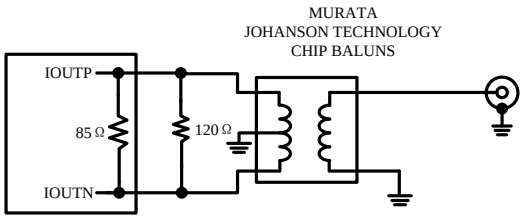



**Figure 6-33 Lowest Cost and Size Configuration for Narrow RF Band Operation**

## 6.4.5 Lab Evaluation of The B9739RB

Figure 6-34 shows a recommended lab setup that was used to characterize the performance of the B9739RB. The DPG2 is a dual port LVDS/CMOS data pattern generator available from Analog Devices, Inc., with an up to 1 GSPS data rate. The DPG2 directly interfaces to the B9739RB evaluation board via Tyco Z-PACK HM-Zd connectors. A low phase noise/jitter RF source, such as an R&S SMA100A signal generator, is used for the DAC clock. A 5 V power supply is used to power up the B9739RB evaluation board, and SMA cabling is used to interface to the supply, clock source, and spectrum analyzer. A USB 2.0 interface to a host PC is used to communicate to both the B9739RB evaluation board and the DPG2.

A high dynamic range spectrum analyzer is required to evaluate the B9739RB reconstructed waveform's ac performance. This is especially the case when measuring ACLR performance for high dynamic range applications, such as multicarrier DOCSIS CMTS applications. Harmonic, SFDR, and IMD measurements pertaining to unmodulated carriers can benefit by using a sufficiently high RF attenuation setting because these artifacts are easy to identify above the spectrum analyzer noise floor. However, reconstructed waveforms having modulated carrier(s) often benefit from the

use of a high dynamic range RF amplifier and/or passive filters to measure close-in and wideband ACLR performance when using spectrum analyzers of limited dynamic range.

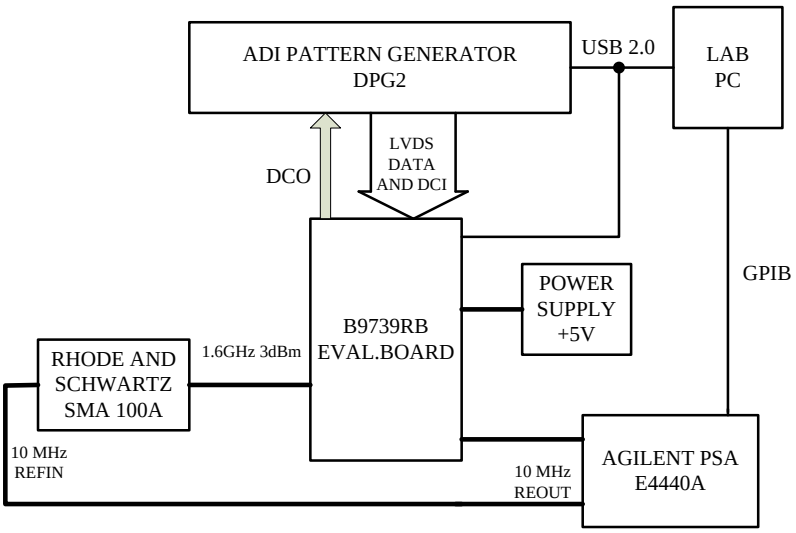



**Figure 6-34 Lab Test Setup Used to Characterize the B9739RB**

## 6.4.6 Power Dissipation And Supply Domains

The power dissipation of the B9739RB is dependent on the DAC clock rate. The current consumption from the 3.3 V supply remains relatively constant because it is used for biasing the DAC core (that is, VDDA) and differential input receivers (that is, VDD33). However, the current consumption from the 1.8 V supply is clock rate dependent and increases linearly with frequency because this supply is used by the digital path (that is, VDD) as well as the clock distribution circuitry (that is, VDDC).

Treat the VDDC supply as an analog supply because the clock distribution circuitry has poor power supply rejection; therefore, noise on this supply can induce clock jitter. To ensure low noise on this sensitive supply, use a separate 1.8 V regulator powered from the 3.3 V analog supply rail that is also used to power VDDA. This supply rail can also be used to power-up VDD33 via an LC filter network. The digital 1.8 V supply, VDD, can be supplied via a well-filtered switching regulator.

## 6.4.7 Recommended Start-Ip Sequence

Upon power-up of the B9739RB, a host processor is required to initialize and configure the B9739RB via its SPI port. Figure 6-35 shows a flowchart of the sequential steps required, while Table 6-19 provides more detail on the SPI register write/read operations required to implement the flowchart steps. Note the following:

- A software reset is optional because the B9739RB has both an internal POR circuit and a RESET pin.

- The mu controller must be first enabled (and in track mode) before the data receiver controller is enabled because the DCO output signal is derived from this circuitry.
- A wait period is related to $f_{DATA}$ periods.
- Limit the number of attempts to lock the controllers to three; locks typically occur on the first attempt.
- Hardware or software interrupts can be used to monitor the status of the controllers.

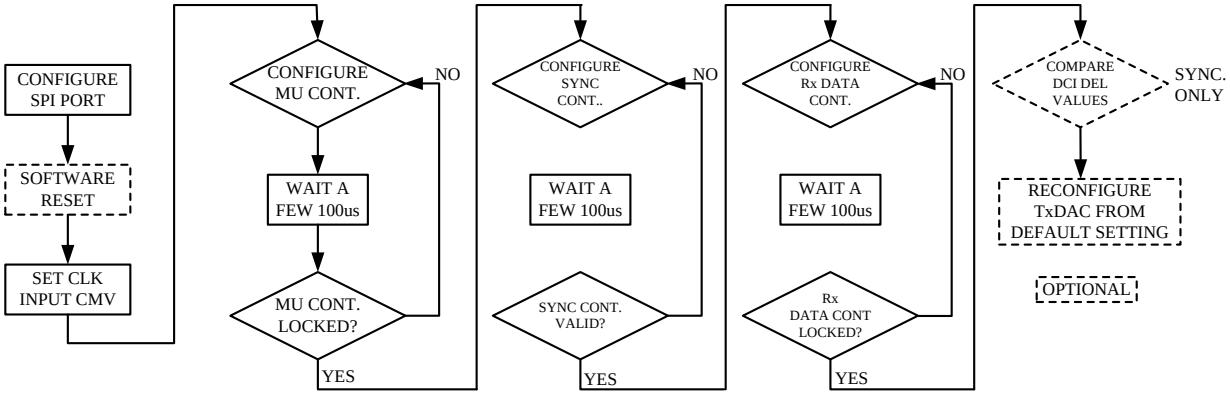



**Figure 6-35 Flowchart for Initialization and Configuration of the B9739RB**

**Table 6-19. Recommended SPI Initialization**

| Step | Address（Hex） | Write Value | Comments |
|---|---|---|---|
| 1 | 0x00 | 0x00 | Configure for the 4-wire SPI mode with MSB. Note that Bits[7:5] must be mirrored onto Bits[2:0] because the MSB/LSB format can be unknown at power-up. |
| 2 | 0x00 | 0x20 | Software reset to default SPI values. |
| 3 | 0x00 | 0x00 | Clear the reset bit. |
| 4 | 0x22 | 0x0F | Set the common-mode voltage of DACCLK_P and DACCLK_N inputs. |
| 5 | 0x23 | 0x0F | |
| 6 | 0x24 | 0x30 | Configure the mu controller. Refer to Table 6-17 for recommended target mu slope and phase settings vs. clock rate. |
| 7 | 0x25 | 0x80 | |
| 8 | 0x27 | 0x44 | |
| 9 | 0x28 | 0x6C | |
| 10 | 0x29 | 0xCB | |
| 11 | 0x26 | 0x02 | |
| 12 | 0x26 | 0x03 | Enable the mu controller search and track mode. |
| 13 | Not applicable | Not applicable | Wait for 160 K $\times 1/f_{DATA}$ cycles. |
| 14 | 0x2A | | Read back Register 0x2A and confirm that it is equal to 0x01 to ensure that the DLL loop is locked. If it is not locked, proceed to Step 10 and |

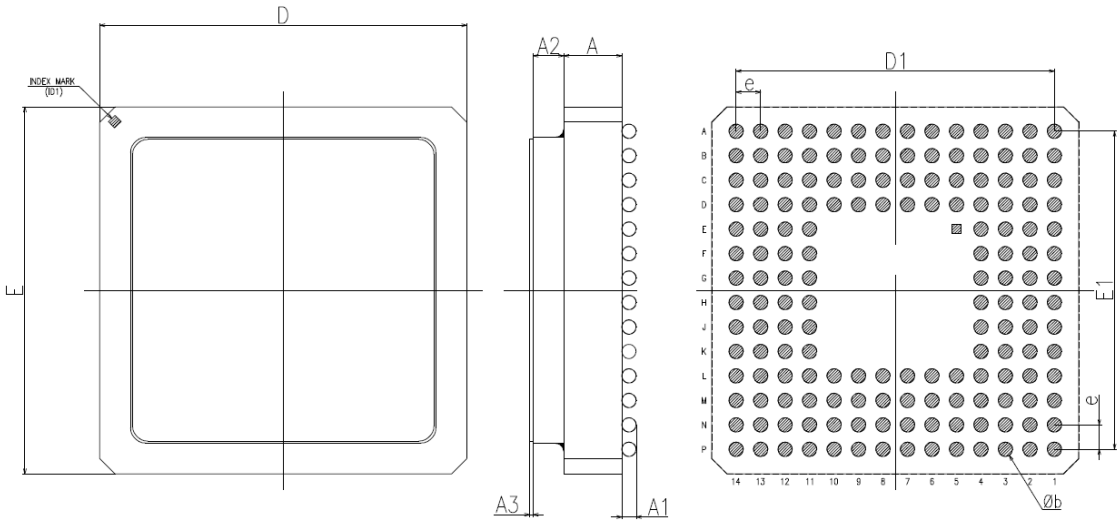
| | | | |
|---|---|---|---|
| | | | repeat. Limit attempts to three before breaking out of the loop and reporting a mu lock failure. |
| 15 | Not applicable | Not applicable | Ensure that the B9739RB is fed with DCI clock input from the data source. |
| 16 | 0x13 | 0x72 | Set FINE_DEL_SKEW to 2. |
| 17 | 0x10 | 0x00 | Disable the data Rx controller before enabling it. |
| 18 | 0x10 | 0x02 | Enable the data Rx controller for loop and IRQ. |
| 19 | 0x10 | 0x03 | Enable the data Rx controller for search and track mode. |
| 20 | Not applicable | Not applicable | Wait for 135 K $\times 1/f_{DATA}$ cycles. |
| 21 | 0x21 | | Read back Register 0x21 and confirm that it is equal to 0x09 to ensure that the DLL loop is locked and tracking. If it is not locked and tracking, advance the CLKDIVPH[1:0] phase in Register 0x14, Bit[7:6] before proceeding to Step 17 to repeat attempt. Limit attempts to three before breaking out of the loop and reporting an Rx data lock failure. |
| 22 | 0x06，0x07 | 0x00，0x02 | Optional: modify the TxDAC IOUTFS setting (the default is 20 mA). |
| 23 | 0x08 | 0x00 | Optional: modify the TxDAC operation mode (the default is normal mode). |

# 7. Applications Field

- Broadband communications systems
- Military jammers
- Instrumentation, automatic test equipment
- Radar, avionics
- Note that in the radiation condition, SPI ports are forbidden to use

# 8. Package Outline Dimensions

B9739RB's package style is CBGA160, its physical size is shown in figure 8-1.




| Symbol | Value(mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| *A* | 1.71 | 1.9 | 1.99 |
| *A1* | 0.45 | — | 0.75 |
| *A2* | — | 1.00 | — |
| *A3* | 0.085 | 0.11 | 0.135 |
| *D* | 11.85 | 12.00 | 12.15 |
| *E* | 11.85 | 12.00 | 12.15 |
| *D1* | — | 10.40 | — |
| *E1* | — | 10.40 | — |
| *e* | — | 0.80 | — |
| *ϕb* | 0.45 | — | 0.55 |

**Figure 8-1. Physical size**

# Appendix Ⅰ Pin Definition

| Pin No. | Mnemonic | Description |
|---|---|---|
| C1,C2,D1,D2,E1,E2,E3,E4 | VDDC | 1.8 V Clock Supply Input. |
| A1,A2,A3,A4,A5,B1,B2,B3,B4,B5, C4,C5,D4,D5 | VSSC | Clock Supply Return. |
| A10,A11,B10,B11,C10,C11,D10,D11 | VDDA | 3.3 V Analog Supply Input. |
| A12,A13,B12,B13,C12,C13,D12,D13 | VSSA | Analog Supply Return. |
| A6,A9,B6,B9,C6,C9,D6,D9,F1,F2,F3, F4,E11,E12,E13,E14,F11,F12 | VSSA Shield | Analog Supply Return Shield. Tie to VSSA at the DAC. |
| A14 | NC | No Connect. Do not connect to this pin. |
| A7,B7,C7,D7 | IOUTN | DAC Negative Current Output Source. |
| A8,B8,C8,D8 | IOUTP | DAC Positive Current Output Source. |
| B14 | I120 | Nominal 1.2 V Reference. Tie to analog ground via a 10 kΩ resistor to generate a 120 μA reference current. |
| C14 | VREF | Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor. |
| D14 | NC | Factory Test Pin. Do not connect to this pin. |
| C3,D3 | DACCLK_N/DACCLK_P | Negative/Positive DAC Clock Input (DACCLK). |
| F13 | IRQ | Interrupt Request Open Drain Output. Active high. Pull up to VDD33 with a 10 kΩ resistor. |
| F14 | RRESET | Reset Input. Active high. Tie to VSS if unused. |
| G13 | $\overline{CS}$ | Serial Port Enable Input. |
| G14 | SDIO | Serial Port Data Input/Output. |
| H13 | SCLK | Serial Port Clock Input. |
| H14 | SDO | Serial Port Data Output. |
| J3,J4,J11,J12 | VDD33 | 3.3 V Digital Supply Input. |
| G1,G2,G3,G4,G11.G12 | VDD | 1.8 V Digital Supply. Input. |
| H1,H2,H3,H4,H11,H12,K3,K4,K11,K12 | VSS | Digital Supply Return. |
| J1,J2 | SYNC_OUT_P/SYNC_OUT_N | Positive/Negative SYNC Output (SYNC_OUT) |
| K1，K2 | SYNC_IN_P/SYNC_IN_N | Positive/Negative SYNC Input (SYNC_IN) |
| J13,J14 | DCO_P/DCO_N | Positive/Negative Data Clock Output (DCO). |
| K13,K14 | DCI_P/DCI_N | Positive/Negative Data Clock Input (DCI). |
| L1,M1 | DB1[0]P/ DB1[0]N | Port 1 Positive/Negative Data Input Bit 0. |
| L2,M2 | DB1[1]P/ DB1[1]N | Port 1 Positive/Negative Data Input Bit 1. |
| L3,M3 | DB1[2]P/ DB1[2]N | Port 1 Positive/Negative Data Input Bit 2. |
| L4,M4 | DB1[3]P/ DB1[3]N | Port 1 Positive/Negative Data Input Bit 3. |
| L5,M5 | DB1[4]P/ DB1[4]N | Port 1 Positive/Negative Data Input Bit 4. |
| L6,M6 | DB1[5]P/ DB1[5]N | Port 1 Positive/Negative Data Input Bit 5. |
| L7,M7 | DB1[6]P/ DB1[6]N | Port 1 Positive/Negative Data Input Bit 6. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| L8,M8 | DB1[7]P/ DB1[7]N | Port 1 Positive/Negative Data Input Bit 7. |
| L9,M9 | DB1[8]P/ DB1[8]N | Port 1 Positive/Negative Data Input Bit 8. |
| L10,M10 | DB1[9]P/ DB1[9]N | Port 1 Positive/Negative Data Input Bit 9. |
| L11,M11 | DB1[10]P/ DB1[10]N | Port 1 Positive/Negative Data Input Bit 10. |
| L12,M12 | DB1[11]P/ DB1[11]N | Port 1 Positive/Negative Data Input Bit 11. |
| L13,M13 | DB1[12]P/ DB1[12]N | Port 1 Positive/Negative Data Input Bit 12. |
| L14,M14 | DB1[13]P/ DB1[13]N | Port 1 Positive/Negative Data Input Bit 13. |
| N1,P1 | DB0[0]P/ DB0[0]N | Port 0 Positive/Negative Data Input Bit 0. |
| N2,P2 | DB0[1]P/ DB0[1]N | Port 0 Positive/Negative Data Input Bit 1. |
| N3,P3 | DB0[2]P/ DB0[2]N | Port 0 Positive/Negative Data Input Bit 2. |
| N4,P4 | DB0[3]P/ DB0[3]N | Port 0 Positive/Negative Data Input Bit 3. |
| N5,P5 | DB0[4]P/ DB0[4]N | Port 0 Positive/Negative Data Input Bit 4. |
| N6,P6 | DB0[5]P/ DB0[5]N | Port 0 Positive/Negative Data Input Bit 5. |
| N7,P7 | DB0[6]P/ DB0[6]N | Port 0 Positive/Negative Data Input Bit 6. |
| N8,P8 | DB0[7]P/ DB0[7]N | Port 0 Positive/Negative Data Input Bit 7. |
| N9,P9 | DB0[8]P/ DB0[8]N | Port 0 Positive/Negative Data Input Bit 8. |
| N10,P10 | DB0[9]P/ DB0[9]N | Port 0 Positive/Negative Data Input Bit 9. |
| N11,P11 | DB0[10]P/ DB0[10]N | Port 0 Positive/Negative Data Input Bit 10. |
| N12,P12 | DB0[11]P/ DB0[11]N | Port 0 Positive/Negative Data Input Bit 11. |
| N13,P13 | DB0[12]P/ DB0[12]N | Port 0 Positive/Negative Data Input Bit 12. |
| N14,P14 | DB0[13]P/ DB0[13]N | Port 0 Positive/Negative Data Input Bit 13. |

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