Dual high slew rate operational amplifier

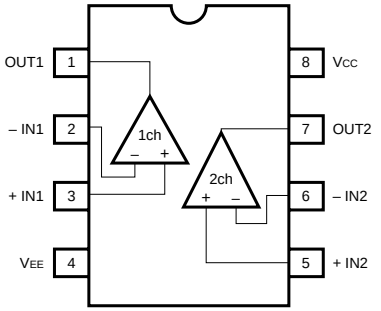
BA4510F / BA4510FV

The BA4510F and BA4510FV are monolithic ICs that contain two operational amplifiers with high slew rate, featuring phase compensation. These ICs can be driven with a low-voltage power supply, requiring a power supply range of ± 1 to ± 3.5V for a dual power supply and 2 to 7V for a single power supply. In addition, an unbuffered type is used which enables ample output even in low voltage ranges, enabling swing at up to nearly the power supply voltage.

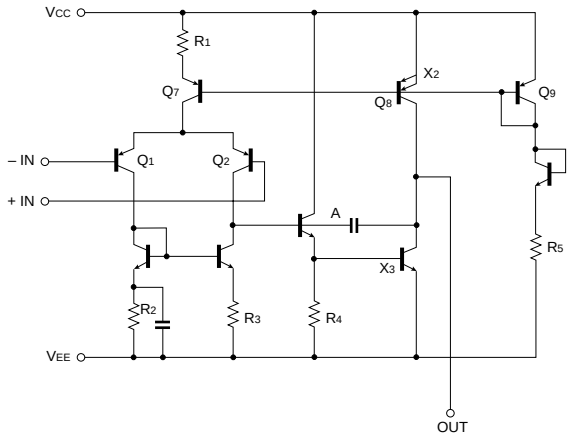
●Features

1) Low-voltage operation.
2) High slew rate.
3) Wide dynamic output range.
4) Compact 8-pin SSOP-B package. (BA4510FV)

●Block diagram



●Internal circuit configuration



●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{CC}	± 5	V
Power dissipation	BA4510F	Pd	550*1 (SOP)	mW
	BA4510FV		350*2 (SSOP)	
Differential input voltage		V_{ID}	± V_{CC}	V
Common-mode input voltage		V_I	0 ~ V_{CC}	V
Operating temperature		Topr	– 20 ~ + 75	°C
Storage temperature		Tstg	– 40 ~ + 125	°C

*1 If used at temperatures higher than 25°C, reduce power by 5.5mW for each 1°C above Ta = 25°C.
This value is the value measured when mounted on a glass epoxy board (50mm × 50mm × 1.6mm).

*2 If used at temperatures higher than 25°C, reduce power by 3.5mW for each 1°C above Ta = 25°C.
This value is the value measured when mounted on a glass epoxy board (70mm × 70mm × 1.6mm).
The value is 300mW when the IC is used alone.

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{CC} = ±2.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Input offset voltage		V_{IO}	—	1	6	mV	R_S = 50Ω
Input offset current		I_{IO}	—	2	200	nA	
Input bias current		I_B	—	80	500	nA	∗1
High-amplitude voltage gain		A_V	60	90	—	dB	R_L≧2kΩ, V_{CC} = 15V
Common-mode input voltage		V_{ICM}	– 1.3	—	1.5	V	
Common-mode rejection ratio		CMRR	60	80	—	dB	
Power supply voltage rejection ratio		PSRR	60	80	—	dB	R_S = 50Ω
Quiescent current		I_Q	2.5	5.0	7.5	mA	R_L = ∞ALL AMPS
Output voltage	High	V_{OH}	2.0	2.4	—	V	R_L = 2kΩ
	Low	V_{OL}	—	– 2.4	– 2.0	V	R_L = 2kΩ
Slew rate		S.R.	—	5	—	V / μs	

∗1 Because the first stage is configured with a PNP transistor, input bias current is from the IC.

●Electrical characteristic curve

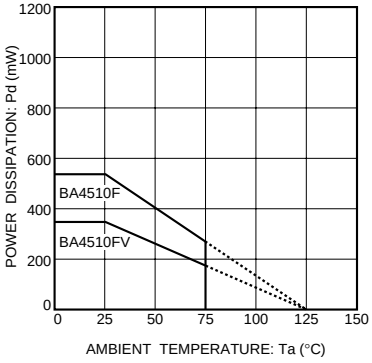


Fig. 1 Power dissipation vs. ambient temperature

●Operation notes

(1) Unused circuit connections

If there are any circuits which are not being used, we recommend making connections as shown in Figure 2, with the non-inverted input pin connected to the potential within the in-phase input voltage range (V_{ICM}).

(2) If used with a voltage follower, be careful of oscillation which may cause problems with the in-line input voltage range or the capacitance load.

(3) If using at power supply voltage + 5.0 or higher, be sure the gain is reduced sufficiently to prevent oscillation.

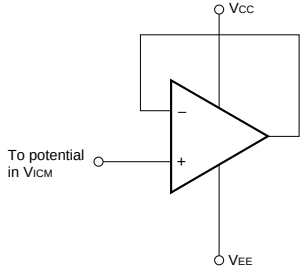
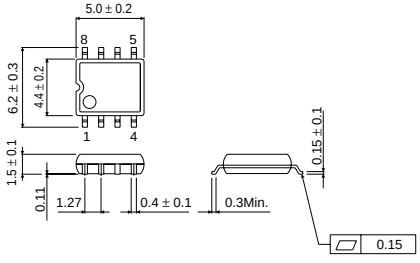


Fig. 2 Unused circuit connections

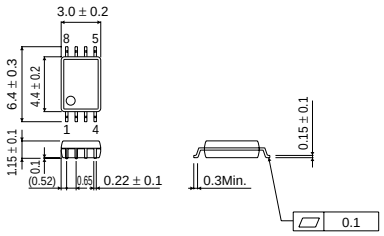
●External dimensions (Units: mm)

BA4510F



SOP8

BA4510FV



SSOP-B8