Enhanced Smoke Detector Flash MCU with Buzzer Driver

BA45F25343

Revision: V1.00   Date: February 26, 2025

Features

CPU Features

- Operating Voltage
  - f_{SYS}=2MHz: 2.2V~5.5V
  - f_{SYS}=4MHz: 2.2V~5.5V
  - f_{SYS}=8MHz: 2.2V~5.5V
- Up to 0.5μs instruction cycle with 8MHz system clock at V_{DD}=5V
- Power down and wake-up functions to reduce power consumption
- Oscillator types
  - Internal High Speed 2/4/8MHz RC – HIRC
  - Internal Low Speed 32.768kHz RC – LIRC
  - External Low Speed 32.768kHz Crystal – LXT
- Multi-mode operation: FAST, SLOW, IDLE and SLEEP
- Fully integrated internal oscillators require no external components
- All instructions executed in 1~3 instruction cycles
- Table read instructions
- 115 powerful instructions
- 8-level subroutine nesting
- Bit manipulation instruction

Peripheral Features

- Flash Program Memory: 4K×16
- RAM Data Memory: 256×8
- True EEPROM Memory: 64×8
- Watchdog Timer function
- Up to 12 bidirectional I/O lines
- Two external interrupt lines shared with I/O pins
- Programmable I/O port source current for LED applications
- Sink current generator for constant current output
- Smoke Detector AFE including two operational amplifiers
- Power Line Transceiver including two comparators, one Operational Amplifier and three D/A converters
- Two Timer Modules for time measure, input capture, compare match output, PWM output or single pulse output function
- Dual Time Base functions for generation of fixed time interrupt signals
- Universial Serial Interface Module – USIM for SPI, I²C or UART communication
- 3 external channel 12-bit resolution A/D converter with Internal Reference Voltage V_{BGREF}
- Temperature sensor with internal reference voltage
- Integrated 16-bit Cyclic Redundancy Check function – CRC
- Low Voltage Reset function

- Low Voltage Detect function
- Package types: 24/28-pin SSOP

Buzzer Driver Feature

- Input voltage (BDV$_{DD}$): 2.2V~5.5V
- Integrated 2-pin and 3-pin buzzer drivers
- Integrated a boost converter
- Integrated a 5V regulator
- Buzzer watchdog timer (BWDT) for MCU failure alarm function

General Description

The BA45F25343 is a Flash Memory A/D type 8-bit high performance RISC architecture microcontroller, designed for smoke detector applications.

For memory features, the Flash Memory offers users the convenience of multi-programming features. Other memory includes an area of RAM Data Memory as well as an area of true EEPROM memory for storage of non-volatile data such as serial numbers, calibration data etc.

Analog features include a multi-channel Analog to Digital converter with an integrated temperature sensor circuitry, a Smoke Detector AFE, a Sink Current generator, and a Power Line Transceiver including two comparators, one operational amplifier and three D/A converters. With regard to internal timers, the device includes multiple and extremely flexible Timer Modules providing functions for timing, pulse generation and PWM output operations. Communication with the outside world is catered for by including a fully integrated SPI, I²C and UART interface functions, three popular interfaces which provide designers with a means of easy communication with external peripheral hardware. Protective features such as an internal Watchdog Timer, Low Voltage Reset and Low Voltage Detector coupled with excellent noise immunity and ESD protection ensure that reliable operation is maintained in hostile electrical environments.

The device also includes a buzzer driver with a boost converter, a 5V regulator and a buzzer watchdog. The buzzer driver supports 2-pin or 3-pin buzzers, the 5V regulator is used to drive the blue LED, and the buzzer watchdog provides the MCU failure alarm function.

A full choice of external low, internal high and low speed oscillators is provided including two fully integrated system oscillators which require no external components for their implementation. The ability to operate and switch dynamically between a range of operating modes using different clock sources gives users the ability to optimise microcontroller operation and minimise power consumption.

This inclusion of flexible I/O programming features, Time Base functions along with many other features ensure that the devices will find excellent use in the smoke detector applications.
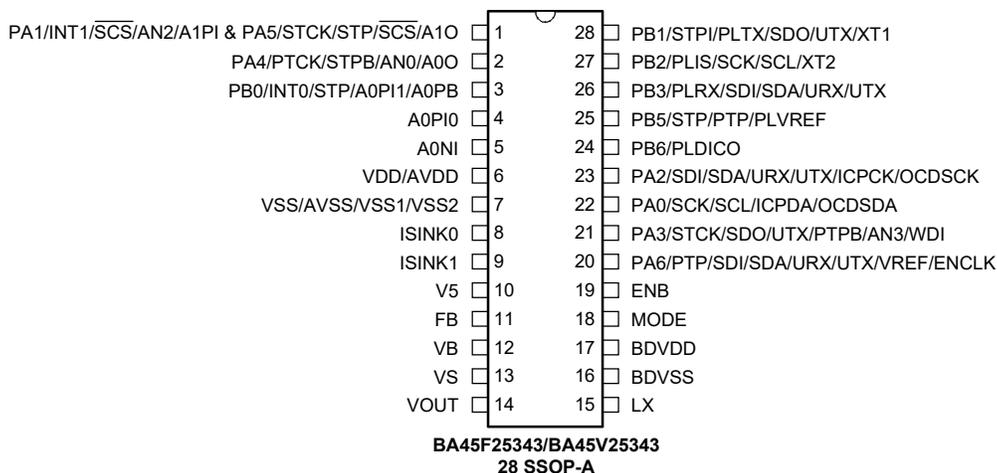
Block Diagram

☐ : Pin-shared Node   ＊ : USIM including SPI, I²C & UART
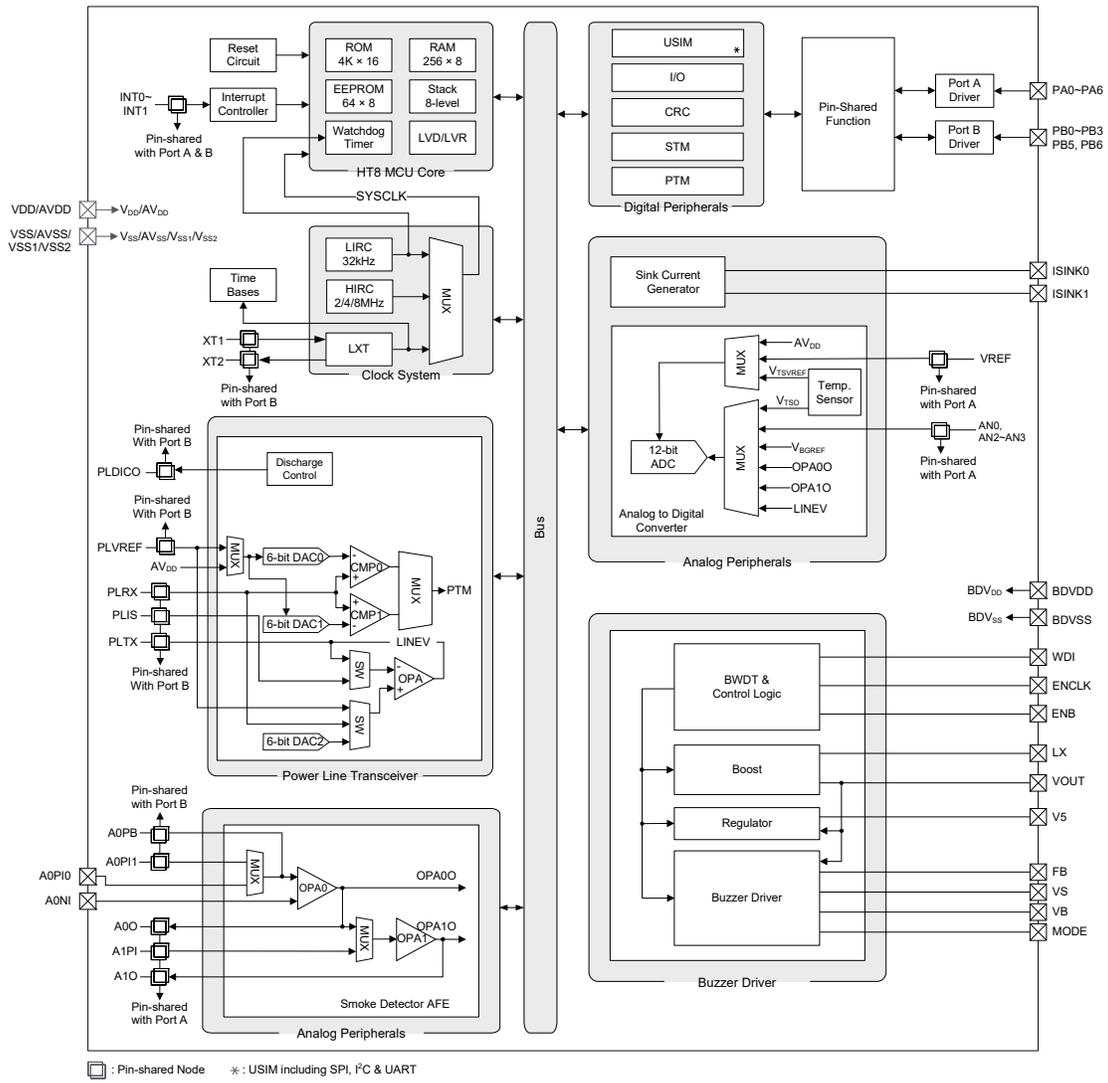
Pin Assignment

PA1/INT1/$\overline{SCS}$/AN2/A1PI ☐ 1   24 ☐ PB1/STPI/PLTX/SDO/UTX/XT1
PB0/INT0/STP/A0PI1/A0PB ☐ 2   23 ☐ PB2/PLIS/SCK/SCL/XT2
A0PI0 ☐ 3   22 ☐ PA2/SDI/SDA/URX/UTX/ICPCK/OCDSCK
A0NI ☐ 4   21 ☐ PA0/SCK/SCL/ICPDA/OCDSDA
VDD/AVDD ☐ 5   20 ☐ PA3/STCK/SDO/UTX/PTPB/AN3/WDI
VSS/AVSS/VSS1/VSS2 ☐ 6   19 ☐ PA6/PTP/SDI/SDA/URX/UTX/VREF/ENCLK
ISINK0 ☐ 7   18 ☐ ENB
ISINK1 ☐ 8   17 ☐ MODE
V5 ☐ 9   16 ☐ BDVDD
FB ☐ 10   15 ☐ BDVSS
VB ☐ 11   14 ☐ LX
VS ☐ 12   13 ☐ VOUT

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PA1/INT1/SCS/AN2/A1PI & PA5/STCK/STP/SCS/A1O  □ 1      28 □  PB1/STPI/PLTX/SDO/UTX/XT1
                    PA4/PTCK/STPB/AN0/A0O  □ 2      27 □  PB2/PLIS/SCK/SCL/XT2
                   PB0/INT0/STP/A0PI1/A0PB  □ 3      26 □  PB3/PLRX/SDI/SDA/URX/UTX
                                    A0PI0  □ 4      25 □  PB5/STP/PTP/PLVREF
                                     A0NI  □ 5      24 □  PB6/PLDICO
                                 VDD/AVDD  □ 6      23 □  PA2/SDI/SDA/URX/UTX/ICPCK/OCDSCK
                      VSS/AVSS/VSS1/VSS2  □ 7      22 □  PA0/SCK/SCL/ICPDA/OCDSDA
                                   ISINK0  □ 8      21 □  PA3/STCK/SDO/UTX/PTPB/AN3/WDI
                                   ISINK1  □ 9      20 □  PA6/PTP/SDI/SDA/URX/UTX/VREF/ENCLK
                                       V5  □ 10     19 □  ENB
                                       FB  □ 11     18 □  MODE
                                       VB  □ 12     17 □  BDVDD
                                       VS  □ 13     16 □  BDVSS
                                     VOUT  □ 14     15 □  LX
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Note: 1. For the BA45F25343/BA45V25343, on Pin 1 there are two sets of pin functions, thePA1/INT1/SCS/AN2/A1PI or PA5/STCK/STP/SCS/A1O, however cannot be used simultaneously. If the PA1/INT1/SCS/AN2/A1PI function set is used, the PA5 should be configured as an input with pull-high function disabled. If the PA5/STCK/STP/SCS/A1O function set is used, the PA1 should be configured as an input with pull-high function disabled.

2. If the pin-shared pin functions have multiple outputs simultaneously, the desired pin-shared function is determined by the corresponding software control bits.

3. For the less pin-count package types, there will be un-bonded pins of which status should be properly configured to avoid the unwanted current consumption resulting from floating input condition. Refer to the "Standby Current Considerations" and "Input/Output Ports" sections.

4. Pin functions OCDSCK and OCDSDA which are pin-shared with PA2 and PA0 are only available in the OCDS EV device BA45V25343.

Pin Description

The function of each pin is listed in the following table, however the details behind how each pin is configured is contained in other sections of the datasheet. As the Pin Description table shows the situation for the package type with the most pins, not all pins in the table will be available on smaller package sizes. In addition, the PA1 and PA5 share the same pin location, refer to the Pin Assignment.

Pin Name	Function	OPT	I/T	O/T	Description
PA0/SCK/SCL/ICPDA/ OCDSDA	PA0	PAPU PAWU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-high and wake-up
	SCK	PAS0 IFS0	ST	CMOS	SPI serial clock
	SCL	PAS0 IFS0	ST	NMOS	I²C clock line
	ICPDA	—	ST	CMOS	ICP data/address
	OCDSDA	—	ST	CMOS	OCDS data/address, for EV chip only

Pin Name	Function	OPT	I/T	O/T	Description
PA1/INT1/$\overline{SCS}$/AN2/A1PI	PA1	PAPU PAWU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-high and wake-up
	INT1	PAS0 INTC0 INTEG	ST	—	External interrupt input 1
	$\overline{SCS}$	PAS0 IFS0	ST	CMOS	SPI slave select
	AN2	PAS0	AN	—	A/D Converter external input channel 2
	A1PI	PAS0	AN	—	SD OPA1 positive input
PA2/SDI/SDA/URX/UTX/ ICPCK/OCDSCK	PA2	PAPU PAWU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-high and wake-up
	SDI	PAS0 IFS0	ST	—	SPI serial data input
	SDA	PAS0 IFS0	ST	NMOS	I²C data line
	URX/UTX	PAS0 IFS0	ST	CMOS	UART serial data input in full-duplex communication or UART serial data input/output in single wire mode communication
	ICPCK	—	ST	—	ICP clock pin
	OCDSCK	—	ST	—	OCDS clock pin, for EV chip only
PA3/STCK/SDO/UTX/ PTPB/AN3/WDI	PA3	PAPU PAWU PAS0	ST	CMOS	General purpose I/O. Register enabled pull-high and wake-up
	STCK	PAS0 IFS1	ST	—	STM clock input
	SDO	PAS0	—	CMOS	SPI serial data output
	UTX	PAS0	—	CMOS	UART serial data output
	PTPB	PAS0	—	CMOS	PTM inverted output
	AN3	PAS0	AN	—	A/D Converter external input channel 3
	WDI	—	ST	—	BWDT Input With Pull-down Resistor
PA4/PTCK/STPB/AN0/ A0O	PA4	PAPU PAWU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-high and wake-up
	PTCK	PAS1	ST	—	PTM clock input or capture input
	STPB	PAS1	—	CMOS	STM inverted output
	AN0	PAS1	AN	—	A/D Converter external input channel 0
	A0O	PAS1	—	AN	SD OPA0 output
PA5/STCK/STP/$\overline{SCS}$/A1O	PA5	PAPU PAWU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-high and wake-up
	STCK	PAS1 IFS1	ST	—	STM clock input
	STP	PAS1	—	CMOS	STM output
	$\overline{SCS}$	PAS1 IFS0	ST	CMOS	SPI slave select
	A1O	PAS1	—	AN	SD OPA1 output

Pin Name	Function	OPT	I/T	O/T	Description
PA6/PTP/SDI/SDA/URX/ UTX/VREF/ENCLK	PA6	PAPU PAWU PAS1	ST	CMOS	General purpose I/O. Register enabled pull-high and wake-up
	PTP	PAS1	—	CMOS	PTM output
	SDI	PAS1 IFS0	ST	—	SPI serial data input
	SDA	PAS0 IFS0	ST	NMOS	I²C data line
	URX/UTX	PAS1 IFS0	ST	CMOS	UART serial data input in full-duplex communication or UART serial data input/output in Single Wire Mode communication
	VREF	PAS1	AN	—	A/D Converter extemal reference voltage input
	ENCLK	—	ST	—	ENCLK Control Boost/Regulator/Buzzer
PB0/INT0/STP/A0PI1/ A0PB	PB0	PBPU PBS0	ST	CMOS	General purpose I/O. Register enabled pull-high
	INT0	PBS0 IFS1 INTC0 INTEG	ST	—	External interrupt input 0
	STP	PBS0	—	CMOS	STM output
	A0PI1	PBS0	AN	—	SD OPA0 positive input channel 1
	A0PB	PBS0	AN	—	SD OPA0 bias input
PB1/STPI/PLTX/SDO/ UTX/XT1	PB1	PBPU PBS0	ST	CMOS	General purpose I/O. Register enabled pull-high
	STPI	PBS0 IFS1	ST	—	STM capture input
	PLTX	PBS0	—	AN	Power Line Transceiver TX output
	SDO	PBS0	—	CMOS	SPI serial data output
	UTX	PBS0	—	CMOS	UART serial data output
	XT1	PBS0	AN	—	LXT oscillator pin
PB2/PLIS/SCK/SCL/XT2	PB2	PBPU PBS0	ST	CMOS	General purpose I/O. Register enabled pull-high
	PLIS	PBS0	AN	—	Power Line Transceiver IS input
	SCK	PBS0 IFS0	ST	CMOS	SPI serial clock
	SCL	PBS0 IFS0	ST	NMOS	I²C clock line
	XT2	PBS0	—	AN	LXT oscillator pin
PB3/PLRX/SDI/SDA/URX/ UTX	PB3	PBPU PBS0	ST	CMOS	General purpose I/O. Register enabled pull-high
	PLRX	PBS0	AN	—	Power Line Transceiver RX input
	SDI	PBS0 IFS0	ST	—	SPI serial data input
	SDA	PBS0 IFS0	ST	NMOS	I²C data line
	URX/UTX	PBS0 IFS0	ST	CMOS	UART serial data input in full-duplex communication or UART serial data input/output in single wire mode communication
PB5/STP/PTP/PLVREF	PB5	PBPU PBS1	ST	CMOS	General purpose I/O. Register enabled pull-high
	STP	PBS1	—	CMOS	STM output
	PTP	PBS1	—	CMOS	PTM output
	PLVREF	PBS1	AN	—	Power Line Transceiver D/A Converter reference

Pin Name	Function	OPT	I/T	O/T	Description
PB6/PLDICO	PB6	PBPU PBS1	ST	CMOS	General purpose I/O. Register enabled pull-high
	PLDICO	PBS1	—	AN	Power Line Transceiver discharge control
A0PI0	A0PI0	—	AN	—	SD OPA0 positive input channel 0
A0NI	A0NI	—	AN	—	SD OPA0 negative input
ISINK0	ISINK0	—	—	AN	Sink current 0 source
ISINK1	ISINK1	—	—	AN	Sink current 1 source
VDD/AVDD	VDD	—	PWR	—	Digital positive power supply
	AVDD	—	PWR	—	Analog positive power supply
VSS/AVSS/VSS1/VSS2	VSS	—	PWR	—	Digital negative power supply
	AVSS	—	PWR	—	Analog negative power supply
	VSS1	—	PWR	—	Sink Current Generator negative power supply
	VSS2	—	PWR	—	Sink Current Generator negative power supply
BDVDD	BDVDD	—	PWR	—	Buzzer positive power supply
BDVSS	BDVSS	—	PWR	—	Buzzer negative power supply, ground
ENB	ENB	—	ST	—	Enable pin, Control Boost/Regulator/Buzzer
MODE	MODE	—	ST	—	MODE pin, Control Boost/Regulator/Buzzer
VOUT	VOUT	—	—	PWR	Boost converter output
LX	LX	—	—	PWR	Power switch output
V5	V5	—	—	PWR	Regulator output
FB	FB	—	ST	—	Feedback pin in 3-pin buzzer mode
VS	VS	—	—	CMOS	Output for Buzzer
VB	VB	—	—	CMOS	Complementary Ootput for buzzer

Legend: I/T: Input type; O/T: Output type;
OPT: Optional by register option; PWR: Power;
ST: Schmitt Trigger input; CMOS: CMOS output;
NMOS: NMOS output; AN: Analog signal.

Absolute Maximum Ratings

Supply Voltage ....V_{SS} - 0.3V to 6.0V

Input Voltage .... V_{SS} - 0.3V to V_{DD}+0.3V

Storage Temperature.. -60°C to 150°C

Operating Temperature.. -40°C to 85°C

I_{OL} Total 80mA

I_{OH} Total... -80mA

VOUT, FB, VB, VS..V_{SS}-0.3V to 18V

Total Power Dissipation 500mW

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of the device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

For data in the following tables, note that factors such as oscillator type, operating voltage, operating frequency, pin load conditions, temperature and program instruction type, etc., can all exert an influence on the measured values.

Operating Voltage Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage – HIRC	f_{SYS}=2MHz	2.2	—	5.5	V
		f_{SYS}=4MHz	2.2	—	5.5	
		f_{SYS}=8MHz	2.2	—	5.5	
	Operating Voltage – LXT	f_{SYS}=32768Hz	2.2	—	5.5	V
	Operating Voltage – LIRC	f_{SYS}=32.768kHz	2.2	—	5.5	V

Operating Current Characteristics

Ta=-40°C~85°C

Symbol	Operating Mode	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{DD}	SLOW Mode (LIRC)	2.2V	f_{SYS}=32.768kHz	—	8	16	μA
		3V		—	10	20	
		5V		—	30	50	
	SLOW Mode (LXT)	2.2V	f_{SYS}=32.768kHz	—	8	16	μA
		3V		—	10	20	
		5V		—	30	50	
	FAST Mode (HIRC)	2.2V	f_{SYS}=2MHz	—	0.15	0.20	mA
		3V		—	0.2	0.3	
		5V		—	0.4	0.6	
		2.2V	f_{SYS}=4MHz	—	0.3	0.5	mA
		3V		—	0.4	0.6	
		5V		—	0.8	1.2	
		2.2V	f_{SYS}=8MHz	—	0.6	1.0	mA
		3V		—	0.8	1.2	
		5V		—	1.6	2.4	

Note: When using the characteristic table data, the following notes should be taken into consideration:

1. Any digital inputs are setup in a non-floating condition.
2. All measurements are taken under conditions of no load and with all peripherals in an off state.
3. There are no DC current paths.
4. All Operating Current values are measured using a continuous NOP instruction program loop.

Standby Current Characteristics

Ta=25°C, unless otherwise specified

Symbol	Standby Mode	Test Conditions		Min.	Typ.	Max.	Max. @85°C	Unit
		V_{DD}	Conditions					
I_{STB}	SLEEP Mode	2.2V	WDT on	—	1.2	2.4	2.9	μA
		3V		—	1.5	3.0	3.6	
		5V		—	3	5	6	
	IDLE0 Mode (LIRC)	2.2V	f_{SUB} on	—	2.4	4.0	4.8	μA
		3V		—	3	5	6	
		5V		—	5	10	12	

Symbol	Standby Mode	Test Conditions		Min.	Typ.	Max.	Max. @85°C	Unit
		V_{DD}	Conditions					
I_{STB}	IDLE0 Mode (LXT)	2.2V	f_{SUB} on	—	2.4	4.0	4.8	μA
		3V		—	3	5	6	
		5V		—	5	10	12	
	IDLE1 Mode (HIRC)	2.2V	f_{SUB} on, f_{SYS}=2MHz	—	60	120	140	μA
		3V		—	70	140	160	
		5V		—	130	260	280	
		2.2V	f_{SUB} on, f_{SYS}=4MHz	—	144	200	240	μA
		3V		—	180	250	300	
		5V		—	400	600	720	
		2.2V	f_{SUB} on, f_{SYS}=8MHz	—	288	400	480	μA
		3V		—	360	500	600	
		5V		—	600	800	960	

Note: When using the characteristic table data, the following notes should be taken into consideration:
1. Any digital inputs are setup in a non-floating condition.
2. All measurements are taken under conditions of no load and with all peripherals in an off state.
3. There are no DC current paths.
4. All Standby Current values are taken after a HALT instruction execution thus stopping all instruction execution.

A.C. Characteristics

For data in the following tables, note that factors such as oscillator type, operating voltage, operating frequency and temperature etc., can all exert an influence on the measured values.

High Speed Internal Oscillator – HIRC – Frequency Accuracy

During the program writing operation the writer will trim the HIRC oscillator at a user selected HIRC frequency and user selected voltage of either 3V or 5V.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Temp.				
f_{HIRC}	2MHz Writer Trimmed HIRC Frequency	3V/5V	25°C	-1%	2	+1%	MHz
			-20°C~60°C	-2%	2	+2%	
			-40°C~85°C	-3%	2	+3%	
		2.2V~5.5V	25°C	-6%	2	+9%	
			-40°C~85°C	-6%	2	+10%	
	4MHz Writer Trimmed HIRC Frequency	3V/5V	25°C	-1%	4	+1%	MHz
			-40°C~85°C	-2%	4	+2%	
		2.2V~5.5V	25°C	-2.5%	4	+2.5%	
			-40°C~85°C	-3%	4	+3%	
	8MHz Writer Trimmed HIRC Frequency	3V/5V	25°C	-1%	8	+1%	MHz
			-40°C~85°C	-2%	8	+2%	
		2.2V~5.5V	25°C	-2.5%	8	+2.5%	
			-40°C~85°C	-3%	8	+3%	

Note: 1. The 3V/5V values for V_{DD} are provided as these are the two selectable fixed voltages at which the HIRC frequency is trimmed by the writer.
2. The row below the 3V/5V trim voltage row is provided to show the values for the full V_{DD} range operating voltage. It is recommended that the trim voltage is fixed at 3V for application voltage ranges from 2.2V to 3.6V and fixed at 5V for application voltage ranges from 3.3V to 5.5V.
3. The minimum and maximum tolerance values provided in the table are only for the frequency at which the writer trims the HIRC oscillator. After trimming at this chosen specific frequency any change in HIRC oscillator frequency using the oscillator register control bits by the application program will give a frequency tolerance to within ±20%.

Low Speed Internal Oscillator Characteristics – LIRC

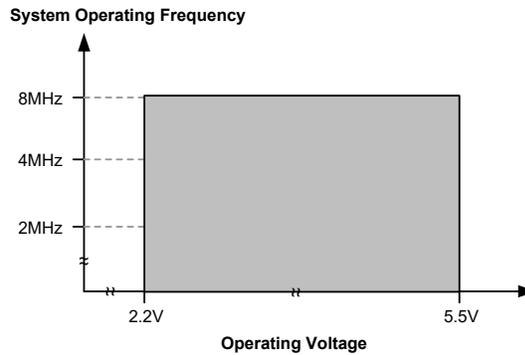| Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Temp.				
f_{LIRC}	LIRC Frequency	3V	-10°C~50°C	-0.5%	32.768	+0.5%	kHz
		3V	-40°C~85°C	-3%	32.768	+3%	
		2.2V~5.5V	-40°C~85°C	-10%	32.768	+10%	
t_{START}	LIRC Start-up Time	—	-40°C~85°C	—	—	100	µs

External Low Speed Crystal Oscillator Characteristics – LXT

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{LXT}	Oscillator Frequency	2.2V~5.5V	—	—	32768	—	Hz
t_{START}	LXT Start-up Time	3V	—	—	—	1000	ms
		5V	—	—	—	1000	ms
Duty Cycle	Duty Cycle	—	—	40	—	60	%
R_{NEG}	Negative Resistance[Note]	2.2V	—	3×ESR	—	—	Ω

Note: C1, C2 and R_P are external components. C1=C2=10pF. R_P=10MΩ, C_L=7pF, ESR=30kΩ.

Operating Frequency Characteristic Curves

System Start Up Time Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{SST}	System Start-up Time (Wake-up from Condition where f_{SYS} is off)	—	$f_{SYS}=f_H~f_H/64$, $f_H=f_{HIRC}$	—	16	—	t_{HIRC}
		—	$f_{SYS}=f_{SUB}=f_{LXT}$	—	1024	—	t_{LXT}
		—	$f_{SYS}=f_{SUB}=f_{LIRC}$	—	2	—	t_{LIRC}
	System Start-up Time (Wake-up from Condition where f_{SYS} is on)	—	$f_{SYS}=f_H~f_H/64$, $f_H=f_{HIRC}$	—	2	—	t_H
		—	$f_{SYS}=f_{SUB}=f_{LIRC}$ or f_{LXT}	—	2	—	t_{SUB}
	System Speed Switch Time (FAST to SLOW Mode or SLOW to FAST Mode)	—	f_{HIRC} switches from off → on	—	16	—	t_{HIRC}
		—	f_{LXT} switches from off → on	—	1024	—	t_{LXT}
t_{RSTD}	System Reset Delay Time (Reset source from Power-on reset or LVR Hardware Reset)	—	RR_{POR}=5V/ms	14	16	18	ms
	System Reset Delay Time (WDTC Register Software Reset)	—	—				
	System Reset Delay Time (WDT Overflow Reset)	—	—				

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{SRESET}	Minimum Software Reset Width to Reset	—	—	45	90	120	µs

Note: 1. For the System Start-up time values, whether f_{SYS} is on or off depends upon the mode type and the chosen f_{SYS} system oscillator. Details are provided in the System Operating Modes section.

2. The time units, shown by the symbols t_{HIRC} etc., are the inverse of the corresponding frequency values as provided in the frequency tables. For example, $t_{HIRC}=1/f_{HIRC}$, $t_{SYS}=1/f_{SYS}$ etc.

3. If the LIRC is used as the system clock and if it is off when in the SLEEP Mode, then an additional LIRC start up time, t_{START}, as provided in the LIRC frequency table, must be added to the t_{SST} time in the table above.

4. The System Speed Switch Time is effectively the time taken for the newly activated oscillator to start up.

Input/Output Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IL}	Input Low Voltage for I/O Ports	5V	—	0	—	1.5	V
		—	—	0	—	$0.2V_{DD}$	
V_{IH}	Input High Voltage for I/O Ports	5V	—	3.5	—	5.0	V
		—	—	$0.8V_{DD}$	—	V_{DD}	
I_{OL}	Sink Current for I/O Ports	3V	$V_{OL}=0.1V_{DD}$	16	32	—	mA
		5V		32	65	—	
I_{OH}	Source Current for I/O Ports	3V	$V_{OH}=0.9V_{DD}$, SLEDC[m+1, m]=00B (m=0, 2, 4, 6)	-0.7	-1.5	—	mA
		5V		-1.5	-2.9	—	
		3V	$V_{OH}=0.9V_{DD}$, SLEDC[m+1, m]=01B (m=0, 2, 4, 6)	-1.3	-2.5	—	
		5V		-2.5	-5.1	—	
		3V	$V_{OH}=0.9V_{DD}$, SLEDC[m+1, m]=10B (m=0, 2, 4, 6)	-1.8	-3.6	—	
		5V		-3.6	-7.3	—	
		3V	$V_{OH}=0.9V_{DD}$, SLEDC[m+1, m]=11B (m=0, 2, 4, 6)	-4	-8	—	
		5V		-8	-16	—	
R_{PH}	Pull-high Resistance for I/O Ports [1]	3V	—	20	60	90	kΩ
		5V		10	30	45	
I_{LEAK}	Input Leakage Current	5V	$V_{IN}=V_{DD}$ or $V_{IN}=V_{SS}$	—	—	±1	µA
t_{INT}	Interrupt Pin Minimum Pulse Width	—	—	10	—	—	µs
t_{TCK}	xTM xTCK Input Pin Minimum Pulse Width	—	—	0.3	—	—	µs
t_{TPI}	STM STPI Input Pin Minimum Pulse Width	—	—	0.3	—	—	µs
f_{TMCLK}	xTM Maximum Timer Clock Source Frequency	5V	—	—	—	1	f_{SYS}
t_{CPW}	xTM Minimum Capture Pulse Width	—	—	t_{CPW}[2]	—	—	µs

Note: 1. The R_{PH} internal pull-high resistance value is calculated by connecting to ground and enabling the input pin with a pull-high resistor and then measuring the pin current at the specified supply voltage level. Dividing the voltage by this measured current provides the R_{PH} value.

2. For PTM:

If PTCAPTS=1, then $t_{CPW}=max(2×t_{TMCLK}, t_{TCK})$

Ex: If PTCAPTS=1, f_{TMCLK}=8MHz, t_{TCK}=0.3µs, then $t_{CPW}=max(0.25µs, 0.3µs)=0.3µs$

For STM:

$t_{CPW}=max(2\times t_{TMCLK}, t_{TPI})$

Ex1: If $f_{TMCLK}=8MHz$, $t_{TPI}=0.3\mu s$, then $t_{CPW}=max(0.25\mu s, 0.3\mu s)=0.3\mu s$

Ex2: If $f_{TMCLK}=4MHz$, $t_{TPI}=0.3\mu s$, then $t_{CPW}=max(0.5\mu s, 0.3\mu s)=0.5\mu s$

Where $t_{TMCLK}=1/f_{TMCLK}$

Memory Characteristics

Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Flash Program Memory							
t_{DEW}	Erase/Write Cycle Time	—	—	—	2	3	ms
I_{DDPGM}	Programming/Erase Current on V_{DD}	—	—	—	—	5	mA
E_P	Cell Endurance	—	—	10K	—	—	E/W
t_{RETD}	ROM Data Retention Time	—	Ta=25°C	—	40	—	Year
Data EEPROM Memory							
V_{DD}	Operating Voltage for Read/Write	—	—	2.2	—	5.5	V
t_{EERD}	Read Cycle Time	—	—	—	—	4	t_{SYS}
t_{EEWR}	Write Cycle Time	—	—	—	4	6	ms
E_P	Cell Endurance	—	—	100K	—	—	E/W
t_{RETD}	Data Retention Time	—	Ta=25°C	—	40	—	Year
RAM Data Memory							
V_{DR}	Data Retention Voltage	—	—	1.0	—	—	V

Note: "E/W" means Erase/Write times.

LVD & LVR Electrical Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{LVR}	Low Voltage Reset Voltage	—	LVR enable	-5%	2.1	+5%	V
V_{LVD}	Low Voltage Detection Voltage	—	LVD enable, voltage select 2.0V	-5%	2.0	+5%	V
			LVD enable, voltage select 2.2V		2.2		
			LVD enable, voltage select 2.4V		2.4		
			LVD enable, voltage select 2.7V		2.7		
			LVD enable, voltage select 3.0V		3.0		
			LVD enable, voltage select 3.3V		3.3		
			LVD enable, voltage select 3.6V		3.6		
			LVD enable, voltage select 4.0V		4.0		
$I_{LVRLVDBG}$	Operating Current	3V	LVD enable, LVR enable, VBGEN=0	—	—	20	μA
		5V		—	20	25	
		3V	LVD enable, LVR enable, VBGEN=1	—	—	25	μA
		5V		—	25	30	
t_{LVDS}	LVDO Stable Time	—	For LVR enable, VBGEN=0, LVD off → on	—	—	18	μs
t_{LVR}	Minimum Low Voltage Width to Reset	—	TLVR[1:0]=00B	120	240	480	μs
		—	TLVR[1:0]=01B	0.5	1.0	2.0	ms
		—	TLVR[1:0]=10B	1	2	4	
		—	TLVR[1:0]=11B	2	4	8	

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{LVD}	Minimum Low Voltage Width to Interrupt	—	—	60	120	240	µs
I_{LVR}	Additional Current for LVR Enable	—	LVD disable, VBGEN=0	—	—	24	µA

Internal Reference Voltage Characteristics

Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.2	—	5.5	V
V_{BGREF}	Bandgap Reference Voltage	—	—	-1%	1.2	+1%	V
I_{BGREF}	Operating Current	5.5V	—	—	25	40	µA
PSRR	Power Supply Rejection Ratio	—	Ta=25°C, V_{RIPPLE}=1V_{P-P}, f_{RIPPLE}=100Hz	75	—	—	dB
En	Output Noise	—	Ta=25°C, no load current, f=0.1Hz~10Hz	—	300	—	µV_{RMS}
I_{DRV}	Buffer Driving Capability	—	$\triangle V_{BGREF}$=-1%	1	—	—	mA
I_{SD}	Shutdown Current	—	VBGREN=0	—	—	0.1	µA
t_{START}	Startup Time	2.2V~5.5V	Ta=25°C	—	—	400	µs

Note: 1. All the above parameters are measured under conditions of no load condition unless otherwise described.

2. A 0.1µF ceramic capacitor should be connected between VDD and GND.

3. The V_{BGREF} voltage is used as the A/D converter reference voltage input.

A/D Converter Electrical Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{ADI}	Input Voltage	—	—	0	—	V_{REF}	V
V_{REF}	Reference Voltage	—	—	2.2	—	AV_{DD}	V
N_R	Resolution	—	—	—	—	12	Bit
DNL	Differential Non-linearity	—	V_{REF}=AV_{DD}, t_{ADCK}=0.5µs, SAMS=0	-3	—	3	LSB
		—	V_{REF}=AV_{DD}, t_{ADCK}=4µs, SAMS=1	-3	—	3	LSB
INL	Integral Non-linearity	—	V_{REF}=AV_{DD}, t_{ADCK}=0.5µs, SAMS=0	-4	—	4	LSB
		—	V_{REF}=AV_{DD}, t_{ADCK}=4µs, SAMS=1	-4	—	4	LSB
I_{ADC}	Additional Current for A/D Converter Enable	2.2V	No load, t_{ADCK}=0.5µs, SAMS=0	—	210	300	µA
		3V		—	240	350	
		5V		—	350	500	
		2.2V	No load, t_{ADCK}=4µs, SAMS=1	—	180	250	µA
		3V		—	200	300	
		5V		—	300	420	

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_{ADCK}	Clock Period	—	AN≠Temperature Sensor, SAMS=0	0.5	—	10.0	µs
		—	AN≠Temperature Sensor, SAMS=1	4	—	10	µs
		2.2V~5.5V	AN=Temperature Sensor, SAMS=0	1	—	2	µs
t_{ON2ST}	A/D Converter On-to-Start Time	—	—	4	—	—	µs
t_{ADS}	Sampling Time	—	AN≠Temperature Sensor	—	4	—	t_{ADCK}
		2.2V~5.5V	AN=Temperature Sensor	—	46	—	t_{ADCK}
t_{ADC}	Conversion Time (Including A/D Sample and Hold Time)	—	AN≠Temperature Sensor	—	16	—	t_{ADCK}
		2.2V~5.5V	AN=Temperature Sensor	—	58	—	t_{ADCK}
GERR	A/D Conversion Gain Error	—	$V_{REF}=AV_{DD}$	-4	—	4	LSB
OSRR	A/D Conversion Offset Error	—	$V_{REF}=AV_{DD}$	-4	—	4	LSB

Temperature Sensor Characteristics

Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.2	—	5.5	V
I_{TS}	Temperature Sensor Operating Current	3V	TSEN=ADCEN=1, t_{ADCK}=1µs, ADC included, SAMS=0	—	1260	1950	µA
		5V		—	1490	2250	µA
t_{TSS}	Temperature Sensor Turn on Stable Time	3V	—	—	—	100	µs
		5V	—	—	—	100	µs
V_{TSVREF}	Temperature Sensor Reference Voltage	3V	—	-5%	2.01	+5%	V
		5V	—	-5%	2.01	+5%	V
T_{ACC}	Temperature Accuracy (Error)	2.7V~4.5V	$V_{REF}=V_{TSVREF}$, Ta=0°C~70°C	-2	—	+2	°C
		2.7V~5.5V		-2.5	—	+2.5	
		—		—	±4	—	
		2.7V~4.5V	$V_{REF}=V_{TSVREF}$, Ta=-40°C~85°C	-4	—	+4	
		—		—	±5	—	
TS_Noise	Temperature Noise	3V	No average	—	0.4	—	°C (p-p)
		5V		—	0.6	—	°C (p-p)

Note: 1. The temperature accuracy T_{ACC} is defined as the error between the actual temperature and the temperature obtained by the conversion of the ADC code through the formula.

2. The relevant characteristics of temperature sensor use normal mode A/D converter (SAMS=0) for voltage conversion.

Sink Current Generator Electrical Characteristics

Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.2	—	5.5	V
I_{SINK0}	Sink Current for ISINK0 Pin	5V	Ta=25°C, V_{ISINK0}=3.0V, ISGDATA0[4:0]=00000B	47.5	50.0	52.5	mA
		—	Ta=-40°C~85°C, V_{ISINK0}=1.0V~4.5V, ISGDATA0[4:0]=00000B	41	50	59	
		—	Ta=-40°C~85°C, V_{ISINK0}=0.7V~1.0V, ISGDATA0[4:0]=00000B	37.5	50.0	50.0	
		5V	Ta=25°C, V_{ISINK0}=3.0V, ISGDATA0[4:0]=11111B	330	360	390	
		—	Ta=-40°C~85°C, V_{ISINK0}=1.0V~4.5V, ISGDATA0[4:0]=11111B	295	360	425	
		—	Ta=-40°C~85°C, V_{ISINK0}=0.7V~1.0V, ISGDATA0[4:0]=11111B	270	360	360	
I_{SINK1}	Sink Current for ISINK1 Pin	5V	Ta=25°C, V_{ISINK1}=3.0V, ISGDATA1[4:0]=00000B	43.5	50.0	56.5	mA
		—	Ta=-40°C~85°C, V_{ISINK1}=1.0V~4.5V, ISGDATA1[4:0]=00000B	41	50	59	
		—	Ta=-40°C~85°C, V_{ISINK1}=0.7V~1.0V, ISGDATA1[4:0]=00000B	37.5	50.0	50.0	
		5V	Ta=25°C, V_{ISINK1}=3.0V, ISGDATA1[4:0]=11111B	178	205	231	
		—	Ta=-40°C~85°C, V_{ISINK1}=1.0V~4.5V, ISGDATA1[4:0]=11111B	168	205	242	
		—	Ta=-40°C~85°C, V_{ISINK1}=0.7V~1.0V, ISGDATA1[4:0]=11111B	154	205	205	
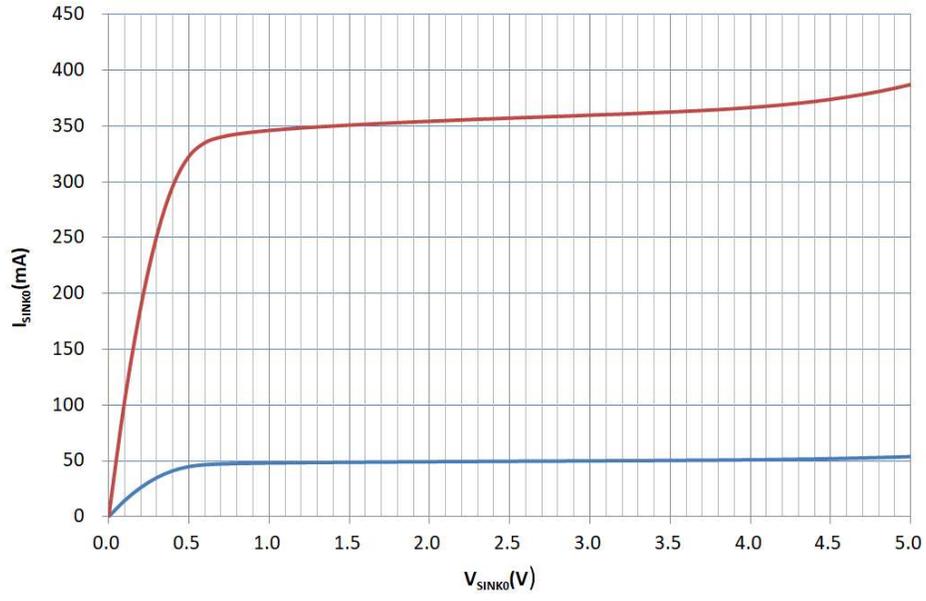
V_{SINK0} VS. I_{SINK0}

ISINK0 Characteristic Curve
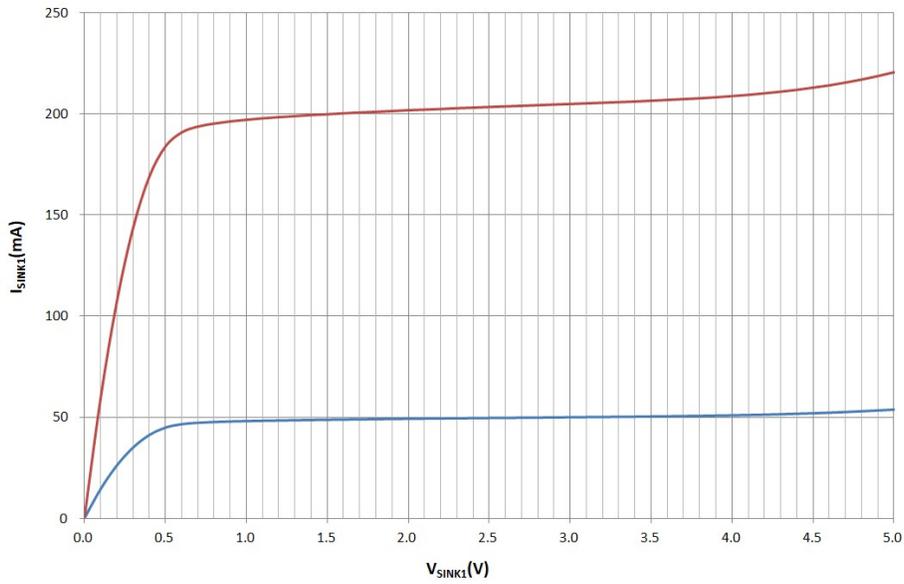
V_{SINK1} VS. I_{SINK1}

ISINK1 Characteristic Curve

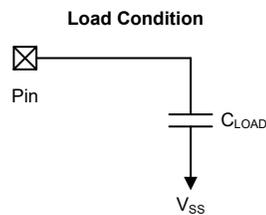## Power Line Transceiver Electrical Characteristics

Comparator Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Comparator Operating Voltage	—	—	2.2	—	5.5	V
I_{CMP}	Additional Current for Comparator Enable	3V	No load, PLTCmIS[1:0]=00B (m=0, 1)	—	1	5	μA
		5V		—	1	5	
		3V	No load, PLTCmIS[1:0]=01B (m=0, 1)	—	14	30	
		5V		—	14	30	
		3V	No load PLTCmIS[1:0]=10B (m=0, 1)	—	36	65	
		5V		—	36	65	
		3V	No load, PLTCmIS[1:0]=11B (m=0, 1)	—	58	110	
		5V		—	58	110	
V_{OS}	Comparator Input Offset Voltage	3V	Without calibration (PLTCmOF[4:0]=10000B, PLTCmIS[1:0]=00B, m=0, 1)	-10	—	+10	mV
		5V		-10	—	+10	
		3V	With calibration	-4	—	+4	
		5V		-4	—	+4	
V_{CM}	Common Mode Voltage Range	—	—	V_{SS}	—	V_{DD} - 1	V
t_{RP}	Response Time	3V	With 10mV overdrive[Note], No debounce, PLTCmIS[1:0]=00B (m=0, 1)	—	—	40	μs
		5V		—	—	40	
		3V	With 10mV overdrive[Note], No debounce, PLTCmIS[1:0]=01B (m=0, 1)	—	—	4	
		5V		—	—	4	
		3V	With 10mV overdrive[Note], No debounce, PLTCmIS[1:0]=10B (m=0, 1)	—	—	2	
		5V		—	—	2	
		3V	With 10mV overdrive[Note], No debounce, PLTCmIS[1:0]=11B (m=0, 1)	—	—	1.5	
		5V		—	—	1.5	
V_{HYS}	Hysteresis	3V	PLTCmHYS[1:0]=00B, PLTCmIS[1:0]=00B (m=0, 1)	0	0	5	mV
		5V		0	0	5	
		3V	PLTCmHYS[1:0]=01B, PLTCmIS[1:0]=01B (m=0, 1)	20	40	65	
		5V		20	40	65	
		3V	PLTCmHYS[1:0]=10B, PLTCmIS[1:0]=10B (m=0, 1)	50	100	150	
		5V		50	100	150	
		3V	PLTCmHYS[1:0]=11B, PLTCmIS[1:0]=11B (m=0, 1)	80	160	240	
		5V		80	160	240	

Note: 1. All the above parameters are measured under condition of comparator input voltage=$(V_{DD}-1)/2$ and remain constant.

2. Load Condition: C_{LOAD}=50pF

Load Condition

Pin

C_{LOAD}

V_{SS}

Operational Amplifier Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.2	—	5.5	V
I_{OPA}	Operating Current	—	PLTABW=0, no load	—	80	128	µA
			PLTABW=1, no load	—	200	320	
V_{OS}	Input Offset Voltage	—	Without calibration (PLTAOF[5:0]=100000B)	-15	—	15	mV
			With calibration	-2	—	2	
I_{OS}	Input Offset Current	—	V_{IN}=1/2 V_{CM}	—	1	10	nA
V_{CM}	Common Mode Voltage Range	—	PLTABW=0 or 1	V_{SS}	—	V_{DD}-1.4	V
PSRR	Power Supply Rejection Ratio	—	PLTABW=0 or 1	50	70	—	dB
CMRR	Common Mode Rejection Ratio	—	PLTABW=0 or 1	50	80	—	dB
A_{OL}	Open Loop Gain	—	PLTABW=0 or 1	60	80	—	dB
SR	Slew Rate	—	R_{LOAD}=1MΩ, C_{LOAD}=60pF, PLTABW=0	180	500	—	V/ms
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, PLTABW=1	600	1800	—	
GBW	Gain Bandwidth	—	R_{LOAD}=1MΩ, C_{LOAD}=60pF, PLTABW=0	400	600	—	kHz
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, PLTABW=1	1300	2000	—	
V_{OR}	Maximum Output Voltage Range	—	PLTABW=0 or 1, R_{LOAD}=5kΩ to V_{DD}/2	V_{SS}+210	—	V_{DD}-230	mV
I_{SC}	Output Short Circuit Current	—	R_{LOAD}=5.1Ω, PLTABW=0 or 1	±8.5	±20	—	mA

Note: These parameters are characterized but not tested.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{OPA}	Operating Current	—	PLTABW=0, no load	—	80	128	µA
			PLTABW=1, no load	—	200	320	
V_{OS}	Input Offset Voltage	—	Without calibration (PLTAOF [5:0]=100000B)	-15	—	15	mV
			With calibration	-2	—	2	
I_{OS}	Input Offset Current	—	V_{IN}=1/2 V_{CM}	—	1	10	nA
V_{CM}	Common Mode Voltage Range	—	PLTABW=0 or 1	V_{SS}	—	V_{DD}-1.4	V
PSRR	Power Supply Rejection Ratio	—	PLTABW=0 or 1	50	70	—	dB
CMRR	Common Mode Rejection Ratio	—	PLTABW=0 or 1	50	80	—	dB
A_{OL}	Open Loop Gain	—	PLTABW=0 or 1	60	80	—	dB
SR	Slew Rate	—	R_{LOAD}=1MΩ, C_{LOAD}=60pF, PLTABW=0	180	500	—	V/ms
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, PLTABW=1	600	1800	—	
GBW	Gain Bandwidth	—	R_{LOAD}=1MΩ, C_{LOAD}=60pF, PLTABW=0	250	600	—	kHz
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, PLTABW=1	800	2000	—	
V_{OR}	Maximum Output Voltage Range	—	PLTABW=0 or 1, R_{LOAD}=5kΩ to V_{DD}/2	V_{SS}+210	—	V_{DD}-230	mV
I_{SC}	Output Short Circuit Current	—	R_{LOAD}=5.1Ω, PLTABW=0 or 1	±2	±20	—	mA

Note: These parameters are characterized but not tested.

D/A Converter Electrical Characteristics

Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DACO}	Output Voltage Range	—	—	V_{SS} +0.1	—	V_{REF} -0.1	V
V_{REF}	Reference Voltage (DAC0 & DAC1)	—	PLTDA0REFS=1 or PLTDA1REFS=1	V_{SS} +0.4	—	V_{DD} -1.0	V
	Reference Voltage (DAC2)	—	—	2	—	V_{DD}	V
I_{DAC}	Additional Current for D/A Converter Enable (DAC0 & DAC1)	3V	PLTDACC[4:3]=00, PLTDACC[1:0]=01 or 10	—	3	6	µA
			PLTDACC[4:3]=00, PLTDACC[1:0]=11	—	6	12	
			V_{PLTREF}=1.6V PLTDACC[4:3]=10, PLTDACC[1:0]=10	—	5.6	11.2	
			V_{PLTREF}=1.6V PLTDACC[4:3]=11, PLTDACC[1:0]=11	—	7.2	14.4	
		5V	PLTDACC[4:3]=00, PLTDACC[1:0]=01 or 10	—	5	10	
			PLTDACC[4:3]=00, PLTDACC[1:0]=11	—	10	20	
			V_{PLTREF}=1.6V PLTDACC[4:3]=10, PLTDACC[1:0]=10	—	6.6	13.2	
			V_{PLTREF}=1.6V PLTDACC[4:3]=11, PLTDACC[1:0]=11	—	8.2	16.4	
	Additional Current for D/A Converter Enable (DAC2)	3V	—	—	—	360	µA
		5V	—	—	—	600	
t_{ST}	Settling Time	3V	C_{LOAD}=50pF	—	—	5	µs
		5V		—	—	5	
DNL	Differential Non-linearity	3V	V_{REF}=V_{DD}	-1	—	+1	LSB
		5V		-1	—	+1	
INL	Integral Non-linearity	3V	V_{REF}=V_{DD}	-1.5	—	+1.5	LSB
		5V		-1.5	—	+1.5	
Ro	R2R Output Resistor	3V	—	—	10	—	kΩ
		5V	—	—	10	—	

Operational Amplifier Characteristics (Smoke Detector AFE)

V_{DD}=5V, Ta=-40°C~85°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
I_{OPA}	Operating Current	—	SDAmBW[1:0]=00B, no load	—	3.0	5.0	µA
			SDAmBW[1:0]=01B, no load	—	10	16	
			SDAmBW[1:0]=10B, no load	—	80	128	
			SDAmBW[1:0]=11B, no load	—	200	320	
V_{OS}	Input Offset Voltage	—	Without calibration (SDAmOF[5:0]=100000B)	-15	—	15	mV
			With calibration	-2	—	2	
I_{OS}	Input Offset Current	—	V_{IN}=1/2 V_{CM}	—	1	10	nA
V_{CM}	Common Mode Voltage Range	—	SDAmBW[1:0]=00, 01, 10, 11	V_{SS}	—	V_{DD}-1.4	V
PSRR	Power Supply Rejection Ratio	—	SDAmBW[1:0]=00, 01, 10, 11	50	70	—	dB
CMRR	Common Mode Rejection Ratio	—	SDAmBW[1:0]=00, 01, 10, 11	50	80	—	dB
A_{OL}	Open Loop Gain	—	SDAmBW[1:0]=00, 01, 10, 11	60	80	—	dB
SR	Slew Rate	—	R_{LOAD}=1MΩ, C_{LOAD}=60pF, SDAmBW[1:0]=00	0.5	1.5	—	V/ms
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, SDAmBW[1:0]=01	5	15	—	
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, SDAmBW[1:0]=10	180	500	—	
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, SDAmBW[1:0]=11	600	1800	—	
GBW	Gain Bandwidth	—	R_{LOAD}=1MΩ, C_{LOAD}=60pF, SDAmBW[1:0]=00	2.5	5.0	—	kHz
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, SDAmBW[1:0]=01	20	40	—	
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, SDAmBW[1:0]=10	400	600	—	
			R_{LOAD}=1MΩ, C_{LOAD}=60pF, SDAmBW[1:0]=11	1300	2000	—	
V_{OR}	Maximum Output Voltage Range	—	SDAmBW[1:0]=00, 01, R_{LOAD}=5kΩ to V_{DD}/2	V_{SS}+140	—	V_{DD}-160	mV
		—	SDAmBW[1:0]=10, 11, R_{LOAD}=5kΩ to V_{DD}/2	V_{SS}+120	—	V_{DD}-140	mV
I_{SC}	Output Short Circuit Current	—	R_{LOAD}=5.1Ω, SDAmBW[1:0]=00, 01	±6	±12	—	mA
		—	R_{LOAD}=5.1Ω, SDAmBW[1:0]=10, 11	±10	±20	—	mA

Note: These parameters are characterized but not tested.

V$_{DD}$=2.2V~5.5V, Ta=-40°C~85°C

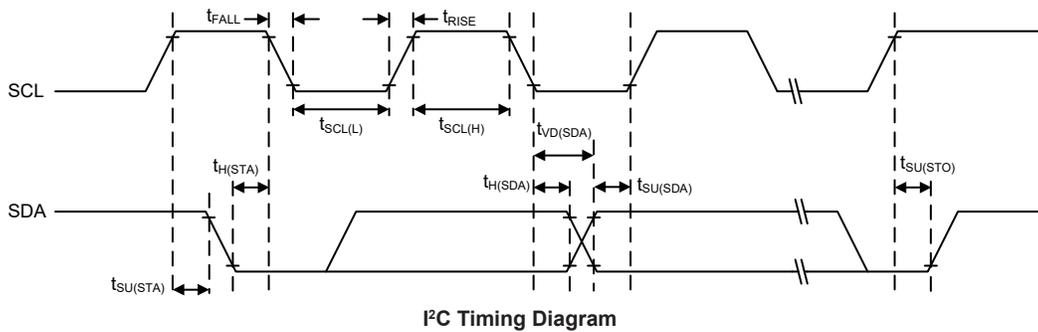| Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V$_{DD}$	Conditions				
I$_{OPA}$	Operating Current	—	SDAmBW[1:0]=00B, no load	—	2.5	4.0	μA
			SDAmBW[1:0]=01B, no load	—	10	16	
			SDAmBW[1:0]=10B, no load	—	80	128	
			SDAmBW[1:0]=11B, no load	—	200	320	
V$_{OS}$	Input Offset Voltage	3V	Without calibration (SDAmOF[5:0]=100000B)	-15	—	15	mV
		5V		-15	—	15	
		3V	With calibration	-2	—	2	
		5V		-2	—	2	
I$_{OS}$	Input Offset Current	—	V$_{IN}$=1/2 V$_{CM}$	—	1	10	nA
V$_{CM}$	Common Mode Voltage Range	—	SDAmBW[1:0]=00, 01, 10, 11	V$_{SS}$	—	V$_{DD}$-1.4	V
PSRR	Power Supply Rejection Ratio	—	SDAmBW[1:0]=00, 01, 10, 11	50	70	—	dB
CMRR	Common Mode Rejection Ratio	—	SDAmBW[1:0]=00, 01, 10, 11	50	80	—	dB
A$_{OL}$	Open Loop Gain	—	SDAmBW[1:0]=00, 01, 10, 11	60	80	—	dB
SR	Slew Rate	—	R$_{LOAD}$=1MΩ, C$_{LOAD}$=60pF, SDAmBW[1:0]=00B	0.5	1.5	—	V/ms
			R$_{LOAD}$=1MΩ, C$_{LOAD}$=60pF, SDAmBW[1:0]=01B	5	15	—	
			R$_{LOAD}$=1MΩ, C$_{LOAD}$=60pF, SDAmBW[1:0]=10B	180	500	—	
			R$_{LOAD}$=1MΩ, C$_{LOAD}$=60pF, SDAmBW[1:0]=11B	600	1800	—	
GBW	Gain Bandwidth	—	R$_{LOAD}$=1MΩ, C$_{LOAD}$=60pF, SDAmBW[1:0]=00B	2	5	—	kHz
			R$_{LOAD}$=1MΩ, C$_{LOAD}$=60pF, SDAmBW[1:0]=01B	15	40	—	
			R$_{LOAD}$=1MΩ, C$_{LOAD}$=60pF, SDAmBW[1:0]=10B	250	600	—	
			R$_{LOAD}$=1MΩ, C$_{LOAD}$=60pF, SDAmBW[1:0]=11B	800	2000	—	
V$_{OR}$	Maximum Output Voltage Range	—	SDAmBW[1:0]=00, 01, R$_{LOAD}$=5kΩ to V$_{DD}$/2	V$_{SS}$+140	—	V$_{DD}$-160	mV
			SDAmBW[1:0]=10, 11, R$_{LOAD}$=5kΩ to V$_{DD}$/2	V$_{SS}$+120	—	V$_{DD}$-140	
I$_{SC}$	Output Short Circuit Current	—	R$_{LOAD}$=5.1Ω, SDAmBW[1:0]=00, 01	±1.2	±12	—	mA
			R$_{LOAD}$=5.1Ω, SDAmBW[1:0]=10, 11	±2	±20	—	
en	Equivalent Input Voltage Noise	—	SDAmBW[1:0]=00B f=1kHz	—	250	—	nV/√Hz
			SDAmBW[1:0]=01B f=1kHz	—	140	—	
			f=10kHz		90		
			SDAmBW[1:0]=10B f=1kHz	—	80	—	
			f=10kHz		40		
			f=100kHz		30		
			SDAmBW[1:0]=11B f=1kHz	—	80	—	
			f=10kHz		40		
			f=100kHz		20		
			f=1000kHz		20		

Note: These parameters are characterized but not tested.

I²C Electrical Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{I2C}	I²C Standard Mode (100kHz) f_{SYS} Frequency [Note]	—	No clock debounce	2	—	—	MHz
			2 system clock debounce	4	—	—	
			4 system clock debounce	4	—	—	
	I²C Fast Mode (400kHz) f_{SYS} Frequency [Note]	—	No clock debounce	4	—	—	MHz
			2 system clock debounce	8	—	—	
			4 system clock debounce	8	—	—	
f_{SCL}	SCL Clock Frequency	3V/5V	Standard mode	—	—	100	kHz
			Fast mode	—	—	400	
$t_{SCL(H)}$	SCL Clock High Time	3V/5V	Standard mode	3.5	—	—	µs
			Fast mode	0.9	—	—	
$t_{SCL(L)}$	SCL Clock Low Time	3V/5V	Standard mode	3.5	—	—	µs
			Fast mode	0.9	—	—	
t_{FALL}	SCL and SDA Fall Time	3V/5V	Standard mode	—	—	1.3	µs
			Fast mode	—	—	0.34	
t_{RISE}	SCL and SDA Rise Time	3V/5V	Standard mode	—	—	1.3	µs
			Fast mode	—	—	0.34	
$t_{SU(SDA)}$	SDA Data Setup Time	3V/5V	Standard mode	0.25	—	—	µs
			Fast mode	0.1	—	—	
$t_{H(SDA)}$	SDA Data Hold Time	3V/5V	—	0.1	—	—	µs
$t_{VD(SDA)}$	SDA Data Valid Time	3V/5V	—	—	—	0.6	µs
$t_{SU(STA)}$	Start Condition Setup Time	3V/5V	Standard mode	3.5	—	—	µs
			Fast mode	0.6	—	—	
$t_{H(STA)}$	Start Condition Hold Time	3V/5V	Standard mode	4.0	—	—	µs
			Fast mode	0.6	—	—	
$t_{SU(STO)}$	Stop Condition Setup Time	3V/5V	Standard mode	3.5	—	—	µs
			Fast mode	0.6	—	—	

Note: Using the debounce function can make the transmission more stable and reduce the probability of communication failure due to interference.

I²C Timing Diagram

Buzzer Driver Electrical Characteristics

BDV_{DD}=3V, C1=47µF, L1=10µH, C2=2.2µF and Ta=25 °C, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Power Supply						
BDV_{DD}	Supply voltage	—	2.2	—	5.5	V
I_Q	Quiescent Current	BDV_{DD}=3V, No load, BWDT ON, other circuits off	—	—	2	µA
I_{IN}	Operating Current	BDV_{DD}=3V, No load, Boost on, Regulator on, 2-pin buzzer mode, f_{ENCLK}=4kHz	—	2	4	mA
I_{IL}	Input Leakage Current	MODE=BDV_{DD} or BDV_{SS}	—	—	±0.1	µA
		ENB=BDV_{DD}	—	—	-0.1	µA
		WDI, ENCLK=BDV_{SS}	—	—	0.1	µA
V_{IH}	High-Level Input Voltage	WDI, ENB, MODE, ENCLK	0.8BDV_{DD}	—	BDV_{DD}	V
V_{IL}	Low-Level Input Voltage	WDI, ENB, MODE, ENCLK	0	—	0.2BDV_{DD}	V
R_{PH}	Pull-High Resistor	BDV_{DD}=3V, ENB	—	200	—	kΩ
R_{PL}	Pull-Low Resistor	BDV_{DD}=3V, ENCLK, WDI	—	1	—	MΩ
BWDT						
t_{WDI}	WDI Period	BDV_{DD}=2.2V~5.5V, Ta=-40~85°C	10.3	11.5	14.3	s
t_{WDTP}	BWDT Reset Pulse Width	—	50	—	—	ns
Boost Converter						
V_{OUT}	Output Voltage	—	8.1	9.0	9.9	V
I_{OUT}	Output Current	—	50	—	—	mA
I_{OCP}	Over Current Protection	—	—	0.95	—	A
f_{SW}	Switching Frequency	—	0.8	1	1.2	MHz
Regulator						
V_{V5}	Regulator Output Voltage	—	4.9	5.2	5.5	V
I_{V5}	Output Current	—	5	—	—	mA
Buzzer						
I_{IL}	Leakage Current	Buzzer off, FB=BDV_{SS}	—	—	1	µA
		Buzzer off, FB=V_{OUT}	—	-2.25	—	
V_{IH}	High-Level Input Voltage	FB	0.7V_{OUT}	—	V_{OUT}	—
V_{IL}	Low-Level Input Voltage	FB	BDV_{SS}	—	0.3V_{OUT}	—
I_{OH}	VB, VS Source Current	V_{OUT}=9V, V_{OH}=0.9V_{OUT}	-70	-90	—	mA
I_{OL}	VB, VS Sink Current	V_{OUT}=9V, V_{OH}=0.1V_{OUT}	70	90	—	mA
t_{PLH}	VB, VS Output Delay Time	C_{LOAD}=10nF, 2-pin buzzer mode	—	1	1.5	µs
t_{PHL}	VB, VS Output Delay Time	C_{LOAD}=10nF, 2-pin buzzer mode	—	1	1.5	µs

Power-on Reset Characteristics

Ta=-40°C~85°C

| Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	—	1	—	—	ms
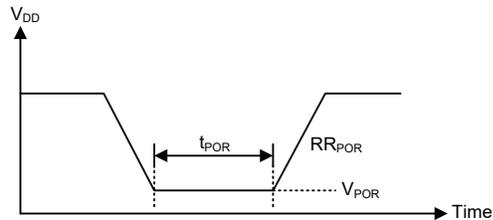
System Architecture

A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to their internal system architecture. The device takes advantage of the usual features found within RISC microcontrollers providing increased speed of operation and enhanced performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one or two cycles for most of the standard or extended instructions respectively. The exceptions to these are branch or call instructions which need one more cycle. An 8-bit wide ALU is used in practically all instruction set operations, which carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O and A/D control system with maximum reliability and flexibility. This makes the device suitable for affordable, high-volume production for controller applications.

Clocking and Pipelining

The main system clock, derived from either an HIRC, LXT or LIRC oscillator is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.

For instructions involving branches, such as jump or call instructions, two machine cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing sensitive applications.
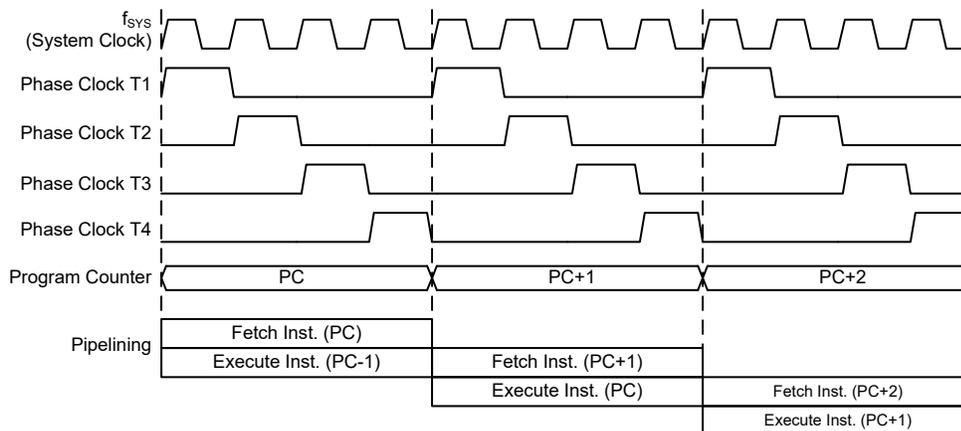
System Clocking and Pipelining

1	MOV A,[12H]	
2	CALL DELAY	
3	CPL [12H]	
4	:	
5	:	
6	DELAY: NOP	
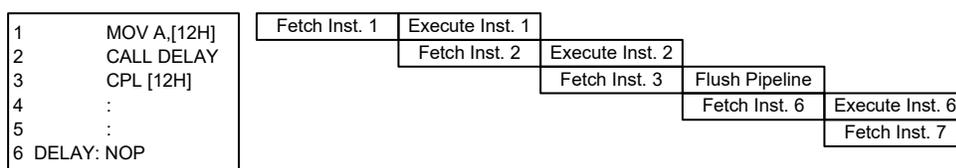
Instruction Fetching

Program Counter

During program execution, the Program Counter is used to keep track of the address of the next instruction to be executed. It is automatically incremented by one each time an instruction is executed except for instructions, such as "JMP" or "CALL" that demands a jump to a non-consecutive Program Memory address. Only the lower 8 bits, known as the Program Counter Low Register, are directly addressable by the application program.

When executing instructions requiring jumps to non-consecutive addresses such as a jump instruction, a subroutine call, interrupt or reset, etc., the microcontroller manages program control by loading the required address into the Program Counter. For conditional skip instructions, once the condition has been met, the next instruction, which has already been fetched during the present instruction execution, is discarded and a dummy cycle takes its place while the correct instruction is obtained.

Program Counter	
High Byte	**Low Byte (PCL)**
PC11~PC8	PCL7~PCL0

Program Counter

The lower byte of the Program Counter, known as the Program Counter Low register or PCL, is available for program control and is a readable and writeable register. By transferring data directly into this register, a short program jump can be executed directly; however, as only this low byte is available for manipulation, the jumps are limited to the present page of memory that is 256 locations. When such program jumps are executed it should also be noted that a dummy cycle will be inserted. Manipulating the PCL register may cause program branching, so an extra cycle is needed to pre-fetch.

Program Counter Read Register

The Program Counter read register is a read only register for reading the program counter value which indicates the current program execution address. Read the low byte register first then the high byte register. Reading the low byte register, PCRL, will read the low byte data of the current program execution address, and place the high byte data of the program counter into the 8-bit PCRH buffer. Then reading the PCRH register will read the corresponding data from the 8-bit PCRH buffer.

The following example shows how to read the current program execution address. When the current program execution address is 123H, the steps to execute the instructions are as follows:

(1) MOV A, PCRL → the ACC value is 23H, and the PCRH value is 01H;

MOV A, PCRH → the ACC value is 01H.

(2) LMOV A, PCRL → the ACC value is 23H, and the PCRH value is 01H;

LMOV A, PCRH → the ACC value is 01H.
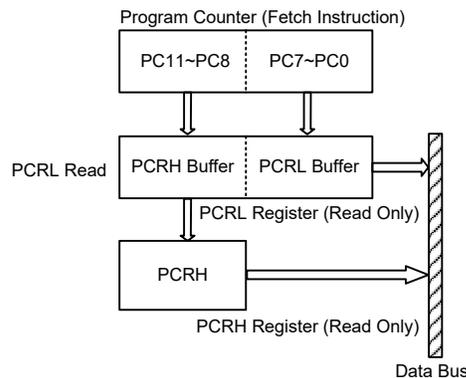
• **PCRL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0　　**D7~D0**: Low byte register bit 7 ~ bit 0

• **PCRH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	D11	D10	D9	D8
R/W	—	—	—	—	R	R	R	R
POR	—	—	—	—	0	0	0	0

Bit 7~4　　Unimplemented, read as "0"
Bit 3~0　　**D11~D8**: High byte register bit 3 ~ bit 0

Stack

This is a special part of the memory which is used to save the contents of the Program Counter only. The stack is organized into 8 levels and neither part of the data nor part of the program space, and is neither readable nor writeable. The activated level is indexed by the Stack Pointer, STKPTR, which is a read only register. At a subroutine call or interrupt acknowledge signal, the contents of the Program Counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled by a return instruction, RET or RETI, the Program Counter is restored to its previous value from the stack. After a device reset, the Stack Pointer will point to the top of the stack.

If the stack is full and an enabled interrupt takes place, the interrupt request flag will be recorded but the acknowledge signal will be inhibited. When the Stack Pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. However, when the stack is full, a CALL subroutine instruction can still be executed which will result in a stack overflow. Precautions should be taken to avoid such cases which might cause unpredictable program branching.

If the stack is overflow, the first Program Counter save in the stack will be lost.

• **STKPTR Register**

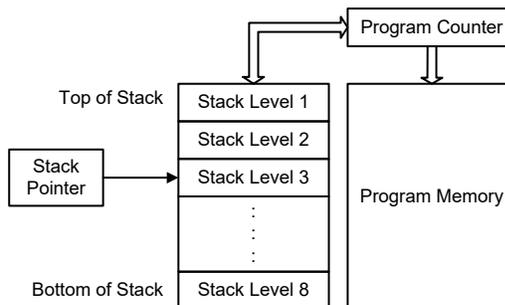| Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	D2	D1	D0
R/W	—	—	—	—	—	R	R	R
POR	—	—	—	—	—	0	0	0

Bit 7~3   Unimplemented, read as "0"

Bit 2~0   **D2~D0**: Stack pointer register bit 2 ~ bit 0

The following example shows how the Stack Pointer changes when program branching conditions occur.

(1) When the CALL subroutine instruction is executed 8 times continuously and the RET instruction is not executed during the period, the corresponding changes of the STKPTR are as follows:

00H→01H→02H→……→06H→07H→00H

(2) Then the RET instruction is executed 8 times continuously after (1), the corresponding changes of the STKPTR are as follows:

00H→07H→06H→……→02H→01H→00H

Arithmetic and Logic Unit – ALU

The arithmetic-logic unit or ALU is a critical area of the microcontroller that carries out arithmetic and logic operations of the instruction set. Connected to the main microcontroller data bus, the ALU receives related instruction codes and performs the required arithmetic or logical operations after which the result will be placed in the specified register. As these ALU calculation or operations may result in carry, borrow or other status changes, the status register will be correspondingly updated to reflect these changes. The ALU supports the following functions:

• Arithmetic operations:
ADD, ADDM, ADC, ADCM, SUB, SUBM, SBC, SBCM, DAA,

LADD, LADDM, LADC, LADCM, LSUB, LSUBM, LSBC, LSBCM, LDAA

• Logic operations:
AND, OR, XOR, ANDM, ORM, XORM, CPL, CPLA,
LAND, LOR, LXOR, LANDM, LORM, LXORM, LCPL, LCPLA

- Rotation:

  RRA, RR, RRCA, RRC, RLA, RL, RLCA, RLC,

  LRR, LRRA, LRRCA, LRRC, LRLA, LRL, LRLCA, LRLC

- Increment and Decrement:

  INCA, INC, DECA, DEC,

  LINCA, LINC, LDECA, LDEC

- Branch decision:

  JMP, SZ, SZA, SNZ, SIZ, SDZ, SIZA, SDZA, CALL, RET, RETI,

  LSZ, LSZA, LSNZ, LSIZ, LSDZ, LSIZA, LSDZA

Flash Program Memory

The Program Memory is the location where the user code or program is stored. For the device the Program Memory is Flash type, which means it can be programmed and re-programmed a large number of times, allowing the user the convenience of code modification on the same device. By using the appropriate programming tools, the Flash device offers users the flexibility to conveniently debug and develop their applications while also offering a means of field programming and updating.

Structure

The Program Memory has a capacity of 4K×16 bits. The Program Memory is addressed by the Program Counter and also contains data, table information and interrupt entries. Table data, which can be setup in any location within the Program Memory, is addressed by a separate table pointer register.
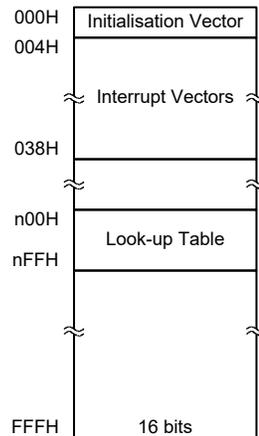
Program Memory Structure

Special Vectors

Within the Program Memory, certain locations are reserved for the reset and interrupts. The location 0000H is reserved for use by the device reset for program initialisation. After a device reset is initiated, the program will jump to this location and begin execution.

Look-up Table

Any location within the Program Memory can be defined as a look-up table where programmers can store fixed data. To use the look-up table, the table pointer must first be setup by placing the address of the look up data to be retrieved in the table pointer registers, TBLP and TBHP. These registers define the total address of the look-up table.

After setting up the table pointer, the table data can be retrieved from the Program Memory using the corresponding table read instruction such as "TABRD [m]" or "TABRDL [m]" respectively when the memory [m] is located in Sector 0. If the memory [m] is located in other sectors, the data can be retrieved from the program memory using the corresponding extended table read instruction such as "LTABRD [m]" or "LTABRDL [m]" respectively. When the instruction is executed, the lower order table byte from the Program Memory will be transferred to the user defined Data Memory register [m] as specified in the instruction. The higher order table data byte from the Program Memory will be transferred to the TBLH special register.

The accompanying diagram illustrates the addressing data flow of the look-up table.
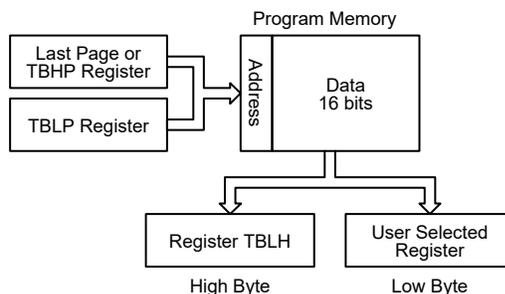
Table Program Example

The following example shows how the table pointer and table data is defined and retrieved from the microcontroller. This example uses raw table data located in the Program Memory which is stored there using the ORG statement. The value at this ORG statement is "0F00H" which refers to the start address of the last page within the 4K Program Memory of the device. The table pointer low byte register is setup here to have an initial value of "06H". This will ensure that the first data read from the data table will be at the Program Memory address "0F06H" or 6 locations after the start of the last page. Note that the value for the table pointer is referenced to the specific address specified by TBLP and TBHP if the "TABRD [m]" or "LTABRD [m]" instruction is being used. The high byte of the table data which in this case is equal to zero will be transferred to the TBLH register automatically when the "TABRD [m]" or "LTABRD [m]" instruction is executed.

Because the TBLH register is a read/write register and can be restored, care should be taken to ensure its protection if both the main routine and Interrupt Service Routine use table read instructions. If using the table read instructions, the Interrupt Service Routines may change the value of the TBLH and subsequently cause errors if used again by the main routine. As a rule, it is recommended that simultaneous use of the table read instructions should be avoided. However, in situations where simultaneous use cannot be avoided, the interrupts should be disabled prior to the execution of any main routine table-read instructions. Note that all table related instructions require two instruction cycles to complete their operation.

Table Read Program Example

```
tempreg1 db ?      ; temporary register #1
tempreg2 db ?      ; temporary register #2
:
:
mov a,06h          ; initialise low table pointer - note that this address is
                   ; referenced
mov tblp,a         ; to the last page or the page that tbhp pointed
mov a,0Fh          ; initialise high table pointer
mov tbhp,a
:
:
tabrd tempreg1     ; transfers value in table referenced by table pointer data at
                   ; program memory address "0F06H" transferred to tempreg1 and TBLH
dec tblp           ; reduce value of table pointer by one
tabrd tempreg2     ; transfers value in table referenced by table pointer data at
                   ; program memory address "0F05H" transferred to tempreg2 and TBLH
                   ; in this example the data "1AH" is transferred to tempreg1 and
                   ; data "0FH" to register tempreg2
:
:
org 0F00h          ; sets initial address of program memory
dc 00Ah, 00Bh, 00Ch, 00Dh, 00Eh, 00Fh, 01Ah, 01Bh
:
:
```

In Circuit Programming – ICP

The provision of Flash Type Program Memory provides the user with a means of convenient and easy upgrades and modifications to their programs on the same device. As an additional convenience, a means of programming the microcontroller in-circuit has provided using a 4-pin interface. This provides manufacturers with the possibility of manufacturing their circuit boards complete with a programmed or un-programmed microcontroller, and then programming or upgrading the program at a later stage. This enables product manufacturers to easily keep their manufactured products supplied with the latest program releases without removal and re-insertion of the device.

The Holtek Flash MCU to Writer Programming Pin correspondence table is as follows:

Holtek Writer Pins	MCU Programming Pins	Pin Description
ICPDA	PA0	Programming Serial Data/Address
ICPCK	PA2	Programming Clock
VDD	VDD	Power Supply
VSS	VSS	Ground

The Program Memory can be programmed serially in-circuit using this 4-wire interface. Data is downloaded and uploaded serially on a single pin with an additional line for the clock. Two additional lines are required for the power supply. The technical details regarding the in-circuit programming of the device is beyond the scope of this document and will be supplied in supplementary literature.

During the programming process, taking control of the ICPDA and ICPCK pins for data and clock programming purposes. The user must there take care to ensure that no other outputs are connected to these two pins.
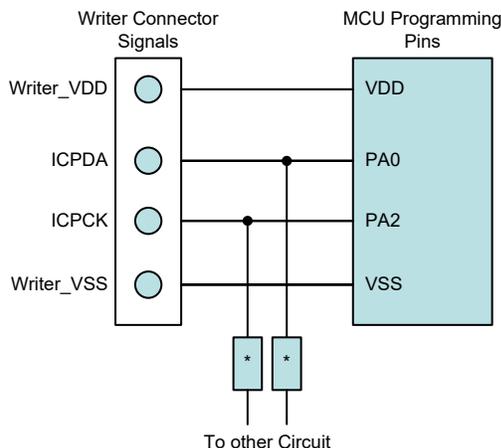
Note: * may be resistor or capacitor. The resistance of * must be greater than 1kΩ or the capacitance
of * must be less than 1nF.

On Chip Debug Support – OCDS

An EV chip exists for the purposes of device emulation. This EV chip device also provides an "On-Chip Debug" function to debug the real MCU device during the development process. The EV chip and the real MCU device are almost functionally compatible except for "On-Chip Debug" function. Users can use the EV chip device to emulate the real chip device behavior by connecting the OCDSDA and OCDSCK pins to the Holtek HT-IDE development tools. The OCDSDA pin is the OCDS Data/Address input/output pin while the OCDSCK pin is the OCDS clock input pin. When users use the EV chip for debugging, other functions which are shared with the OCDSDA and OCDSCK pins in the device will have no effect in the EV chip. However, the two OCDS pins which are pin-shared with the ICP programming pins are still used as the Flash Memory programming pins for ICP. For more detailed OCDS information, refer to the corresponding document named "Holtek e-Link for 8-bit MCU OCDS User's Guide".

Holtek e-Link Pins	EV Chip Pins	Pin Description
OCDSDA	OCDSDA	On-Chip Debug Support Data/Address input/output
OCDSCK	OCDSCK	On-Chip Debug Support Clock input
VDD	VDD	Power Supply
VSS	VSS	Ground

Data Memory

The Data Memory is a volatile area of 8-bit wide RAM internal memory and is the location where temporary information is stored.

Categorized into two types, the first of these is an area of RAM where special function registers are located. These registers have fixed locations and are necessary for correct operation of the device. Many of these registers can be read from and written to directly under program control, however, some remain protected from user manipulation. The second area of Data Memory is reserved for general purpose use. All locations within this area are read and write accessible under program control.

Switching between the different Data Memory sectors is achieved by properly setting the Memory Pointers to correct value when using the indirect addressing method.

Structure

The Data Memory is subdivided into several sectors, all of which are implemented in 8-bit wide RAM. Each of the Data Memory Sector is categorized into two types, the special Purpose Data Memory and the General Purpose Data Memory. The address range of the Special Purpose Data Memory for the device is from 00H to 7FH while the General Purpose Data Memory address range is from 80H to FFH.

Special Purpose Data Memory	General Purpose Data Memory	
Located Sectors	Capacity	Sector: Address
0: 00H~7FH 1: 40H (EEC only)	256×8	0: 80H~FFH 1: 80H~FFH

Data Memory Structure
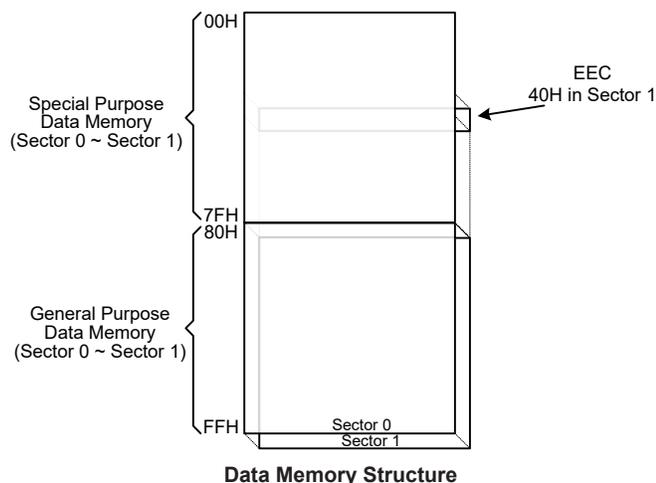
Data Memory Addressing

For the device that supports the extended instructions, there is no Bank Pointer for Data Memory addressing. The desired Sector is pointed by the MP1H or MP2H register and the certain Data Memory address in the selected sector is specified by the MP1L or MP2L register when using indirect addressing access.

Direct Addressing can be used in all sectors using the corresponding instruction which can address all available data memory space. For the accessed data memory which is located in any data memory sectors except Sector 0, the extended instructions can be used to access the data memory instead of using the indirect addressing access. The main difference between standard instructions and extended instructions is that the data memory address "m" in the extended instructions has 9 valid bits, the high byte indicates a sector and the low byte indicates a specific address within the sector.

General Purpose Data Memory

All microcontroller programs require an area of read/write memory where temporary data can be stored and retrieved for use later. It is this area of RAM memory that is known as General Purpose Data Memory. This area of Data Memory is fully accessible by the user programing for both reading and writing operations. By using the bit operation instructions individual bits can be set or reset under program control giving the user a large range of flexibility for bit manipulation in the Data Memory.

Special Purpose Data Memory

This area of Data Memory is where registers, necessary for the correct operation of the microcontroller, are stored. Most of the registers are both readable and writeable but some are protected and are readable only, the details of which are located under the relevant Special Function Register section. Note that for locations that are unused, any read instruction to these addresses will return the value "00H".

	Sector 0	Sector 1
00H	IAR0	
01H	MP0	
02H	IAR1	
03H	MP1L	
04H	MP1H	
05H	ACC	
06H	PCL	
07H	TBLP	
08H	TBLH	
09H	TBHP	
0AH	STATUS	
0BH	VBGRC	
0CH	IAR2	
0DH	MP2L	
0EH	MP2H	
0FH	RSTFC	
10H	TB0C	
11H	TB1C	
12H	SCC	
13H	HIRCC	
14H	PA	
15H	PAC	
16H	PAPU	
17H	PAWU	
18H	PB	
19H	PBC	
1AH	PBPU	
1BH	SLEDC	
1CH	LXTC	
1DH	PSCR	
1EH	LVDC	
1FH	TLVRC	
20H	SDSW0	
21H	SDSW1	
22H	SDPGAC0	
23H	SDPGAC1	
24H	SDA0C	
25H	SDA0VOS	
26H	SDA1C	
27H	SDA1VOS	
28H	STMC0	
29H	STMC1	
2AH	STMDL	
2BH	STMDH	
2CH	STMAL	
2DH	STMAH	
2EH	ORMC	
2FH	PLTSW	
30H	PLTDACC	
31H	PLTDA0L	
32H	PLTDA1L	
33H	PLTDA2L	
34H	PLTC0C	
35H	PLTC0VOS	
36H	PLTC1C	
37H	PLTC1VOS	
38H	PLTCHYC	
39H	PLTAC	
3AH	PLTAVOS	
3BH	PLTDICC1	
3CH	PLTDICC0	
3DH	WDTC	
3EH	EEA	
3FH	EED	

	Sector 0	Sector 1
40H		EEC
41H	PCRL	
42H	PCRH	
43H	CRCCR	
44H	CRCIN	
45H	CRCDL	
46H	CRCDH	
47H	INTEG	
48H	INTC0	
49H	INTC1	
4AH	INTC2	
4BH	INTC3	
4CH	PAS0	
4DH	PAS1	
4EH	PBS0	
4FH	PBS1	
50H	IFS0	
51H	IFS1	
52H	PTMC0	
53H	PTMC1	
54H	PTMC2	
55H	PTMDL	
56H	PTMDH	
57H	PTMAL	
58H	PTMAH	
59H	PTMBL	
5AH	PTMBH	
5BH	PTMRPL	
5CH	PTMRPH	
5DH	ISGENC	
5EH	ISGDATA0	
5FH	ISGDATA1	
60H	SADC0	
61H	SADC1	
62H	SADC2	
63H	SADOL	
64H	SADOH	
65H		
66H		
67H		
68H		
69H	SIMC0	
6AH	SIMC1/UUCR1	
6BH	SIMD/UTXR_RXR	
6CH	SIMA/SIMC2/UUCR2	
6DH	UUCR3	
6EH	SIMTOC/UBRG	
6FH	UUSR	
70H	IECC	
71H	STKPTR	
72H		
73H		
74H		
75H		
76H		
77H		
78H		
79H		
7AH		
7BH		
7CH		
7DH		
7EH		
7FH		

▭ : Unused, read as 00H   ▨ : Reserved, cannot be changed

Special Purpose Data Memory Structure

Special Function Register Description

Most of the Special Function Register details will be described in the relevant functional sections however several registers require a separate description in this section.

Indirect Addressing Registers – IAR0, IAR1, IAR2

The Indirect Addressing Registers, IAR0, IAR1 and IAR2, although having their locations in normal RAM register space, do not actually physically exist as normal registers. The method of indirect addressing for RAM data manipulation uses these Indirect Addressing Registers and Memory Pointers, in contrast to direct memory addressing, where the actual memory address is specified. Actions on the IAR0, IAR1 and IAR2 registers will result in no actual read or write operation to these registers but rather to the memory location specified by their corresponding Memory Pointers, MP0, MP1L/MP1H or MP2L/MP2H. Acting as a pair, IAR0 and MP0 can together access data only from Sector 0 while the IAR1 register together with the MP1L/MP1H register pair and IAR2 register together with the MP2L/MP2H register pair can access data from any Data Memory Sector. As the Indirect Addressing Registers are not physically implemented, reading the Indirect Addressing Registers will return a result of "00H" and writing to the registers will result in no operation.

Memory Pointers – MP0, MP1L, MP1H, MP2L, MP2H

Five Memory Pointers, known as MP0, MP1L, MP1H, MP2L, MP2H, are provided. These Memory Pointers are physically implemented in the Data Memory and can be manipulated in the same way as normal registers providing a convenient way with which to address and track data. When any operation to the relevant Indirect Addressing Registers is carried out, the actual address that the microcontroller is directed to is the address specified by the related Memory Pointer. MP0, together with Indirect Addressing Register, IAR0, are used to access data from Sector 0, while MP1L/MP1H together with IAR1 and MP2L/MP2H together with IAR2 are used to access data from all sectors according to the corresponding MP1H or MP2H register. Direct Addressing can be used in all sectors using the corresponding instruction which can address all available data memory space.

The following example shows how to clear a section of four Data Memory locations already defined as locations adres1 to adres4.

Indirect Addressing Program Example 1

```
data .section ´data´
adres1  db ?
adres2  db ?
adres3  db ?
adres4  db ?
block   db ?
code .section at 0 ´code´
org 00h
start:
    mov a, 04h              ; setup size of block
    mov block, a
    mov a, offset adres1    ; Accumulator loaded with first RAM address
    mov mp0, a              ; setup memory pointer with first RAM address
loop:
    clr IAR0               ; clear the data at address defined by MP0
    inc mp0                ; increase memory pointer
    sdz block              ; check if last memory location has been cleared
    jmp loop
continue:
```

Indirect Addressing Program Example 2

```
data .section 'data'
adres1  db ?
adres2  db ?
adres3  db ?
adres4  db ?
block   db ?
code .section at 0 'code'
org 00h
start:
    mov a, 04h              ; setup size of block
    mov block, a
    mov a, 01h              ; setup the memory sector
    mov mp1h, a
    mov a, offset adres1    ; Accumulator loaded with first RAM address
    mov mp1l, a             ; setup memory pointer with first RAM address
loop:
    clr IAR1               ; clear the data at address defined by MP1L
    inc mp1l              ; increase memory pointer MP1L
    sdz block             ; check if last memory location has been cleared
    jmp loop
continue:
```

The important point to note here is that in the example shown above, no reference is made to specific Data Memory addresses.

Direct Addressing Program Example using extended instructions

```
data .section 'data'
temp db ?
code .section at 0 'code'
org 00h
start:
    lmov a, [m]           ; move [m] data to acc
    lsub a, [m+1]         ; compare [m] and [m+1] data
    snz  c                ; [m]>[m+1]?
    jmp  continue         ; no
    lmov a, [m]           ; yes, exchange [m] and [m+1] data
    mov  temp, a
    lmov a, [m+1]
    lmov [m], a
    mov  a, temp
    lmov [m+1], a
continue:
```

Note: Here "m" is a data memory address located in any data memory sectors. For example, m=1F0H, it indicates address 0F0H in Sector 1.

Accumulator – ACC

The Accumulator is central to the operation of any microcontroller and is closely related with operations carried out by the ALU. The Accumulator is the place where all intermediate results from the ALU are stored. Without the Accumulator it would be necessary to write the result of each calculation or logical operation such as addition, subtraction, shift, etc., to the Data Memory resulting in higher programming and timing overheads. Data transfer operations usually involve the temporary storage function of the Accumulator; for example, when transferring data between one user-defined register and another, it is necessary to do this by passing the data through the Accumulator as no direct transfer between two registers is permitted.

Program Counter Low Byte Register – PCL

To provide additional program control functions, the low byte of the Program Counter is made accessible to programmers by locating it within the Special Purpose area of the Data Memory. By manipulating this register, direct jumps to other program locations are easily implemented. Loading a value directly into this PCL register will cause a jump to the specified Program Memory location, however, as the register is only 8-bit wide, only jumps within the current Program Memory page are permitted. When such operations are used, note that a dummy cycle will be inserted.

Look-up Table Registers – TBLP, TBHP, TBLH

These three special function registers are used to control operation of the look-up table which is stored in the Program Memory. TBLP and TBHP are the table pointers and indicate the location where the table data is located. Their value must be setup before any table read commands are executed. Their value can be changed, for example using the "INC" or "DEC" instructions, allowing for easy table data pointing and reading. TBLH is the location where the high order byte of the table data is stored after a table read data instruction has been executed. Note that the lower order table data byte is transferred to a user defined location.

Option Memory Mapping Register – ORMC

The ORMC register is used to enable Option Memory Mapping function. The Option Memory capacity is 64 words. When a specific pattern of 55H and AAH is consecutively written into this register, the Option Memory Mapping function will be enabled and then the Option Memory code can be read by using the table read instruction. The Option Memory addresses 00H~3FH will be mapped to Program Memory last page addresses C0H~FFH.

To successfully enable the Option Memory Mapping function, the specific pattern of 55H and AAH must be written into the ORMC register in two consecutive instruction cycles. It is therefore recommended that the global interrupt bit EMI should first be cleared before writing the specific pattern, and then set high again at a proper time according to users' requirements after the pattern is successfully written. An internal timer will be activated when the pattern is successfully written. The mapping operation will be automatically finished after a period of $4 \times t_{LIRC}$. Therefore, users should read the data in time, otherwise the Option Memory Mapping function needs to be restarted. After the completion of each consecutive write operation to the ORMC register, the timer will recount.

When the table read instructions are used to read the Option Memory code, both "TABRD [m]" and "TABRDL [m]" instructions can be used. However, care must be taken if the "TABRD [m]" instruction is used, the table pointer defined by the TBHP register must be referenced to the last page. Refer to corresponding sections about the table read instruction for more details.

• ORMC Register

Bit	7	6	5	4	3	2	1	0
Name	ORMC7	ORMC6	ORMC5	ORMC4	ORMC3	ORMC2	ORMC1	ORMC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **ORMC7~ORMC0**: Option Memory Mapping specific pattern
When a specific pattern of 55H and AAH is written into this register, the Option Mapping function will be enabled. Note lhat the register content will be cleared after the MCU is woke up from the IDEL/SLEEP mode.

Status Register – STATUS

This 8-bit register contains the SC flag, CZ flag, zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). These arithmetic/ logical operation and system management flags are used to record the status and operation of the microcontroller.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition, operations related to the status register may give different results due to the different instruction operations. The TO flag can be affected only by a system power-up, a WDT time-out or by executing the "CLR WDT" or "HALT" instruction. The PDF flag is affected only by executing the "HALT" or "CLR WDT" instruction or during a system power-up.

The Z, OV, AC, C, SC and CZ flags generally reflect the status of the latest operations.

- C is set if an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.

- AC is set if an operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.

- Z is set if the result of an arithmetic or logical operation is zero; otherwise Z is cleared.

- OV is set if an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.

- PDF is cleared by a system power-up or executing the "CLR WDT" instruction. PDF is set by executing the "HALT" instruction.

- TO is cleared by a system power-up or executing the "CLR WDT" or "HALT" instruction. TO is set by a WDT time-out.

- CZ is the operational result of different flags for different instructions. Refer to register definitions for more details.

- SC is the result of the "XOR" operation which is performed by the OV flag and the MSB of the current instruction operation result.

In addition, on entering an interrupt sequence or executing a subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status register are important and if the subroutine can corrupt the status register, precautions must be taken to correctly save it.

- **STATUS Register**

Bit	7	6	5	4	3	2	1	0
Name	SC	CZ	TO	PDF	OV	Z	AC	C
R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W
POR	x	x	0	0	x	x	x	x

"x": unknown

Bit 7   **SC**: The result of the "XOR" operation which is performed by the OV flag and the MSB of the instruction operation result

Bit 6   **CZ**: The operational result of different flags for different instructions

For SUB/SUBM/LSUB/LSUBM instructions, the CZ flag is equal to the Z flag.

For SBC/SBCM/LSBC/LSBCM instructions, the CZ flag is the "AND" operation result which is performed by the previous operation CZ flag and current operation zero flag.

For other instructions, the CZ flag will not be affected.

Bit 5   **TO**: Watchdog Time-out flag

         0: After power up or executing the "CLR WDT" or "HALT" instruction

         1: A watchdog time-out occurred.

Bit 4   **PDF**: Power down flag

         0: After power up or executing the "CLR WDT" instruction

         1: By executing the "HALT" instruction

Bit 3   **OV**: Overflow flag

         0: No overflow

         1: An operation results in a carry into the highest-order bit but not a carry out of the highest-order bit or vice versa

Bit 2   **Z**: Zero flag

         0: The result of an arithmetic or logical operation is not zero

         1: The result of an arithmetic or logical operation is zero

Bit 1   **AC**: Auxiliary flag

         0: No auxiliary carry

         1: An operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction

Bit 0   **C**: Carry flag

         0: No carry-out

         1: An operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation

     The "C" flag is also affected by a rotate through carry instruction.

EEPROM Data Memory

This device contains an area of internal EEPROM Data Memory. EEPROM is by its nature a non-volatile form of re-programmable memory, with data retention even when its power supply is removed. By incorporating this kind of data memory, a whole new host of application possibilities are made available to the designer. The availability of EEPROM storage allows information such as product identification numbers, calibration values, specific user data, system setup data or other product information to be stored directly within the product microcontroller. The process of reading and writing data to the EEPROM memory has been reduced to a very trivial affair.

EEPROM Data Memory Structure

The EEPROM Data Memory capacity is 64×8 bits for the device. Unlike the Program Memory and RAM Data Memory, the EEPROM Data Memory is not directly mapped into memory space and is therefore not directly addressable in the same way as the other types of memory. Read and Write operations to the EEPROM are carried out in single byte operations using an address register and a data register in Sector 0 and a single control register in Sector 1.

EEPROM Registers

Three registers control the overall operation of the internal EEPROM Data Memory. These are the address register, EEA, the data register, EED and a single control register, EEC. As both the EEA and EED registers are located in Sector 0, they can be directly accessed in the same way as any other Special Function Register. The EEC register however, being located in Sector 1, can only be read from or written to indirectly using the MP1L/MP1H or MP2L/MP2H Memory Pointer pairs and Indirect Addressing Register, IAR1/IAR2. Because the EEC control register is located at address 40H in Sector 1, the MP1L or MP2L Memory Pointer must first be set to the value 40H and the MP1H or MP2H Memory Pointer high byte set to the value, 01H, before any operations on the EEC register are executed.

Register	Bit							
Name	7	6	5	4	3	2	1	0
EEA	—	—	EEA5	EEA4	EEA3	EEA2	EEA1	EEA0
EED	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0
EEC	—	—	—	—	WREN	WR	RDEN	RD

EEPROM Register List

• **EEA Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	EEA5	EEA4	EEA3	EEA2	EEA1	EEA0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6   Unimplemented, read as "0"

Bit 5~0   **EEA5~EEA0**: Data EEPROM address bit 5 ~ bit 0

• **EED Register**

Bit	7	6	5	4	3	2	1	0
Name	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **EED7~EED0**: Data EEPROM data bit 7 ~ bit 0

• **EEC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	WREN	WR	RDEN	RD
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4   Unimplemented, read as "0"

Bit 3   **WREN**: Data EEPROM Write Enable
        0: Disable
        1: Enable

        This is the Data EEPROM Write Enable Bit which must be set high before Data EEPROM write operations are carried out. Clearing this bit to zero will inhibit Data EEPROM write operations.

Bit 2   **WR**: EEPROM Write Control
        0: Write cycle has finished
        1: Activate a write cycle

        This is the Data EEPROM Write Control Bit and when set high by the application program will activate a write cycle. This bit will be automatically reset to zero by the hardware after the write cycle has finished. Setting this bit high will have no effect if the WREN has not first been set high.

Bit 1   **RDEN**: Data EEPROM Read Enable
        0: Disable
        1: Enable

        This is the Data EEPROM Read Enable Bit which must be set high before Data EEPROM read operations are carried out. Clearing this bit to zero will inhibit Data EEPROM read operations.

Bit 0   **RD**: EEPROM Read Control
        0: Read cycle has finished
        1: Activate a read cycle

This is the Data EEPROM Read Control Bit and when set high by the application program will activate a read cycle. This bit will be automatically reset to zero by the hardware after the read cycle has finished. Setting this bit high will have no effect if the RDEN has not first been set high.

Note: 1. The WREN, WR, RDEN and RD cannot be set high at the same time in one instruction. The WR and RD cannot be set high at the same time.

2. Ensure that the f_{SUB} clock is stable before executing the write operation.

3. Ensure that the write operation is totally complete before changing the contents of the EEPROM related registers.

Reading Data from the EEPROM

To read data from the EEPROM, the EEPROM address of the data to be read must first be placed in the EEA register. Then the read enable bit, RDEN, in the EEC register must be set high to enable the read function. If the RD bit in the EEC register is now set high, a read cycle will be initiated. Setting the RD bit high will not initiate a read operation if the RDEN bit has not been set. When the read cycle terminates, the RD bit will be automatically cleared to zero, after which the data can be read from the EED register. The data will remain in the EED register until another read or write operation is executed. The application program can poll the RD bit to determine when the data is valid for reading.

Writing Data to the EEPROM

To write data to the EEPROM, the EEPROM address of the data to be written must first be placed in the EEA register and the data placed in the EED register. To initiate a write cycle, the write enable bit, WREN, in the EEC register must first be set high to enable the write function. After this, the WR bit in the EEC register must be immediately set high to initiate a write cycle. These two instructions must be executed in two consecutive instruction cycles. The global interrupt bit EMI should also first be cleared before implementing any write operations, and then set again after the write cycle has started. Note that setting the WR bit high will not initiate a write cycle if the WREN bit has not been set. As the EEPROM write cycle is controlled using an internal timer whose operation is asynchronous to microcontroller system clock, a certain time will elapse before the data will have been written into the EEPROM. Detecting when the write cycle has finished can be implemented either by polling the WR bit in the EEC register or by using the EEPROM interrupt. When the write cycle terminates, the WR bit will be automatically cleared to zero by the microcontroller, informing the user that the data has been written to the EEPROM. The application program can therefore poll the WR bit to determine when the write cycle has ended.

Write Protection

Protection against inadvertent write operation is provided in several ways. After the device is powered-on the Write Enable bit in the control register will be cleared preventing any write operations. Also at power-on the Memory Pointer high byte register, MP1H or MP2H, will be reset to zero, which means that Data Memory Sector 0 will be selected. As the EEPROM control register is located in Sector 1, this adds a further measure of protection against spurious write operations. During normal program operation, ensuring that the Write Enable bit in the control register is cleared will safeguard against incorrect write operations.

EEPROM Interrupt

The EEPROM write interrupt is generated when an EEPROM write cycle has ended. The EEPROM interrupt must first be enabled by setting the DEE bit in the relevant interrupt register. When an EEPROM write cycle ends, the DEF request flag will be set high. If the global and EEPROM interrupts are enabled and the stack is not full, a jump to the EEPROM interrupt vector will take place. When the interrupt is serviced, the EEPROM interrupt flag will be automatically reset. The

EMI bit will also automatically cleared to disable other interrupts. More details can be obtained in the Interrupt section.

Programming Considerations

Care must be taken that data is not inadvertently written to the EEPROM. Protection can be enhanced by ensuring that the Write Enable bit is normally cleared to zero when not writing. Also the Memory Pointer high byte register, MP1H or MP2H, could be normally cleared to zero as this would inhibit access to Sector 1 where the EEPROM control register exists. Although certainly not necessary, consideration might be given in the application program to the checking of the validity of new write data by a simple read back process.

When writing data, the WR bit must be set high immediately after the WREN bit has been set high, to ensure the write cycle executes correctly. The global interrupt bit EMI should also be cleared before a write cycle is executed and then set high again after a valid write activation procedure has completed. Note that the device should not enter the IDLE or SLEEP mode until the EEPROM read or write operation is totally complete. Otherwise, the EEPROM read or write operation will fail.

Programming Examples

Reading data from the EEPROM – Polling Method

```
MOV A, EEPROM_ADRES        ; user defined address
MOV EEA, A
MOV A, 040H                ; setup memory pointer MP1L
MOV MP1L, A                ; MP1L points to EEC register
MOV A, 01H                 ; setup memory pointer MP1H
MOV MP1H, A
SET IAR1.1                 ; set RDEN bit, enable read operations
SET IAR1.0                 ; start Read Cycle - set RD bit
BACK:
SZ  IAR1.0                 ; check for read cycle end
JMP BACK
CLR IAR1                   ; disable EEPROM read if no more read operations are
                           ; required
CLR MP1H
MOV A, EED                 ; move read data to register
MOV READ_DATA, A
```

Note: For each read operation, the address register should be re-specified followed by setting the RD bit high to activate a read cycle even if the target address is consecutive.

Writing Data to the EEPROM – Polling Method

```
MOV A, EEPROM_ADRES        ; user defined address
MOV EEA, A
MOV A, EEPROM_DATA         ; user defined data
MOV EED, A
MOV A, 040H                ; setup memory pointer MP1L
MOV MP1L, A                ; MP1L points to EEC register
MOV A, 01H                 ; setup memory pointer MP1H
MOV MP1H, A
CLR EMI
SET IAR1.3                 ; set WREN bit, enable write operations
SET IAR1.2                 ; start Write Cycle - set WR bit – executed immediately
                           ; after setting WREN bit
SET EMI
BACK:
SZ  IAR1.2                 ; check for write cycle end
JMP BACK
CLR MP1H
```

Oscillators

Various oscillator options offer the user a wide range of functions according to their various application requirements. The flexible features of the oscillator functions ensure that the best optimisation can be achieved in terms of speed and power saving. Oscillator operations are selected through the combination of configuration options and relevant control registers.

Oscillator Overview

In addition to being the source of the main system clock, the oscillators also provide clock sources for the Watchdog Timer and Time Base Interrupts. External oscillator requiring some external components as well as fully integrated internal oscillators, requiring no external components, are provided to form a wide range of both fast and slow system oscillators. The higher frequency oscillator provides higher performance but carry with it the disadvantage of higher power requirements, while the opposite is of course true for the lower frequency oscillators. With the capability of dynamically switching between fast and slow system clock, the device has the flexibility to optimize the performance/power ratio, a feature especially important in power sensitive portable applications.

Type	Name	Frequency	Pins
Internal High Speed RC	HIRC	2/4/8MHz	—
Internal Low Speed RC	LIRC	32.768kHz	—
External Low Speed Crystal	LXT	32.768kHz	XT1/XT2

Oscillator Types

System Clock Configurations

There are three oscillator sources, a high speed oscillator and two low speed oscillators. The high speed system clock is sourced from the internal 2/4/8MHz RC oscillator, HIRC. The low speed oscillators are the internal 32.768kHz RC oscillator, LIRC, and the external 32.768kHz crystal oscillator, LXT. Selecting whether the low or high speed oscillator is used as the system oscillator is implemented using the CKS2~CKS0 bits in the SCC register and as the system clock can be dynamically selected.

The actual source clock used for the low speed oscillator is chosen via the FSS bit in the SCC register. The frequency of the slow speed or high speed system clock is determined using the CKS2~CKS0 bits in the SCC register. Note that two oscillator selections must be made namely one high speed and one low speed system oscillators.

System Clock Configurations
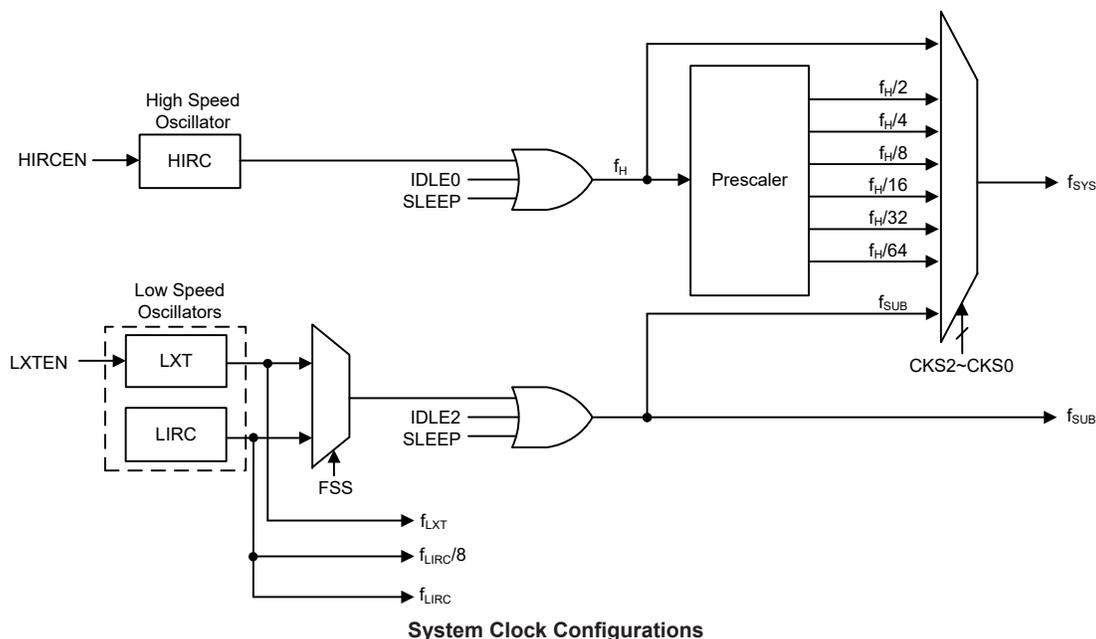
Internal High Speed RC Oscillator – HIRC

The high speed internal RC oscillator is a fully integrated system oscillator requiring no external components. The internal RC oscillator has three fixed frequencies of 2MHz, 4MHz and 8MHz, which are selected by HIRC1~HIRC0 bits in the HIRCC register. These bit must be setup to match the selected configuration option frequency to ensure that the HIRC frequency accuracy specified in the A.C. Characteristics is achieved. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised.

Internal 32.768kHz Oscillator – LIRC

The internal 32.768kHz System Oscillator is one of the low frequency oscillator choices, which is selected via a software control bit, FSS. It is a fully integrated RC oscillator with a typical frequency of 32.768kHz, requiring no external components for its implementation. In addition of supplying f_{LIRC} with the frequency of 32.768kHz, the clock source provides a divided version of $f_{LIRC}/8$ for the Watchdog Timer function. Device trimming during the manufacturing process and the inclusion of internal frequency compensation circuits are used to ensure that the influence of the power supply voltage, temperature and process variations on the oscillation frequency are minimised.

Exyernal 32.768kHz Crystal Oscillator – LXT

The external 32.768kHz crystal system oscillator is one of the low frequency oscillator choices, which is selected via a software control bit, FSS. This clock source has a fixed frequency of 32.768kHz and requires a 32.768kHz crystal to be connected between pins XT1 and XT2. The external resistor and capacitor components connected to the 32.768kHz crystal are necessary to provide oscillation. For applications where precise frequencies are essential, these components may be required to provide frequency compensation due to different crystal manufacturing tolerances. After the LXT oscillator is enabled by setting the LXTEN bit to 1, there is a time delay associated with the LXT oscillator waiting for it to start-up.

When the microcontroller enters the SLEEP or IDLE Mode, the system clock is switched off to stop microcontroller activity and to conserve power. However, in many microcontroller applications it may be necessary to keep the internal timers operational even when the microcontroller is in the SLEEP or IDLE Mode. To do this, another clock, independent of the system clock, must be provided.

However, for some crystals, to ensure oscillation and accurate frequency generation, it is necessary to add two small value external capacitors, C1 and C2. The exact values of C1 and C2 should be selected in consultation with the crystal or resonator manufacturer's specification. The external parallel feedback resistor, R_P, is required.

The pin-shared software control bits determine if the XT1/XT2 pins are used for the LXT oscillator or as I/O or other pin-shared functional pins.

- If the LXT oscillator is not used for any clock source, the XT1/XT2 pins can be used as normal I/O or other pin-shared functional pins.

- If the LXT oscillator is used for any clock source, the 32.768kHz crystal should be connected to the XT1/XT2 pins.

For oscillator stability and to minimise the effects of noise and crosstalk, it is important to ensure that the crystal and any associated resistors and capacitors along with interconnecting lines are all located as close to the MCU as possible.
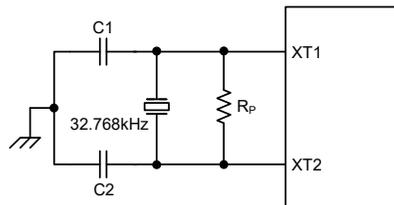
Note: 1. R_P, C1 and C2 are required.
2. Although not shown XT1/XT2 pins have a parasitic capacitance of around 7pF.

External LXT Oscillator

LXT Oscillator C1 and C2 Values		
Crystal Frequency	**C1**	**C2**
32.768kHz	10pF	10pF
Note: 1. C1 and C2 values are for guidance only. 2. R_P=5MΩ~10MΩ is recommended.		

32.768kHz Crystal Recommended Capacitor Values

LXT Oscillator Low Power Function

The LXT oscillator can function in one of two modes, the Speed Up Mode and the Low Power Mode. The mode selection is executed using the LXTSP bit in the register.

LXTSP	LXT Mode
0	Low Power
1	Speed Up

When the LXTSP bit is set to high, the LXT Speed Up Mode will be enabled. In the Speed Up Mode the LXT oscillator will power up and stabilise quickly. However, after the LXT oscillator has fully powered up, it can be placed into the Low Power Mode by clearing the LXTSP bit to zero and the oscillator will continue to run but with reduced current consumption. It is important to note that the LXT operating mode switching must be properly controlled before the LXT oscillator clock is selected as the system clock source. Once the LXT oscillator clock is selected as the system clock source using the CKS2~CKS0 bits and FSS bit in the SCC register, the LXT oscillator operating mode can not be changed.

It should be noted that, no matter what condition the LXTSP bit is set to, the LXT oscillator will always function normally, the only difference is that it will take more time to start up if it is in the Low-power mode.

Operating Modes and System Clocks

Present day applications require that their microcontrollers have high performance but often still demand that they consume as little power as possible, conflicting requirements that are especially true in battery powered portable applications. The fast clocks required for high performance will by their nature increase current consumption and of course vice versa, lower speed clocks reduce current consumption. As Holtek has provided the device with both high and low speed clock sources and the means to switch between them dynamically, the user can optimise the operation of their microcontroller to achieve the best performance/power ratio.

System Clocks

The device has many different clock sources for both the CPU and peripheral function operation. By providing the user with a wide range of clock options using register programming, a clock system can be configured to obtain maximum application performance.

The main system clock, can come from a high frequency, f_H, or low frequency, f_{SUB}, source, and is selected using the CKS2~CKS0 bits in the SCC register. The high speed system clock is sourced from the HIRC oscillator. The low speed system clock source can be sourced from the internal clock f_{SUB}. If f_{SUB} is selected then it can be sourced by either the LXT or LIRC oscillator, selected via configuring the FSS bit in the SCC register. The other choice, which is a divided version of the high speed system oscillator has a range of $f_H/2 \sim f_H/64$.
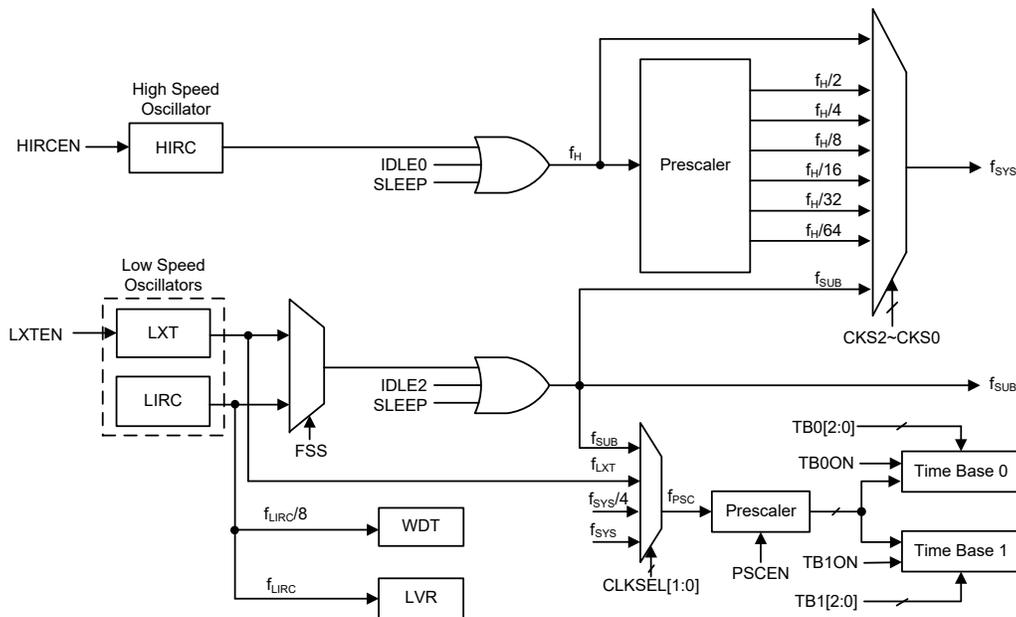
Device Clock Configurations

Note: When the system clock source f_{SYS} is switched to f_{SUB} from f_H, the high speed oscillator will stop to conserve the power or continue to oscillate to provide the clock source, $f_H \sim f_H/64$, for peripheral circuit to use, which is determined by configuring the corresponding high speed oscillator enable control bit.

System Operation Modes

There are six different modes of operation for the microcontroller, each one with its own special characteristics and which can be chosen according to the specific performance and power requirements of the application. There are two modes allowing normal operation of the microcontroller, the FAST Mode and SLOW Mode. The remaining four modes, the SLEEP, IDLE0, IDLE1 and IDLE2 Modes are used when the microcontroller CPU is switched off to conserve power.

Operation Mode	CPU	Register Setting			f_{SYS}	f_H	f_{SUB}	f_{LIRC}	$f_{LIRC}/8$
		FHIDEN	FSIDEN	CKS2~CKS0					
FAST	On	x	x	000~110	f_H~f_H/64	On	On	On	On
SLOW	On	x	x	111	f_{SUB}	On/Off [1]	On	On	On
IDLE0	Off	0	1	000~110	Off	Off	On	On	On
				111	On				
IDLE1	Off	1	1	xxx	On	On	On	On	On
IDLE2	Off	1	0	000~110	On	On	Off	On	On
				111	Off				
SLEEP	Off	0	0	xxx	Off	Off	Off	Off	On[2]

"x": Don't care

Note: 1. The f_H clock will be switched on or off by configuring the corresponding oscillator enable bit in the SLOW mode.
2. The $f_{LIRC}/8$ clock is always on as the WDT function is always enabled.

FAST Mode

This is one of the main operating modes where the microcontroller has all of its functions operational and where the system clock is provided by the high speed oscillator. This mode operates allowing the microcontroller to operate normally with a clock source come from the high speed oscillator, HIRC. The high speed oscillator will however first be divided by a ratio ranging from 1 to 64, the actual ratio being selected by the CKS2~CKS0 bits in the SCC register. Although a high speed oscillator is used, running the microcontroller at a divided clock ratio reduces the operating current.

SLOW Mode

This is also a mode where the microcontroller operates normally although now with a slower speed clock source. The clock source used will be from f_{SUB}. The f_{SUB} clock is derived from either the LIRC or LXT oscillator determined by the FSS bit in the SCC register.

SLEEP Mode

The SLEEP Mode is entered when a HALT instruction is executed and when the FHIDEN and FSIDEN bit both are low. In the SLEEP mode the CPU will be stopped. The f_{SUB} clock provided to the peripheral function will also be stopped. However, the $f_{LIRC}/8$ clock will continue to operate as the WDT function is always enabled.

IDLE0 Mode

The IDLE0 Mode is entered when a HALT instruction is executed and when the FHIDEN bit in the SCC register is low and the FSIDEN bit in the SCC register is high. In the IDLE0 Mode the CPU will be switched off but the low speed oscillator will be turned on to drive some peripheral functions.

IDLE1 Mode

The IDLE1 Mode is entered when a HALT instruction is executed and when the FHIDEN bit in the SCC register is high and the FSIDEN bit in the SCC register is high. In the IDLE1 Mode the CPU will be switched off but both the high and low speed oscillators will be turned on to provide a clock source to keep some peripheral functions operational.

IDLE2 Mode

The IDLE2 Mode is entered when a HALT instruction is executed and when the FHIDEN bit in the SCC register is high and the FSIDEN bit in the SCC register is low. In the IDLE2 Mode the CPU will be switched off but the high speed oscillator will be turned on to provide a clock source to keep some peripheral functions operational.

Control Registers

The registers, SCC, HIRCC and LXTC are used to control the system clock and the corresponding oscillator configurations.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SCC	CKS2	CKS1	CKS0	—	—	FSS	FHIDEN	FSIDEN
HIRCC	—	—	—	—	HIRC1	HIRC0	HIRCF	HIRCEN
LXTC	—	—	—	—	—	LXTSP	LXTF	LXTEN

System Operating Mode Control Register List

• **SCC Register**

Bit	7	6	5	4	3	2	1	0
Name	CKS2	CKS1	CKS0	—	—	FSS	FHIDEN	FSIDEN
R/W	R/W	R/W	R/W	—	—	R/W	R/W	R/W
POR	1	1	1	—	—	0	0	0

Bit 7~5   **CKS2~CKS0**: System clock selection
     000: f_H
     001: $f_H/2$
     010: $f_H/4$
     011: $f_H/8$
     100: $f_H/16$
     101: $f_H/32$
     110: $f_H/64$
     111: f_{SUB}
     These three bits are used to select which clock is used as the system clock source. In addition to the system clock source directly derived from f_H or f_{SUB}, a divided version of the high speed system oscillator can also be chosen as the system clock source.

Bit 4~3   Unimplemented, read as "0"

Bit 2   **FSS**: Low Frequency oscillator selection
     0: LIRC
     1: LXT

Bit 1   **FHIDEN**: High Frequency oscillator control when CPU is switched off
     0: Disable
     1: Enable
     This bit is used to control whether the high speed oscillator is activated or stopped when the CPU is switched off by executing a "HALT" instruction.

Bit 0   **FSIDEN**: Low Frequency oscillator control when CPU is switched off
     0: Disable
     1: Enable

This bit is used to control whether the low speed oscillator is activated or stopped when the CPU is switched off by executing a "HALT" instruction.

Note: A certain delay is required before the relevant clock is successfully switched to the target clock source after any clock switching setup using the CKS2~CKS0 bits or FSS bit. A proper delay time must be arranged before executing the following operations which require immediate reaction with the target clock source.

Clock switching delay time$=4\times t_{SYS}+[0\sim(1.5\times t_{Curr.}+0.5\times t_{Tar.})]$, where $t_{Curr.}$ indicates the current clock period, $t_{Tar.}$ indicates the target clock period and t_{SYS} indicates the current system clock period.

• **HIRCC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	HIRC1	HIRC0	HIRCF	HIRCEN
R/W	—	—	—	—	R/W	R/W	R	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4   Unimplemented, read as "0"

Bit 3~2   **HIRC1~HIRC0**: HIRC frequency selection
        00: 2MHz
        01: 4MHz
        10: 8MHz
        11: 2MHz

        When the HIRC oscillator is enabled or the HIRC frequency selection is changed by application program, the clock frequency will automatically be changed after the HIRCF flag is set high.

        It is recommended that the HIRC frequency selected by these two bits should be same with the frequency determined by the configuration option to achieve the HIRC frequency accuracy specified in the A.C. Characteristics.

Bit 1   **HIRCF**: HIRC oscillator stable flag
        0: HIRC unstable
        1: HIRC stable

        This bit is used to indicate whether the HIRC oscillator is stable or not. When the HIRCEN bit is set to 1 to enable the HIRC oscillator, the HIRCF bit will first be cleared to 0 and then set to 1 after the HIRC oscillator is stable.

Bit 0   **HIRCEN**: HIRC oscillator enable control
        0: Disable
        1: Enable

• **LXTC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	LXTSP	LXTF	LXTEN
R/W	—	—	—	—	—	R/W	R	R/W
POR	—	—	—	—	—	0	0	0

Bit 7~3   Unimplemented, read as "0"

Bit 2   **LXTSP**: LXT speed up control
        0: Disable – Low power
        1: Enable – Speed up

        This bit is used to control whether the LXT oscillator is operating in the low power or speed up mode. When the LXTSP bit is set high, the LXT oscillator will oscillate quickly but consume more power. If the LXTSP bit is cleared to zero, the LXT oscillator will consume less power but take longer time to stablise. It is important to note that this bit cannot be changed after the LXT oscillator is selected as the system clock source using the CKS2~CKS0 and FSS bits in the SCC register.

Bit 1   **LXTF**: LXT oscillator stable flag
        0: LXT unstable
        1: LXT stable
     This bit is used to indicate whether the LXT oscillator is stable or not. When the LXTEN bit is set to 1 to enable the LXT oscillator, the LXTF bit will first be cleared to 0 and then set to 1 after the LXT oscillator is stable.

Bit 0   **LXTEN**: LXT oscillator enable control
        0: Disable
        1: Enable
     When the LXTEN bit is set to 1, the LXT oscillator will be turned on and provides the clock source for Time Base.

Operating Mode Switching

The device can switch between operating modes dynamically allowing the user to select the best performance/power ratio for the present task in hand. In this way microcontroller operations that do not require high performance can be executed using slower clocks thus requiring less operating current and prolonging battery life in portable applications.

In simple terms, Mode Switching between the FAST Mode and SLOW Mode is executed using the CKS2~CKS0 bits in the SCC register while Mode Switching from the FAST/SLOW Modes to the SLEEP/IDLE Modes is executed via the HALT instruction. When a HALT instruction is executed, whether the device enters the IDLE Mode or the SLEEP Mode is determined by the condition of the FHIDEN and FSIDEN bits in the SCC register.
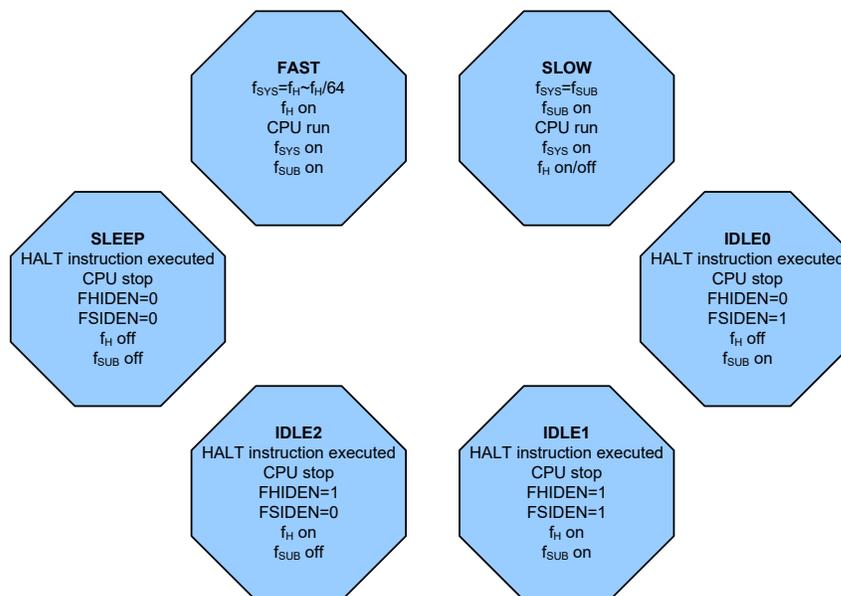
FAST Mode to SLOW Mode Switching

When running in the FAST Mode, which uses the high speed system oscillator, and therefore consumes more power, the system clock can switch to run in the SLOW Mode by setting the CKS2~CKS0 bits to "111" in the SCC register. This will then use the low speed system oscillator which will consume less power. Users may decide to do this for certain operations which do not require high performance and can subsequently reduce power consumption.

The SLOW Mode system clock is sourced from the LXT or LIRC oscillator determined by the FSS bit in the SCC register and therefore requires the selected oscillator to be stable before full mode switching occurs.

```
                                        ┌──────────────┐
                                        │  FAST Mode   │
                                        └──────────────┘

                            CKS2~CKS0=111
                                        ┌──────────────┐
                            ───────────▶│  SLOW Mode   │
                                        └──────────────┘

                  FHIDEN=0, FSIDEN=0
                  HALT instruction is executed
                                        ┌──────────────┐
                            ───────────▶│  SLEEP Mode  │
                                        └──────────────┘

            FHIDEN=0, FSIDEN=1
            HALT instruction is executed
                                        ┌──────────────┐
                            ───────────▶│  IDLE0 Mode  │
                                        └──────────────┘

      FHIDEN=1, FSIDEN=1
      HALT instruction is executed
                                        ┌──────────────┐
                            ───────────▶│  IDLE1 Mode  │
                                        └──────────────┘

FHIDEN=1, FSIDEN=0
HALT instruction is executed
                                        ┌──────────────┐
                            ───────────▶│  IDLE2 Mode  │
                                        └──────────────┘
```
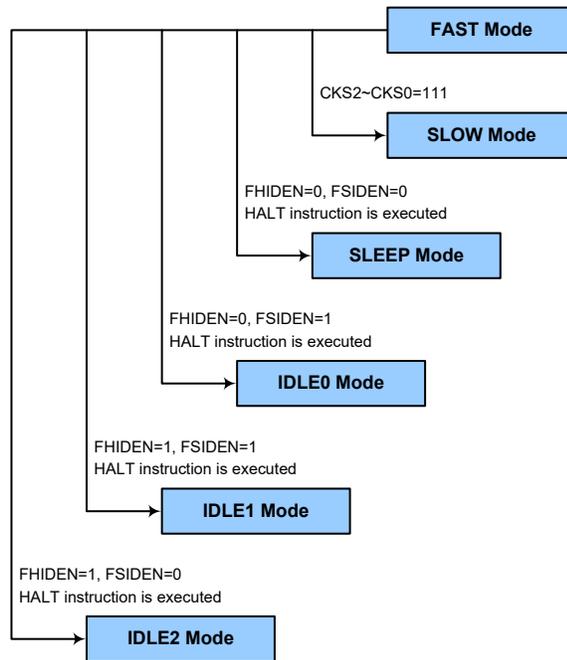
SLOW Mode to FAST Mode Switching

In SLOW mode the system clock is derived from f_{SUB}. When system clock is switched back to the FAST mode from f_{SUB}, the CKS2~CKS0 bits should be set to "000"~"110" and then the system clock will respectively be switched to f_H~$f_H/64$.

However, if f_H is not used in SLOW mode and thus switched off, it will take some time to re-oscillate and stabilise when switching to the FAST mode from the SLOW Mode. This is monitored using the HIRCF bit in the HIRCC register. The time duration required for the high speed system oscillator stabilization is specified in the System Start Up Time Characteristics.
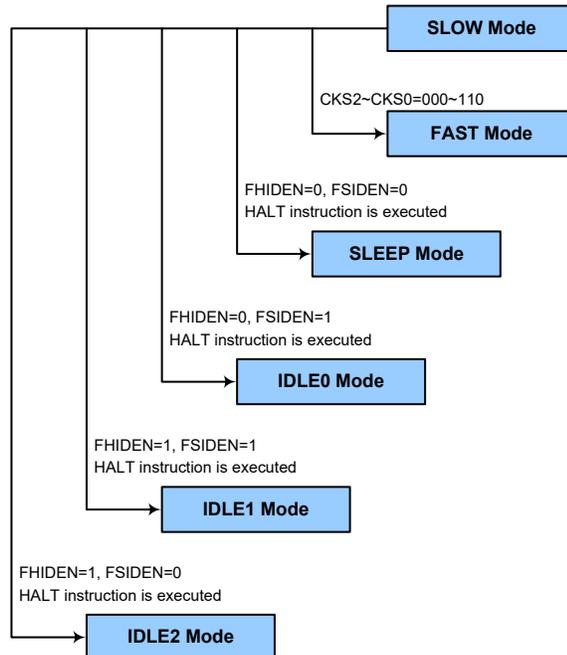
```
                                        ┌──────────────┐
                                        │  SLOW Mode   │
                                        └──────────────┘

                            CKS2~CKS0=000~110
                                        ┌──────────────┐
                            ───────────▶│  FAST Mode   │
                                        └──────────────┘

                  FHIDEN=0, FSIDEN=0
                  HALT instruction is executed
                                        ┌──────────────┐
                            ───────────▶│  SLEEP Mode  │
                                        └──────────────┘

            FHIDEN=0, FSIDEN=1
            HALT instruction is executed
                                        ┌──────────────┐
                            ───────────▶│  IDLE0 Mode  │
                                        └──────────────┘

      FHIDEN=1, FSIDEN=1
      HALT instruction is executed
                                        ┌──────────────┐
                            ───────────▶│  IDLE1 Mode  │
                                        └──────────────┘

FHIDEN=1, FSIDEN=0
HALT instruction is executed
                                        ┌──────────────┐
                            ───────────▶│  IDLE2 Mode  │
                                        └──────────────┘
```

Entering the SLEEP Mode

There is only one way for the device to enter the SLEEP Mode and that is to execute the "HALT" instruction in the application program with both the FHIDEN and FSIDEN bits in the SCC register equal to "0". In this mode all the clocks and functions will be switched off except the WDT function. When this instruction is executed under the conditions described above, the following will occur:

• The system clock will be stopped and the application program will stop at the "HALT" instruction.

• The Data Memory contents and registers will maintain their present condition.

• The I/O ports will maintain their present conditions.

• In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

• The WDT will be cleared and resume counting as the WDT function is always enabled.

Entering the IDLE0 Mode

There is only one way for the device to enter the IDLE0 Mode and that is to execute the "HALT" instruction in the application program with the FHIDEN bit in the SCC register equal to "0" and the FSIDEN bit in the SCC register equal to "1". When this instruction is executed under the conditions described above, the following will occur:

• The f_H clock will be stopped and the application program will stop at the "HALT" instruction, but the f_{SUB} clock will be on.

• The Data Memory contents and registers will maintain their present condition.

• The I/O ports will maintain their present conditions.

• In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

• The WDT will be cleared and resume counting as the WDT function is always enabled.

Entering the IDLE1 Mode

There is only one way for the device to enter the IDLE1 Mode and that is to execute the "HALT" instruction in the application program with both the FHIDEN and FSIDEN bits in the SCC register equal to "1". When this instruction is executed under the conditions described above, the following will occur:

• The f_H and f_{SUB} clocks will be on but the application program will stop at the "HALT" instruction.

• The Data Memory contents and registers will maintain their present condition.

• The I/O ports will maintain their present conditions.

• In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

• The WDT will be cleared and resume counting as the WDT function is always enabled.

Entering the IDLE2 Mode

There is only one way for the device to enter the IDLE2 Mode and that is to execute the "HALT" instruction in the application program with the FHIDEN bit in the SCC register equal to "1" and the FSIDEN bit in the SCC register equal to "0". When this instruction is executed under the conditions described above, the following will occur:

• The f_H clock will be on but the f_{SUB} clock will be off and the application program will stop at the "HALT" instruction.

• The Data Memory contents and registers will maintain their present condition.

- The I/O ports will maintain their present conditions.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.
- The WDT will be cleared and resume counting as the WDT function is always enabled.

Standby Current Considerations

As the main reason for entering the SLEEP or IDLE Mode is to keep the current consumption of the device to as low a value as possible, perhaps only in the order of several micro-amps in the IDLE1 and IDLE2 Mode, there are other considerations which must also be taken into account by the circuit designer if the power consumption is to be minimised. Special attention must be made to the I/O pins on the device. All high-impedance input pins must be connected to either a fixed high or low level as any floating input pins could create internal oscillations and result in increased current consumption. This also applies to the device which has different package types, as there may be unbonded pins. These pins must either be setup as outputs or if setup as inputs must have pull-high resistors connected.

Care must also be taken with the loads, which are connected to I/O pins, which are setup as outputs. These should be placed in a condition in which minimum current is drawn or connected only to external circuits that do not draw current, such as other CMOS inputs. Also note that additional standby current will also be required if the LIRC or LXT oscillator has been enabled.

In the IDLE1 and IDLE2 Mode the high speed oscillator is on, if the peripheral function clock source is derived from the high speed oscillator, the additional standby current will also be perhaps in the order of several hundred micro-amps.

Wake-up

To minimise power consumption the device can enter the SLEEP or any IDLE Mode, where the CPU will be switched off. However, when the device is woken up again, it will take a considerable time for the original system oscillator to restart, stabilise and allow normal operation to resume.

After the system enters the SLEEP or IDLE Mode, it can be woken up from one of various sources listed as follows:

- An external falling edge on Port A
- A system interrupt
- A WDT overflow

When the device executes the "HALT" instruction, it will enter the IDLE or SLEEP mode and the PDF flag will be set high. The PDF flag is cleared to 0 if the device experience a system power-up or executs the clear Watchdog Timer instruction. If the system is woken up by a WDT overflow, a Watchdog Timer Time-out reset will be initiated and the TO flag will be set to 1. The TO flag is set high if a WDT time-out occurs, and causes a wake-up that only resets the Program Counter and Stack Pointer, the other flags remain in their original status.

Each pin on Port A can be setup using the PAWU register to permit a negative transition on the pin to wake-up the system. When a pin wake-up occurs, the program will resume execution at the instruction following the "HALT" instruction. If the system is woken up by an interrupt, then two possible situations may occur. The first is where the related interrupt is disabled or the interrupt is enabled but the stack is full, in which case the program will resume execution at the instruction following the "HALT" instruction. In this situation, the interrupt which woke up the device will not be immediately serviced, but will rather be serviced later when the related interrupt is finally enabled or when a stack level becomes free. The other situation is where the related interrupt is enabled and the stack is not full, in which case the regular interrupt response takes place. If an interrupt request flag is set high before entering the SLEEP or IDLE Mode, the wake-up function of the related interrupt will be disabled.

Watchdog Timer

The Watchdog Timer is provided to prevent program malfunctions or sequences from jumping to unknown locations, due to certain uncontrollable external events such as electrical noise.

Watchdog Timer Clock Source

The Watchdog Timer clock source is provided by the internal clock, $f_{LIRC}/8$, which is sourced from the LIRC oscillator. The LIRC internal oscillator has an approximate frequency of 32.768kHz and this specified internal clock period can vary with V_{DD}, temperature and process variations. The Watchdog Timer source clock is then subdivided by a ratio of 2^8 to 2^{18} to give longer timeouts, the actual value being chosen using the WS2~WS0 bits in the WDTC register.

Watchdog Timer Control Register

A single register, WDTC, controls the required timeout period as well as the enable and reset MCU operation.

• WDTC Register

Bit	7	6	5	4	3	2	1	0
Name	WE4	WE3	WE2	WE1	WE0	WS2	WS1	WS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	0	1	0	0	1	1

Bit 7~3   **WE4~WE0**: WDT function software control
        10101 or 01010: Enable
        Other values: Reset MCU

When these bits are changed by the environmental noise or software setting to reset the microcontroller, the reset operation will be activated after a delay time, t_{SRESET} and the WRF bit in the RSTFC register will be set high.

Bit 2~0   **WS2~WS0**: WDT time-out period selection
        000: $2^8/f_{LIRC}$
        001: $2^{10}/f_{LIRC}$
        010: $2^{12}/f_{LIRC}$
        011: $2^{14}/f_{LIRC}$
        100: $2^{15}/f_{LIRC}$
        101: $2^{16}/f_{LIRC}$
        110: $2^{17}/f_{LIRC}$
        111: $2^{18}/f_{LIRC}$

These three bits determine the division ratio of the watchdog timer source clock, which in turn determines the time-out period.

• RSTFC Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	LVRF	—	WRF
R/W	—	—	—	—	—	R/W	—	R/W
POR	—	—	—	—	—	x	—	0

"x": unknown

Bit 7~3   Unimplemented, read as "0"
Bit 2   **LVRF**: LVR function reset flag
        Refer to the Low Voltage Reset section.
Bit 1   Unimplemented, read as "0"
Bit 0   **WRF**: WDTC register software reset flag
        0: Not occurred
        1: Occurred

This bit is set to 1 by the WDTC register software reset and cleared to zero by the application program. Note that this bit can be cleared to zero only by the application program.

Watchdog Timer Operation

The Watchdog Timer operates by providing a device reset when its timer overflows. This means that in the application program and during normal operation the user has to strategically clear the Watchdog Timer before it overflows to prevent the Watchdog Timer from executing a reset. This is done using the clear watchdog instruction. If the program malfunctions for whatever reason, jumps to an unknown location, or enters an endless loop, the clear instruction will not be executed in the correct manner, in which case the Watchdog Timer will overflow and reset the device. There are five bits, WE4~WE0, in the WDTC register to offer the enable and reset control of the Watchdog Timer. The WDT function will be enabled when the WE4~WE0 bits are equal to 10101B or 01010B. If the WE4~WE0 bits are set to any other values, other than 01010B and 10101B, it will reset the device after a delay time, t_{SRESET}. After power-on these bits will have a value of 01010B.

WE4~WE0 Bits	WDT Function
10101B or 01010B	Enable
Any other values	Reset MCU

Watchdog Timer Enable/Reset Control

Under normal program operation, a Watchdog Timer time-out will initialise a device reset and set the status bit TO high. However, if the system is in the SLEEP or IDLE Mode, when a Watchdog Timer time-out occurs, the TO bit in the status register will be set high and only the Program Counter and Stack Pointer will be reset. Three methods can be adopted to clear the contents of the Watchdog Timer. The first is a WDTC software reset, which means a certain value except 01010B and 10101B written into the WE4~WE0 bits, the second is using the Watchdog Timer software clear instruction and the third is via a HALT instruction.

There is only one method of using software instruction to clear the Watchdog Timer. That is to use the single "CLR WDT" instruction to clear the WDT.

The maximum time out period is when the 2^{18} division ratio is selected. As an example, with a 32.768kHz LIRC oscillator as its source clock, this will give a maximum watchdog period of around 8 seconds for the 2^{18} division ratio, and a minimum timeout of 8ms for the 2^8 division ration.

Watchdog Timer
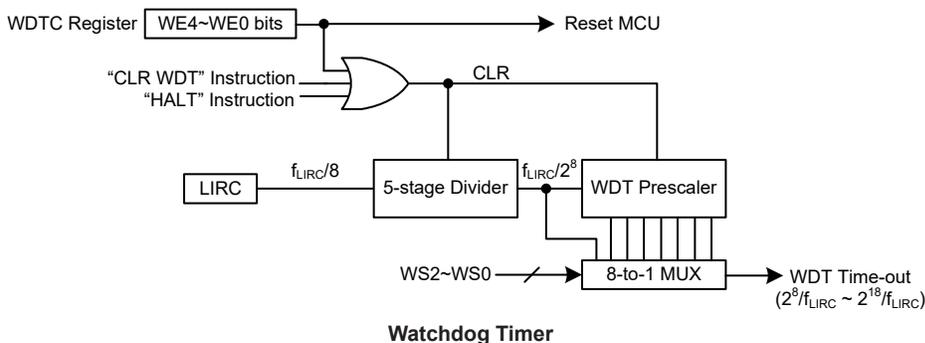
Reset and Initialisation

A reset function is a fundamental part of any microcontroller ensuring that the device can be set to some predetermined condition irrespective of outside parameters. The most important reset condition is after power is first applied to the microcontroller. In this case, internal circuitry will ensure that the microcontroller, after a short delay, will be in a well-defined state and ready to execute the first program instruction. After this power-on reset, certain important internal registers will be set to defined states before the program commences. One of these registers is the Program Counter, which will be reset to zero forcing the microcontroller to begin program execution from the lowest Program Memory address.

Another reset exists in the form of a Low Voltage Reset, LVR, where a full reset is implemented in situations where the power supply voltage falls below a certain threshold. Another type of reset is when the Watchdog Timer overflows and resets the microcontroller. All types of reset operations result in different register conditions being setup.

Reset Functions

There are several ways in which a microcontroller reset can occur, through events occurring internally.

Power-on Reset

The most fundamental and unavoidable reset is the one that occurs after power is first applied to the microcontroller. As well as ensuring that the Program Memory begins execution from the first memory address, a power-on reset also ensures that certain other registers are preset to known conditions. All the I/O port and port control registers will power up in a high condition ensuring that all pins will be first set to inputs.
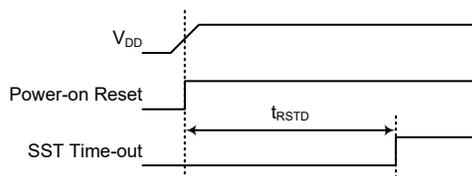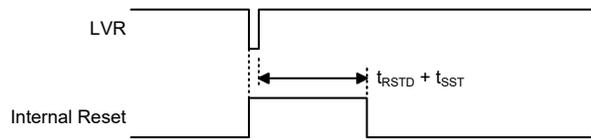

Power-on Reset Timing Chart

Low Voltage Reset – LVR

The microcontroller contains a low voltage reset circuit in order to monitor the supply voltage of the device and provide an MCU reset when the value falls below a certain predefined level.

The LVR function is always enabled in normal operation with a specific LVR voltage V_{LVR}. For the devices the V_{LVR} value is fixed at 2.1V. If the supply voltage of the devices drop to within a range of $0.9V \sim V_{LVR}$ such as might occur when changing the battery in battery powered applications, the LVR will automatically reset the devices internally and the LVRF bit in the RSTFC register will also be set to 1. For a valid LVR signal, a low supply voltage, i.e., a voltage in the range between $0.9V \sim V_{LVR}$ must exist for a time greater than that specified by t_{LVR} in the LVD & LVR Electrical Characteristics. If the low supply voltage state does not exceed this value, the LVR will ignore the low supply voltage and will not perform a reset function. The actual tLVR value can be selected by the TLVR1~TLVR0 bits in the TLVRC register.

Note that the LVR function will be automatically disabled when the device enters the SLEEP or IDLE mode.

Low Voltage Reset Timing Chart

- **TLVRC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	TLVR1	TLVR0
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	1

Bit 7~2   Unimplemented, read as "0"

Bit 1~0   **TLVR1~TLVR0**: Minimum low voltage width to reset time (t_{LVR})

00: $(7{\sim}8){\times}t_{LIRC}$
01: $(31{\sim}32){\times}t_{LIRC}$
10: $(63{\sim}64){\times}t_{LIRC}$
11: $(127{\sim}128){\times}t_{LIRC}$

- **RSTFC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	LVRF	—	WRF
R/W	—	—	—	—	—	R/W	—	R/W
POR	—	—	—	—	—	x	—	0

"x": unknown

Bit 7~3   Unimplemented, read as "0"

Bit 2   **LVRF**: LVR function reset flag

0: Not occurred
1: Occurred

This bit is set to 1 when an actual Low Voltage Reset situation condition occurs. This bit can only be cleared to 0 by the application program.

Bit 1   Unimplemented, read as "0"

Bit 0   **WRF**: WDTC register software reset flag

Refer to the Watchdog Timer Control Register section.

Watchdog Time-out Reset during Normal Operation

The Watchdog Time-out Reset during normal operation in the FAST or SLOW mode is the same as a Power On reset except that the Watchdog time-out flag TO will be set to "1".
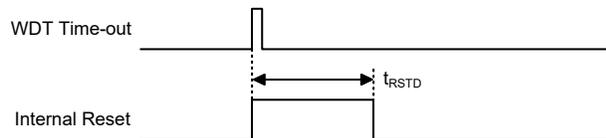
WDT Time-out Reset during Normal Operation Timing Chart

Watchdog Time-out Reset during SLEEP or IDLE Mode

The Watchdog Time-out Reset during SLEEP or IDLE Mode is a little different from other kinds of reset. Most of the conditions remain unchanged except that the Program Counter and the Stack Pointer will be cleared to "0" and the TO flag will be set to "1". Refer to the System Start Up Time Characteristics for t_{SST} details.
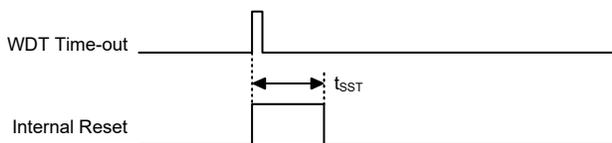
WDT Time-out Reset during SLEEP or IDLE Timing Chart

Reset Initial Conditions

The different types of reset described affect the reset flags in different ways. These flags, known as PDF and TO are located in the status register and are controlled by various microcontroller operations, such as the SLEEP or IDLE Mode function or Watchdog Timer. The reset flags are shown in the table:

TO	PDF	Reset Conditions
0	0	Power-on reset
u	u	LVR reset during FAST or SLOW Mode operation
1	u	WDT time-out reset during FAST or SLOW Mode operation
1	1	WDT time-out reset during IDLE or SLEEP Mode operation

"u" stands for unchanged

The following table indicates the way in which the various components of the microcontroller are affected after a power-on reset occurs.

Item	Condition after Reset
Program Counter	Reset to zero
Interrupts	All interrupts will be disabled
WDT, Time Bases	Cleared after reset, WDT begins counting
Timer Modules	Timer Modules will be turned off
Input/Output Ports	I/O ports will be setup as inputs
Stack Pointer	Stack Pointer will point to the top of the stack

The different kinds of resets all affect the internal registers of the microcontroller in different ways. To ensure reliable continuation of normal program execution after a reset occurs, it is important to know what condition the microcontroller is in after a particular reset occurs. The following table describes how each type of reset affects each of the microcontroller internal registers. Note that where more than one package type exists the table will reflect the situation for the larger package type.

Register	Power-On Reset	WDT Time-out (Normal Operation)	WDT Time-out (IDLE/SLEEP)
IAR0	0000 0000	0000 0000	uuuu uuuu
MP0	0000 0000	0000 0000	uuuu uuuu
IAR1	0000 0000	0000 0000	uuuu uuuu
MP1L	0000 0000	0000 0000	uuuu uuuu
MP1H	0000 0000	0000 0000	uuuu uuuu
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	0000 0000
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBLH	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBHP	---- xxxx	---- uuuu	---- uuuu
STATUS	xx00 xxxx	uu1u uuuu	uu11 uuuu
VBGRC	---- ---0	---- ---0	---- ---u
IAR2	0000 0000	0000 0000	uuuu uuuu

Register	Power-On Reset	WDT Time-out (Normal Operation)	WDT Time-out (IDLE/SLEEP)
MP2L	0000 0000	0000 0000	uuuu uuuu
MP2H	0000 0000	0000 0000	uuuu uuuu
RSTFC	- - - - - x - 0	- - - - - u - u	- - - - - u - u
TB0C	0 - - - - 0 0 0	0 - - - - 0 0 0	u - - - - u u u
TB1C	0 - - - - 0 0 0	0 - - - - 0 0 0	u - - - - u u u
SCC	1 1 1 - - 0 0 0	1 1 1 - - 0 0 0	u u u - - u u u
HIRCC	- - - - 0 0 0 0	- - - - 0 0 0 0	- - - - u u u u
PA	1111 1111	1111 1111	uuuu uuuu
PAC	1111 1111	1111 1111	uuuu uuuu
PAPU	0000 0000	0000 0000	uuuu uuuu
PAWU	0000 0000	0000 0000	uuuu uuuu
PB	- 111 1111	- 111 1111	- uuu uuuu
PBC	- 111 1111	- 111 1111	- uuu uuuu
PBPU	- 000 0000	- 000 0000	- uuu uuuu
SLEDC	0000 0000	0000 0000	uuuu uuuu
LXTC	- - - - - 0 0 0	- - - - - 0 0 0	- - - - - u u u
PSCR	- - - - - 0 0 0	- - - - - 0 0 0	- - - - - u u u
LVDC	- - 00 0000	- - 00 0000	- - uu uuuu
TLVRC	- - - - - - 0 1	- - - - - - 0 1	- - - - - - u u
SDSW0	1000 0000	1000 0000	uuuu uuuu
SDSW1	0 - 00 - - - 0	0 - 00 - - - 0	u - uu - - - u
SDPGAC0	- - 00 0000	- - 00 0000	- - uu uuuu
SDPGAC1	0000 0000	0000 0000	uuuu uuuu
SDA0C	- 00 - - - 00	- 00 - - - 00	- - uu −uu
SDA0VOS	0010 0000	0010 0000	uuuu uuuu
SDA1C	- 00 - - - 00	- 00 - - - 00	- - uu - - uu
SDA1VOS	0010 0000	0010 0000	uuuu uuuu
STMC0	0000 0000	0000 0000	uuuu uuuu
STMC1	0000 0000	0000 0000	uuuu uuuu
STMDL	0000 0000	0000 0000	uuuu uuuu
STMDH	- - - - - - 00	- - - - - - 00	- - - - - - u u
STMAL	0000 0000	0000 0000	uuuu uuuu
STMAH	- - - - - - 00	- - - - - - 00	- - - - - - u u
ORMC	0000 0000	0000 0000	0000 0000
PLTSW	- - - - 0001	- - - - 0001	- - - - uuuu
PLTDACC	- - - 0 0000	- - - 0 0000	- - - u uuuu
PLTDA0L	- - 00 0000	- - 00 0000	- - uu uuuu
PLTDA1L	- - 00 0000	- - 00 0000	- - uu uuuu
PLTDA2L	- - 00 0000	- - 00 0000	- - uu uuuu
PLTC0C	0000 0000	0000 0000	uuuu uuuu
PLTC0VOS	- 001 0000	- 001 0000	- uuu uuuu
PLTC1C	0000 0000	0000 0000	uuuu uuuu

Register	Power-On Reset	WDT Time-out (Normal Operation)	WDT Time-out (IDLE/SLEEP)
PLTC1VOS	- 0 0 1 0 0 0 0	- 0 0 1 0 0 0 0	- u u u u u u u
PLTCHYC	- 0 0 0 0 0 0 0	- 0 0 0 0 0 0 0	- u u u u u u u
PLTAC	- 0 0 - - - - 0	- 0 0 - - - - 0	- u u - - - - u
PLTAVOS	0 0 1 0 0 0 0 0	0 0 1 0 0 0 0 0	u u u u u u u u
PLTDICC1	0 0 0 - - 0 0 0	0 0 0 - - 0 0 0	u u u - - u u u
PLTDICC0	0 - - - - - 0 0	0 - - - - - 0 0	u - - - - - u u
WDTC	0 1 0 1 0 0 1 1	0 1 0 1 0 0 1 1	u u u u u u u u
EEA	- - 0 0 0 0 0 0	- - 0 0 0 0 0 0	- - u u u u u u
EED	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PCRL	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PCRH	- - - - 0 0 0 0	- - - - 0 0 0 0	- - - - u u u u
CRCCR	- - - - - - - 0	- - - - - - - 0	- - - - - - - u
CRCIN	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
CRCDL	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
CRCDH	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
INTEG	- - - - 0 0 0 0	- - - - 0 0 0 0	- - - - u u u u
INTC0	- 0 0 0 0 0 0 0	- 0 0 0 0 0 0 0	- u u u u u u u
INTC1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
INTC2	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
INTC3	- 0 0 0 - 0 0 0	- 0 0 0 - 0 0 0	- u u u - u u u
PAS0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PAS1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PBS0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PBS1	- - 0 0 0 0 0 0	- - 0 0 0 0 0 0	- - u u u u u u
IFS0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
IFS1	- - 0 0 0 0 0 0	- - 0 0 0 0 0 0	- - u u u u u u
PTMC0	0 0 0 0 0 - - -	0 0 0 0 0 - - -	u u u u u - - -
PTMC1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PTMC2	- - - - - 0 0 0	- - - - - 0 0 0	- - - - - u u u
PTMDL	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PTMDH	- - - - - - 0 0	- - - - - - 0 0	- - - - - - u u
PTMAL	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PTMAH	- - - - - - 0 0	- - - - - - 0 0	- - - - - - u u
PTMBL	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PTMBH	- - - - - - 0 0	- - - - - - 0 0	- - - - - - u u
PTMRPL	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
PTMRPH	- - - - - - 0 0	- - - - - - 0 0	- - - - - - u u
ISGENC	0 - - - - - 0 0	0 - - - - - 0 0	u - - - - - u u
ISGDATA0	- - - 0 0 0 0 0	- - - 0 0 0 0 0	- - - u u u u u
ISGDATA1	- - - 0 0 0 0 0	- - - 0 0 0 0 0	- - - u u u u u
SADC0	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u
SADC1	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	u u u u u u u u

Register	Power-On Reset	WDT Time-out (Normal Operation)	WDT Time-out (IDLE/SLEEP)
SADC2	0 - - - - - 1 0	0 - - - - - 1 0	u - - - - - u u
SADOL	x x x x - - - -	x x x x - - - -	u u u u - - - - (ADRFS=0)
			u u u u u u u u (ADRFS=1)
SADOH	x x x x x x x x	x x x x x x x x	u u u u u u u u (ADRFS=0)
			- - - - u u u u (ADRFS=1)
SIMC0	1110 0000	1110 0000	u u u u u u u u
SIMC1 (UMD=0)	1000 0001	1000 0001	u u u u u u u u
UUCR1* (UMD=1)	0000 00x0	0000 00x0	u u u u u u u u
SIMD/UTXR_RXR	x x x x x x x x	x x x x x x x x	u u u u u u u u
SIMA/SIMC2/UUCR2	0000 0000	0000 0000	u u u u u u u u
UUCR3	- - - - - - - 0	- - - - - - - 0	- - - - - - - u
SIMTOC (UMD=0)	0000 0000	0000 0000	u u u u u u u u
UBRG* (UMD=1)	x x x x x x x x	x x x x x x x x	u u u u u u u u
UUSR	0000 1011	0000 1011	u u u u u u u u
IECC	0000 0000	0000 0000	u u u u u u u u
STKPTR	- - - - - 0 0 0	- - - - - 0 0 0	- - - - - u u u
EEC	- - - - 0000	- - - - 0000	- - - - u u u u

Note: "u" stands for unchanged

"x" stands for unknown

"-" stands for unimplemented

"*": The UUCR1 and SIMC1 registers share the same memory address while the UBRG and SIMTOC registers share the same memory address. The default value of the UUCR1 or UBRG register can be obtained when the UMD bit is set high by application program after a reset.

Input/Output Ports

Holtek microcontrollers offer considerable flexibility on their I/O ports. With the input or output designation of every pin fully under user program control, pull-high selections for all ports and wake-up selections on certain pins, the user is provided with an I/O structure to meet the needs of a wide range of application possibilities.

The device provides bidirectional input/output lines labeled with port names PA~PB. These I/O ports are mapped to the RAM Data Memory with specific addresses as shown in the Special Purpose Data Memory table. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, which means the inputs must be ready at the T2 rising edge of instruction "MOV A, [m]", where m denotes the port address. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Register Name	Bit							
	7	6	5	4	3	2	1	0
PA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
PAC	PAC7*	PAC6	PAC5	PAC4	PAC3	PAC2	PAC1	PAC0
PAPU	PAPU7**	PAPU6	PAPU5	PAPU4	PAPU3	PAPU2	PAPU1	PAPU0
PAWU	PAWU7**	PAWU6	PAWU5	PAWU4	PAWU3	PAWU2	PAWU1	PAWU0
PB	—	PB6	PB5	PB4	PB3	PB2	PB1	PB0
PBC	—	PBC6	PBC5	PBC4*	PBC3	PBC2	PBC1	PBC0
PBPU	—	PBPU6	PBPU5	PBPU4**	PBPU3	PBPU2	PBPU1	PBPU0

"—": Unimplemented, read as "0"

I/O Logic Function Register List

Note: The control bit with an asterisk * should be cleared to 0 and the control bit with an asterisk ** should remain the POR value after power-on reset. This can set these unbonded and not internally used pins as outputs to prevent additional power consumption.

Pull-high Resistors

Many product applications require pull-high resistors for their switch inputs usually requiring the use of an external resistor. To eliminate the need for these external resistors, all I/O pins, when configured as a digital input have the capability of being connected to an internal pull-high resistor. These pull-high resistors are selected using registers PAPU~PBPU, and are implemented using weak PMOS transistors.

Note that the pull-high resistor can be controlled by the relevant pull-high control register only when the pin-shared functional pin is selected as a digital input or NMOS output. Otherwise, the pull-high resistors cannot be enabled.

• **PxPU Register**

Bit	7	6	5	4	3	2	1	0
Name	PxPU7	PxPU6	PxPU5	PxPU4	PxPU3	PxPU2	PxPU1	PxPU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

PxPUn: I/O Port x Pin pull-high function control
0: Disable
1: Enable

The PxPUn bit is used to control the pin pull-high function. Here the "x" can be A and B. However, the actual available bits for each I/O Port may be different.

Port A Wake-up

The HALT instruction forces the microcontroller into the SLEEP or IDLE Mode which preserves power, a feature that is important for battery and other low-power applications. Various methods exist to wake up the microcontroller, one of which is to change the logic condition on one of the Port A pins from high to low. This function is especially suitable for applications that can be woken up via external switches. Each pin on Port A can be selected individually to have this wake-up feature using the PAWU register.

Note that the wake-up function can be controlled by the wake-up control register only when the pin is selected as a general purpose input and the MCU enters the IDLE or SLEEP mode.

• PAWU Register

Bit	7	6	5	4	3	2	1	0
Name	PAWU7	PAWU6	PAWU5	PAWU4	PAWU3	PAWU2	PAWU1	PAWU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **PAWU7**: This bit should remain unchanged after power-on reset
Bit 6~0   **PAWU6~PAWU0**: PA6~PA0 wake-up function control
      0: Disable
      1: Enable

I/O Port Control Registers

Each I/O port has its own control register known as PAC~PBC, to control the input/output configuration. With this control register, each CMOS output or input can be reconfigured dynamically under software control. Each pin of the I/O ports is directly mapped to a bit in its associated port control register. For the I/O pin to function as an input, the corresponding bit of the control register must be written as a "1". This will then allow the logic state of the input pin to be directly read by instructions. When the corresponding bit of the control register is written as a "0", the I/O pin will be setup as a CMOS output. If the pin is currently setup as an output, instructions can still be used to read the output register. However, it should be noted that the program will in fact only read the status of the output data latch and not the actual logic status of the output pin when the IECM is set to "0".

• PxC Register

Bit	7	6	5	4	3	2	1	0
Name	PxC7	PxC6	PxC5	PxC4	PxC3	PxC2	PxC1	PxC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

PxCn: I/O Port x Pin type selection
      0: Output
      1: Input

The PxCn bit is used to control the pin type selection. Here the "x" can be A and B. However, the actual available bits for each I/O Port may be different.

The WDI and ENCLK are pin-shard with PA3 and PA6 pins respectively, the PAC3 and PAC6 bits should be properly configured to ensure correct signal direction.

I/O Port Source Current Control

Each pin in this device can be configured with different output source current which is selected by the corresponding source current selection bits. These source current selection bits are available only when the corresponding pin is configured as a CMOS output. Otherwise, these select bits have no effect. Users should refer to the Input/Output Characteristics section to obtain the exact value for different applications.

• **SLEDC Register**

Bit	7	6	5	4	3	2	1	0
Name	SLEDC7	SLEDC6	SLEDC5	SLEDC4	SLEDC3	SLEDC2	SLEDC1	SLEDC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **SLEDC7~SLEDC6**: PB6~PB5 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Bit 5~4   **SLEDC5~SLEDC4**: PB3~PB0 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Bit 3~2   **SLEDC3~SLEDC2**: PA6~PA4 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Bit 1~0   **SLEDC1~SLEDC0**: PA3~PA0 source current selection
     00: Source current=Level 0 (Min.)
     01: Source current=Level 1
     10: Source current=Level 2
     11: Source current=Level 3 (Max.)

Pin-shared Functions

The flexibility of the microcontroller range is greatly enhanced by the use of pins that have more than one function. Limited numbers of pins can force serious design constraints on designers but by supplying pins with multi-functions, many of these difficulties can be overcome. For these pins, the desired function of the multi-function I/O pins is selected by a series of registers via the application program control.

Pin-shared Function Selection Registers

The limited number of supplied pins in a package can impose restrictions on the amount of functions a certain device can contain. However, by allowing the same pins to share several different functions and providing a means of function selection, a wide range of different functions can be incorporated into even relatively small package sizes. The device includes Port "x" Output Function Selection register "n", labeled as PxSn, and Input Function Selection register "i", labeled as IFSi, which can select the desired functions of the multi-function pin-shared pins.

The most important point to note is to make sure that the desired pin-shared function is properly selected and also deselected. For most pin-shared functions, to select the desired pin-shared function, the pin-shared function should first be correctly selected using the corresponding pin-shared control register. After that the corresponding peripheral functional setting should be configured and then the

peripheral function can be enabled. However, a special point must be noted for some digital input pins, such as INTn, xTCK, STPI, etc, which share the same pin-shared control configuration with their corresponding general purpose I/O functions when setting the relevant pin-shared control bit fields. To select these pin functions, in addition to the necessary pin-shared control and peripheral functional setup aforementioned, they must also be set as an input by setting the corresponding bit in the I/O port control register. To correctly deselect the pin-shared function, the peripheral function should first be disabled and then the corresponding pin-shared function control register can be modified to select other pin-shared functions.

Register Name	Bit							
	7	6	5	4	3	2	1	0
PAS0	PAS07	PAS06	PAS05	PAS04	PAS03	PAS02	PAS01	PAS00
PAS1	D7	D6	PAS15	PAS14	PAS13	PAS12	PAS11	PAS10
PBS0	PBS07	PBS06	PBS05	PBS04	PBS03	PBS02	PBS01	PBS00
PBS1	—	—	PBS15	PBS14	PBS13	PBS12	D1	D0
IFS0	IFS07	IFS06	IFS05	IFS04	IFS03	IFS02	IFS01	IFS00
IFS1	—	—	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10

Pin-shared Function Selection Register List

• **PAS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PAS07	PAS06	PAS05	PAS04	PAS03	PAS02	PAS01	PAS00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PAS07~PAS06**: PA3 Pin-shared function selection
        00: PA3/STCK
        01: SDO/UTX
        10: PTPB
        11: AN3
    These bits should be set to 00 when it is required to use the WDI pin function of the Buzzer Driver.

Bit 5~4   **PAS05~PAS04**: PA2 Pin-shared function selection
        00: PA2
        01: SDI/SDA/URX/UTX
        10: PA2
        11: PA2

Bit 3~2   **PAS03~PAS02**: PA1 Pin-shared function selection
        00: PA1/INT1
        01: $\overline{SCS}$
        10: AN2
        11: A1PI
    Note: The PA1 and PA5 share one external pin, it is important to note that PA5 should be configured as an input with the pull-high function disabled when using these bits to select the pin function on PA1 pin.

Bit 1~0   **PAS01~PAS00**: PA0 Pin-shared function selection
        00: PA0
        01: SCK/SCL
        10: PA0
        11: PA0

• **PAS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	PAS15	PAS14	PAS13	PAS12	PAS11	PAS10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **D7~D6**: Reserved bits, should remain unchanged after power-on reset

Bit 5~4   **PAS15~PAS14**: PA6 Pin-shared function selection
    00: PA6
    01: PTP
    10: SDI/SDA/URX/UTX
    11: VREF

    These bits should be set to 01 when it is required to use the ENCLK pin function of the Buzzer Driver.

Bit 3~2   **PAS13~PAS12**: PA5 Pin-shared function selection
    00: PA5/STCK
    01: STP
    10: $\overline{\text{SCS}}$
    11: A1O

    Note: The PA1 and PA5 share one external pin, it is important to note that PA1 should be configured as an input with the pull-high function disabled when using these bits to select the pin function on PA5 pin.

Bit 1~0   **PAS11~PAS10**: PA4 Pin-shared function selection
    00: PA4/PTCK
    01: STPB
    10: AN0
    11: A0O

• **PBS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PBS07	PBS06	PBS05	PBS04	PBS03	PBS02	PBS01	PBS00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PBS07~PBS06**: PB3 Pin-shared function selection
    00: PB3
    01: PLRX
    10: SDI/SDA/URX/UTX
    11: PB3

Bit 5~4   **PBS05~PBS04**: PB2 Pin-shared function selection
    00: PB2
    01: PLIS
    10: SCK/SCL
    11: XT2

Bit 3~2   **PBS03~PBS02**: PB1 Pin-shared function selection
    00: PB1/STPI
    01: PLTX
    10: SDO/UTX
    11: XT1

Bit 1~0   **PBS01~PBS00**: PB0 Pin-shared function selection
    00: PB0/INT0
    01: STP
    10: A0PI1
    11: A0PB

- **PBS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	PBS15	PBS14	PBS13	PBS12	D1	D0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6   Unimplemented, read as "0"

Bit 5~4   **PBS15~PBS14**: PB6 Pin-shared function selection
        00: PB6
        01: PLDICO
        10: PB6
        11: PB6

Bit 3~2   **PBS13~PBS12**: PB5 Pin-shared function selection
        00: PB5
        01: STP
        10: PTP
        11: PLVREF

Bit 1~0   **D1~D0**: Reserved bits, should remain unchanged after power-on reset

- **IFS0 Register**

Bit	7	6	5	4	3	2	1	0
Name	IFS07	IFS06	IFS05	IFS04	IFS03	IFS02	IFS01	IFS00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **IFS07~IFS06**: PTPI input source selection
        00: CXCAP
        01: Reserved
        10: CXCAP
        11: CXCAP
        Note: The CXCAP signal is from the Power Line Transceiver comparator output
             signal.

Bit 5~4   **IFS05~IFS04**: $\overline{SCS}$ input source pin selection
        00: PA5
        01: Reserved
        10: PA1
        11: PA5

Bit 3~2   **IFS03~IFS02**: SCK/SCL input source pin selection
        00: PB2
        01: PA0
        10: Reserved
        11: PB2

Bit 1~0   **IFS01~IFS00**: SDI/SDA/URX/UTX input source pin selection
   00: PB3
        01: PA2
        10: PA6
        11: PB3

• **IFS1 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	IFS15	IFS14	IFS13	IFS12	IFS11	IFS10
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6   Unimplemented, read as "0"

Bit 5~4   **IFS15~IFS14**: INT0 input source pin selection
        00: PB0
        01: Reserved
        10: PB0
        11: PB0

Bit 3~2   **IFS13~IFS12**: STPI input source pin selection
        00: PB1
        01: Reserved
        10: PB1
        11: PB1

Bit 1~0   **IFS11~IFS10**: STCK input source pin selection
        00: PA3
        01: PA5
        10: PA3
        11: PA3

I/O Pin Structures

The accompanying diagram illustrates the internal structures of the I/O logic function. As the exact logical construction of the I/O pin will differ from this diagram, it is supplied as a guide only to assist with the functional understanding of the logic function I/O pins. The wide range of pin-shared structures does not permit all types to be shown.

Logic Function Input/Output Structure
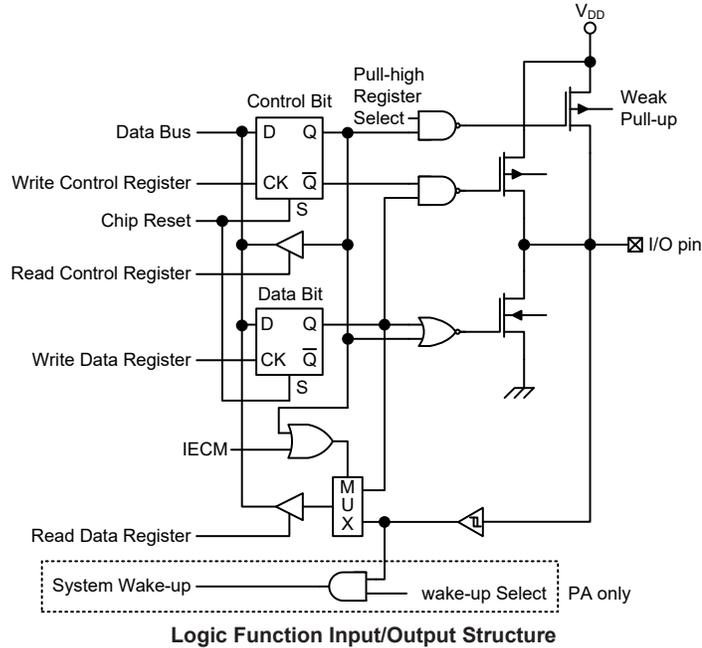
READ PORT Function

The READ PORT function is used to manage the reading of the output data from the data latch or I/O pin, which is specially designed for the IEC 60730 self-diagnostic test on the I/O function and A/D paths. There is a register, IECC, which is used to control the READ PORT function. If the READ PORT function is disabled, the pin function will operate as the selected pin-shared function. When a specific data pattern, "11001010", is written into the IECC register, the internal signal named IECM will be set high to enable the READ PORT function. If the READ PORT function is enabled, the value on the corresponding pins will be passed to the accumulator ACC when the read port instruction "mov acc, Px" is executed where the "x" stands for the corresponding I/O port name.

Note that the READ PORT mode can only control the input path and will not affect the pin-shared function assignment and the current MCU operation. However, when the IECC register content is set to any other values rather than "11001010", the IECM internal signal will be cleared to 0 to disable the READ PORT function, and the reading path will be from the data latch. If the READ PORT function is disabled, the pin function will operate as the selected pin-shared function.

• **IECC Register**

| Bit	7	6	5	4	3	2	1	0
Name	IECS7	IECS6	IECS5	IECS4	IECS3	IECS2	IECS1	IECS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **IECS7~IECS0**: READ PORT function enable control bit 7 ~ bit 0
11001010: IECM=1 – READ PORT function is enabled
Others: IECM=0 – READ PORT function is disabled

READ PORT Function	Disabled		Enabled	
Port Control Register Bit – PxC.n	1	0	1	0
I/O Function	Pin value	Data latch value	Pin value	
Digital Input Function				
Digital Output Function (except USIM)	0			
USIM: SCK/SCL, SDI/SDA, URX/UTX	Pin value			
Analog Function	0			

Note: The value in the above table is the content of the ACC register after "mov a, Px" instruction is executed where "x" means the relevant port name.

The additional function of the READ PORT mode is to check the A/D path. When the READ PORT function is disabled, the A/D path from the external pin to the internal analog input will be switched off if the A/D input pin function is not selected by the corresponding selection bits. For the MCU with A/D converter channels, such as A/D AN0, AN2~AN3, the desired A/D channel can be switched on by properly configuring the external analog input channel selection bits in the A/D Control Register together with the corresponding analog input pin function is selected. However, the additional function of the READ PORT mode is to force the A/D path to be switched on. For example, when the AN0 is selected as the analog input channel as the READ PORT function is enabled, the AN0 analog input path will be switched on even if the AN0 analog input pin function is not selected. In this way, the AN0 analog input path can be examined by internally connecting the digital output on this shared pin with the AN0 analog input pin switch and then converting the corresponding digital data without any external analog input voltage connected.

Note that the A/D converter reference voltage should be equal to the I/O power supply voltage when examining the A/D path using the READ PORT function.
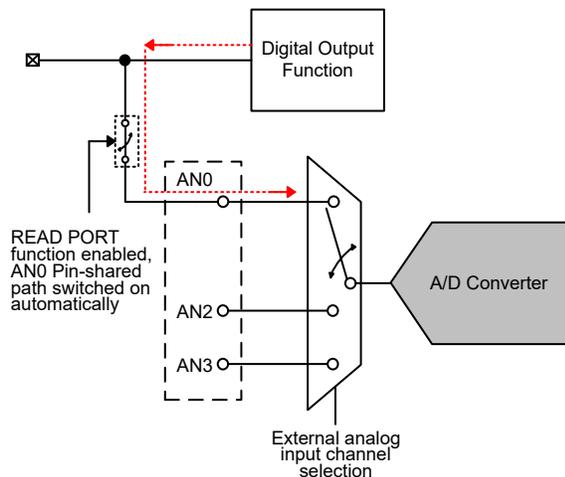
A/D Channel Input Path Internally Connection

Programming Considerations

Within the user program, one of the first things to consider is port initialisation. After a reset, all of the I/O data and port control registers will be set high. This means that all I/O pins will default to an input state, the level of which depends on the other connected circuitry and whether pull-high selections have been chosen. If the port control registers are then programmed to setup some pins as outputs, these output pins will have an initial high output value unless the associated port data registers are first programmed. Selecting which pins are inputs and which are outputs can be achieved byte-wide by loading the correct values into the appropriate port control register or by programming individual bits in the port control register using the "SET [m].i" and "CLR [m].i" instructions. Note that when using these bit control instructions, a read-modify-write operation takes place. The microcontroller must first read in the data on the entire port, modify it to the required new bit values and then rewrite this data back to the output ports.

Port A has the additional capability of providing wake-up functions. When the device is in the SLEEP or IDLE Mode, various methods are available to wake the device up. One of these is a high to low transition of any of the Port A pins. Single or multiple pins on Port A can be setup to have this function.

Timer Modules – TM

One of the most fundamental functions in any microcontroller devices are the ability to control and measure time. To implement time related functions the device includes two Timer Modules, abbreviated to the name TM. The TMs are multi-purpose timing units and serve to provide operations such as Timer/Counter, Input Capture, Compare Match Output and Single Pulse Output as well as being the functional unit for the generation of PWM signals. Each of the TMs has two individual interrupts. The addition of input and output pins for each TM ensures that users are provided with timing units with a wide and flexible range of features.

The common features of the different TM types are described here with more detailed information provided in the individual Standard and Periodic Type TM sections.

Introduction

The device contains two TMs and each individual TM can be categorised as a certain type, namely Standard Type TM and Periodic Type TM. Although similar in nature, the different TM types vary in their feature complexity. The common features to all of the Standard and Periodic TMs will be described in this section. The detailed operation regarding each of the TM types will be described in separate sections. The main features and differences between the two types of TMs are summarised in the accompanying table.

Function	STM	PTM
Timer/Counter	√	√
Input Capture	√	√
Compare Match Output	√	√
PWM Output	√	√
Single Pulse Output	√	√
PWM Alignment	Edge	Edge
PWM Adjustment Period & Duty	Duty or Period	Duty or Period

TM Function Summary

TM Operation

The different types of TM offer a diverse range of functions, from simple timing operations to PWM signal generation. The key to understanding how the TM operates is to see it in terms of a free running counter whose value is then compared with the value of pre-programmed internal comparators. When the free running count-up counter has the same value as the pre-programmed comparator, known as a compare match situation, a TM interrupt signal will be generated which can clear the counter and perhaps also change the condition of the TM output pin. The internal TM counter is driven by a user selectable clock source, which can be an internal clock or an external pin.

TM Clock Source

The clock source which drives the main counter in each TM can originate from various sources. The selection of the required clock source is implemented using the xTCK2~xTCK0 bits in the xTM control registers, where "x" stands for S or P type TM. The clock source can be a ratio of the system clock f_{SYS} or the internal high clock f_H, the f_{SUB} clock source or the external xTCK pin. The xTCK pin clock source is used to allow an external signal to drive the TM as an external clock source or for event counting.

TM Interrupts

The Standard and Periodic type TMs each have two internal interrupts, one for each of the internal comparator A or comparator P, which generate a TM interrupt when a compare match condition occurs. When a TM interrupt is generated it can be used to clear the counter and also to change the state of the TM output pin.

TM External Pins

Each of the TMs, irrespective of what type, has one or two TM input pins, with the label xTCK and STPI respectively. The xTM input pin, xTCK, is essentially a clock source for the xTM and is selected using the xTCK2~xTCK0 bits in the xTMC0 register. This external TM input pin allows an external clock source to drive the internal TM. The xTCK input pin can be chosen to have either a rising or falling active edge. The xTCK pin is also used as the external trigger input pin in single pulse output mode.

The other STM input pin, STPI, is the capture input whose active edge can be a rising edge, a falling edge or both rising and falling edges and the active edge transition type is selected using the STIO1~STIO0 bits in the STMC1 register. There is another capture input, PTCK, for PTM capture input mode, which can be used as the external trigger input source.

The TMs each have two output pins, xTP and xTPB. When the TM is in the Compare Match Output Mode, the xTPB pin can be controlled by the TM to switch to a high or low level or to toggle when a compare match situation occurs. The xTPB pin outputs the inverted signal of the xTP. The external xTP and xTPB output pin are also the pins where the TM generates the PWM output waveform.

As the TM input and output pins are pin-shared with other functions, the TM input and output functions must first be setup using the relevant pin-shared function selection bits. The details of the pin-shared function selection are described in the pin-shared function section.

STM		PTM	
Input	**Output**	**Input**	**Output**
STCK, STPI	STP, STPB	PTCK	PTP, PTPB

TM External Pins
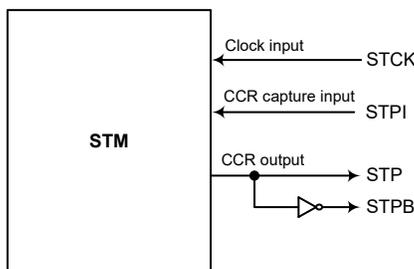
**STM Function Pin Block Diagram**
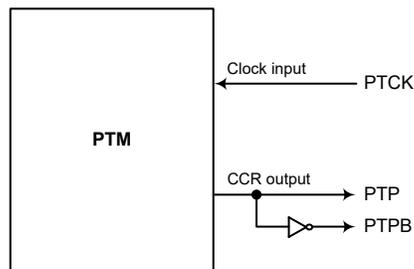
PTM Function Pin Block Diagram

Programming Considerations

The TM Counter Registers and the Capture/Compare CCRA and CCRP registers as well as the PTM CCRB register, all have a low and high byte structure. The high bytes can be directly accessed, but as the low bytes can only be accessed via an internal 8-bit buffer, reading or writing to these register pairs must be carried out in a specific way. The important point to note is that data transfer to and from the 8-bit buffer and its related low byte only takes place when a write or read operation to its corresponding high byte is executed.

As the CCRA, CCRB and CCRP registers are implemented in the way shown in the following diagram and accessing these register pairs is carried out in a specific way as described above, it is recommended to use the "MOV" instruction to access the CCRA, CCRB and CCRP low byte registers, named xTMAL, PTMBL, PTMRPL, using the following access procedures. Accessing the CCRA, CCRB or CCRP low byte register without following these access procedures will result in unpredictable values.
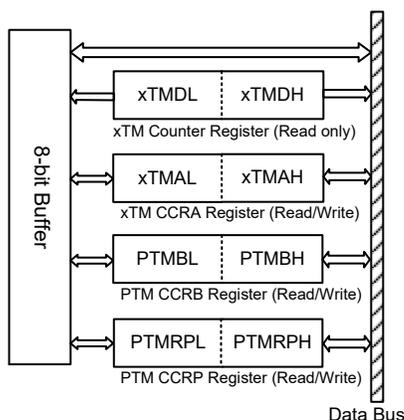
The following steps show the read and write procedures:

• Writing Data to CCRA, CCRB or CCRP

  ⬥ Step 1. Write data to Low Byte xTMAL, PTMBL or PTMRPL

    – Note that here data is only written to the 8-bit buffer.

  ⬥ Step 2. Write data to High Byte xTMAH, PTMBH or PTMRPH

    – Here data is written directly to the high byte registers and simultaneously data is latched from the 8-bit buffer to the Low Byte registers.

• Reading Data from the Counter Registers, CCRA, CCRB or CCRP

  ⬥ Step 1. Read data from the High Byte xTMDH, xTMAH, PTMBH or PTMRPH

    – Here data is read directly from the High Byte registers and simultaneously data is latched from the Low Byte register into the 8-bit buffer.

  ⬥ Step 2. Read data from the Low Byte xTMDL, xTMAL, PTMBL or PTMRPL

    – This step reads data from the 8-bit buffer.

Standard Type TM – STM

The Standard type TM contains five operating modes, which are Compare Match Output, Timer/Event Counter, Capture Input, Single Pulse Output and PWM Output modes. The Standard type TM can also be controlled with two external input pins and can drive two external output pins.
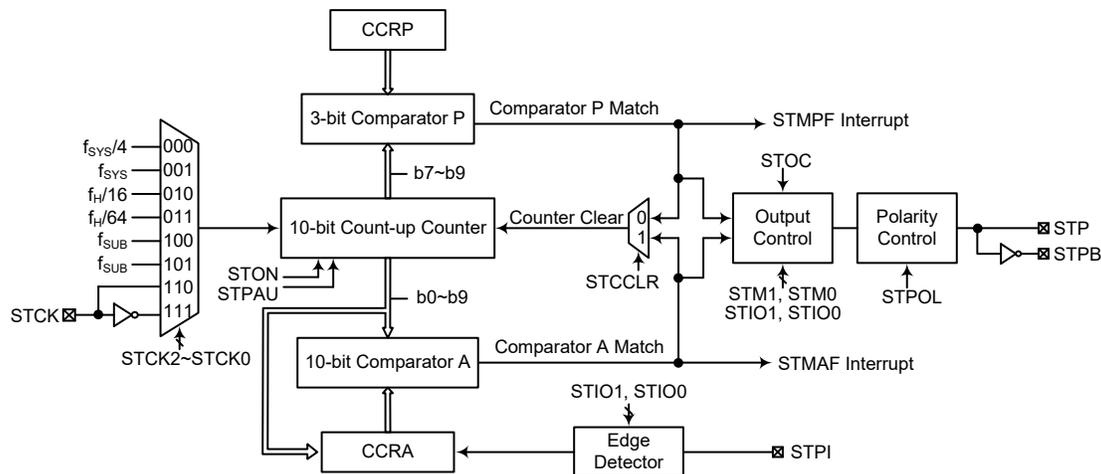
Note: 1. As the STM external pins are pin-shared with other functions, so before using the STM function, ensure that the relevant pin-shared function registers have been set properly to enable the STM pin function. The STCK and STPI pin, if used, must also be set as an input by setting the corresponding bits in the port control register.

   2. The STPB is the inverted signal of the STP.

10-bit Standard Type TM Block Diagram

Standard Type TM Operation

Its core is a 10-bit count-up counter which is driven by a user selectable internal or external clock source. There are also two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with CCRP and CCRA registers. The CCRP is three bits wide whose value is compared with the highest three bits in the counter while the CCRA is the ten bits and therefore compares with all counter bits.

The only way of changing the value of the 10-bit counter using the application program, is to clear the counter by changing the STON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, an STM interrupt signal will also usually be generated. The Standard Type TM can operate in a number of different operational modes, can be driven by different clock sources including an input pin and can also control two output pins. All operating setup conditions are selected using relevant internal registers.

Standard Type TM Register Description

Overall operation of the Standard type TM is controlled using several registers. A read only register pair exists to store the internal counter 10-bit value, while a read/write register pair exists to store the internal 10-bit CCRA value. The remaining two registers are control registers which setup the different operating and control modes as well as the three CCRP bits.

Register Name	Bit							
	7	6	5	4	3	2	1	0
STMC0	STPAU	STCK2	STCK1	STCK0	STON	STRP2	STRP1	STRP0
STMC1	STM1	STM0	STIO1	STIO0	STOC	STPOL	STDPX	STCCLR
STMDL	D7	D6	D5	D4	D3	D2	D1	D0
STMDH	—	—	—	—	—	—	D9	D8
STMAL	D7	D6	D5	D4	D3	D2	D1	D0
STMAH	—	—	—	—	—	—	D9	D8

10-bit Standard Type TM Register List

• **STMC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	STPAU	STCK2	STCK1	STCK0	STON	STRP2	STRP1	STRP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **STPAU**: STM Counter Pause Control
　　0: Run
　　1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the STM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4   **STCK2~STCK0**: Select STM Counter Clock
　　000: $f_{SYS}/4$
　　001: f_{SYS}
　　010: $f_H/16$
　　011: $f_H/64$
　　100: f_{SUB}
　　101: f_{SUB}
　　110: STCK rising edge clock
　　111: STCK falling edge clock

These three bits are used to select the clock source for the STM. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source f_{SYS} is the system clock, while f_H and f_{SUB} are other internal clocks, the details of which can be found in the "Operating Modes and System Clocks" section.

Bit 3   **STON**: STM Counter On/Off Control
　　0: Off
　　1: On

This bit controls the overall on/off function of the STM. Setting the bit high enables the counter to run while clearing the bit disables the STM. Clearing this bit to zero will stop the counter from counting and turn off the STM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again.

If the STM is in the Compare Match Output Mode, PWM Output Mode or Single Pulse Output Mode then the STM output pin will be reset to its initial condition, as specified by the STOC bit, when the STON bit changes from low to high.

Bit 2~0   **STRP2~STRP0**: STM CCRP 3-bit register, compared with the STM counter bit 9~bit 7

Comparator P Match Period=
- 000: 1024 STM clocks
- 001: 128 STM clocks
- 010: 256 STM clocks
- 011: 384 STM clocks
- 100: 512 STM clocks
- 101: 640 STM clocks
- 110: 768 STM clocks
- 111: 896 STM clocks

These three bits are used to setup the value on the internal CCRP 3-bit register, which are then compared with the internal counter's highest three bits. The result of this comparison can be selected to clear the internal counter if the STCCLR bit is set to zero. Clearing the STCCLR bit to zero ensures that a compare match with the CCRP values will reset the internal counter. As the CCRP bits are only compared with the highest three counter bits, the compare values exist in 128 clock cycle multiples. Clearing all three bits to zero is in effect allowing the counter to overflow at its maximum value.

- **STMC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	STM1	STM0	STIO1	STIO0	STOC	STPOL	STDPX	STCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **STM1~STM0**: Select STM Operating Mode
- 00: Compare Match Output Mode
- 01: Capture Input Mode
- 10: PWM Output Mode or Single Pulse Output Mode
- 11: Timer/Counter Mode

These bits setup the required operating mode for the STM. To ensure reliable operation the STM should be switched off before any changes are made to the STM1 and STM0 bits. In the Timer/Counter Mode, the STM output pin state is undefined.

Bit 5~4   **STIO1~STIO0**: Select STM external pins function

Compare Match Output Mode
- 00: No change
- 01: Output low
- 10: Output high
- 11: Toggle output

PWM Output Mode/Single Pulse Output Mode
- 00: PWM output inactive state
- 01: PWM output active state
- 10: PWM output
- 11: Single Pulse Output

Capture Input Mode
- 00: Input capture at rising edge of STPI
- 01: Input capture at falling edge of STPI
- 10: Input capture at both rising and falling edges of STPI
- 11: Input capture disabled

Timer/Counter Mode
- Unused

These two bits are used to determine how the STM external pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the STM is running.

In the Compare Match Output Mode, the STIO1 and STIO0 bits determine how the STM output pin changes state when a compare match occurs from the Comparator A. The TM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the STM output pin should be setup using the STOC bit in the STMC1 register. Note that the output level requested by the STIO1 and STIO0 bits must be different from the initial value setup using the STOC bit otherwise no change will occur on the STM output pin when a compare match occurs. After the STM output pin changes state, it can be reset to its initial level by changing the level of the STON bit from low to high.

In the PWM Output Mode, the STIO1 and STIO0 bits determine how the STM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to change the values of the STIO1 and STIO0 bits only after the STM has been switched off. Unpredictable PWM outputs will occur if the STIO1 and STIO0 bits are changed when the STM is running.

Bit 3　　**STOC**: STM STP Output control

Compare Match Output Mode
　　0: Initial low
　　1: Initial high
PWM Output Mode/Single Pulse Output Mode
　　0: Active low
　　1: Active high

This is the output control bit for the STM output pin. Its operation depends upon whether STM is being used in the Compare Match Output Mode or in the PWM Output Mode/Single Pulse Output Mode. It has no effect if the STM is in the Timer/Counter Mode. In the Compare Match Output Mode it determines the logic level of the STM output pin before a compare match occurs. In the PWM Output Mode it determines if the PWM signal is active high or active low. In the Single Pulse Output Mode it determines the logic level of the STP output pin when the STON bit changes from low to high.

Bit 2　　**STPOL**: STP Output Polarity control
　　0: Non-inverted
　　1: Inverted

This bit controls the polarity of the STP output pin. When the bit is set high the STM output pin will be inverted and not inverted when the bit is zero. It has no effect if the STM is in the Timer/Counter Mode.

Bit 1　　**STDPX**: STM PWM duty/period control
　　0: CCRP – period; CCRA – duty
　　1: CCRP – duty; CCRA – period

This bit determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

Bit 0　　**STCCLR**: STM Counter Clear condition selection
　　0: Comparator P match
　　1: Comparator A match

This bit is used to select the method which clears the counter. Remember that the Standard TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the STCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The STCCLR bit is not used in the PWM Output, Single Pulse Output or Capture Input Mode.

• **STMDL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: STM Counter Low Byte Register bit 7 ~ bit 0
                 STM 10-bit Counter bit 7 ~ bit 0

• **STMDH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R	R
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"
Bit 1~0   **D9~D8**: STM Counter High Byte Register bit 1 ~ bit 0
                 STM 10-bit Counter bit 9 ~ bit 8

• **STMAL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: STM CCRA Low Byte Register bit 7 ~ bit 0
                 STM 10-bit CCRA bit 7 ~ bit 0

• **STMAH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"
Bit 1~0   **D9~D8**: STM CCRA High Byte Register bit 1 ~ bit 0
                 STM 10-bit CCRA bit 9 ~ bit 8

Standard Type TM Operating Modes

The Standard Type TM can operate in one of five operating modes, Compare Match Output Mode, PWM Output Mode, Single Pulse Output Mode, Capture Input Mode or Timer/Counter Mode. The operating mode is selected using the STM1 and STM0 bits in the STMC1 register.
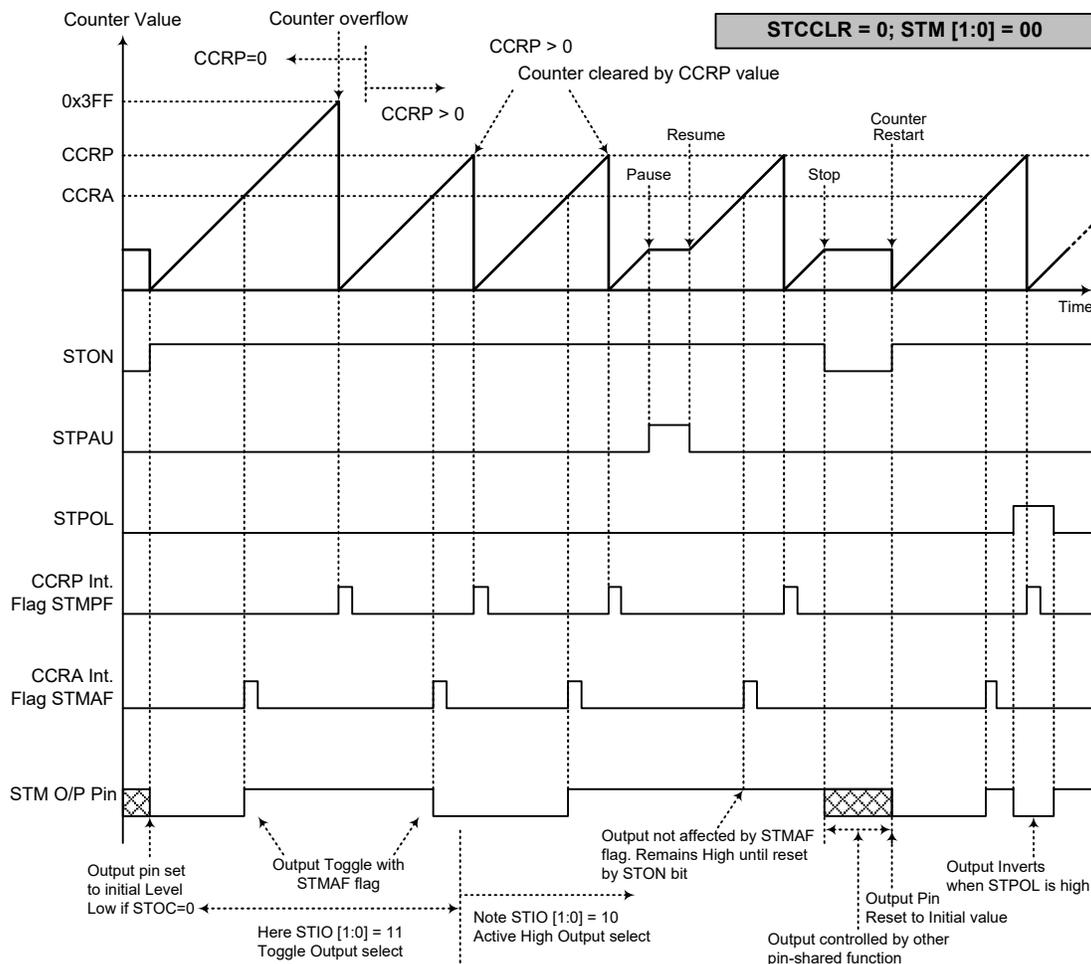
Compare Match Output Mode

To select this mode, bits STM1 and STM0 in the STMC1 register, should be set to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the STCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both STMAF and STMPF interrupt request flags for Comparator A and Comparator P respectively, will both be generated.

If the STCCLR bit in the STMC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the STMAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when STCCLR is high no STMPF interrupt request flag will be generated. In the Compare Match Output Mode, the CCRA can not be set to "0".

If the CCRA bits are all zero, the counter will overflow when it reaches its maximum 10-bit, 3FF Hex, value, however here the STMAF interrupt request flag will not be generated.

As the name of the mode suggests, after a comparison is made, the STM output pin, will change state. The STM output pin condition however only changes state when a STMAF interrupt request flag is generated after a compare match occurs from Comparator A. The STMPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the STM output pin. The way in which the STM output pin changes state are determined by the condition of the STIO1 and STIO0 bits in the STMC1 register. The STM output pin can be selected using the STIO1 and STIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the STM output pin, which is setup after the STON bit changes from low to high, is setup using the STOC bit. Note that if the STIO1 and STIO0 bits are zero then no pin change will take place.

Compare Match Output Mode – STCCLR=0

Note: 1. With STCCLR=0, a Comparator P match will clear the counter
2. The STM output pin controlled only by the STMAF flag
3. The output pin reset to initial state by a STON bit rising edge
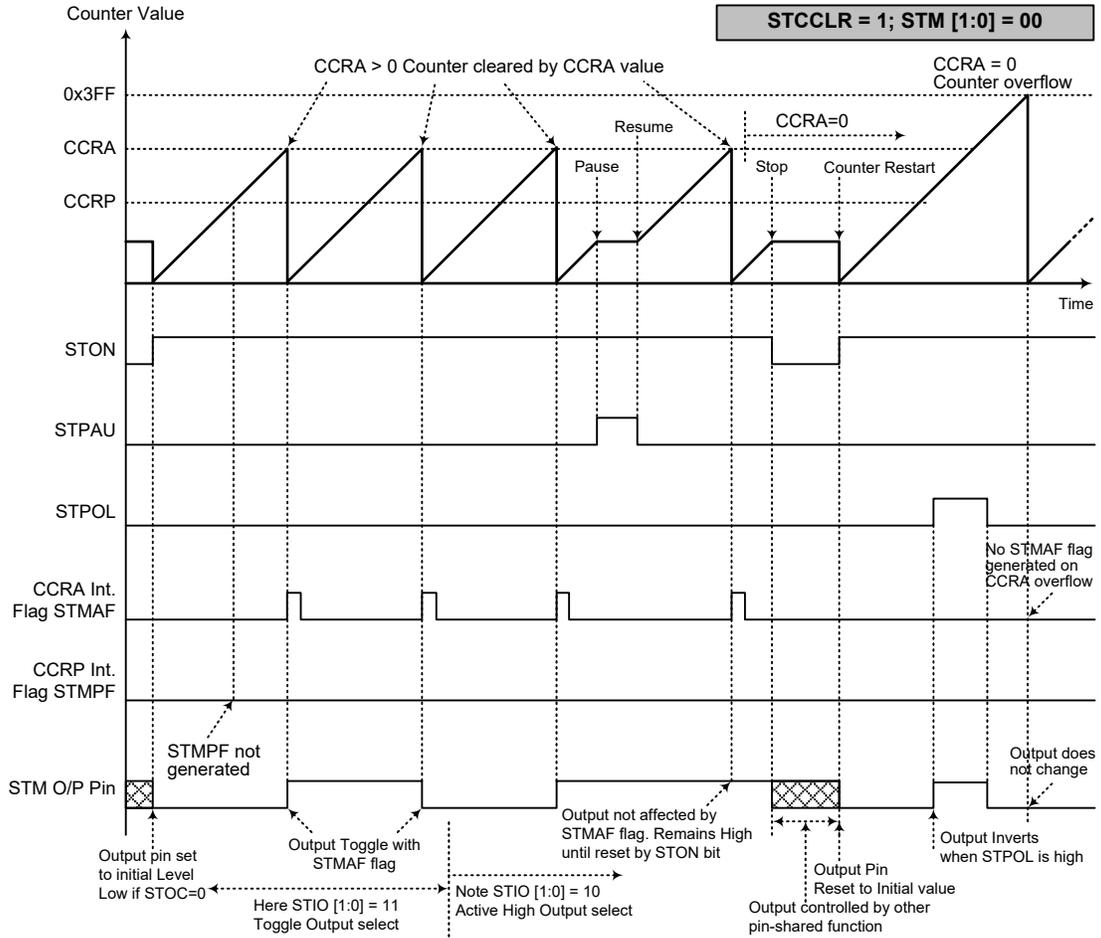
Compare Match Output Mode – STCCLR=1

Note: 1. With STCCLR=1, a Comparator A match will clear the counter

2. The STM output pin controlled only by the STMAF flag

3. The output pin reset to initial state by a STON rising edge

4. The STMPF flags is not generated when STCCLR=1

Timer/Counter Mode

To select this mode, bits STM1 and STM0 in the STMC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the STM output pin is not used. Therefore the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the STM output pin is not used in this mode, the pin can be used as a normal I/O pin or other pin-shared function.

PWM Output Mode

To select this mode, bits STM1 and STM0 in the STMC1 register should be set to 10 respectively. The PWM function within the STM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the STM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM Output mode, the STCCLR bit has no effect as the PWM period. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. Which register is used to control either frequency or duty cycle is determined using the STDPX bit in the STMC1 register. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The STOC bit in the STMC1 register is used to select the required polarity of the PWM waveform while the two STIO1 and STIO0 bits are used to enable the PWM output or to force the STM output pin to a fixed high or low level. The STPOL bit is used to reverse the polarity of the PWM output waveform.

• **10-bit STM, PWM Output Mode, Edge-aligned Mode, STDPX=0**

CCRP	1~7	0
Period	CCRP×128	1024
Duty	CCRA	

If f_{SYS}=8MHz, STM clock source is f_{SYS}/4, CCRP=2, CCRA=128,

The STM PWM output frequency=(f_{SYS}/4)/(2×128)=f_{SYS}/1024=8kHz, duty=128/(2×128)=50%.

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

• **10-bit STM, PWM Output Mode, Edge-aligned Mode, STDPX=1**

CCRP	1~7	0
Period	CCRA	
Duty	CCRP×128	1024

The PWM output period is determined by the CCRA register value together with the STM clock while the PWM duty cycle is defined by the CCRP register value.
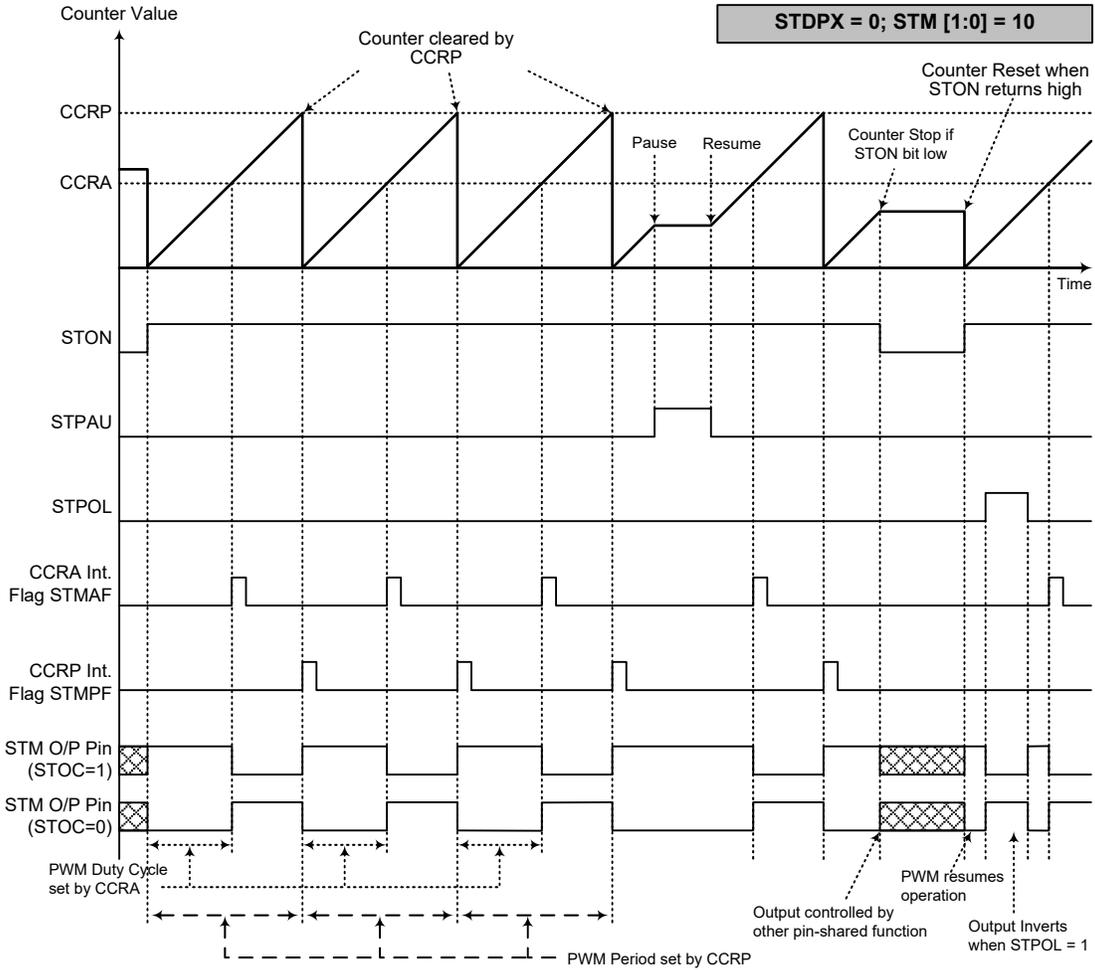
PWM Output Mode – STDPX=0

Note: 1. Here STDPX=0 – Counter cleared by CCRP

2. A counter clear sets PWM Period

3. The internal PWM function continues running even when STIO[1:0]=00 or 01

4. The STCCLR bit has no influence on PWM operation
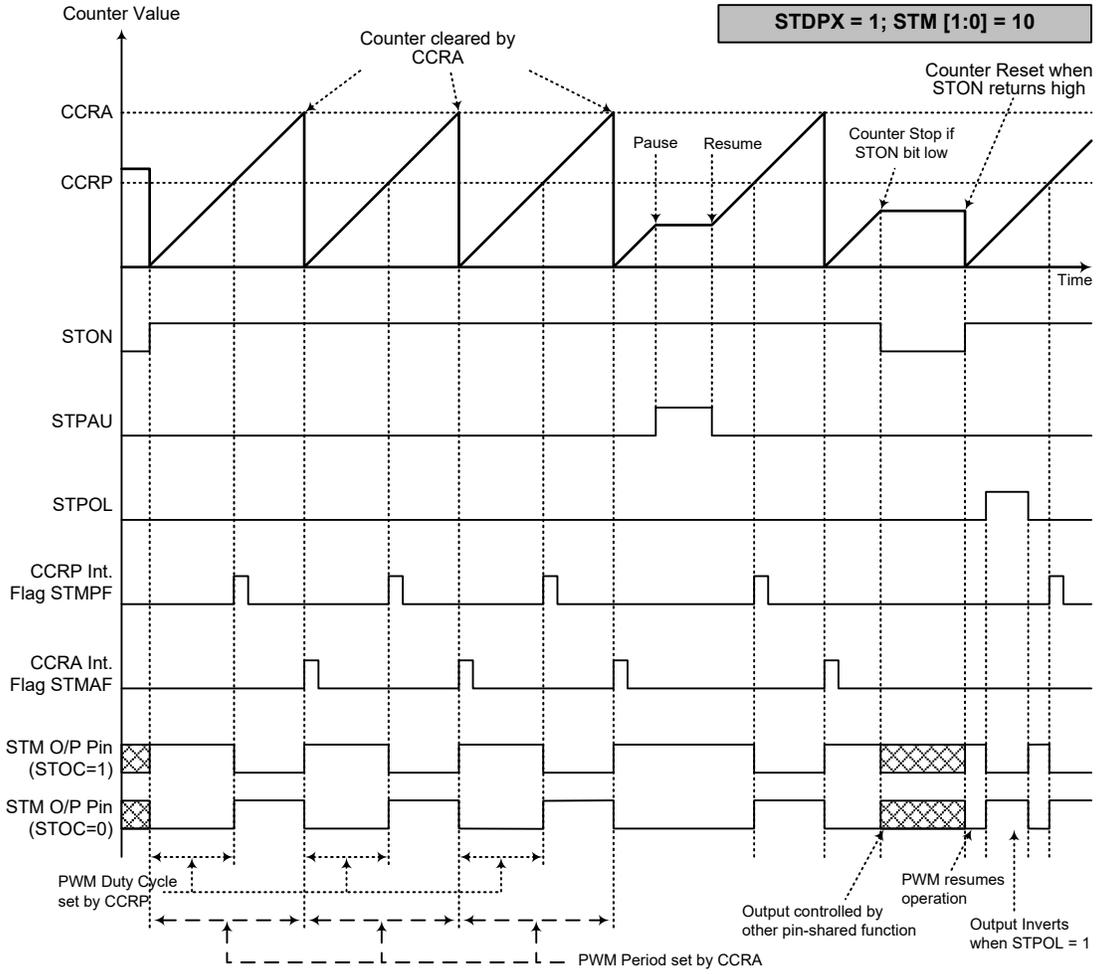
PWM Output Mode – STDPX=1

Note: 1. Here STDPX=1 – Counter cleared by CCRA

2. A counter clear sets PWM Period

3. The internal PWM function continues even when STIO[1:0]=00 or 01

4. The STCCLR bit has no influence on PWM operation

Single Pulse Output Mode

To select this mode, bits STM1 and STM0 in the STMC1 register should be set to 10 respectively and also the STIO1 and STIO0 bits should be set to 11 respectively. The Single Pulse Output Mode, as the name suggests, will generate a single shot pulse on the STM output pin.

The trigger for the pulse output leading edge is a low to high transition of the STON bit, which can be implemented using the application program. However in the Single Pulse Output Mode, the STON bit can also be made to automatically change from low to high using the external STCK pin, which will in turn initiate the Single Pulse output. When the STnON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated. The STON bit should remain high when the pulse is in its active state. The generated pulse trailing edge will be generated when the STON bit is cleared to zero, which can be implemented using the application program or when a compare match occurs from Comparator A.

However a compare match from Comparator A will also automatically clear the STON bit and thus generate the Single Pulse output trailing edge. In this way the CCRA value can be used to control the pulse width. A compare match from Comparator A will also generate an STM interrupt. The counter can only be reset back to zero when the STON bit changes from low to high when the counter restarts. In the Single Pulse Output Mode CCRP is not used. The STCCLR and STDPX bits are not used in this mode.

Single Pulse Generation
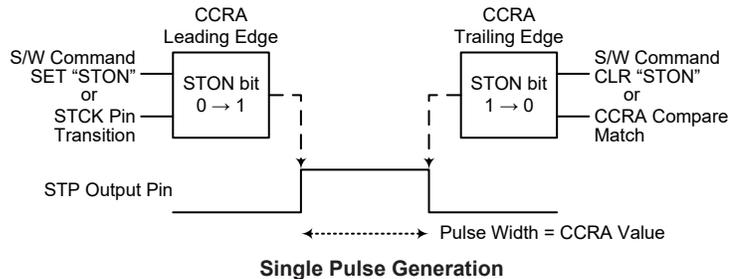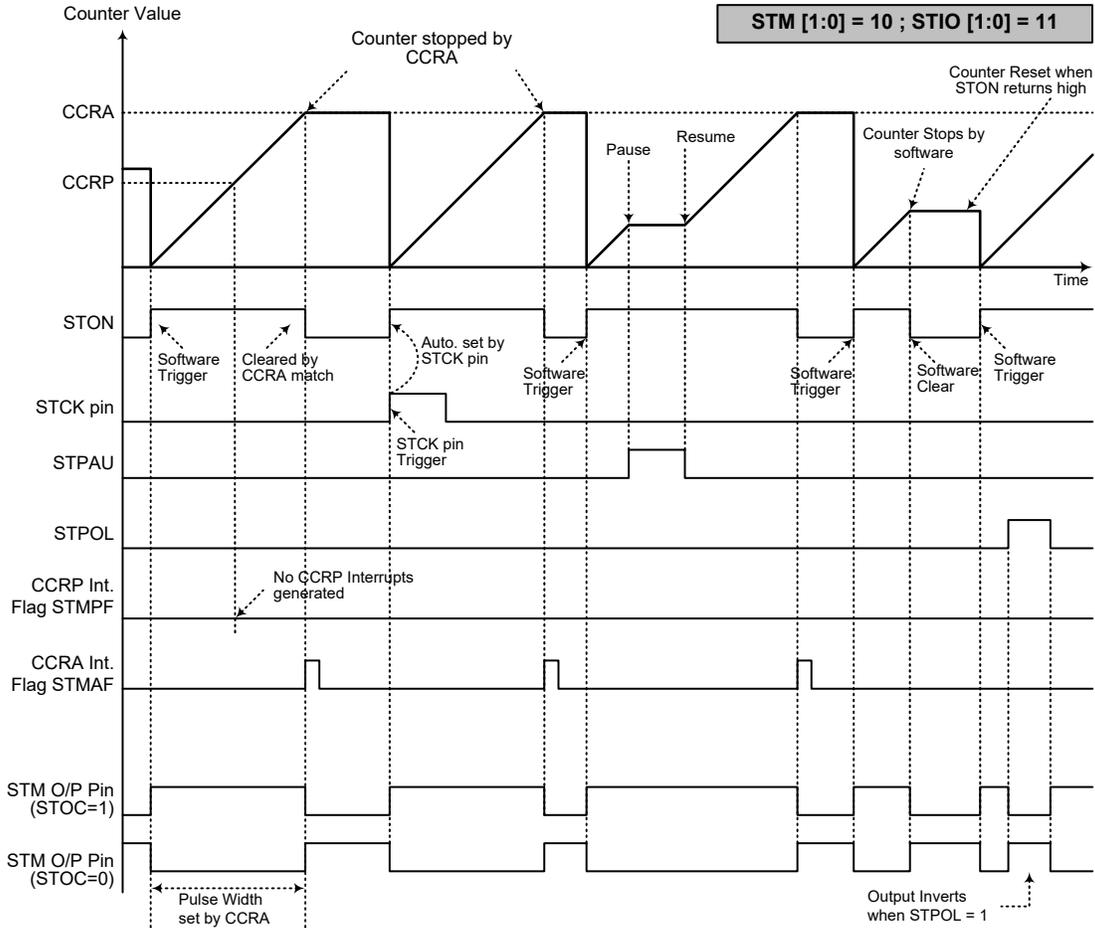
Single Pulse Output Mode

Note: 1. Counter stopped by CCRA

2. CCRP is not used

3. The pulse triggered by the STCK pin or by setting the STON bit high

4. An STCK pin active edge will automatically set the STON bit high

5. In the Single Pulse Output Mode, STIO [1:0] must be set to "11" and can not be changed

Capture Input Mode

To select this mode bits STM1 and STM0 in the STMC1 register should be set to 01 respectively. This mode enables external signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurements. The external signal is supplied on the STPI pin, whose active edge can be a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the STIO1 and STIO0 bits in the STMC1 register. The counter is started when the STON bit changes from low to high which is initiated using the application program.

When the required edge transition appears on the STPI pin the present value in the counter will be latched into the CCRA registers and an STM interrupt generated. Irrespective of what events occur on the STPI pin the counter will continue to free run until the STON bit changes from high to low. When a CCRP compare match occurs the counter will reset back to zero; in this way the CCRP value can be used to control the maximum counter value. When a CCRP compare match occurs from Comparator P, an STM interrupt will also be generated. Counting the number of overflow interrupt signals from the CCRP can be a useful method in measuring long pulse widths. The STIO1 and STIO0 bits can select the active trigger edge on the STPI pin to be a rising edge, falling edge or both edge types. If the STIO1 and STIO0 bits are both set high, then no capture operation will take place irrespective of what happens on the STPI pin, however it must be noted that the counter will continue to run. The STCCLR and STDPX bits are not used in this mode.

There are some considerations that should be noted. If the captured pulse width is less than 2 timer clock periods, it may be ignored by hardware. After the counter value is latched to the CCRA registers by an active capture edge, the STMAF flag will be set high after 0.5 timer clock period. The dalay time from the active capture edge received to the action of latching counter value to CCRA registers is less than 1.5 timer clock periods.
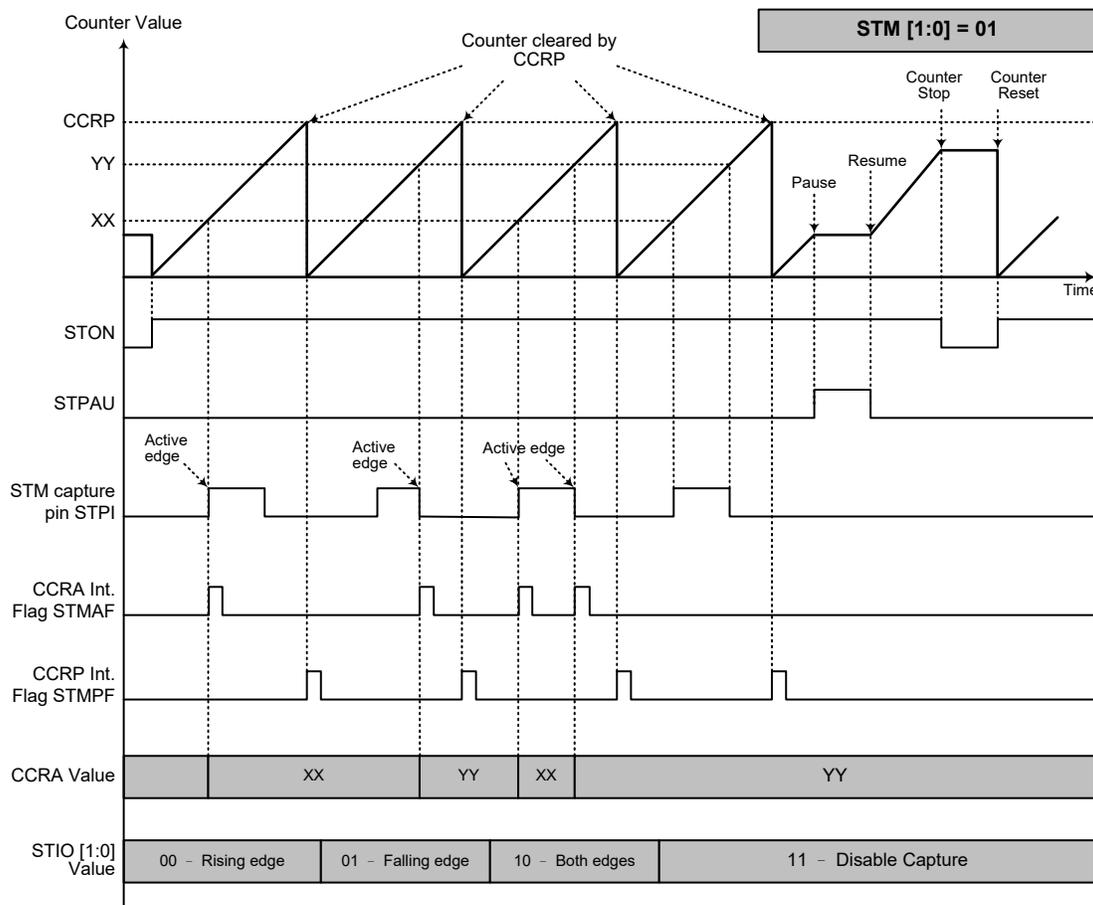
Capture Input Mode

Note: 1. STM [1:0]=01 and active edge set by the STIO [1:0] bits

2. An STM Capture input pin active edge transfers the counter value to CCRA

3. STCCLR bit not used

4. No output function – STOC and STPOL bits are not used

5. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero

6. The capture input mode cannot be used if the selected STM counter clock is not available

Periodic Type TM – PTM

The Periodic Type TM contains five operating modes, which are Compare Match Output, Timer/ Event Counter, Capture Input, Single Pulse Output and PWM Output modes. The Periodic TMs can be controlled with two external input pins and can drive two external output pins.

Note: 1. The CXCAP is the PowerLine Transceiver comparator output signal.

2. The PTPI signal can be from from the internal CXCAP signal, which is selected using the IFS0[7:6] bits.

3. As the PTM external pins are pin-shared with other functions, so before using the PTM function, ensure that the relevant pin-shared function registers have be set properly to enable the PTM pin function. The PTCK pin, if used, must also be set as an input by setting the corresponding bits in the port control register.

4. The PTPB is the inverted signal of the PTP.

Periodic Type TM Block Diagram

Periodic TM Operation

The Periodic Type TM core is a 10-bit count-up counter which is driven by a user selectable internal or external clock source. There are also two internal comparators with the names, Comparator A and Comparator P. These comparators will compare the value in the counter with CCRA and CCRP registers. The CCRA and CCRP comparators are 10-bit wide whose value is respectively compared with all counter bits.

The only way of changing the value of the 10-bit counter using the application program, is to clear the counter by changing the PTON bit from low to high. The counter will also be cleared automatically by a counter overflow or a compare match with one of its associated comparators. When these conditions occur, a PTM interrupt signal will also usually be generated. The Periodic Type TM can operate in a number of different operational modes and can be driven by different clock sources including two input pins and also control two output pins. All operating setup conditions are selected using relevant internal registers.

Periodic Type TM Register Description

Overall operation of the Periodic Type TM is controlled using a series of registers. A read only register pair exists to store the internal 10-bit counter value, while three read/write register pairs exist to store the internal 10-bit CCRA value, CCRP value and CCRB value. The remaining three registers are control registers which setup the different operating and control modes.

Register	Bit							
Name	7	6	5	4	3	2	1	0
PTMC0	PTPAU	PTCK2	PTCK1	PTCK0	PTON	—	—	—
PTMC1	PTM1	PTM0	PTIO1	PTIO0	PTOC	PTPOL	PTCAPTS	PTCCLR
PTMC2	—	—	—	—	—	PTTCLR1	PTTCLR0	PTVLF
PTMDL	D7	D6	D5	D4	D3	D2	D1	D0
PTMDH	—	—	—	—	—	—	D9	D8
PTMAL	D7	D6	D5	D4	D3	D2	D1	D0
PTMAH	—	—	—	—	—	—	D9	D8
PTMBL	D7	D6	D5	D4	D3	D2	D1	D0
PTMBH	—	—	—	—	—	—	D9	D8
PTMRPL	D7	D6	D5	D4	D3	D2	D1	D0
PTMRPH	—	—	—	—	—	—	D9	D8

10-bit Periodic TM Register List

- **PTMC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PTPAU	PTCK2	PTCK1	PTCK0	PTON	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	—	—	—
POR	0	0	0	0	0	—	—	—

Bit 7   **PTPAU**: PTM counter pause control

       0: Run

       1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the PTM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

Bit 6~4   **PTCK2~PTCK0**: PTM counter clock selection

       000: $f_{SYS}/4$

       001: f_{SYS}

       010: $f_H/16$

       011: $f_H/64$

       100: f_{SUB}

       101: f_{SUB}

       110: PTCK rising edge clock

       111: PTCK falling edge clock

These three bits are used to select the clock source for the PTM. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source f_{SYS} is the system clock, while f_H and f_{SUB} are other internal clocks, the details of which can be found in the oscillator section.

Bit 3   **PTON**: PTM counter on/off control

       0: Off

       1: On

This bit controls the overall on/off function of the PTM. Setting the bit high enables the counter to run, clearing the bit disables the PTM. Clearing this bit to zero will stop the counter from counting and turn off the PTM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again.

If the PTM is in the Compare Match Output Mode, PWM output Mode or Single Pulse Output Mode then the PTM output pin will be reset to its initial condition, as specified by the PTOC bit, when the PTON bit changes from low to high.

Bit 2~0   Unimplemented, read as "0"

• **PTMC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	PTM1	PTM0	PTIO1	PTIO0	PTOC	PTPOL	PTCAPTS	PTCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **PTM1~PTM0**: PTM operating mode selection

    00: Compare Match Output Mode

    01: Capture Input Mode

    10: PWM Output Mode or Single Pulse Output Mode

    11: Timer/Counter Mode

These bits setup the required operating mode for the PTM. To ensure reliable operation the PTM should be switched off before any changes are made to the PTM1 and PTM0 bits. In the Timer/Counter Mode, the PTM output pin state is undefined.

Bit 5~4   **PTIO1~PTIO0**: PTM external pin function selection

Compare Match Output Mode

    00: No change

    01: Output low

    10: Output high

    11: Toggle output

PWM Output Mode/Single Pulse Output Mode

    00: PWM output inactive state

    01: PWM output active state

    10: PWM output

    11: Single pulse output

Capture Input Mode

PTTCLR[1:0]=00B:

    00: Input capture at rising edge of CXCAP or PTCK, and the counter value will be latched into CCRA

    01: Input capture at falling edge of CXCAP or PTCK, and the counter value will be latched into CCRA

    10: Input capture at both falling and rising edges of CXCAP or PTCK, and the counter value will be latched into CCRA

    11: Input capture disabled

PTTCLR[1:0]=01B, 10B or 11B:

    00: Input capture at rising edge of CXCAP or PTCK, and the counter value will be latched into CCRB

    01: Input capture at falling edge of CXCAP or PTCK, and the counter value will be latched into CCRA

    10: Input capture at both falling and rising edges of CXCAP or PTCK, and the counter value will be latched into CCRA at falling edge or CCRB at rising edge

    11: Input capture disabled

Timer/Counter Mode

    Unused

These two bits are used to determine how the PTM functions when a certain condition is reached. The function that these bits select depends upon in which mode the PTM is running.

In the Compare Match Output Mode, the PTIO1 and PTIO0 bits determine how the PTM output pin changes state when a compare match occurs from the Comparator A. The PTM output can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the PTM output should be setup using the PTOC bit in the PTMC1 register. Note that the output level requested by the PTIO1 and PTIO0 bits must be different from the initial value setup using the PTOC bit otherwise no change will occur on the PTM noutput when a

compare match occurs. After the PTM output pin changes state, it can be reset to its initial level by changing the level of the PTON bit from low to high.

In the PWM Output Mode, the PTIO1 and PTIO0 bits determine how the PTM output changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to change the values of the PTIO1 and PTIO0 bits only after the PTM has been switched off. Unpredictable PWM outputs will occur if the PTIO1 and PTIO0 bits are changed when the PTM is running.

Bit 3   **PTOC**: PTM PTP output control bit

Compare Match Output Mode
   0: Initial low
   1: Initial high

PWM Output Mode/Single Pulse Output Mode
   0: Active low
   1: Active high

This is the output control bit for the PTM output. Its operation depends upon whether PTM is being used in the Compare Match Output Mode or in the PWM Output Mode/ Single Pulse Output Mode. It has no effect if the PTM is in the Timer/Counter Mode. In the Compare Match Output Mode, it determines the logic level of the PTM output before a compare match occurs. In the PWM Output Mode it determines if the PWM signal is active high or active low. In the Single Pulse Output Mode, it determines the logic level of the PTM output when the PTON bit changes from low to high.

Bit 2   **PTPOL**: PTM PTP output polarity control
   0: Non-invert
   1: Invert

This bit controls the polarity of the PTP output. When the bit is set high the PTM output will be inverted and not inverted when the bit is zero. It has no effect if the PTM is in the Timer/Counter Mode.

Bit 1   **PTCAPTS**: PTM capture trigger source selection
   0: From the internal CXCAP signal, selected using the IFS0[7:6] bits
   1: From the PTCK pin

Bit 0   **PTCCLR**: PTM counter clear condition selection
   0: PTM Comparator P match
   1: PTM Comparator A match

This bit is used to select the method which clears the counter. Remember that the Periodic TM contains two comparators, Comparator A and Comparator P, either of which can be selected to clear the internal counter. With the PTCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The PTCCLR bit is not used in the PWM Output Mode, Single Pulse Output Mode or Capture Input Mode.

• **PTMC2 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	PTTCLR1	PTTCLR0	PTVLF
R/W	—	—	—	—	—	R/W	R/W	R
POR	—	—	—	—	—	0	0	0

Bit 7~3   Unimplemented, read as "0"

Bit 2~1   **PTTCLR1~PTTCLR0**: PTM counter clear condition selection (Capture Input Mode only)
        00: Comparator P match
        01: Comparator P match or PTCK/CXCAP rising edge
        10: Comparator P match or PTCK/CXCAP falling edge
        11: Comparator P match or PTCK/CXCAP dual edges

    Note that these bit selections can be available only when the PTM operates in the Capture Input Mode.

Bit 0   **PTVLF**: PTM counter value latch edge flag
        0: Falling edge triggers the counter value latch
        1: Rising edge triggers the counter value latch

    When the PTTCLR1~PTTCLR0 bits are equal to 00B, ignore this flag status.

• **PTMDL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: PTM Counter Low Byte Register bit 7 ~ bit 0
    PTM 10-bit Counter bit 7 ~ bit 0

• **PTMDH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R	R
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"

Bit 1~0   **D9~D8**: PTM Counter High Byte Register bit 1 ~ bit 0
    PTM 10-bit Counter bit 9 ~ bit 8

• **PTMAL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: PTM CCRA Low Byte Register bit 7 ~ bit 0
    PTM 10-bit CCRA bit 7 ~ bit 0

• **PTMAH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"
Bit 1~0   **D9~D8**: PTM CCRA High Byte Register bit 1 ~ bit 0
PTM 10-bit CCRA bit 9 ~ bit 8

• **PTMBL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: PTM CCRB Low Byte Register bit 7 ~ bit 0
PTM 10-bit CCRB bit 7 ~ bit 0

• **PTMBH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"
Bit 1~0   **D9~D8**: PTM CCRB High Byte Register bit 1 ~ bit 0
PTM 10-bit CCRB bit 9 ~ bit 8

• **PTMRPL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: PTM CCRP Low Byte Register bit 7 ~ bit 0
PTM 10-bit CCRP bit 7 ~ bit 0

• **PTMRPH Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	D9	D8
R/W	—	—	—	—	—	—	R/W	R/W
POR	—	—	—	—	—	—	0	0

Bit 7~2   Unimplemented, read as "0"
Bit 1~0   **D9~D8**: PTM CCRP High Byte Register bit 1 ~ bit 0
PTM 10-bit CCRP bit 9 ~ bit 8

Periodic Type TM Operating Modes

The Periodic Type TM can operate in one of five operating modes, Compare Match Output Mode, PWM Output Mode, Single Pulse Output Mode, Capture Input Mode or Timer/Counter Mode. The operating mode is selected using the PTM1 and PTM0 bits in the PTMC1 register.
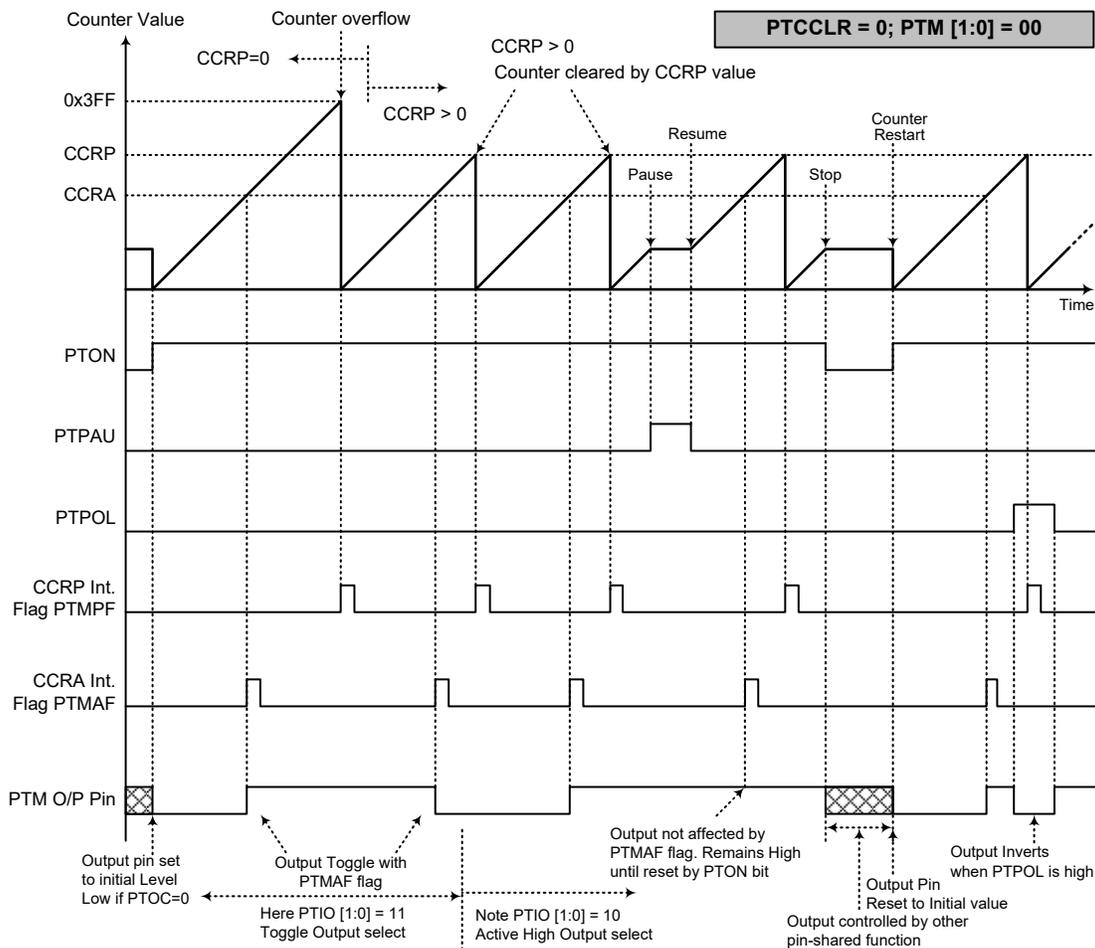
Compare Match Output Mode

To select this mode, bits PTM1 and PTM0 in the PTMC1 register, should be set to 00 respectively. In this mode once the counter is enabled and running it can be cleared by three methods. These are a counter overflow, a compare match from Comparator A and a compare match from Comparator P. When the PTCCLR bit is low, there are two ways in which the counter can be cleared. One is when a compare match from Comparator P, the other is when the CCRP bits are all zero which allows the counter to overflow. Here both PTMAF and PTMPF interrupt request flags for Comparator A and Comparator P respectively, will both be generated.

If the PTCCLR bit in the PTMC1 register is high then the counter will be cleared when a compare match occurs from Comparator A. However, here only the PTMAF interrupt request flag will be generated even if the value of the CCRP bits is less than that of the CCRA registers. Therefore when PTCCLR is high no PTMPF interrupt request flag will be generated. In the Compare Match Output Mode, the CCRA can not be cleared to zero.

If the CCRA bits are all zero, the counter will overflow when its reaches its maximum 3FF Hex value, however here the PTMAF interrupt request flag will not be generated.

As the name of the mode suggests, after a comparison is made, the PTM output will change state. The PTM output condition however only changes state when a PTMAF interrupt request flag is generated after a compare match occurs from Comparator A. The PTMPF interrupt request flag, generated from a compare match occurs from Comparator P, will have no effect on the PTM output. The way in which the PTM output changes state are determined by the condition of the PTIO1 and PTIO0 bits in the PTMC1 register. The PTM output can be selected using the PTIO1 and PTIO0 bits to go high, to go low or to toggle from its present condition when a compare match occurs from Comparator A. The initial condition of the PTM output, which is setup after the PTON bit changes from low to high, is setup using the PTOC bit. Note that if the PTIO1 and PTIO0 bits are zero then no output change will take place.

Compare Match Output Mode – PTCCLR=0

Note: 1. With PTCCLR=0 a Comparator P match will clear the counter

2. The PTM output is controlled only by the PTMAF flag

3. The output is reset to its initial state by a PTON bit rising edge
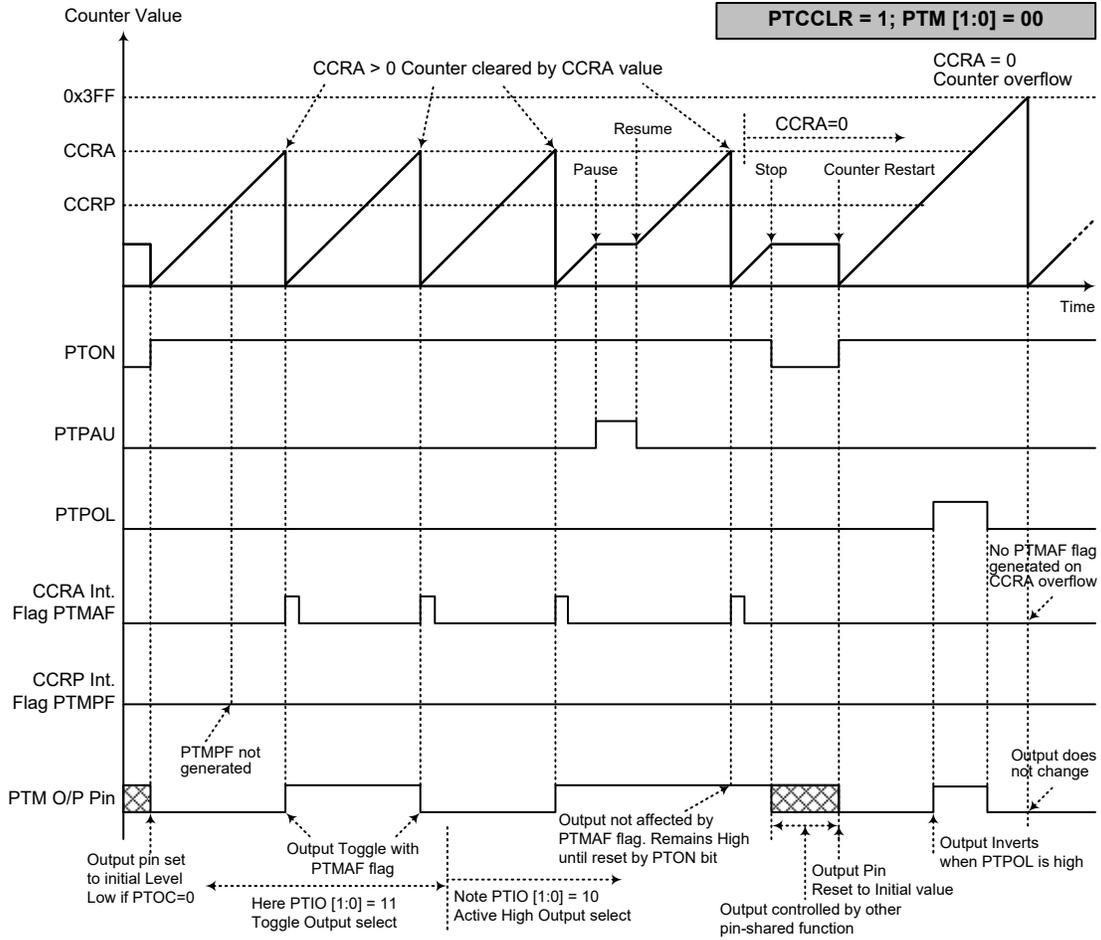
Compare Match Output Mode – PTCCLR=1

Note: 1. With PTCCLR=1 a Comparator A match will clear the counter

2. The PTM output is controlled only by the PTMAF flag

3. The output is reset to its initial state by a PTON bit rising edge

4. A PTMPF flag is not generated when PTCCLR=1

Timer/Counter Mode

To select this mode, bits PTM1 and PTM0 in the PTMC1 register should be set to 11 respectively. The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the PTM output pins are not used. Therefore, the above description and Timing Diagrams for the Compare Match Output Mode can be used to understand its function. As the PTM output pins are not used in this mode, the pins can be used as normal I/O pins or other pin-shared functions.

PWM Output Mode

To select this mode, bits PTM1 and PTM0 in the PTMC1 register should be set to 10 respectively. The PWM function within the PTM is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the PTM output pin, a square wave AC waveform can be generated with varying equivalent DC RMS values.

As both the period and duty cycle of the PWM waveform can be controlled, the choice of generated waveform is extremely flexible. In the PWM Output Mode, the PTCCLR bit has no effect on the PWM operation. Both of the CCRA and CCRP registers are used to generate the PWM waveform, one register is used to clear the internal counter and thus control the PWM waveform frequency, while the other one is used to control the duty cycle. The PWM waveform frequency and duty cycle can therefore be controlled by the values in the CCRA and CCRP registers.

An interrupt flag, one for each of the CCRA and CCRP, will be generated when a compare match occurs from either Comparator A or Comparator P. The PTOC bit in the PTMC1 register is used to select the required polarity of the PWM waveform while the two PTIO1 and PTIO0 bits are used to enable the PWM output or to force the PTM output to a fixed high or low level. The PTPOL bit is used to reverse the polarity of the PWM output waveform.
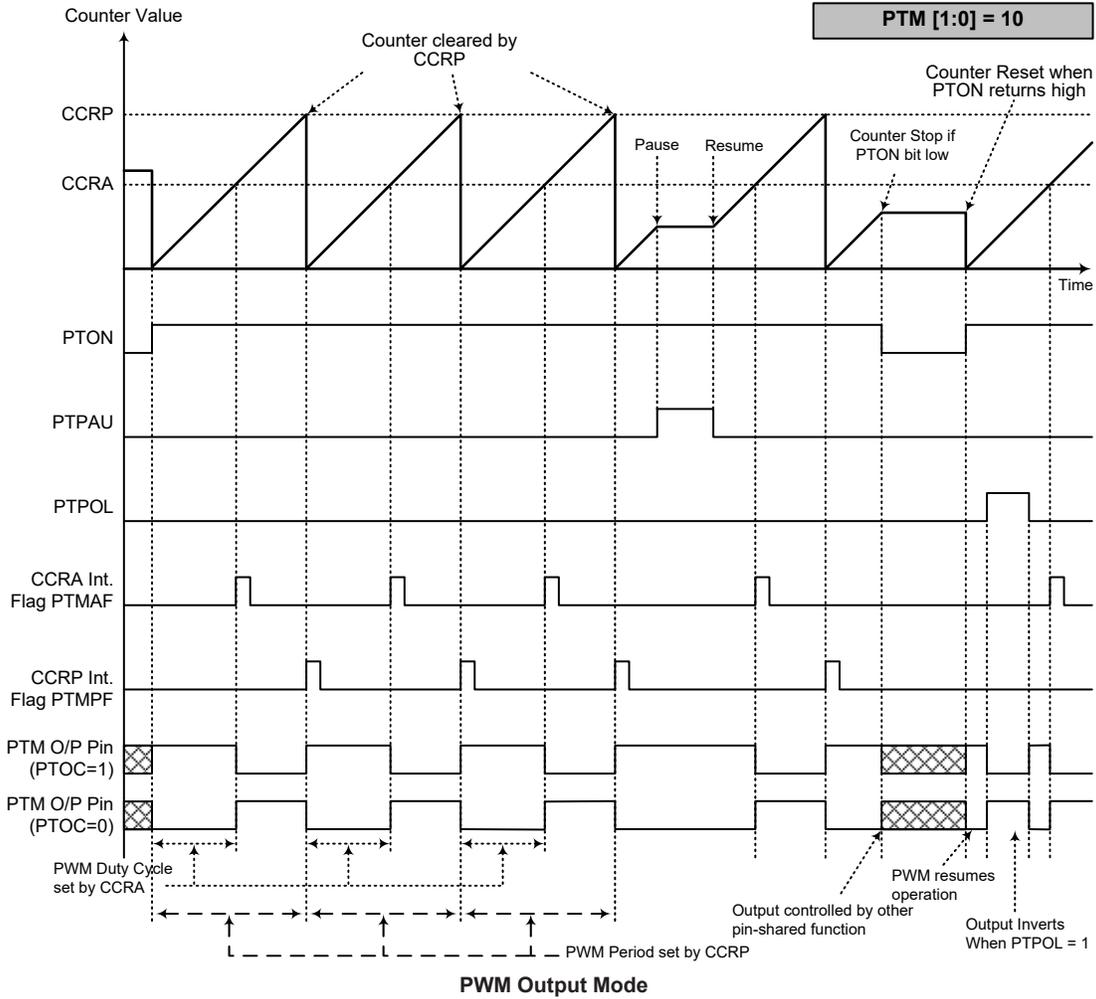
• 10-bit PTM, PWM Output Mode, Edge-aligned Mode

CCRP	1~1023	0
Period	1~1023	1024
Duty	CCRA	

If f_{SYS}=8MHz, PTM clock source select f_{SYS}/4, CCRP=512 and CCRA=128,

The PTM PWM output frequency=(f_{SYS}/4)/512=f_{SYS}/2048=4kHz, duty=128/512=25%.

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.
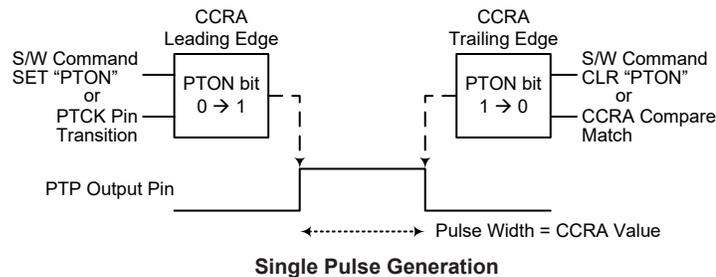
PWM Output Mode

Note: 1. Counter cleared by CCRP

2. A counter clear sets the PWM Period

3. The internal PWM function continues running even when PTIO[1:0]=00 or 01

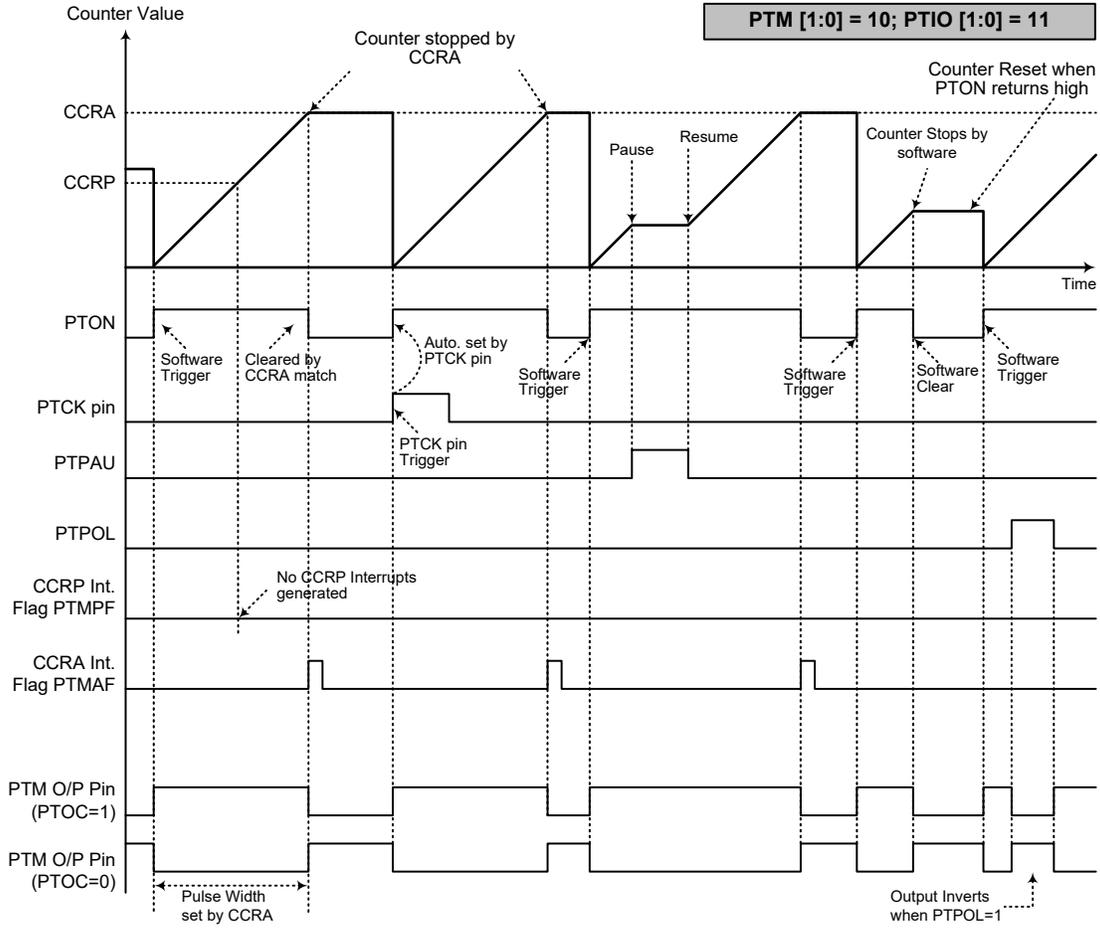4. The PTCCLR bit has no influence on PWM operation

Single Pulse Output Mode

To select this mode, bits PTM1 and PTM0 in the PTMC1 register should be set to 10 respectively and also the PTIO1 and PTIO0 bits should be set to 11 respectively. The Single Pulse Output Mode, as the name suggests, will generate a single shot pulse on the PTM output pin.

The trigger for the pulse output leading edge is a low to high transition of the PTON bit, which can be implemented using the application program. However, in the Single Pulse Mode, the PTON bit can also be made to automatically change from low to high using the external PTCK pin, which will in turn initiate the Single Pulse output. When the PTON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated. The PTON bit should remain high when the pulse is in its active state. The generated pulse trailing edge will be generated when the PTON bit is cleared to zero, which can be implemented using the application program or when a compare match occurs from Comparator A.

However, a compare match from Comparator A will also automatically clear the PTON bit and thus generate the Single Pulse output trailing edge. In this way the CCRA value can be used to control the pulse width. A compare match from Comparator A will also generate a PTM interrupt. The counter can only be reset back to zero when the PTON bit changes from low to high when the counter restarts. In the Single Pulse Output Mode CCRP is not used. The PTCCLR bit is not used in this Mode.

Single Pulse Generation

Single Pulse Output Mode

Note: 1. Counter stopped by CCRA

2. CCRP is not used

3. The pulse is triggered by the PTCK pin or by setting the PTON bit high

4. A PTCK pin active edge will automatically set the PTON bit high

5. In the Single Pulse Mode, PTIO[1:0] must be set to "11" and cannot be changed
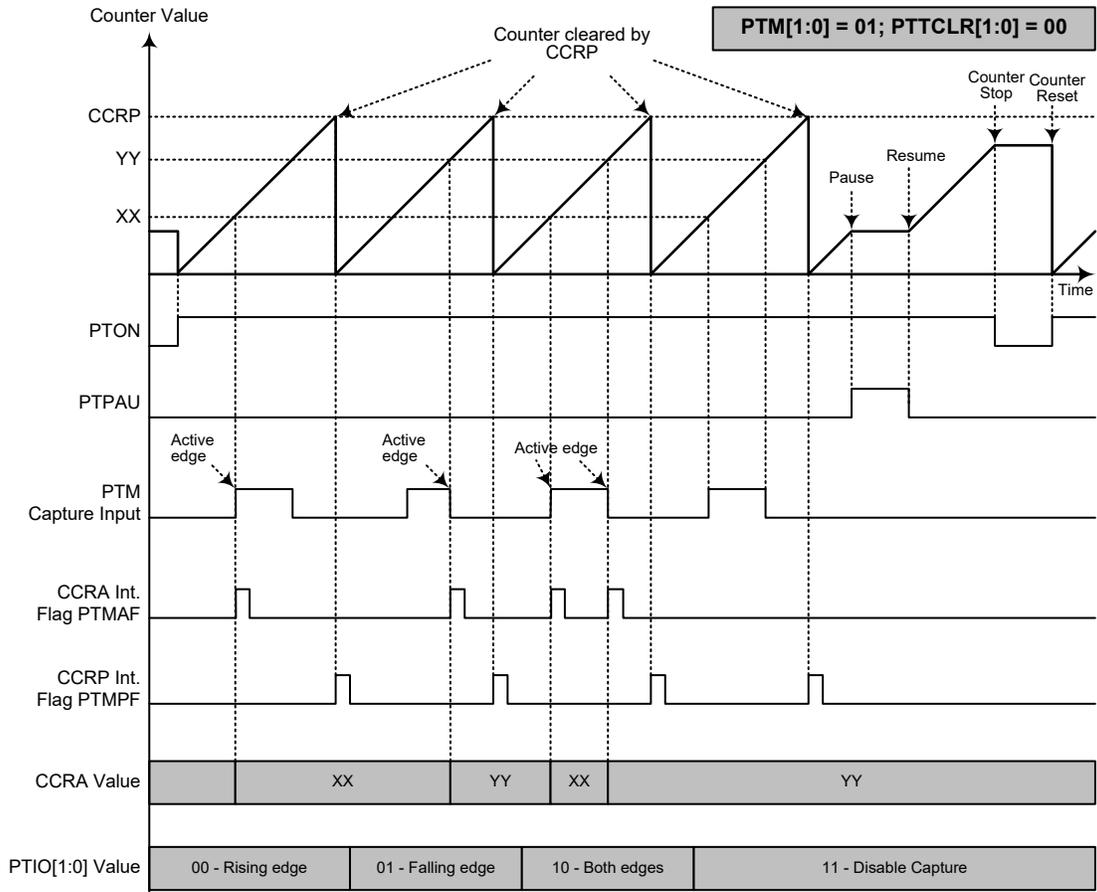
Capture Input Mode

To select this mode, bits PTM1 and PTM0 in the PTMC1 register should be set to 01 respectively. This mode enables external or internal signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurements. The external or internal signal is supplied on the PTCK pin or PTPI signal, which is selected using the PTCAPTS bit in the PTMC1 register. While the PTPI signal can be from the internal CXCAP signal, which is selected using the IFS0[7:6] bits in the IFS0 register. The input pin active edge can be either a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the PTIO1 and PTIO0 bits in the PTMC1 register. The counter is started when the PTON bit changes from low to high which is initiated using the application program.

The PTIO1 and PTIO0 bits decide which active edge transition type to latch counter value and generate an interrupt. The PTTCLR1 and PTTCLR0 bits decide the condition that the counter reset back to zero. The present counter value being latched into CCRA or CCRB is decided by both PTIO1~PTIO0 and PTTCLR1~PTTCLR0 settings. The PTIO1~PTIO0 and PTTCLR1~PTTCLR0 settings are independent and uninfluenced on each other.

When the required edge transition appears on the PTCK pin or CXCAP signal, the present value in the counter will be latched into the CCRA registers or CCRB registers and a PTM interrupt will be generated. Irrespective of what events occur on the PTCK pin or CXCAP signal, the counter will continue to free run until the PTON bit changes from high to low. When a CCRP compare match occurs the counter will reset back to zero; in this way the CCRP value can be used to control the maximum counter value. When a CCRP compare match occurs from Comparator P, a PTM interrupt will also be generated. Counting the number of overflow interrupt signals from the CCRP can be a useful method in measuring long pulse widths. The PTIO1 and PTIO0 bits can select the active trigger edge on the PTCK pin or CXCAP signal to be a rising edge, falling edge or both edge types. If the PTIO1 and PTIO0 bits are both set high, then no capture operation will take place irrespective of what happens on the PTCK pin or CXCAP signal, however it must be noted that the counter will continue to run. The PTCCLR, PTOC and PTPOL bits are not used in this mode.

There are some considerations that should be noted. If PTCK is used as the capture input source, then it cannot be selected as the PTM clock source. If the captured pulse width is less than 2 timer clock periods, it may be ignored by hardware. After the counter value is latched to the CCRA or CCRB registers by an active capture edge, the PTMAF flag will be set high and the PTVLF flag status will be changed after 0.5 timer clock period. The delay time from the active capture edge received to the action of latching counter value to CCRA or CCRB registers is less than 1.5 timer clock periods.

Capture Input Mode – PTTCLR[1:0]=00

Note: 1. PTM[1:0]=01, PTTCLR[1:0]=00 and active edge set by the PTIO[1:0] bits

2. A PTM capture input (PTCK pin or CXCAP signal) active edge transfers the counter value to CCRA

3. Comparator P match will clear the counter

4. PTCCLR bit is not used

5. No output function – PTOC and PTPOL bits are not used

6. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero

7. Ignore the PTVLF bit status when PTTCLR[1:0]=00

8. The capture input mode cannot be used if the selected PTM counter clock is not available
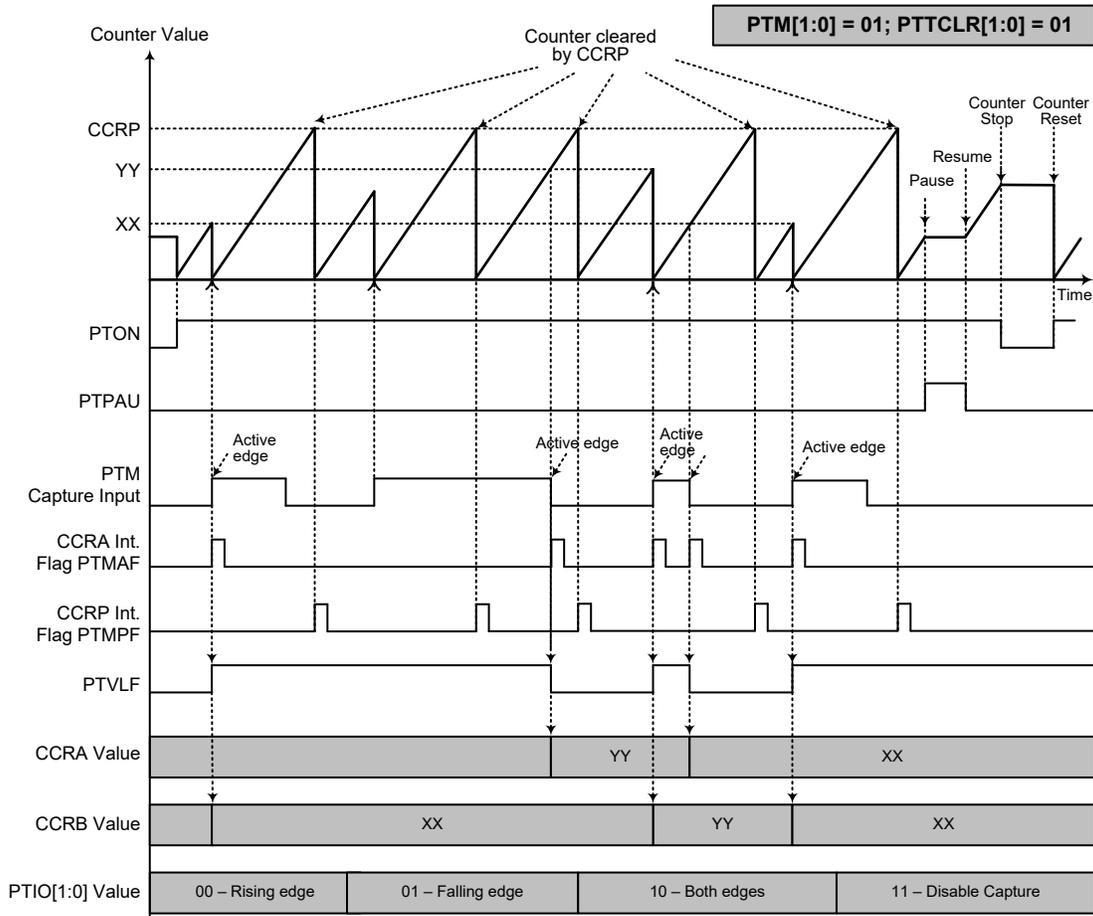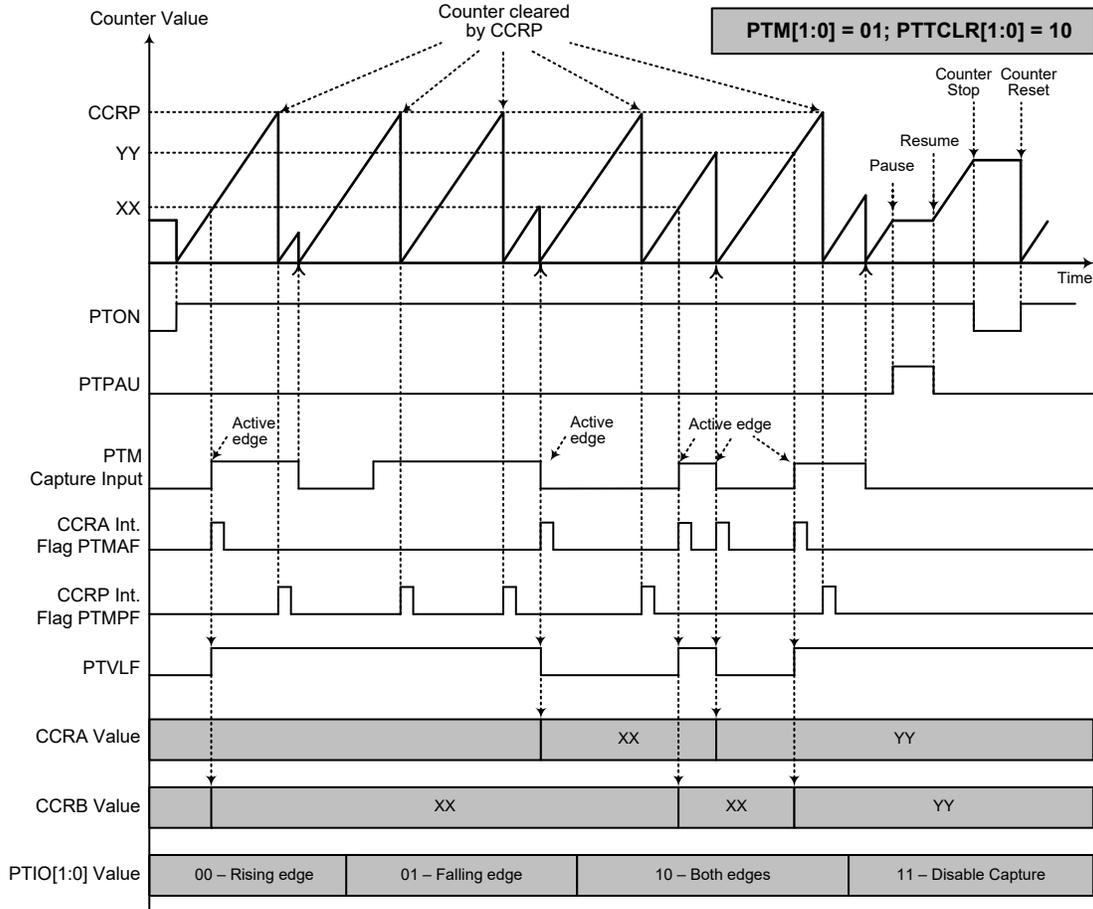
Capture Input Mode – PTTCLR[1:0]=01

Note: 1. PTM[1:0]=01, PTTCLR[1:0]=01 and active edge set by the PTIO[1:0] bits

2. A PTM capture input (PTCK pin or CXCAP signal) active edge transfers the counter value to CCRA or CCRB

3. Comparator P match or PTM capture input rising edge will clear the counter

4. PTCCLR bit is not used

5. No output function – PTOC and PTPOL bits are not used

6. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero

7. The capture input mode cannot be used if the selected PTM counter clock is not available

Capture Input Mode – PTTCLR[1:0]=10

Note: 1. PTM[1:0]=01, PTTCLR[1:0]=10 and active edge set by the PTIO[1:0] bits

2. A PTM capture input (PTCK pin or CXCAP signal) active edge transfers the counter value to CCRA or CCRB

3. Comparator P match or PTM capture input falling edge will clear the counter

4. PTCCLR bit is not used

5. No output function – PTOC and PTPOL bits are not used

6. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero

7. The capture input mode cannot be used if the selected PTM counter clock is not available
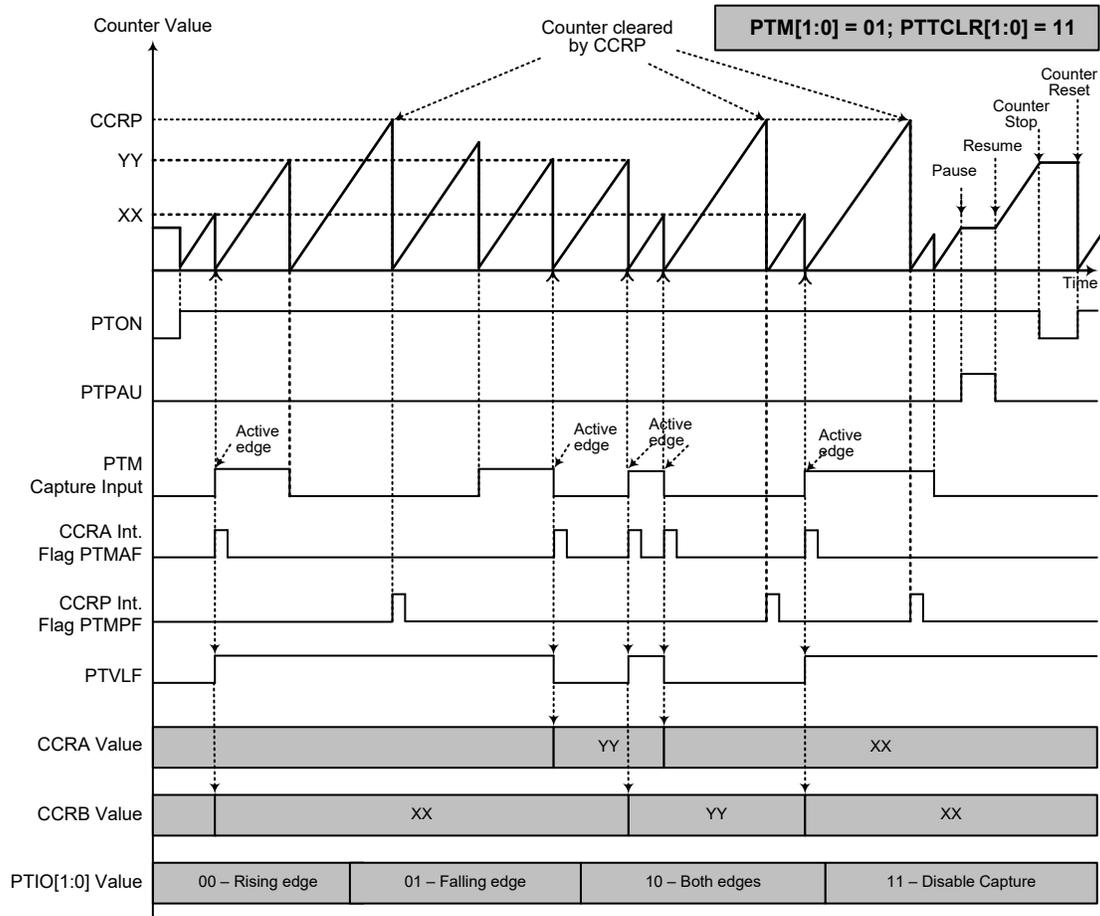
Capture Input Mode – PTTCLR[1:0]=11

Note: 1. PTM[1:0]=01, PTTCLR[1:0]=11 and active edge set by the PTIO[1:0] bits

2. A PTM capture input (PTCK pin or CXCAP signal) active edge transfers the counter value to CCRA or CCRB

3. Comparator P match or PTM capture input rising or falling edge will clear the counter

4. PTCCLR bit is not used

5. No output function – PTOC and PTPOL bits are not used

6. CCRP determines the counter value and the counter has a maximum count value when CCRP is equal to zero

7. The capture input mode cannot be used if the selected PTM counter clock is not available
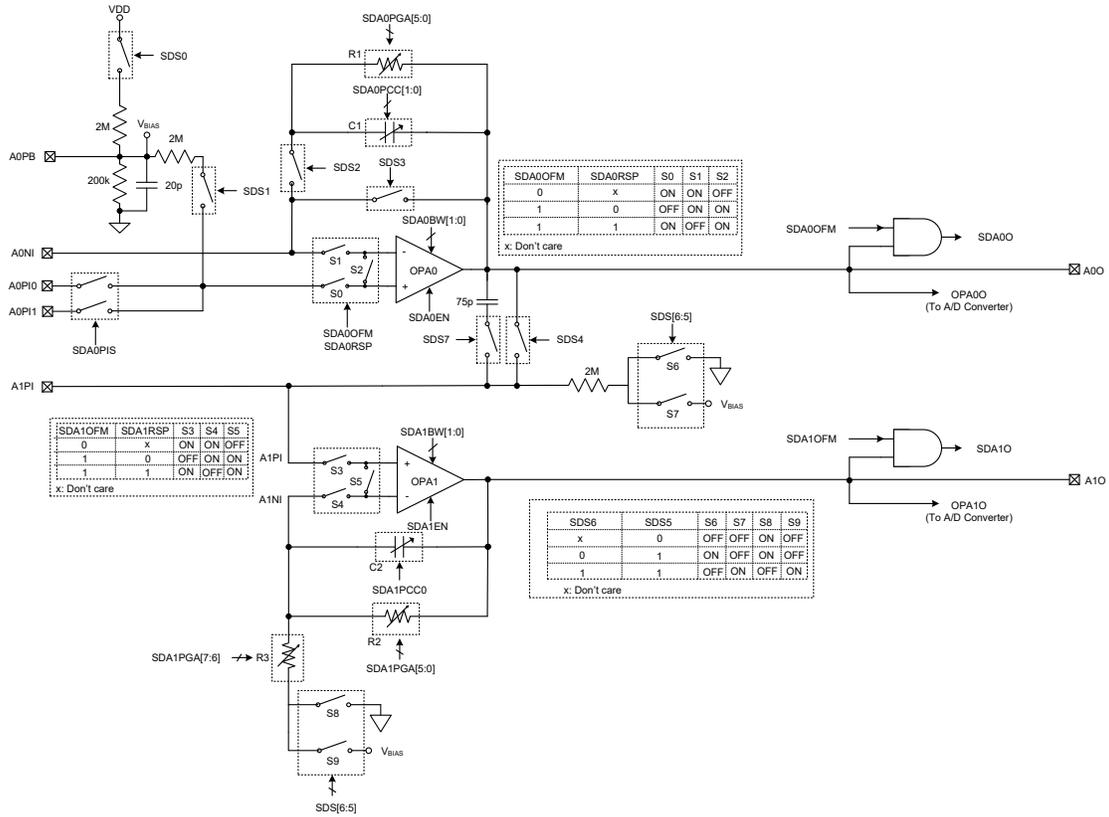
Smoke Detector AFE

The device provides a Smoke Detector AFE circuit which can be used for optical signal detection in Smoke Detector applications. The circuit consists of two fully integrated Operational Amplifiers. The optical signal can be detected and processed by the operational amplifiers.

SDA0OFM	SDA0RSP	S0	S1	S2
0	x	ON	ON	OFF
1	0	OFF	ON	ON
1	1	ON	OFF	ON

x: Don't care

SDA1OFM	SDA1RSP	S3	S4	S5
0	x	ON	ON	OFF
1	0	OFF	ON	ON
1	1	ON	OFF	ON

x: Don't care

SDS[6:5]		S6	S7

SDS6	SDS5	S6	S7	S8	S9
x	0	OFF	OFF	ON	OFF
0	1	ON	OFF	OFF	OFF
1	1	OFF	ON	OFF	ON

x: Don't care

Smoke Detector AFE Block Diagram

Note that although the SD OPAn bandwidth is determined by the SDAnBW1~SDAnBW0 bits there are some limitations when using the OPAn together with the A/D converter. As the OPAn bandwidth will result in a small current output, care must be taken for SD OPAn bandwidths. Refer to the following table for examples, where values marked with a "√" are usable and ensure that the values read by the 12-bit A/D converter are less than 1 LSB.

SD OPAn Bandwidth Selection	A/D Converter Clock Frequency (kHz)							
	15.625	31.25	62.5	125	250	500	1000	2000
SDAnBW[1:0]=00	√	—	—	—	—	—	—	—
SDAnBW[1:0]=01	√	√	√	√	—	—	—	—
SDAnBW[1:0]=10	√	√	√	√	√	√	√	√
SDAnBW[1:0]=11	√	√	√	√	√	√	√	√

Smoke Detector AFE SD OPAn Bandwidth Examples (n=0~1)

Smoke Detector AFE Registers

Overall operation of the Smoke Detector AFE circuit is controlled using a series of registers. The SDSW0 register is used to control the switches on or off thus controlling the OPAn operating mode. The SDSW1 register is used to select the OPA0 positive input channel and the C1, C2 capacitance. The SDPGAC0 and SDPGAC1 registers are used to select the R1, R2 and R3 resistance. The SDAnC register where n=0~1, is used to control the SD OPAn enable/disable and bandwidth functions as well as store the output status. The SDAnVOS register is used to select and control the SD OPAn input offset voltage calibration function.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SDSW0	SDS7	SDS6	SDS5	SDS4	SDS3	SDS2	SDS1	SDS0
SDSW1	SDA0PIS	—	SDA0PCC1	SDA0PCC0	—	—	—	SDA1PCC0
SDPGAC0	—	—	SDA0PGA5	SDA0PGA4	SDA0PGA3	SDA0PGA2	SDA0PGA1	SDA0PGA0
SDPGAC1	SDA1PGA7	SDA1PGA6	SDA1PGA5	SDA1PGA4	SDA1PGA3	SDA1PGA2	SDA1PGA1	SDA1PGA0
SDA0C	—	SDA0EN	SDA0O	—	—	—	SDA0BW1	SDA0BW0
SDA1C	—	SDA1EN	SDA1O	—	—	—	SDA1BW1	SDA1BW0
SDA0VOS	SDA0OFM	SDA0RSP	SDA0OF5	SDA0OF4	SDA0OF3	SDA0OF2	SDA0OF1	SDA0OF0
SDA1VOS	SDA1OFM	SDA1RSP	SDA1OF5	SDA1OF4	SDA1OF3	SDA1OF2	SDA1OF1	SDA1OF0

Smoke Detector AFE Register List

• **SDSW0 Register**

Bit	7	6	5	4	3	2	1	0
Name	SDS7	SDS6	SDS5	SDS4	SDS3	SDS2	SDS1	SDS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	0	0	0	0	0	0	0

Bit 7   **SDS7**: SDS7 switch on/off control
        0: Off
        1: On

Bit 6~5   **SDS6~SDS5**: Mode control
        00: External mode
        01: AC coupling mode
        10: External mode
        11: DC coupling mode (SDS1 cannot be on at the same time)

Bit 4   **SDS4**: SDS4 switch on/off control
        0: Off
        1: On

Bit 3   **SDS3**: SDS3 switch on/off control
        0: Off
        1: On

Bit 2   **SDS2**: SDS2 switch on/off control
        0: Off
        1: On

Bit 1   **SDS1**: SDS1 switch on/off control
        0: Off
        1: On

Bit 0   **SDS0**: SDS0 switch on/off control
        0: Off
        1: On

• **SDSW1 Register**

Bit	7	6	5	4	3	2	1	0
Name	SDA0PIS	—	SDA0PCC1	SDA0PCC0	—	—	—	SDA1PCC0
R/W	R/W	—	R/W	R/W	—	—	—	R/W
POR	0	—	0	0	—	—	—	0

Bit 7   **SDA0PIS**: SD OPA0 positive input selection
           0: A0PI0
           1: A0PI1
Bit 6   Unimplemented, read as "0"
Bit 5~4   **SDA0PCC1~SDA0PCC0**: SD OPA0 C1 control
           00: 20p
           01: 15p
           10: 10p
           11: 20p
Bit 3~1   Unimplemented, read as "0"
Bit 0   **SDA1PCC0**: SD OPA1 C2 control
           0: 30p
           1: 15p

• **SDPGAC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	SDA0PGA5	SDA0PGA4	SDA0PGA3	SDA0PGA2	SDA0PGA1	SDA0PGA0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6   Unimplemented, read as "0"
Bit 5~0   **SDA0PGA5~SDA0PGA0**: R1 control
           R1=(SDA0PGA[5:0]×100kΩ)
           These bits are used to select the R1 resistance value. Note that R1≠0Ω when these bits
           are set to "000000" due to the switch on-resistance.

• **SDPGAC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	SDA1PGA7	SDA1PGA6	SDA1PGA5	SDA1PGA4	SDA1PGA3	SDA1PGA2	SDA1PGA1	SDA1PGA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **SDA1PGA7~SDA1PGA6**: R3 control
           00: 10kΩ
           01: 20kΩ
           10: 30kΩ
           11: 40kΩ
Bit 5~0   **SDA1PGA5~SDA1PGA0**: R2 control
           R2=(SDA1PGA[5:0]×100kΩ)
           These bits are used to select the R2 resistance value. Note that R2≠0Ω when these bits
           are set to "000000" due to the switch on-resistance.

• **SDA0C Register**

Bit	7	6	5	4	3	2	1	0
Name	—	SDA0EN	SDA0O	—	—	—	SDA0BW1	SDA0BW0
R/W	—	R/W	R	—	—	—	R/W	R/W
POR	—	0	0	—	—	—	0	0

Bit 7   Unimplemented, read as "0"

Bit 6   **SDA0EN**: SD OPA0 enable or disable control
              0: Disable
              1: Enable

Bit 5   **SDA0O**: SD OPA0 output status (positive logic)
              This bit is read only.
              When the SDA0OFM bit is set to 1, SDA0O is defined as SD OPA0 output status, refer to the "Operational Amplifier Input Offset Calibration" section for details.
              When the SDA0OFM bit is cleared to 0, this bit will be fixed at a low level.

Bit 4~2   Unimplemented, read as "0"

Bit 1~0   **SDA0BW1~SDA0BW0**: SD OPA0 bandwidth control
              00: 5kHz
              01: 40kHz
              10: 600kHz
              11: 2MHz
              Refer to "Operational Amplifier Electrical Characteristics" for details.

• **SDA1C Register**

Bit	7	6	5	4	3	2	1	0
Name	—	SDA1EN	SDA1O	—	—	—	SDA1BW1	SDA1BW0
R/W	—	R/W	R	—	—	—	R/W	R/W
POR	—	0	0	—	—	—	0	0

Bit 7   Unimplemented, read as "0"

Bit 6   **SDA1EN**: SD OPA1 enable or disable control
              0: Disable
              1: Enable

Bit 5   **SDA1O**: SD OPA1 output status (positive logic)
              This bit is read only.
              When the SDA1OFM bit is set to 1, SDA1O is defined as SD OPA1 output status, refer to the "Operational Amplifier Input Offset Calibration" section for details.
              When the SDA1OFM bit is cleared to 0, this bit will be fixed at a low level.

Bit 4~2   Unimplemented, read as "0"

Bit 1~0   **SDA1BW1~SDA1BW0**: SD OPA1 bandwidth control
              00: 5kHz
              01: 40kHz
              10: 600kHz
              11: 2MHz
              Refer to "Operational Amplifier Electrical Characteristics" for details.

• **SDA0VOS Register**

Bit	7	6	5	4	3	2	1	0
Name	SDA0OFM	SDA0RSP	SDA0OF5	SDA0OF4	SDA0OF3	SDA0OF2	SDA0OF1	SDA0OF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	0	0	0	0	0

Bit 7   **SDA0OFM**: SD OPA0 normal operation or input offset voltage calibration mode selection
         0: Normal operation
         1: Offset calibration mode

Bit 6   **SDA0RSP**: SD OPA0 input offset voltage calibration reference selection
         0: Input reference voltage comes from A0NI
         1: Input reference voltage comes from A0PI

Bit 5~0   **SDA0OF5~SDA0OF0**: SD OPA0 input offset voltage calibration control
         This 6-bit field is used to perform the operational amplifier input offset calibration operation and the value for the SD OPA0 input offset Calibration can be restored into this bit field. More detailed information is described in the "Operational Amplifier Input Offset Calibration" section.

• **SDA1VOS Register**

Bit	7	6	5	4	3	2	1	0
Name	SDA1OFM	SDA1RSP	SDA1OF5	SDA1OF4	SDA1OF3	SDA1OF2	SDA1OF1	SDA1OF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	0	0	0	0	0

Bit 7   **SDA1OFM**: SD OPA1 normal operation or input offset voltage calibration mode selection
         0: Normal operation
         1: Offset calibration mode

Bit 6   **SDA1RSP**: SD OPA1 input offset voltage calibration reference selection
         0: Input reference voltage comes from A1NI
         1: Input reference voltage comes from A1PI

Bit 5~0   **SDA1OF5~SDA1OF0**: SD OPA1 input offset voltage calibration control
         These 6 bits are used to perform the operational amplifier input offset calibration operation and the value for the SD OPA1 input offset Calibration can be restored into this bit field. More detailed information is described in the "Operational Amplifier Input Offset Calibration" section.

Operational Amplifier Operation

There are two fully integrated Operational Amplifiers in the device, OPA0 and OPA1. These OPAs can be used for signal amplification according to specific user requirements. The OPAs can be disabled or enabled entirely under software control using internal registers. With specific control registers, some OPA related applications can be more flexible and easier to be implemented, such as Unit Gain Buffer, Non-Inverting Amplifier, Inverting Amplifier and various kinds of filters, etc.

Operational Amplifier Input Offset Calibration

Note that if the SD Operational Amplifier inputs are pin-shared with I/O pins, they should be configured as the SD Operational Amplifier input function before the Input Offset Calibration.

Step 1. Set SDAnOFM=1 and SDAnRSP=1, the SD Operational Amplifier n is now under the input offset Calibration mode, S0 and S2 on. To make sure the V_{AnOS} as minimal as possible after calibration, the input reference voltage in calibration should be the same as input DC operating voltage in normal operation.

Step 2. Set SDAnOF[5:0]=000000 and then read the SDAnO bit.

Step 3. Increase the SDAnOF[5:0] value by 1 and then read the SDAnO bit.

If the SDAnO bit state has not changed, then repeat Step 3 until the SDAnO bit state has changed.

If the SDAnO bit state has changed, record the SDAnOF[5:0] value as V_{AnOS1} and then go to Step 4.

Step 4. Set SDAnOF[5:0]=111111 and read the SDAnO bit.

Step 5. Decrease the SDAnOF[5:0] value by 1 and then read the SDAnO bit.

If the SDAnO bit state has not changed, then repeat Step 5 until the SDAnO bit state has changed.

If the SDAnO bit state has changed, record the SDAnOF[5:0] value as V_{AnOS2} and then go to Step 6.

Step 6. Restore the SD Operational Amplifier n input offset calibration value V_{OS} into the SDAnOF[5:0] bits. The offset Calibration procedure is now finished.

$V_{AnOS}=(V_{AnOS1}+V_{AnOS2})/2$.

If $(V_{AnOS1}+V_{AnOS2})/2$ is not integral, discard the decimal.

Power Line Transceiver – PLT

The device provides a power line transceiver circuit which can be used for power line data transmission and reception. The circuit consists of three 6-bit D/A Converters, one fully integrated Operational Amplifier and two Comparators. The reference voltage of the DAC0/DAC1 is selected by the PLTDA0REFS/PLTDA1REFS bit. If the bit is cleared to 0, the AV_{DD} is seleted; if the bit is set to 1, the V_{PLTREF} is selected. Note that the PLVREF pin is pin-shared with other functions, it should be properly configure the corresponding pin-shared function control bits before using the V_{PLTREF} voltage.

Note: 1. After the ONE-SHOT circuit is triggered, it will not be triggered repeatedly during its operation.

2. When the PLTDICMS bit is equal to 0 and the ONE-SHOT circuit is not triggered, the PLDICO pin is high-impadance.

Power Line Transceiver Block Diagram

Power Line Transceiver Registers

Overall operation of the Power Line Transceiver circuit is controlled using a series of registers. The DACn outputs, the Operational Amplifier, Comparator input signal selection, operating modes, output signals all can be setup using these registers by application program.

Register Name	Bit							
	7	6	5	4	3	2	1	0
PLTSW	—	—	—	—	PLTS3	PLTS2	PLTS1	PLTS0
PLTDACC	—	—	—	PLTDA1REFS	PLTDA0REFS	PLTDAC2EN	PLTDAC1EN	PLTDAC0EN
PLTDA0L	—	—	D5	D4	D3	D2	D1	D0
PLTDA1L	—	—	D5	D4	D3	D2	D1	D0
PLTDA2L	—	—	D5	D4	D3	D2	D1	D0
PLTC0C	PLTC0OUT	PLTC0EN	PLTC0O	PLTC0DEB2	PLTC0DEB1	PLTC0DEB0	PLTC0IS1	PLTC0IS0
PLTC1C	PLTC1OUT	PLTC1EN	PLTC1O	PLTC1DEB2	PLTC1DEB1	PLTC1DEB0	PLTC1IS1	PLTC1IS0
PLTC0VOS	—	PLTC0OFM	PLTC0RSP	PLTC0OF4	PLTC0OF3	PLTC0OF2	PLTC0OF1	PLTC0OF0
PLTC1VOS	—	PLTC1OFM	PLTC1RSP	PLTC1OF4	PLTC1OF3	PLTC1OF2	PLTC1OF1	PLTC1OF0
PLTCHYC	—	PLTCXOSW	PLTC1POL	PLTC0POL	PLTC1HYS1	PLTC1HYS0	PLTC0HYS1	PLTC0HYS0
PLTAC	—	PLTAEN	PLTAO	—	—	—	—	PLTABW
PLTAVOS	PLTAOFM	PLTARSP	PLTAOF5	PLTAOF4	PLTAOF3	PLTAOF2	PLTAOF1	PLTAOF0
PLTDICC0	PLTDICMS	—	—	—	—	—	PLTDICOC1	PLTDICOC0
PLTDICC1	PLTDICS	PLTDICES1	PLTDICES0	—	—	PLTDICT2	PLTDICT1	PLTDICT0

Power Line Transceiver Register List

• PLTSW Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	PLTS3	PLTS2	PLTS1	PLTS0
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	1

Bit 7~4　　Unimplemented, read as "0"

Bit 3~2　　**PLTS3~PLTS2**: PLTS[3:2] switch selection
　　　　　　00: Connect to PLTDAC2O
　　　　　　01: Connect to PLRX
　　　　　　1x: Connected to PLVREF

Bit 1　　　**PLTS1**: PLTS1 switch selection
　　　　　　0: Connect to PLIS
　　　　　　1: Connect to LINEV

Bit 0　　　**PLTS0**: PLTX switch selection
　　　　　　0: PLTX switch to GND
　　　　　　1: PLTX switch to AO

• PLTDACC Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	PLTDA1REFS	PLTDA0REFS	PLTDAC2EN	PLTDAC1EN	PLTDAC0EN
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	—	—	—	0	0	0	0	0

Bit 7~5　　Unimplemented, read as "0"

Bit 4　　　**PLTDA1REFS**: PLT DAC1 reference voltage ($V_{PLTDA1REF}$) selection
　　　　　　0: AV_{DD}
　　　　　　1: V_{PLTREF}

Bit 3   **PLTDA0REFS**: PLT DAC0 reference voltage ($V_{PLTDA0REF}$) selection
      0: AV_{DD}
      1: V_{PLTREF}

Bit 2   **PLTDAC2EN**: PLT DAC2 enable or disable control
      0: Disable (PLTDAC2O high impedance)
      1: Enable

Bit 1   **PLTDAC1EN**: PLT DAC1 enable or disable control
      0: Disable (CMP1 negative input is V_{PLTREF})
      1: Enable (CMP1 negative input is PLTDAC1O)

Bit 0   **PLTDAC0EN**: PLT DAC0 enable or disable control
      0: Disable (CMP0 negative input is V_{PLTREF})
      1: Enable (CMP0 negative input is PLTDAC0O)

• **PLTDA0L Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	D5	D4	D3	D2	D1	D0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6   Unimplemented, read as "0"
Bit 5~0   **D5~D0**: PLT DAC0 output control code
      $PLTDAC0O=(DAC\ V_{PLTDA0REF}/2^6)\times PLTDA0L[5:0]$

• **PLTDA1L Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	D5	D4	D3	D2	D1	D0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6   Unimplemented, read as "0"
Bit 5~0   **D5~D0**: PLT DAC1 output control code
      $PLTDAC1O=(DAC\ V_{PLTDA1REF}/2^6)\times PLTDA1L[5:0]$

• **PLTDA2L Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	D5	D4	D3	D2	D1	D0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6   Unimplemented, read as "0"
Bit 5~0   **D5~D0**: PLT DAC2 output control code
      $PLTDAC2O=(DAC\ AV_{DD}/2^6)\times PLTDA2L[5:0]$

• **PLTC0C Register**

Bit	7	6	5	4	3	2	1	0
Name	PLTC0OUT	PLTC0EN	PLTC0O	PLTC0DEB2	PLTC0DEB1	PLTC0DEB0	PLTC0IS1	PLTC0IS0
R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **PLTC0OUT**: PLT Comparator 0 output bit
      If PLTC0POL=0 and input voltages of the comparator are
        C0PI > C0NI → PLTC0OUT=1
        C0NI > C0PI → PLTC0OUT=0

If PLTC0POL=1 and input voltages of the comparator are
C0PI < C0NI → PLTC0OUT=1
C0NI < C0PI → PLTC0OUT=0

Bit 6   **PLTC0EN**: PLT Comparator 0 enable or disable control
0: Comparator disable
1: Comparator enable

This is the PLT Comparator 0 on/off control bit. If the comparator is disabled, the comparator output will be cleared to 0. Therefore, PLTC0OUT=0 when PLTC0POL=0, or PLTC0OUT=1 when PLTC0POL=1.

Bit 5   **PLTC0O**: PLT Comparator 0 debounced output
The PLTC0O is the de-bounce version of PLTC0OUT.

If PLTC0POL=0, the PLTC0O outputs "1" only when the current and previous N samples of PLTC0OUT are "1".

If PLTC0POL=1, The PLTC0O outputs "0" only when the current and previous N samples of PLTC0OUT are "0". N depends on PLTC0DEB [1:0] configuration bits.

Bit 4~2   **PLTC0DEB2~PLTC0DEB0**: PLT Comparator 0 debounce time control
000: No debounce
001: $2^1 \times t_{SYS}$
010: $2^2 \times t_{SYS}$
011: $2^3 \times t_{SYS}$
100: $2^4 \times t_{SYS}$
101: $2^5 \times t_{SYS}$
110: $2^6 \times t_{SYS}$
111: $2^7 \times t_{SYS}$
Note: $t_{SYS}=1/f_{SYS}$.

Bit 1~0   **PLTC0IS1~PLTC0IS0**: PLT Comparator 0 current control
Refer to the "Comparator Electrical Characteristics" table for details.

• **PLTC1C Register**

Bit	7	6	5	4	3	2	1	0
Name	PLTC1OUT	PLTC1EN	PLTC1O	PLTC1DEB2	PLTC1DEB1	PLTC1DEB0	PLTC1IS1	PLTC1IS0
R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **PLTC1OUT**: PLT Comparator 1 output bit
If PLTC1POL=0 and input voltages of the comparator are
C1PI > C1NI → PLTC1OUT=1
C1NI > C1PI → PLTC1OUT=0
If PLTC1POL=1 and input voltages of the comparator are
C1PI < C1NI → PLTC1OUT=1
C1NI < C1PI → PLTC1OUT=0

Bit 6   **PLTC1EN**: PLT Comparator 1 enable or disable control
0: Comparator disable
1: Comparator enable

This is the PLT Comparator 1 on/off control bit. If the comparator is disabled, the comparator output will be cleared to 0. Therefore, PLTC1OUT=0 when PLTC1POL=0, or PLTC1OUT=1 when PLTC1POL=1.

Bit 5   **PLTC1O**: PLT Comparator 1 debounced output
The PLTC1O is the de-bounce version of PLTC1OUT.

If PLTC1POL=0, the PLTC1O outputs "1" only when the current and previous N samples of PLTC1OUT are "1". If PLTC1POL=1, The PLTC1O outputs "0" only when the current and previous N samples of PLTC1OUT are "0". N depends on PLTC1DEB [1:0] configuration bits.

Bit 4~2   **PLTC1DEB2~PLTC1DEB0**: PLT Comparator 1 debounce time control

000: No debounce

001: $2^1 \times t_{SYS}$

010: $2^2 \times t_{SYS}$

011: $2^3 \times t_{SYS}$

100: $2^4 \times t_{SYS}$

101: $2^5 \times t_{SYS}$

110: $2^6 \times t_{SYS}$

111: $2^7 \times t_{SYS}$

Note: $t_{SYS}=1/f_{SYS}$.

Bit 1~0   **PLTC1IS1~PLTC1IS0**: PLT Comparator 1 current control

Refer to the "Comparator Electrical Characteristics" table for details.

• **PLTC0VOS Register**

Bit	7	6	5	4	3	2	1	0
Name	—	PLTC0OFM	PLTC0RSP	PLTC0OF4	PLTC0OF3	PLTC0OF2	PLTC0OF1	PLTC0OF0
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	0	0	1	0	0	0	0

Bit 7   Unimplemented, read as "0"

Bit 6   **PLTC0OFM**: PLT Comparator 0 normal operation or input offset voltage calibration mode selection

0: Normal operation

1: Offset calibration mode

Bit 5   **PLTC0RSP**: PLT Comparator 0 input offset voltage calibration reference selection

0: Input reference voltage comes from C0NI

1: Input reference voltage comes from C0PI

Bit 4~0   **PLTC0OF4~PLTC0OF0**: PLT Comparator 0 input offset voltage calibration control

This 5-bit field is used to perform the PLT comparator 0 input offset calibration operation and the value for the PLT Comparator 0 input offset calibration can be restored into this bit field. More detailed information is described in the "Comparator Input Offset Calibration" section.

• **PLTC1VOS Register**

Bit	7	6	5	4	3	2	1	0
Name	—	PLTC1OFM	PLTC1RSP	PLTC1OF4	PLTC1OF3	PLTC1OF2	PLTC1OF1	PLTC1OF0
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	0	0	1	0	0	0	0

Bit 7   Unimplemented, read as "0"

Bit 6   **PLTC1OFM**: PLT Comparator 1 normal operation or input offset voltage calibration mode selection

0: Normal operation

1: Offset calibration mode

Bit 5   **PLTC1RSP**: PLT Comparator 1 input offset voltage calibration reference selection

0: Input reference voltage comes from C1NI

1: Input reference voltage comes from C1PI

Bit 4~0   **PLTC1OF4~PLTC1OF0**: PLT Comparator 1 input offset voltage calibration control

This 5-bit field is used to perform the PLT comparator 1 input offset calibration operation and the value for the PLT Comparator 1 input offset calibration can be restored into this bit field. More detailed information is described in the "Comparator Input Offset Calibration" section.

• **PLTCHYC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	PLTCXOSW	PLTC1POL	PLTC0POL	PLTC1HYS1	PLTC1HYS0	PLTC0HYS1	PLTC0HYS0
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	0	0	0	0	0	0	0

Bit 7   Unimplemented, read as "0"

Bit 6   **PLTCXOSW**: Comparator 0 or Comparator 1 output selection
             0: Comparator 0 Output
             1: Comparator 1 Output
             This is the Comparator 0 or Comparator 1 output selection bit. If the bit is zero, then the PLTC0O bit will be output indicating the output condition of the comparator 0. If the bit is high the comparator PLTC1O bit will be output indicating the output condition of the comparator 1.

Bit 5   **PLTC1POL**: PLT Comparator 1 output polarity control
             0: Non-invert
             1: Invert
             This is the PLT Comparator 1 polarity bit. If the bit is zero, then the PLTC1OUT bit will reflect the non-inverted output condition of the comparator. If the bit is high the comparator PLTC1OUT bit will be inverted.

Bit 4   **PLTC0POL**: PLT Comparator 0 output polarity control
             0: Non-invert
             1: Invert
             This is the PLT Comparator 0 polarity bit. If the bit is zero, then the PLTC0OUT bit will reflect the non-inverted output condition of the comparator 0. If the bit is high the comparator PLTC0OUT bit will be inverted.

Bit 3~2   **PLTC1HYS1~PLTC1HYS0**: PLT Comparator 1 hysteresis voltage window control
             Refer to "Comparator Characteristics" table for details.

Bit 1~0   **PLTC0HYS1~PLTC0HYS0**: PLT Comparator 0 hysteresis voltage window control
             Refer to "Comparator Characteristics" table for details.

• **PLTAC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	PLTAEN	PLTAO	—	—	—	—	PLTABW
R/W	—	R/W	R	—	—	—	—	R/W
POR	—	0	0	—	—	—	—	0

Bit 7   Unimplemented, read as "0"

Bit 6   **PLTAEN**: PLT OPA enable or disable control
             0: Disable (AO high impedenece)
             1: Enable

Bit 5   **PLTAO**: PLT OPA output status (positive logic)
             This bit is read only.
             When the PLTAOFM bit is set to 1, PLTAO is defined as PLT OPA output status, refer to Offset calibration procedure. When the PLTAOFM bit is cleared to 0, this bit will be fixed at a low level.

Bit 4~1   Unimplemented, read as "0"

Bit 0   **PLTABW**: PLT OPA Gain bandwith control bit
             0: 600kHz
             1: 2MHz
             Refer to "Operational Amplifier Electrical Characteristics" table for details.

• **PLTAVOS Register**

Bit	7	6	5	4	3	2	1	0
Name	PLTAOFM	PLTARSP	PLTAOF5	PLTAOF4	PLTAOF3	PLTAOF2	PLTAOF1	PLTAOF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	0	0	0	0	0

Bit 7   **PLTAOFM**: PLT OPA normal operation or input offset voltage cancellation mode selection
       0: Normal operation
       1: Offset calibration mode

Bit 6   **PLTARSP**: PLT OPA input offset voltage calibration reference selection
       0: Input reference voltage comes from ANI
       1: Input reference voltage comes from API

Bit 5~0   **PLTAOF5~PLTAOF0**: PLT OPA input offset voltage calibration control
       This 6-bit field is used to perform the PLT OPA input offset calibration operation and the value for the PLT OPA input offset calibration can be restored into this bit filed. More detailed information is described in the "Operational Amplifier Input Offset Calibration" section.

• **PLTDICC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	PLTDICMS	—	—	—	—	—	PLTDICOC1	PLTDICOC0
R/W	R/W	—	—	—	—	—	R/W	R/W
POR	0	—	—	—	—	—	0	0

Bit 7   **PLTDICMS**: PLT discharge mode selection
       0: Automatic discharge mode
       1: Manual discharge mode
       When this bit is set high, the discharge capacity will be selected by PLTDICOC1~ PLTDICOC0 bits.

Bit 6~2   Unimplemented, read as "0"

Bit 1~0   **PLTDICOC1~PLTDICOC0**: PLT discharge capacity selection
       00: 75µA
       01: 150µA
       10: 300µA
       11: 600µA

• **PLTDICC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	PLTDICS	PLTDICES1	PLTDICES0	—	—	PLTDICT2	PLTDICT1	PLTDICT0
R/W	R/W	R/W	R/W	—	—	R/W	R/W	R/W
POR	0	0	0	—	—	0	0	0

Bit 7   **PLTDICS**: PLT discharge function trigger source selection
       0: PLTC0ODIC
       1: PLTC1ODIC

Bit 6~5   **PLTDICES1~PLTDICES0**: PLT active edge selection
       00: Disable
       01: Falling edge
       10: Rising edge
       11: Both falling and rising edges

Bit 4~3   Unimplemented, read as "0"

Bit 2~0　　　**PLTDICT2~PLTDICT0**: PLT discharge time selection

000: $2^1 \times t_{SYS}$
001: $2^2 \times t_{SYS}$
010: $2^3 \times t_{SYS}$
011: $2^4 \times t_{SYS}$
100: $2^5 \times t_{SYS}$
101: $2^6 \times t_{SYS}$
110: $2^7 \times t_{SYS}$
111: $2^1 \times t_{SYS}$

Note: $t_{SYS}=1/f_{SYS}$.

Discharge Circuit Operation

There is a discharge circuit in the device. The discharge trigger source is selected by the PLTDICS bit. The active edge of trigger signal can be disabled, a rising edge, a falling edge or both rising and falling edges; the active edge transition type is selected using the PLTDICES1 and PLTDICES0 bits. The ONE-SHOT circuit is initiated by the trigger signal. The discharge capacity is set by the PLTDICOC1 and PLTDICOC0 bits; the discharge time is set by the PLTDICT[2:0] bits.

In addition, the discharge function can also be initiated through software, set PLTDICMS to 1, and set the discharge capacity according to PLTDICOC1 and PLTDICOC0 bits until PLTDICMS is cleared to 0 to disable the discharge function.

Offset Calibration Procedure

To operate in the input offset calibration mode for the PLT Operational Amplifier or the Comparators, the PLTAOFM or PLTCnOFM bit should first be set to "1" to select the input offset voltage calibration mode. Note that as the comparator or Operational Amplifier input is from the PLRX or PLIS pin which is pin-shared with I/O or other functions, before the calibration, they should be configured as PLT comparator or operational amplifier input pin function first.

Comparator Input Offset Calibration

Step 1. Set PLTCnOFM=1 and PLTCnRSP=1, the PLT Comparator n is now operating in the comparator input offset calibration mode, S0 and S2 on or S3 and S5 on. To make sure V_{CnOS} as minimal as possible after calibration, the input reference voltage in calibration should be the same as input DC operating voltage in normal operation.

Step 2. Set PLTCnOF[4:0]=00000 and read the PLTCnOUT bit.

Step 3. Increase the PLTCnOF[4:0] value by 1 and then read the PLTCnOUT bit.

If the PLTCnOUT bit state has not changed, then repeat Step 3 until the PLTCnOUT bit state has changed.

If the PLTCnOUT bit state has changed, record the PLTCnOF[4:0] value as V_{CnOS1} and then go to Step 4.

Step 4. Set PLTCnOF[4:0]=11111 and then read the PLTCnOUT bit.

Step 5. Decrease the PLTCnOF[4:0] value by 1 and then read the PLTCnOUT bit.

If the PLTCnOUT bit state has not changed, then repeat Step 5 until the PLTCnOUT bit state has changed.

If the PLTCnOUT bit state has changed, record the PLTCnOF[4:0] value as V_{CnOS2} and then go to Step 6.

Step 6. Restore the PLT Comparator n input offset calibration value V_{CnOS} into the PLTCnOF[4:0] bit field. The offset Calibration procedure is now finished.

$V_{CnOS}=(V_{CnOS1}+V_{CnOS2})/2$. If $(V_{CnOS1}+V_{CnOS2})/2$ is not integral, discard the decimal.

Operational Amplifier Input Offset Calibration

Step1. Set PLTAOFM=1 and PTLARSP=1, the PLT Operational Amplifier is now under offset calibration mode, S6 and S8 on. To make sure V_{AOS} as minimal as possible after calibration, the input reference voltage in calibration should be the same as input DC operating voltage in normal mode operation.

Step2. Set PTLAOF[5:0]=000000 and then read PTLAO bit

Step3. Increase the PLTAOF[5:0] value by 1 and then read the PLTAO bit.

If the PLTAO bit state has not changed, then repeat Step 3 until the PLTAO bit state has changed.

If the PLTAO bit state has changed, record the PLTAOF[5:0] value as V_{AOS1} and then go to Step 4.

Step4. Set PTLAOF[5:0]=111111 then read PLTAO bit.

Step5. Decrease the PLTAOF[5:0] value by 1 and then read the PLTAO bit.

If the PLTAO bit state has not changed, then repeat Step 5 until the PLTAO bit state has changed.

If the PLTAO bit state has changed, record the PLTAOF[5:0] value as V_{AOS2} and then go to Step 6.

Step6. Restore the PLT Operational Amplifier input offset calibration value V_{AOS} into the PLTAOF[5:0] bit field. The offset Calibration procedure is now finished.

$V_{AOS}=(V_{AOS1}+V_{AOS2})/2$. If $(V_{AOS1}+V_{AOS2})/2$ is not integral, discard the decimal.

Analog to Digital Converter

The need to interface to real world analog signals is a common requirement for many electronic systems. However, to properly process these signals by a microcontroller, they must first be converted into digital signals by A/D converters. By integrating the A/D conversion electronic circuitry into the microcontroller, the need for external components is reduced significantly with the corresponding follow-on benefits of lower costs and reduced component space requirements.

A/D Converter Overview

The device contains a multi-channel 12-bit analog to digital converter which can directly interface to external analog signals, such as that from sensors or other control signals and convert these signals directly into a 12-bit digital value. It also can convert the internal signals, the high performance bandgap reference voltage V_{BGREF}, the SD operational amplifier 0 output signal OPA0O and the SD operational amplifier 1 output signal OPA1O, PLT operational amplifier output signal, LINEV, or the temperature sensor output voltage, V_{TSO}, into a 12-bit digital value. The external or internal analog signal to be converted is determined by the SAINS2~SAINS0 bits together with the SACS3~SACS0 bits. Note that when the internal analog signal is to be converted, the SAINS2~SAINS0 and SACS3~SACS0 bits should be properly configured to avoid external channel input.More detailed information about the A/D input signal is described in the "A/D Converter Control Registers" and "A/D Converter Input Signals" sections respectively.

This A/D converter also includes a temperature sensor circuitry which contains a temperature sensor, two operational amplifiers and an internal reference voltage. The temperature sensor can detect the temperature and then output a voltage proportional to the temperature. The output voltage can be amplified by the OPA and then converted to a 12-bit digital data using the A/D converter.

External Input Channels	Internal Signals	Channel Select Bits
3: AN0, AN2~AN3	5: V_{BGREF}, OPA0O, OPA1O, LINEV, V_{TSO}	SAINS2~SAINS0, SACS3~SACS0

The accompanying block diagram shows the overall internal structure of the A/D converter with temperature sensor, together with its associated registers.
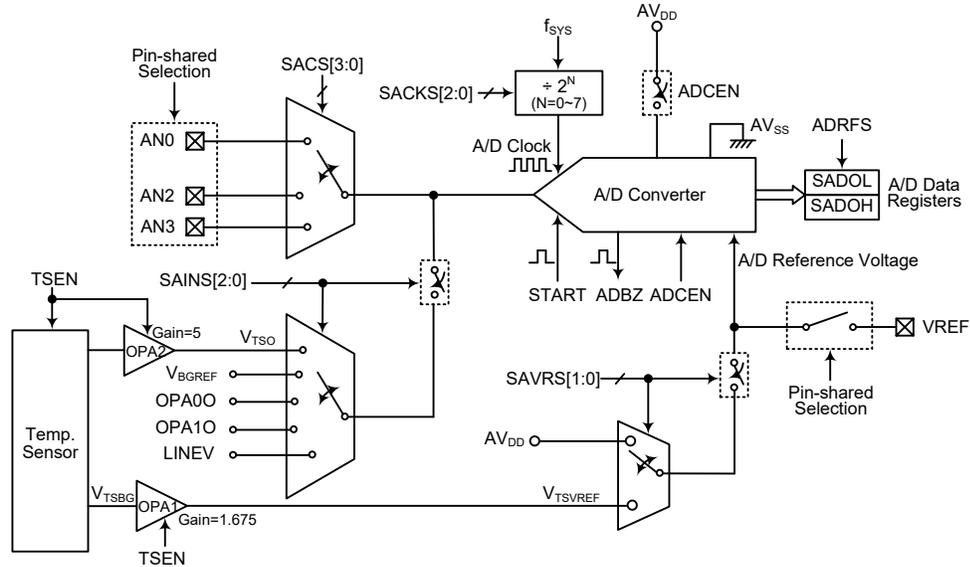
A/D Converter with temperature sensor Structure

A/D Converter Register Description

Overall operation of the A/D converter with temperature sensor is controlled using several registers. A read only register pair exists to store the A/D converter data 12-bit value. Two registers, SADC0 and SADC1, are control registers which setup the operating and control function of the A/D converter. The SADC2 register is used to enable/disable the integrated temperature sensor circuitry and select the A/D converter conversion mode. The VBGRC resigter is used to enable/disable the A/D converter internal bandgap reference voltage ouput.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SADOH (ADRFS=0)	D11	D10	D9	D8	D7	D6	D5	D4
SADOH (ADRFS=1)	—	—	—	—	D11	D10	D9	D8
SADOL (ADRFS=0)	D3	D2	D1	D0	—	—	—	—
SADOL (ADRFS=1)	D7	D6	D5	D4	D3	D2	D1	D0
SADC0	START	ADBZ	ADCEN	ADRFS	SACS3	SACS2	SACS1	SACS0
SADC1	SAINS2	SAINS1	SAINS0	SAVRS1	SAVRS0	SACKS2	SACKS1	SACKS0
SADC2	SAMS	—	—	—	—	—	D1	TSEN
VBGRC	—	—	—	—	—	—	—	VBGREN

A/D Converter with temperature sensor Register List

A/D Converter Data Registers – SADOL, SADOH

As the device contains an internal 12-bit A/D converter, it requires two data registers to store the converted value. These are a high byte register, known as SADOH, and a low byte register, known as SADOL. After the conversion process takes place, these registers can be directly read by the microcontroller to obtain the digitised conversion value. As only 12 bits of the 16-bit register space is utilised, the format in which the data is stored is controlled by the ADRFS bit in the SADC0 register as shown in the accompanying table. D0~D11 are the A/D conversion result data bits. Any unused bits will be read as zero. Note that A/D Converter data register contents will be unchanged if the A/D converter is disabled.

ADRFS	SADOH								SADOL							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	0	0	0	0	0
1	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A/D Converter Data Registers

A/D Converter Control Registers – SADC0, SADC1

To control the function and operation of the A/D converter, two control registers known as SADC0 and SADC1 are provided. These 8-bit registers define functions such as the selection of which analog channel is connected to the internal A/D converter, the digitised data format, the A/D clock source as well as controlling the start function and monitoring the A/D converter busy status. As the device contains only one actual analog to digital converter hardware circuit, each of the external or internal analog signal inputs must be routed to the converter. The SACS3~SACS0 bits in the SADC0 register are used to determine which external channel input is selected to be converted. The SAINS2~SAINS0 bits in the SADC1 register are used to determine that the analog signal to be converted comes from the internal analog signal or external analog channel input.

The relevant pin-shared function selection bits determine which pins on I/O Ports are used as analog inputs for the A/D converter input and which pins are not to be used as the A/D converter input. When the pin is selected to be an A/D input, its original function whether it is an I/O or other pin-shared function will be removed. In addition, any internal pull-high resistor connected to the pin will be automatically removed if the pin is selected to be an A/D converter input.

• SADC0 Register

Bit	7	6	5	4	3	2	1	0
Name	START	ADBZ	ADCEN	ADRFS	SACS3	SACS2	SACS1	SACS0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **START**: Start the A/D conversion
0→1→0: Start
This bit is used to initiate an A/D conversion process. The bit is normally low but if set high and then cleared low again, the A/D converter will initiate a conversion process.

Bit 6 **ADBZ**: A/D converter busy flag
0: No A/D conversion is in progress
1: A/D conversion is in progress
This read only flag is used to indicate whether the A/D conversion is in progress or not. When the START bit is set from low to high and then to low again, the ADBZ flag will be set to 1 to indicate that the A/D conversion is initiated. The ADBZ flag will be cleared to 0 after the A/D conversion is complete.

Bit 5   **ADCEN**: A/D converter function enable control
  0: Disable
  1: Enable

This bit controls the A/D internal function. This bit should be set to one to enable the A/D converter. If the bit is set low, then the A/D converter will be switched off reducing the device power consumption. When the A/D converter function is disabled, the contents of the A/D data register pair known as SADOH and SADOL will be unchanged.

Bit 4   **ADRFS**: A/D converter data format selection
  0: A/D converter data format → SADOH=D[11:4]; SADOL=D[3:0]
  1: A/D converter data format → SADOH=D[11:8]; SADOL=D[7:0]

This bit controls the format of the 12-bit converted A/D value in the two A/D data registers. Details are provided in the A/D data register section.

Bit 3~0   **SACS3~SACS0**: A/D converter external analog channel input selection
  0000: AN0
  0001: Reserved
  0010: AN2
  0011: AN3
  0100~1111: Non-existed channel, the input will be floating

- **SADC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	SAINS2	SAINS1	SAINS0	SAVRS1	SAVRS0	SACKS2	SACKS1	SACKS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~5   **SAINS2~SAINS0**: A/D converter input signal selection
  000: External input – External analog channel input
  001: Internal input – Internal high performance bandgap reference voltage, V_{BGREF}
  010: Internal input – Internal temperature Sensor output voltage, V_{TSO}
  011: Internal input – Internal SD operational amplifier 0 output signal, OPA0O
  100: Internal input – Internal SD operational amplifier 1 output signal, OPA1O
  101: Internal input – Internal PLT operational amplifier output signal, LINEV
  110: External input – External analog channel input
  111: Forbidden data, SAINS2~SAINS0 bits can not be written with "111"

Care must be taken if the SAINS2~SAINS0 bits are set from "001~101" to select the internal analog signal to be converted. When the internal analog signal is selected to be converted, the external input pin must never be selected as the A/D input signal by properly setting the SACS3~SACS0 bits. Otherwise, the external channel input will be connected together with the internal analog signal. This will result in unpredictable situations such as an irreversible damage.

Bit 4~3   **SAVRS1~SAVRS0**: A/D converter reference voltage selection
  00:From external VREF pin
  01: Internal A/D converter power, AV_{DD}
  10: Internal temperature sensor reference voltage, V_{TSVREF}
  11: Internal A/D converter power, AV_{DD}

These bits are used to select the A/D converter reference voltage. Care must be taken if the SAVRS1~SAVRS0 bits are set to "01~11" to select the internal A/D converter power or temperature sensor reference voltage as the reference voltage source. When the internal A/D converter power or temperature sensor reference voltage is selected as the reference voltage, the VREF pin cannot be configured as the reference voltage input by properly configuring the corresponding pin-shared function control bits. Otherwise, the external input voltage on VREF pin will be connected to the internal A/D converter power.

Bit 2~0   **SACKS2~SACKS0**: A/D conversion clock source select
000: f_{SYS}
001: $f_{SYS}/2$
010: $f_{SYS}/4$
011: $f_{SYS}/8$
100: $f_{SYS}/16$
101: $f_{SYS}/32$
110: $f_{SYS}/64$
111: $f_{SYS}/128$
These three bits are used to select the clock source for the A/D converter.

Bandgap Referenc Voltage Control Register – VBGRC

A high performance bandgap voltage reference is included in the device. It has an accurate voltage reference output, V_{BGREF}, when input supply voltage change or temperature variation. The VBGRC register is used to control the bandgap reference voltage circuit enable or disable.

• VBGRC Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	VBGREN
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	0

Bit 7~1   Unimplemented, read as "0"
Bit 0   **VBGREN**: Bandgap enable/disable control
0: Disable
1: Enable

This bit is used to enable/disable the internal Bandgap reference circuit. The internal Bandgap reference circuit should first be enabled before the V_{BGREF} voltage is selected to be used.

When the VBGREN bit is cleared to zero, the Bandgap voltage output is in a high impedance state.

Temperature Sensor Control Register – SADC2

The SADC2 register is used to enable/disable the integrated temperature sensor circuitry and select the A/D converter conversion mode.

• SADC2 Register

Bit	7	6	5	4	3	2	1	0
Name	SAMS	—	—	—	—	—	D1	TSEN
R/W	R/W	—	—	—	—	—	R/W	R/W
POR	0	—	—	—	—	—	1	0

Bit 7   **SAMS**: A/D converter conversion mode selection
0: Normal mode, A/D converter clock rate up to 2MHz
1: Low current mode

This bit is used to select the A/D converter conversion mode. The low current mode A/D converter is suitable for continuous static signal conversion, and its clock frequency range is limited to 100kHz~250kHz.

Bit 6~2   Unimplemented, read as "0"
Bit 1   **D1**: Reserved bit, should be fixed to 1
Bit 0   **TSEN**: Temperature sensor circuitry enable control
0: Disable
1: Enable

This bit controls the internal temperature sensor circuitry. If the temperature sensor output will be converted or the temperature sensor reference voltage will be selected as the A/D conversion reference voltage, the temperature sensor circuitry should be turned on by setting the TSEN bit high first. When the temperature sensor is enabled by setting the TSEN bit to 1, a time named as t_{TSS} should be allowed for the temperature sensor circuit to stabilise before implementing relevant temperature sensor operation.

A/D Converter Operation

The START bit in the SADC0 register is used to start the AD conversion. When the microcontroller sets this bit from low to high and then low again, an analog to digital conversion cycle will be initiated.

The ADBZ bit in the SADC0 register is used to indicate whether the analog to digital conversion process is in progress or not. This bit will be automatically set to 1 by the microcontroller after an A/D conversion is successfully initiated. When the A/D conversion is complete, the ADBZ will be cleared to 0. In addition, the corresponding A/D interrupt request flag will be set in the interrupt control register, and if the interrupts are enabled, an appropriate internal interrupt signal will be generated. This A/D internal interrupt signal will direct the program flow to the associated A/D internal interrupt address for processing. If the A/D internal interrupt is disabled, the microcontroller can poll the ADBZ bit in the SADC0 register to check whether it has been cleared as an alternative method of detecting the end of an A/D conversion cycle.

The clock source for the A/D converter, which originates from the system clock f_{SYS}, can be chosen to be either f_{SYS} or a subdivided version of f_{SYS}. The division ratio value is determined by the SACKS2~SACKS0 bits in the SADC1 register. Although the A/D clock source is determined by the system clock f_{SYS} and by bits SACKS2~SACKS0, there are some limitations on the maximum A/D clock source speed that can be selected. As the recommended range of permissible A/D clock period, t_{ADCK}, is from 0.5μs to 10μs, care must be taken for system clock frequencies. For example, as the system clock operates at a frequency of 8MHz, the SACKS2~SACKS0 bits should not be set to 000, 001 or 111. Doing so will give A/D clock periods that are less or larger than the minimum or maximum A/D clock period which may result in inaccurate A/D conversion values. Refer to the following table for examples, where values marked with an asterisk * show where special care must be taken, as the values may be less or larger than the specified A/D Clock Period range.

If the input signal to be converted is the temperature sensor output voltage, the permissible A/D clock period is from 1μs to 2μs.

f_{SYS}	A/D Clock Period (t_{ADCK})							
	SACKS[2:0] =000 (f_{SYS})	SACKS[2:0] =001 (f_{SYS}/2)	SACKS[2:0] =010 (f_{SYS}/4)	SACKS[2:0] =011 (f_{SYS}/8)	SACKS[2:0] =100 (f_{SYS}/16)	SACKS[2:0] =101 (f_{SYS}/32)	SACKS[2:0] =110 (f_{SYS}/64)	SACKS[2:0] =111 (f_{SYS}/128)
1MHz	1μs	2μs	4μs	8μs	16μs *	32μs *	64μs *	128μs *
2MHz	500ns	1μs	2μs	4μs	8μs	16μs *	32μs *	64μs *
4MHz	250ns *	500ns	1μs	2μs	4μs	8μs	16μs *	32μs *
8MHz	125ns *	250ns *	500ns	1μs	2μs	4μs	8μs	16μs *

A/D Clock Period Examples

Controlling the power on/off function of the A/D converter circuitry is implemented using the ADCEN bit in the SADC0 register. This bit must be set high to power on the A/D converter. When the ADCEN bit is set high to power on the A/D converter internal circuitry a certain delay, as indicated in the timing diagram, must be allowed before an A/D conversion is initiated. Even if no pins are selected for use as A/D inputs, if the ADCEN bit is high, then some power will still be consumed. In power conscious applications it is therefore recommended that the ADCEN is set low to reduce power consumption when the A/D converter function is not being used.

The SAMS bit in the SADC2 register is used to select the A/D converter conversion mode. The low current mode A/D converter is suitable for continuous static signal conversion, and its clock rate range is limited to 100kHz~250kHz.

A/D Converter Reference Voltage

The reference voltage supply to the A/D converter can be supplied from the power supply AV_{DD}, or from the temperature sensor reference voltage, V_{TSVREF}, or from an external reference source supplied on pin VREF. The desired selection is made using the SAVRS1~SAVRS0 bits. When the SAVRS1~SAVRS0 bits are set to "01" or "11", the A/D converter reference voltage will come from the AV_{DD}. If the temperature sensor reference voltage is required to use, the SAVRS1~SAVRS0 bits should be set to "10". As the temperature sensor circuitry is controlled by the TSEN bit in the SADC2 register, the TSEN bit should be set high to enable the temperature sensor. Otherwise, if the SAVRS1~SAVRS0 bits are set to "00", the A/D converter reference voltage will come from the VREF pin. As the VREF pin is pin-shared with other functions, when the VREF pin is selected as the reference voltage supply pin, the VREF pin-shared function control bit should be properly configured to disable other pin function. However, if the internal A/D converter power AV_{DD} or temperature sensor reference voltage is selected as the reference voltage, the VREF pin must not be configured as the reference voltage input function to avoid the internal connection between the VREF pin and the power supply. The analog input values must not be allowed to exceed the value of the selected A/D reference voltage.

SAVRS[1:0]	Reference	Description
00	VREF pin	External A/D converter reference pin VREF
01, 11	AV_{DD}	Internal A/D converter power supply voltage
10	V_{TSVREF}	Internal Temperature Sensor reference voltage, V_{TSVREF}

A/D Converter Reference Voltage Selection

A/D Converter Input Signals

All the external A/D analog channel input pins are pin-shared with the I/O pins as well as other functions. The corresponding control bits for each A/D external input pin in the PxS0 and PxS1 registers determine whether the input pins are setup as A/D converter analog input channel or whether they have other functions. If the pin is setup to be as an A/D analog channel input, the original pin functions will be disabled. In this way, pins can be changed under program control to change their function between A/D inputs and other functions. All pull-high resistors, which are setup through register programming, will be automatically disconnected if the pins are setup as A/D inputs. Note that it is not necessary to first setup the A/D pin as an input in the port control register to enable the A/D input as when the pin-shared function control bits enable an A/D input, the status of the port control register will be overridden.

There are some internal analog signals derived from the high performance bandgap reference voltage, V_{BGREF}, the SD operational amplifier 0 output signal OPA0O and the SD operational amplifier 1 output signal OPA1O and PLT operational amplifier output signal, LINEV, or the temperature sensor output voltage which can be connected to the A/D converter as the analog input signal by configuring the SAINS2~SAINS0 bits. If the external channel input is selected to be converted, the SAINS2~SAINS0 bits should be set to "000" or "110" and the SACS3~SACS0 bits can determine which external channel is selected. If the internal analog signal is selected to be converted, the external input channel determined by the SACS3~SACS0 bits must be switched to a non-existed A/D input channel by properly setting the SACS3~SACS0 bits with a value from 0100 to 1111. Otherwise, the internal analog signal will be connected together with the external channel input. This will result in unpredictable situations.

This V_{BGREF} is the internal high performance bandgap voltage reference with driver capability. It has accurate voltage reference output when input supply voltage AV_{DD} change or temperature variation. And, this bandgap will startup at a low supply voltage. Therefore, this voltage reference has high power supply rejection ratio (PSRR) for low dropout regulator (LDO) is presented.

SAINS[2:0]	SACS[3:0]	Input Signals	Description
000, 110	0000, 0010~0011	AN0, AN2~AN3	External pin analog input
	0100~1111	—	Non-existed channel, input is floating
001	0100~1111	V_{BGREF}	Internal high performance Bandgap reference voltage
010	0100~1111	V_{TSO}	Internal temperature sensor output voltage
011	0100~1111	OPA0O	Internal SD operational amplifier 0 output signal
100	0100~1111	OPA1O	Internal SD operational amplifier 1 output signal
101	0100~1111	LINEV	Internal PLT operational amplifier output signal
111	Forbidden data, SAINS2~SAINS0 bits can not be written with "111"		

A/D Converter Input Signal Selection

Conversion Rate and Timing Diagram

A complete A/D conversion contains two parts, data sampling and data conversion. If the conversion input signal is not the temperature sensor output, the data sampling which is defined as t_{ADS} takes 4 A/D clock periods and the data conversion takes 12 A/D clock periods. Therefore a total of 16 A/D clock periods for an A/D conversion which is defined as t_{ADC} are necessary. However, an A/D conversion for an internal temperature sensor signal will take a total of 58 A/D clock periods, which includes 46 A/D clock periods for data sampling and 12 A/D clock periods for data conversion.

Maximum single A/D conversion rate = 1/(A/D clock period × 16) (Temperature sensor output signal is not used)

Maximum single A/D conversion rate = 1/(A/D clock period × 58) (Temperature sensor output signal is used)

The accompanying diagram shows graphically the various stages involved in an analog to digital conversion process and its associated timing. After an A/D conversion process has been initiated by the application program, the microcontroller internal hardware will begin to carry out the conversion, during which time the program can continue with other functions. The time taken for the A/D conversion is 16 t_{ADCK} where t_{ADCK} is equal to the A/D clock period.
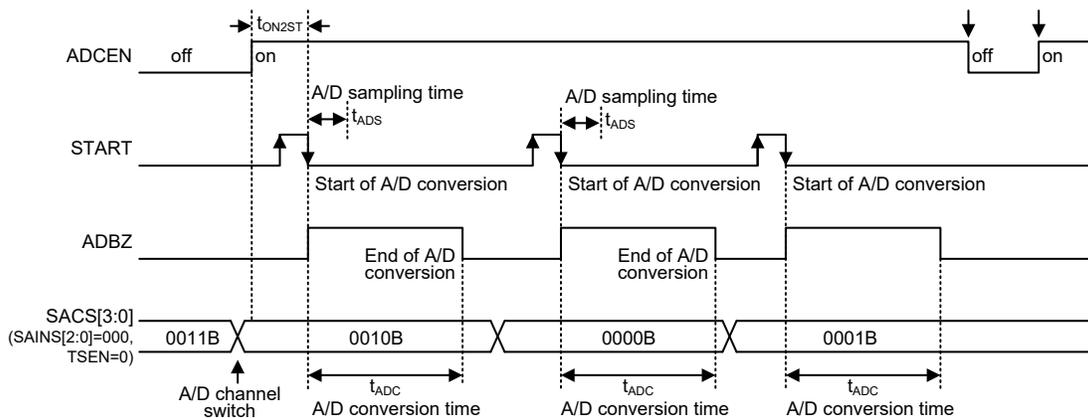
A/D Conversion Timing – External Channel Input

Summary of A/D Conversion Steps

The following summarises the individual steps that should be executed in order to implement an A/D conversion process.

- Step 1

Select the required A/D conversion clock and A/D conversion mode by correctly programming bits SACKS2~SACKS0 in the SADC1 register and SAMS bit in the SADC2 register.

- Step 2

Enable the A/D converter by setting the ADCEN bit in the SADC0 register to 1.

- Step 3

Select which signal is to be connected to the internal A/D converter by correctly configuring the SAINS2~SAINS0 bits.

Select the external channel input to be converted, go to Step 4.

Select the internal analog signal to be converted, go to Step 5.

- Step 4

If the A/D input signal comes from the external channel input selected by configuring the SAINS2~SAINS0 bits, the corresponding pins should be configured as A/D input function by configuring the relevant pin-shared function control bits. The desired analog channel then should be selected by configuring the SACS3~SACS0 bits. After this step, go to Step 6.

- Step 5

Before the A/D input signal is selected to come from the internal analog signal by configuring the SAINS2~SAINS0 bits, the corresponding external input pin must be switched to a non-existed channel input by properly configured the SACS3~SACS0 bits. The desired internal analog signal then can be selected by configuring the SAINS2~SAINS0 bits. After this step, go to Step 6.

- Step 6

Select the reference voltage source by configuring the SAVRS1~SAVRS0 bits in the SADC1 register. Care should be taken in this step which can refer to the A/D Converter Reference Voltage section for details.

- Step 7

Select A/D converter output data format by setting the ADRFS bit in the SADC0 register.

- Step 8

If A/D conversion interrupt is used, the interrupt control registers must be correctly configured to ensure the A/D interrupt function is active. The master interrupt control bit, EMI, and the A/D conversion interrupt control bit, ADE, must both be set high in advance.

- Step 9

The A/D conversion procedure can now be initialized by setting the START bit from low to high and then low again.

- Step 10

If A/D conversion is in progress, the ADBZ flag will be set high. After the A/D conversion process is complete, the ADBZ flag will go low and then the output data can be read from SADOH and SADOL registers.

Note: When checking for the end of the conversion process, if the method of polling the ADBZ bit in the SADC0 register is used, the interrupt enable step above can be omitted.

Programming Considerations

During microcontroller operations where the A/D converter is not being used, the A/D internal circuitry can be switched off to reduce power consumption, by clearing bit ADCEN to 0 in the SADC0 register. When this happens, the internal A/D converter circuits will not consume power irrespective of what analog voltage is applied to their input lines. If the A/D converter input lines are used as normal I/O pins, then care must be taken as if the input voltage is not at a valid logic level, then this may lead to some increase in power consumption.

A/D Conversion Function

As the device contains a 12-bit A/D converter, its full-scale converted digitised value is equal to FFFH. Since the full-scale analog input value is equal to the actual A/D converter reference voltage, V_{REF}, this gives a single bit analog input value of V_{REF} divided by 4096.

$$1\ LSB = V_{REF} \div 4096$$

The A/D Converter input voltage value can be calculated using the following equation:

$$A/D\ input\ voltage = A/D\ output\ digital\ value \times (V_{REF} \div 4096)$$

The diagram shows the ideal transfer function between the analog input value and the digitised output value for the A/D converter. Except for the digitised zero value, the subsequent digitised values will change at a point 0.5 LSB below where they would change without the offset, and the last full scale digitised value will change at a point 1.5 LSB below the V_{REF} level.

Note that here the V_{REF} voltage is the actual A/D converter reference voltage determined by the SAVRS1~SAVRS0 bits.

Ideal A/D Transfer Function
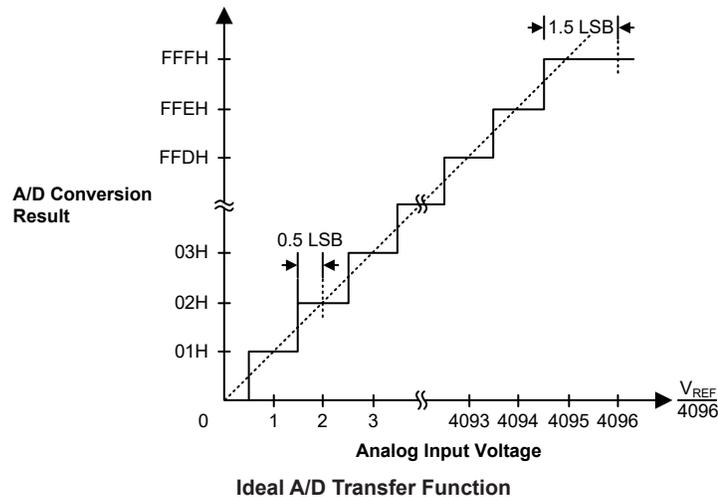
Temperature Measurement Function

As the temperature sensor output voltage, V_{TSO}, has a linear relationship with temperature, the V_{TSO} A/D converted data value will also have a linear relationship with temperature. The current temperature Tx can be proportionally calculated from its A/D converted value ADCx using the following formula.

Tx=Remove LSB 12 bits of (slope×ADCx) – Tos; take lower 12 bits of the final result

The slope and T_{OS} code are stored in the Option Memory and can be read from the Program Memory last page using the table read instruction when the Option Memory mapping function is enabled.

At the end of every conversion or say MCU calculation, the final data Tx is in two's complement format, has a data width of 12 bits and a resolution of 0.0625 (1/16)°C. The following table shows multiple examples of binary or hex data that can be read as temperature result.

Temperature	Digital Format (1 LSB=1/16=0.0625°C)	
Tx(°C)	BINARY	HEX
-40	1101 1000 0000	D80
-25	1110 0111 0000	E70
-10	1111 0110 0000	F60
-1	1111 1111 0000	FF0
-0.25	1111 1111 1100	FFC
-0.0625	1111 1111 1111	FFF
0	0000 0000 0000	000
0.0625	0000 0000 0001	001
0.25	0000 0000 0100	004
1	0000 0001 0000	010
10	0000 1010 0000	0A0
25	0001 1001 0000	190
40	0010 1000 0000	280
70	0100 0110 0000	460
85	0101 0101 0000	550

For example:

- Step 1

  Read the Option Memory slope = 0x0AB9, T_{OS}=0x407.

- Step 2

  Enable temperature sensor & A/D function, then start A/D and read back A/D data registers.

- Step 3

  If ADCx=0x514, slope×ADCx=0x367374. Then remove the lower LSB 12 bits, get 0x0367.

- Step 4

  Minus T_{OS}, the result is 0x0367-0x407=FF60H (2's complement). Take the lower LSB 12 bits, then Tx=F60H=-10.0°C.

Name	Mapped Address in Program Memory	Description
slope	FD5H	16-bit slope value bit 15~bit 8
	FD6H	16-bit slope value bit 7~bit 0
T_{OS}	FD7H	12-bit T_{OS} value bit 11~bit 4
	FD8H	12-bit T_{OS} value bit 3~bit 0 (1LSB=1/16°C)

Temperature Measurement Reference Items

The Option Memory mapping function is enabled using the ORMC register. For more details, refer to the "Option Memory Mapping Register – ORMC" in the Special Function Register Description section.

A/D Conversion Programming Examples

The following two programming examples illustrate how to setup and implement an A/D conversion. In the first example, the method of polling the ADBZ bit in the SADC0 register is used to detect when the conversion cycle is complete, whereas in the second example, the A/D interrupt is used to determine when the conversion is complete.

Example: using an ADBZ polling method to detect the end of conversion

```
clr ADE             ; disable ADC interrupt
clr TSEN            ; disable temperature sensor circuitry
clr SAMS            ; set A/D converter conversion in the normal mode
mov a, 0BH
mov SADC1, a        ; select input signal from external channel input, reference
                    ; voltage from A/D internal power and f_SYS/8 as A/D clock
mov a, 02h          ; set PAS1 register to configure pin AN0
mov PAS1, a
mov a, 20h
mov SADC0, a        ; enable A/D converter and connect AN0 channel to A/D converter
:
start_conversion:
clr START           ; high pulse on start bit to initiate conversion
set START           ; reset A/D
clr START           ; start A/D
polling_EOC:
sz  ADBZ            ; poll the SADC0 register ADBZ bit to detect end of A/D
                    ; conversion
jmp polling_EOC     ; continue polling
mov a, SADOL        ; read low byte conversion result value
mov SADOL_buffer, a ; save result to user defined register
mov a, SADOH        ; read high byte conversion result value
mov SADOH_buffer, a ; save result to user defined register
:
:
jmp start_conversion ; start next A/D conversion
```

Example: using the interrupt method to detect the end of conversion

```
clr ADE             ; disable ADC interrupt
clr TSEN            ; disable temperature sensor circuitry
clr SAMS            ; set A/D converter conversion in the normal mode
mov a, 0BH
mov SADC1, a        ; select input signal from external channel input, reference ;
                    ; voltage from A/D internal power and f_SYS/8 as A/D clock
mov a, 02h          ; set PAS1 register to configure pin AN0
mov PAS1, a
mov a, 20h
mov SADC0, a        ; enable A/D converter and connect AN0 channel to A/D converter
Start_conversion:
clr START           ; high pulse on START bit to initiate conversion
set START           ; reset A/D
clr START           ; start A/D
clr ADF             ; clear ADC interrupt request flag
set ADE             ; enable ADC interrupt
set EMI             ; enable global interrupt
:
:
; ADC interrupt service routine
ADC_ISR:
mov acc_stack, a    ; save ACC to user defined memory
mov a, STATUS
mov status_stack, a ; save STATUS to user defined memory
:
:
mov a, SADOL        ; read low byte conversion result value
mov SADOL_buffer, a ; save result to user defined register
mov a, SADOH        ; read high byte conversion result value
mov SADOH_buffer, a ; save result to user defined register
:
```

```
:
EXIT_INT_ISR:
mov a, status_stack
mov STATUS, a          ; restore STATUS from user defined memory
mov a, acc_stack       ; restore ACC from user defined memory
reti
```

Sink Current Generator

The sink current source generator could provide constant current no matter what V_{ISINK} voltage is from 0.7V to 4.5V, and the V_{DD} voltage is from 2.2V to 5.5V. The constant current value is controlled by the ISGDATA0/ISGDATA1 register, and the sink current range is 50mA~360mA.
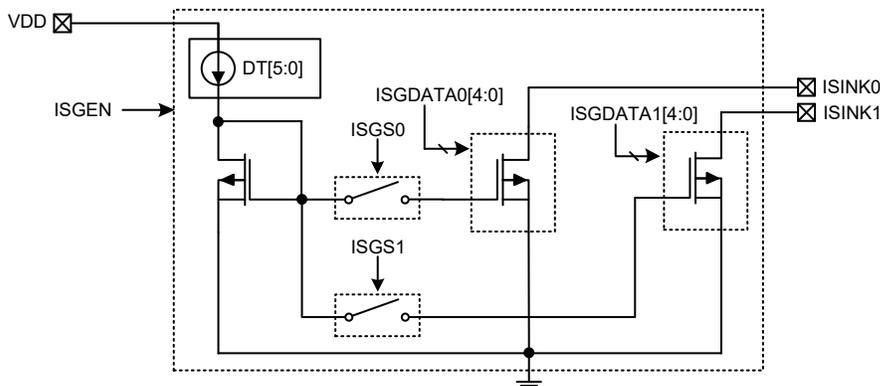
Sink Current Generator Registers

There are a series of registers control the overall operation of the Sink Current Generator function.

Register Name	Bit							
	7	6	5	4	3	2	1	0
ISGENC	ISGEN	—	—	—	—	—	ISGS1	ISGS0
ISGDATA0	—	—	—	D4	D3	D2	D1	D0
ISGDATA1	—	—	—	D4	D3	D2	D1	D0

Sink Current Generator Register List

- **ISGENC Register**

Bit	7	6	5	4	3	2	1	0
Name	ISGEN	—	—	—	—	—	ISGS1	ISGS0
R/W	R/W	—	—	—	—	—	R/W	R/W
POR	0	—	—	—	—	—	0	0

Bit 7　　**ISGEN**: Sink current generator enable control
　　　　　0: Disable
　　　　　1: Enable

When the ISGEN bit is cleared to zero to disable the sink current generator, the ISINK0 and ISINK1 pin status are VISINK0/1=floating, IISINK0/1=0.

Bit 6~2　Unimplemented, read as "0"

Bit 1　　**ISGS1**: ISINK1 pin sink current control
　　　　　0: Disable
　　　　　1: Enable

Bit 0　　**ISGS0**: ISINK0 pin sink current control
　　　　　0: Disable
　　　　　1: Enable

• **ISGDATA0 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	D4	D3	D2	D1	D0
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	—	—	—	0	0	0	0	0

Bit 7~5   Unimplemented, read as "0"

Bit 4~0   **D4~D0**: Sink current generator control for ISINK0 pin

Current value (mA)=50+10×(ISGDATA0[4:0])

When the ISGS0 bit is cleared to 0, the ISGDATA0[4:0] should be cleared to 00000 to avoid the leakage situation occur.

Refer to "Sink Current Generator Electrical Characteristics" table for more details.

• **ISGDATA1 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	D4	D3	D2	D1	D0
R/W	—	—	—	R/W	R/W	R/W	R/W	R/W
POR	—	—	—	0	0	0	0	0

Bit 7~5   Unimplemented, read as "0"

Bit 4~0   **D4~D0**: Sink current generator control for ISINK1 pin

Current value (mA)=50+5×(ISGDATA1[4:0])

When the ISGS1 bit is cleared to 0, the ISGDATA1[4:0] should be cleared to 00000 to avoid the leakage situation occur.

Refer to "Sink Current Generator Electrical Characteristics" table for more details.

Universal Serial Interface Module – USIM

The device contains a Universal Serial Interface Module, which includes the four-line SPI interface, the two-line I²C interface and the two-line/single-wire UART interface types, to allow an easy method of communication with external peripheral hardware. Having relatively simple communication protocols, these serial interface types allow the microcontroller to interface to external SPI, I²C or UART based hardware such as sensors, Flash or EEPROM memory, etc. The USIM interface pins are pin-shared with other I/O pins therefore the USIM interface functional pins must first be selected using the corresponding pin-shared function selection bits. As all the interface types share the same pins and registers, the choice of whether the UART, SPI or I²C type is used is made using the UART mode selection bit, named UMD, and the SPI/I²C operating mode control bits, named SIM2~SIM0, in the SIMC0 register. These pull-high resistors of the USIM pin-shared I/O pins are selected using pull-high control registers when the USIM function is enabled and the corresponding pins are used as USIM input pins.

SPI Interface

The SPI interface is often used to communicate with external peripheral devices such as sensors, Flash or EEPROM memory devices etc. Originally developed by Motorola, the four-line SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.

The communication is full duplex and operates as a slave/master type, where the device can be either master or slave. Although the SPI interface specification can control multiple slave devices from a single master, but the device provides only one $\overline{\text{SCS}}$ pin. If the master needs to control multiple slave devices from a single master, the master can use I/O pin to select the slave devices.

SPI Interface Operation

The SPI interface is a full duplex synchronous serial data link. It is a four-line interface with pin names SDI, SDO, SCK and $\overline{\text{SCS}}$. Pins SDI and SDO are the Serial Data Input and Serial Data Output lines, the SCK pin is the Serial Clock line and $\overline{\text{SCS}}$ is the Slave Select line. As the SPI interface pins are pin-shared with normal I/O pins and with the I²C/UART function pins, the SPI interface pins must first be selected by configuring the pin-shared function selection bits and setting the correct bits in the SIMC0 and SIMC2 registers. Communication between devices connected to the SPI interface is carried out in a slave/master mode with all data transfer initiations being implemented by the master. The Master also controls the clock signal. As the device only contains a single $\overline{\text{SCS}}$ pin only one slave device can be utilized. The $\overline{\text{SCS}}$ pin is controlled by software, set CSEN bit to 1 to enable $\overline{\text{SCS}}$ pin function, set CSEN bit to 0 the $\overline{\text{SCS}}$ pin will be floating state.
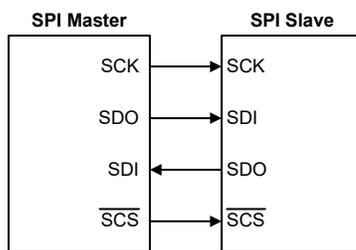

SPI Master/Slave Connection

The SPI function in the device offers the following features:

• Full duplex synchronous data transfer

• Both Master and Slave modes

• LSB first or MSB first data transmission modes

• Transmission complete flag

• Rising or falling active clock edge

The status of the SPI interface pins is determined by a number of factors such as whether the device is in the master or slave mode and upon the condition of certain control bits such as CSEN and SIMEN.
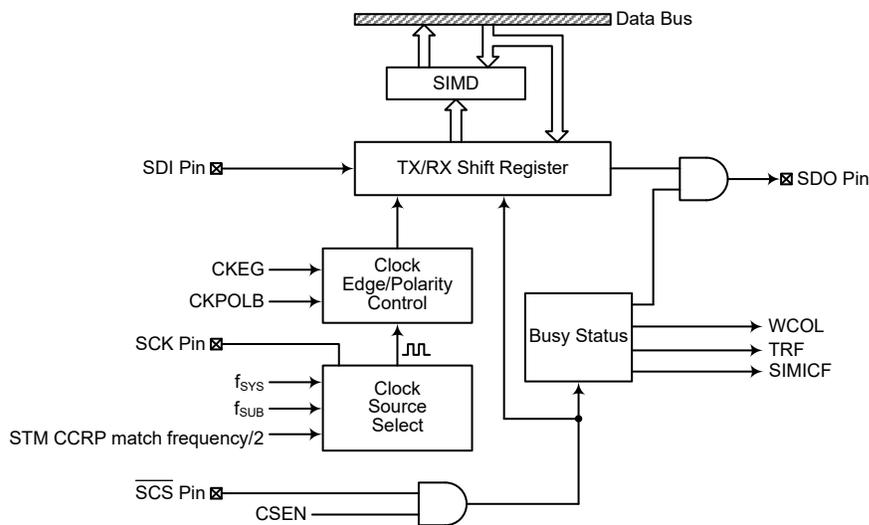
SPI Block Diagram

SPI Registers

There are three internal registers which control the overall operation of the SPI interface. These are the SIMD data register and two control registers, SIMC0 and SIMC2. Note that the SIMC2 and SIMD registers and their POR values are only available when the SPI mode is selected by properly configuring the UMD and SIM2~SIM0 bits in the SIMC0 register.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	UMD	SIMDEB1	SIMDEB0	SIMEN	SIMICF
SIMC2	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF
SIMD	D7	D6	D5	D4	D3	D2	D1	D0

SPI Register List

SPI Data Register

The SIMD register is used to store the data being transmitted and received. The same register is used by both the SPI and I²C functions. Before the device writes data to the SPI bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the SPI bus, the device can read it from the SIMD register. Any transmission or reception of data from the SPI bus must be made via the SIMD register.

• **SIMD Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": unknown

Bit 7~0　　**D7~D0**: USIM SPI/I²C data register bit 7 ~ bit 0

SPI Control Registers

There are also two control registers for the SPI interface, SIMC0 and SIMC2. The SIMC0 register is used to control the enable/disable function and to set the data transmission clock frequency. The SIMC2 register is used for other control functions such as LSB/MSB selection, write collision flag etc.

• **SIMC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	UMD	SIMDEB1	SIMDEB0	SIMEN	SIMICF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	0	0	0	0	0

Bit 7~5　　**SIM2~SIM0**: USIM SPI/I²C Operating Mode Control
　　　　　　000: SPI master mode; SPI clock is $f_{SYS}/4$
　　　　　　001: SPI master mode; SPI clock is $f_{SYS}/16$
　　　　　　010: SPI master mode; SPI clock is $f_{SYS}/64$
　　　　　　011: SPI master mode; SPI clock is f_{SUB}
　　　　　　100: SPI master mode; SPI clock is STM CCRP match frequency/2
　　　　　　101: SPI slave mode
　　　　　　110: I²C slave mode
　　　　　　111: Unused mode
　　　　　　When the UMD bit is cleared to zero, these bits setup the SPI or I²C operating mode of the USIM function. As well as selecting if the I²C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The

SPI clock is a function of the system clock but can also be chosen to be sourced from STM and f_{SUB}. If the SPI Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4   **UMD**: UART mode selection bit

0: SPI or I²C mode
1: UART mode

This bit is used to select the UART mode. When this bit is cleared to zero, the actual SPI or I²C mode can be selected using the SIM2~SIM0 bits.

Bit 3~2   **SIMDEB1~SIMDEB0**: I²C Debounce Time Selection

These bits are only available when the USIM is configured to operate in the I²C mode. Refer to the I²C register section.

Bit 1   **SIMEN**: USIM SPI/I²C Enable Control

0: Disable
1: Enable

The bit is the overall on/off control for the USIM SPI/I²C interface. When the SIMEN bit is cleared to zero to disable the USIM SPI/I²C interface, the SDI, SDO, SCK and SCS, or SDA and SCL lines will lose their SPI or I²C function and the USIM operating current will be reduced to a minimum value. When the bit is high the USIM SPI/I²C interface is enabled. If the USIM is configured to operate as an SPI interface via the UMD and SIM2~SIM0 bits, the contents of the SPI control registers will remain at the previous settings when the SIMEN bit changes from low to high and should therefore be first initialised by the application program. If the USIM is configured to operate as an I²C interface via the UMD and SIM2~SIM0 bits and the SIMEN bit changes from low to high, the contents of the I²C control bits such as HTX and TXAK will remain at the previous settings and should therefore be first initialised by the application program while the relevant I²C flags such as HCF, HAAS, HBB, SRW and RXAK will be set to their default states.

Bit 0   **SIMICF**: USIM SPI Incomplete Flag

0: USIM SPI incomplete condition is not occurred
1: USIM SPI incomplete condition is occurred

This bit is only available when the USIM is configured to operate in an SPI slave mode. If the SPI operates in the slave mode with the SIMEN and CSEN bits both being set high but the SCS line is pulled high by the external master device before the SPI data transfer is completely finished, the SIMICF bit will be set high together with the TRF bit. When this condition occurs, the corresponding interrupt will occur if the interrupt function is enabled. However, the TRF bit will not be set to 1 if the SIMICF bit is set to 1 by software application program.

• **SIMC2 Register**

| Bit	7	6	5	4	3	2	1	0
Name	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6   **D7~D6**: Undefined bits

These bits can be read or written by the application program.

Bit 5   **CKPOLB**: SPI clock line base condition selection

0: The SCK line will be high when the clock is inactive
1: The SCK line will be low when the clock is inactive

The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive.

Bit 4　　　**CKEG**: SPI SCK clock active edge type selection

　　　　　CKPOLB=0
　　　　　　0: SCK is high base level and data capture at SCK rising edge
　　　　　　1: SCK is high base level and data capture at SCK falling edge
　　　　　CKPOLB=1
　　　　　　0: SCK is low base level and data capture at SCK falling edge
　　　　　　1: SCK is low base level and data capture at SCK rising edge

　　　　　The CKEG and CKPOLB bits are used to setup the way that the clock signal outputs and inputs data on the SPI bus. These two bits must be configured before data transfer is executed otherwise an erroneous clock edge may be generated. The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive. The CKEG bit determines active clock edge type which depends upon the condition of CKPOLB bit.

Bit 3　　　**MLS**: SPI data shift order
　　　　　　0: LSB first
　　　　　　1: MSB first

　　　　　This is the data shift select bit and is used to select how the data is transferred, either MSB or LSB first. Setting the bit high will select MSB first and low for LSB first.

Bit 2　　　**CSEN**: SPI $\overline{\text{SCS}}$ pin control
　　　　　　0: Disable
　　　　　　1: Enable

　　　　　The CSEN bit is used as an enable/disable for the $\overline{\text{SCS}}$ pin. If this bit is low, then the $\overline{\text{SCS}}$ pin will be disabled and placed into a floating condition. If the bit is high the $\overline{\text{SCS}}$ pin will be enabled and used as a select pin.

Bit 1　　　**WCOL**: SPI write collision flag
　　　　　　0: No collision
　　　　　　1: Collision

　　　　　The WCOL flag is used to detect if a data collision has occurred. If this bit is high it means that data has been attempted to be written to the SIMD register during a data transfer operation. This writing operation will be ignored if data is being transferred. The bit can be cleared by the application program.

Bit 0　　　**TRF**: SPI Transmit/Receive complete flag
　　　　　　0: SPI data is being transferred
　　　　　　1: SPI data transmission is completed

　　　　　The TRF bit is the Transmit/Receive Complete flag and is set "1" automatically when an SPI data transmission is completed, but must set to "0" by the application program. It can be used to generate an interrupt.

SPI Communication

After the SPI interface is enabled by setting the SIMEN bit high, then in the Master Mode, when data is written to the SIMD register, transmission/reception will begin simultaneously. When the data transfer is completed, the TRF flag will be set high automatically, but must be cleared using the application program. In the Slave Mode, when the clock signal from the master has been received, any data in the SIMD register will be transmitted and any data on the SDI pin will be shifted into the SIMD register. The master should output an $\overline{\text{SCS}}$ signal to enable the slave devices before a clock signal is provided. The slave data to be transferred should be well prepared at the appropriate moment relative to the SCK signal depending upon the configurations of the CKPOLB bit and CKEG bit. The accompanying timing diagrams show the relationship between the slave data and SCK signal for various configurations of the CKPOLB and CKEG bits.
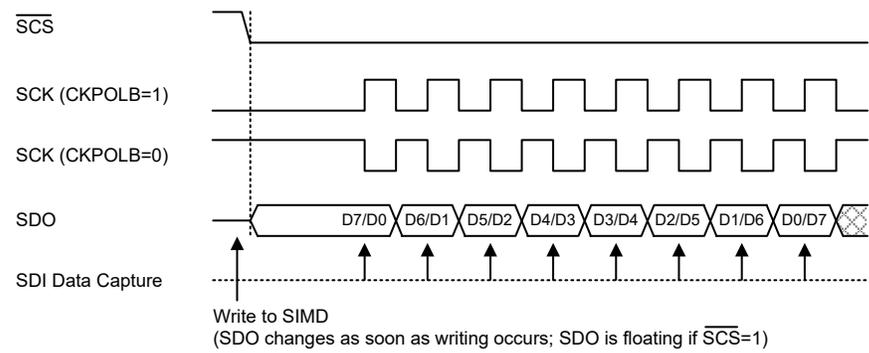
The SPI will continue to function in certain IDLE Modes if the clock source used by the SPI interface is still active.
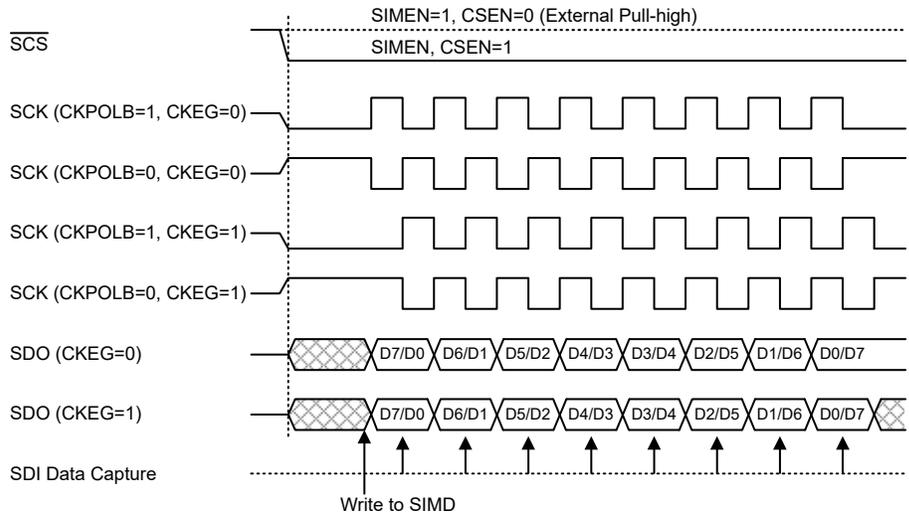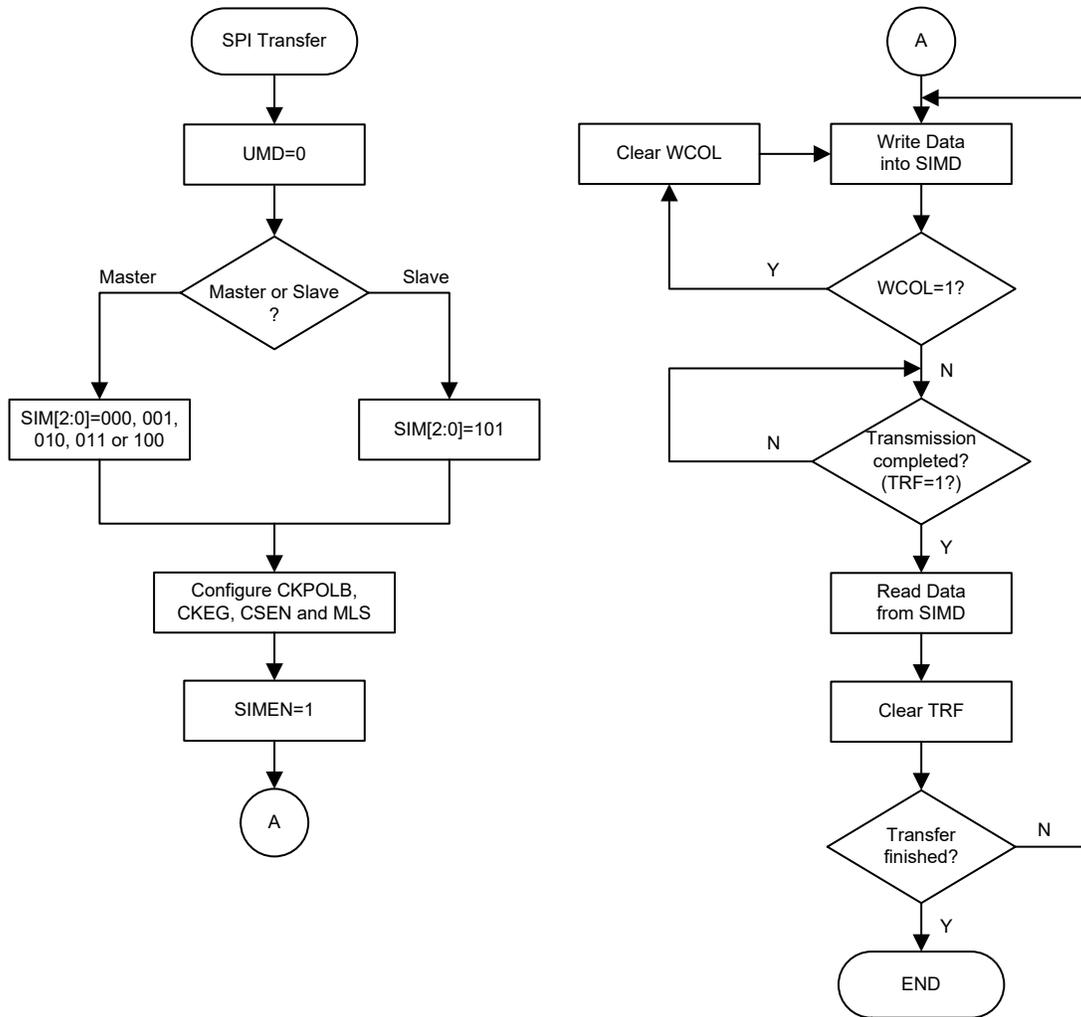
SPI Master Mode Timing
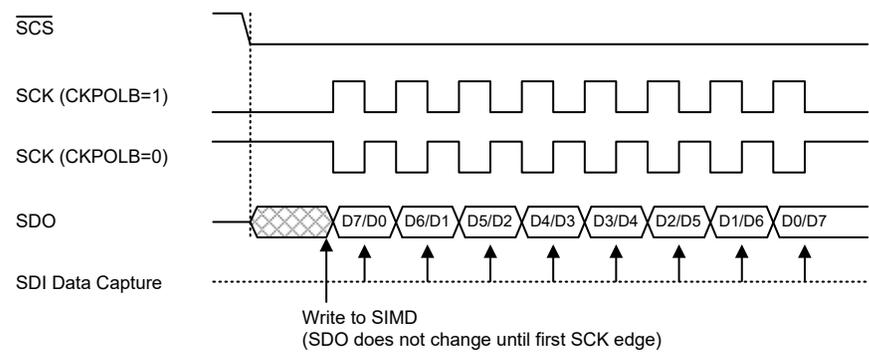
SPI Slave Mode Timing – CKEG=0

Note: For SPI slave mode, if SIMEN=1 and CSEN=0, SPI is always enabled and ignores the $\overline{SCS}$ level.

SPI Slave Mode Timing – CKEG=1

SPI Transfer Control Flowchart

SPI Bus Enable/Disable

To enable the SPI bus, set CSEN=1 and $\overline{SCS}$=0, then wait for data to be written into the SIMD (TXRX buffer) register. For the Master Mode, after data has been written to the SIMD (TXRX buffer) register, then transmission or reception will start automatically. When all the data has been transferred, the TRF bit should be set. For the Slave Mode, when clock pulses are received on SCK, data in the TXRX buffer will be shifted out or data on SDI will be shifted in.

When the SPI bus is disabled, SCK, SDI, SDO and $\overline{SCS}$ can become I/O pins or other pin-shared functions using the corresponding pin-shared control bits.

SPI Operation Steps

All communication is carried out using the 4-line interface for either Master or Slave Mode.

The CSEN bit in the SIMC2 register controls the $\overline{SCS}$ pin function of the SPI interface. Setting this bit high will enable the SPI interface by allowing the $\overline{SCS}$ line to be active, which can then be used to control the SPI interface. If the CSEN bit is low, the SPI interface will be disabled and the $\overline{SCS}$ line will be in a floating condition and can therefore not be used for control of the SPI interface. If the CSEN bit and the SIMEN bit in the SIMC0 are set high, this will place the SDI

line in a floating condition and the SDO line high. If in Master Mode the SCK line will be either high or low depending upon the clock polarity selection bit CKPOLB in the SIMC2 register. If in Slave Mode the SCK line will be in a floating condition. If the SIMEN bit is low, then the bus will be disabled and $\overline{SCS}$, SDI, SDO and SCK will all become I/O pins or the other functions using the corresponding pin-shared control bits. In the Master Mode the Master will always generate the clock signal. The clock and data transmission will be initiated after data has been written into the SIMD register. In the Slave Mode, the clock signal will be received from an external master device for both data transmission and reception. The following sequences show the order to be followed for data transfer in both Master and Slave Mode.

Master Mode

- Step 1

  Select the SPI Master mode and clock source using the UMD and SIM2~SIM0 bits in the SIMC0 control register.

- Step 2

  Setup the CSEN bit and setup the MLS bit to choose if the data is MSB or LSB first, this setting must be the same with the Slave devices.

- Step 3

  Setup the SIMEN bit in the SIMC0 control register to enable the SPI interface.

- Step 4

  For write operations: write the data to the SIMD register, which will actually place the data into the TXRX buffer. Then use the SCK and SDO lines to output the data. After this, go to step 5.

  For read operations: the data transferred in on the SDI line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SIMD register.

- Step 5

  Check the WCOL bit if set high then a collision error has occurred so return to step 4. If equal to zero then go to the following step.

- Step 6

  Check the TRF bit or wait for a USIM SPI serial bus interrupt.

- Step 7

  Read data from the SIMD register.

- Step 8

  Clear TRF.

- Step 9

  Go to step 4.

Slave Mode

- Step 1

  Select the SPI Slave mode using the UMD and SIM2~SIM0 bits in the SIMC0 control register

- Step 2

  Setup the CSEN bit and setup the MLS bit to choose if the data is MSB or LSB first, this setting must be the same with the Master devices.

- Step 3

  Setup the SIMEN bit in the SIMC0 control register to enable the SPI interface.

- Step 4

    For write operations: write the data to the SIMD register, which will actually place the data into the TXRX buffer. Then wait for the master clock SCK and $\overline{SCS}$ signal. After this, go to step 5.

    For read operations: the data transferred in on the SDI line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SIMD register.

- Step 5

    Check the WCOL bit if set high then a collision error has occurred so return to step 4. If equal to zero then go to the following step.

- Step 6

    Check the TRF bit or wait for a USIM SPI serial bus interrupt.

- Step 7

    Read data from the SIMD register.

- Step 8

    Clear TRF.

- Step 9

    Go to step 4.

Error Detection

The WCOL bit in the SIMC2 register is provided to indicate errors during data transfer. The bit is set by the SPI serial Interface but must be cleared by the application program. This bit indicates that a data collision has occurred which happens if a write to the SIMD register takes place during a data transfer operation and will prevent the write operation from continuing.

I²C Interface

The I²C interface is used to communicate with external peripheral devices such as sensors, EEPROM memory etc. Originally developed by Philips, it is a two-line low speed serial interface for synchronous serial data transfer. The advantage of only two lines for communication, relatively simple communication protocol and the ability to accommodate multiple devices on the same bus has made it an extremely popular interface type for many applications.


I²C Master Slave Bus Connection
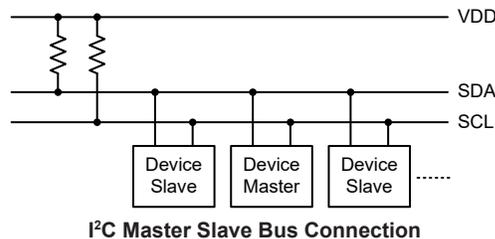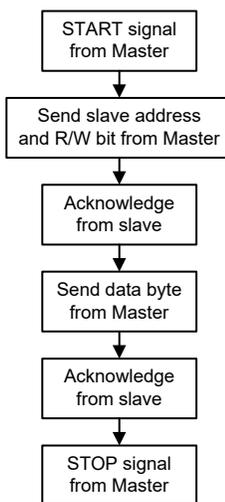
I²C Interface Operation

The I²C serial interface is a two-line interface, a serial data line, SDA, and serial clock line, SCL. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I²C bus is identified by a unique address which will be transmitted and received on the I²C bus.

When two devices communicate with each other on the bidirectional I²C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data,

however, it is the master device that has overall control of the bus. For the device, which only operates in slave mode, there are two methods of transferring data on the I²C bus, the slave transmit mode and the slave receive mode. The pull-high control function pin-shared with SCL/SDA pin is still applicable even if I²C device is activated and the related internal pull-high register could be controlled by its corresponding pull-high control register.
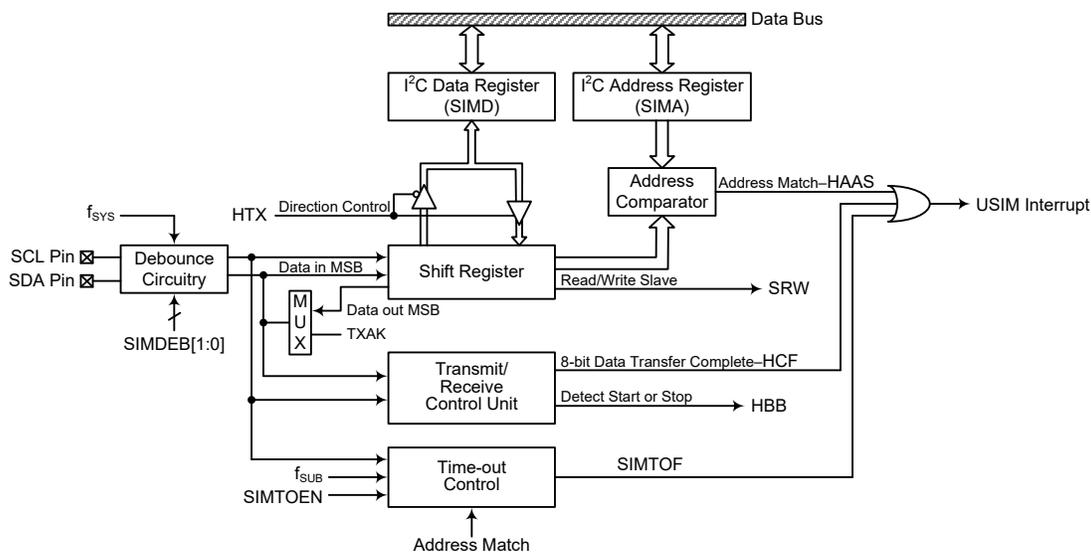
I²C Block Diagram

I²C Interface Operation

The SIMDEB1 and SIMDEB0 bits determine the debounce time of the I²C interface. This uses the internal clock to in effect add a debounce time to the external clock to reduce the possibility of glitches on the clock line causing erroneous operation. The debounce time, if selected, can be chosen to be either 2 or 4 system clocks. To achieve the required I²C data transfer speed, there exists a relationship between the system clock, f_{SYS}, and the I²C debounce time. For either the I²C Standard or Fast mode operation, users must take care of the selected system clock frequency and the configured debounce time to match the criterion shown in the following table.

I²C Debounce Time Selection	I²C Standard Mode (100kHz)	I²C Fast Mode (400kHz)
No Debounce	$f_{SYS}>2MHz$	$f_{SYS}>4MHz$
2 system clock debounce	$f_{SYS}>4MHz$	$f_{SYS}>8MHz$
4 system clock debounce	$f_{SYS}>4MHz$	$f_{SYS}>8MHz$

I²C Minimum f_{SYS} Frequency Requirements

I²C Registers

There are three control registers associated with the I²C bus, SIMC0, SIMC1 and SIMTOC, one address register SIMA and one data register, SIMD. Note that the SIMC1, SIMD, SIMA and SIMTOC registers and their POR values are only available when the I²C mode is selected by properly configuring the UMD and SIM2~SIM0 bits in the SIMC0 register.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	UMD	SIMDEB1	SIMDEB0	SIMEN	SIMICF
SIMC1	HCF	HAAS	HBB	HTX	TXAK	SRW	IAMWU	RXAK
SIMD	D7	D6	D5	D4	D3	D2	D1	D0
SIMA	SIMA6	SIMA5	SIMA4	SIMA3	SIMA2	SIMA1	SIMA0	D0
SIMTOC	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0

I²C Register List

I²C Data Register

The SIMD register is used to store the data being transmitted and received. The same register is used by both the SPI and I²C functions. Before the device writes data to the I²C bus, the actual data to be transmitted must be placed in the SIMD register. After the data is received from the I²C bus, the device can read it from the SIMD register. Any transmission or reception of data from the I²C bus must be made via the SIMD register.

• **SIMD Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": unknown

Bit 7~0   **D7~D0**: USIM SPI/I²C data register bit 7~bit 0

I²C Address Register

The SIMA register is also used by the SPI interface but has the name of SIMC2. The SIMA register is the location where the 7-bit slave address of the slave device is stored. Bits 7~1 of the SIMA register define the device slave address. Bit 0 is not defined. When a master device, which is connected to the I²C bus, sends out an address, which matches the slave address in the SIMA register, the slave device will be selected.

• **SIMA Register**

Bit	7	6	5	4	3	2	1	0
Name	SIMA6	SIMA5	SIMA4	SIMA3	SIMA2	SIMA1	SIMA0	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~1   **SIMA6~SIMA0**: I²C slave address

SIMA6~SIMA0 is the I²C slave address bit 6~bit 0.

Bit 0   **D0**: Reserved bit, can be read or written

I²C Control Registers

There are three control registers for the I²C interface, SIMC0, SIMC1 and SIMTOC. The SIMC0 register is used to control the enable/disable function and to select the I²C slave mode and debounce time. The SIMC1 register contains the relevant flags which are used to indicate the I²C communication status. Another register, SIMTOC, is used to control the I²C time-out function and is described in the corresponding section.

• **SIMC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	UMD	SIMDEB1	SIMDEB0	SIMEN	SIMICF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	0	0	0	0	0

Bit 7~5   **SIM2~SIM0**: USIM SPI/I²C Operating Mode Control
    000: SPI master mode; SPI clock is $f_{SYS}/4$
    001: SPI master mode; SPI clock is $f_{SYS}/16$
    010: SPI master mode; SPI clock is $f_{SYS}/64$
    011: SPI master mode; SPI clock is f_{SUB}
    100: SPI master mode; SPI clock is STM CCRP match frequency/2
    101: SPI slave mode
    110: I²C slave mode
    111: Unused mode

When the UMD bit is cleared to zero, these bits setup the SPI or I²C operating mode of the USIM function. As well as selecting if the I²C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The SPI clock is a function of the system clock but can also be chosen to be sourced from STM and f_{SUB}. If the SPI Slave Mode is selected then the clock will be supplied by an external Master device.

Bit 4   **UMD**: UART mode selection bit
    0: SPI or I²C mode
    1: UART mode

This bit is used to select the UART mode. When this bit is cleared to zero, the actual SPI or I²C mode can be selected using the SIM2~SIM0 bits. Note that the UMD bit must be set low for SPI or I²C mode.

Bit 3~2   **SIMDEB1~SIMDEB0**: I²C Debounce Time Selection
    00: No debounce
    01: 2 system clock debounce
    1x: 4 system clock debounce

These bits are used to select the I²C debounce time when the USIM is configured as the I²C interface function by setting the UMD bit to "0" and the SIM2~SIM0 bits to "110".

Bit 1   **SIMEN**: USIM SPI/I²C Enable Control
    0: Disable
    1: Enable

The bit is the overall on/off control for the USIM SPI/I²C interface. When the SIMEN bit is cleared to zero to disable the USIM SPI/I²C interface, the SDI, SDO, SCK and $\overline{SCS}$, or SDA and SCL lines will lose their SPI or I²C function and the USIM operating current will be reduced to a minimum value. When the bit is high the USIM SPI/I²C interface is enabled. If the USIM is configured to operate as an SPI interface via the UMD and SIM2~SIM0 bits, the contents of the SPI control registers will remain at the previous settings when the SIMEN bit changes from low to high and should therefore be first initialised by the application program. If the USIM is configured to operate as an I²C interface via the UMD and SIM2~SIM0 bits and the SIMEN bit changes from low to high, the contents of the I²C control bits such as HTX and TXAK will remain at the previous settings and should therefore be first initialised by the application program while the relevant I²C flags such as HCF, HAAS, HBB, SRW and RXAK will be set to their default states.

Bit 0   **SIMICF**: USIM SPI Incomplete Flag

This bit is only available when the USIM is configured to operate in an SPI slave mode. Refer to the SPI register section.

• **SIMC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	HCF	HAAS	HBB	HTX	TXAK	SRW	IAMWU	RXAK
R/W	R	R	R	R/W	R/W	R	R/W	R
POR	1	0	0	0	0	0	0	1

Bit 7   **HCF**: I²C Bus data transfer completion flag

0: Data is being transferred
1: Completion of an 8-bit data transfer

The HCF flag is the data transfer flag. This flag will be zero when data is being transferred. Upon completion of an 8-bit data transfer the flag will go high and an interrupt will be generated. Below is an example of the flow of a two-byte I²C data transfer. First, I²C slave device receives a start signal from I²C master and then HCF bit is automatically cleared to zero. Second, I²C slave device finishes receiving the 1st data byte and then HCF bit is automatically set high. Third, user read the 1st data byte from SIMD register by the application program and then HCF bit is automatically cleared to zero. Fourth, I²C slave device finishes receiving the 2nd data byte and then HCF bit is automatically set to one and so on. Finally, I²C slave device receives a stop signal from I²C master and then HCF bit is automatically set high.

Bit 6   **HAAS**: I²C Bus address match flag

0: Not address match
1: Address match

The HAAS flag is the address match flag. This flag is used to determine if the slave device address is the same as the master transmit address. If the addresses match then this bit will be high, if there is no match then the flag will be low.

Bit 5   **HBB**: I²C Bus busy flag

0: I²C Bus is not busy
1: I²C Bus is busy

The HBB flag is the I²C busy flag. This flag will be "1" when the I²C bus is busy which will occur when a START signal is detected. The flag will be set to "0" when the bus is free which will occur when a STOP signal is detected.

Bit 4   **HTX**: I²C slave device is transmitter or receiver selection

0: Slave device is the receiver
1: Slave device is the transmitter

Bit 3   **TXAK**: I²C Bus transmit acknowledge flag

0: Slave send acknowledge flag
1: Slave do not send acknowledge flag

The TXAK bit is the transmit acknowledge flag. After the slave device receipt of 8 bits of data, this bit will be transmitted to the bus on the 9th clock from the slave device. The slave device must always set TXAK bit to "0" before further data is received.

Bit 2   **SRW**: I²C Slave Read/Write flag

0: Slave device should be in receive mode
1: Slave device should be in transmit mode

The SRW flag is the I²C Slave Read/Write flag. This flag determines whether the master device wishes to transmit or receive data from the I²C bus. When the transmitted address and slave address match, that is when the HAAS flag is set high, the slave device will check the SRW flag to determine whether it should be in transmit mode or receive mode. If the SRW flag is high, the master is requesting to read data from the bus, so the slave device should be in transmit mode. When the SRW flag is zero, the master will write data to the bus, therefore the slave device should be in receive mode to read this data.

Bit 1   **IAMWU**: I²C Address Match Wake-up control

0: Disable

1: Enable

This bit should be set to 1 to enable the I²C address match wake-up from the SLEEP or IDLE Mode. If the IAMWU bit has been set before entering either the SLEEP or IDLE mode to enable the I²C address match wake-up, then this bit must be cleared by the application program after wake-up to ensure correction device operation.

Bit 0   **RXAK**: I²C Bus Receive acknowledge flag

0: Slave receive acknowledge flag

1: Slave does not receive acknowledge flag

The RXAK flag is the receiver acknowledge flag. When the RXAK flag is "0", it means that a acknowledge signal has been received at the 9th clock, after 8 bits of data have been transmitted. When the slave device in the transmit mode, the slave device checks the RXAK flag to determine if the master receiver wishes to receive the next byte. The slave transmitter will therefore continue sending out data until the RXAK flag is "1". When this occurs, the slave transmitter will release the SDA line to allow the master to send a STOP signal to release the I²C Bus.

I²C Bus Communication

Communication on the I²C bus requires four separate steps, a START signal, a slave device address transmission, a data transmission and finally a STOP signal. When a START signal is placed on the I²C bus, all devices on the bus will receive this signal and be notified of the imminent arrival of data on the bus. The first seven bits of the data will be the slave address with the first bit being the MSB. If the address of the slave device matches that of the transmitted address, the HAAS bit in the SIMC1 register will be set and a USIM interrupt will be generated. After entering the interrupt service routine, the slave device must first check the condition of the HAAS and SIMTOF bits to determine whether the interrupt source originates from an address match or from the completion of an 8-bit data transfer completion or from the I²C bus time-out occurrence. During a data transfer, note that after the 7-bit slave address has been transmitted, the following bit, which is the 8th bit, is the read/write bit whose value will be placed in the SRW bit. This bit will be checked by the slave device to determine whether to go into transmit or receive mode. Before any transfer of data to or from the I²C bus, the microcontroller must initialise the bus, the following are steps to achieve this:

• Step 1

Set the UMD, SIM2~SIM0 and SIMEN bits in the SIMC0 register to "0", "110" and "1" respectively to enable the I²C bus.

• Step 2

Write the slave address of the device to the I²C bus address register SIMA.

• Step 3

Set the USIME interrupt enable bit of the interrupt control register to enable the USIM interrupt.
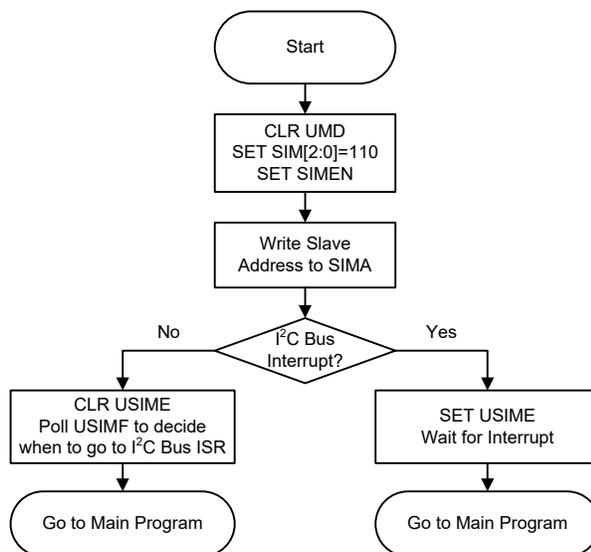
I²C Bus Initialisation Flow Chart

I²C Bus Start Signal

The START signal can only be generated by the master device connected to the I²C bus and not by the slave device. This START signal will be detected by all devices connected to the I²C bus. When detected, this indicates that the I²C bus is busy and therefore the HBB bit will be set. A START condition occurs when a high to low transition on the SDA line takes place when the SCL line remains high.

I²C Slave Address

The transmission of a START signal by the master will be detected by all devices on the I²C bus. To determine which slave device the master wishes to communicate with, the address of the slave device will be sent out immediately following the START signal. All slave devices, after receiving this 7-bit address data, will compare it with their own 7-bit slave address. If the address sent out by the master matches the internal address of the microcontroller slave device, then an internal USIM I²C bus interrupt signal will be generated. The next bit following the address, which is the 8th bit, defines the read/write status and will be saved to the SRW bit of the SIMC1 register. The slave device will then transmit an acknowledge bit, which is a low level, as the 9th bit. The slave device will also set the status flag HAAS when the addresses match.

As an USIM I²C bus interrupt can come from three sources, when the program enters the interrupt subroutine, the HAAS and SIMTOF bits should be examined to see whether the interrupt source has come from a matching slave address or from the completion of a data byte transfer or from the I²C bus time-out occurrence. When a slave address is matched, the device must be placed in either the transmit mode and then write data to the SIMD register, or in the receive mode where it must implement a dummy read from the SIMD register to release the SCL line.

I²C Bus Read/Write Signal

The SRW bit in the SIMC1 register defines whether the master device wishes to read data from the I²C bus or write data to the I²C bus. The slave device should examine this bit to determine if it is to be a transmitter or a receiver. If the SRW flag is "1" then this indicates that the master device wishes to read data from the I²C bus, therefore the slave device must be setup to send data to the I²C bus as a transmitter. If the SRW flag is "0" then this indicates that the master wishes to send data to the I²C bus, therefore the slave device must be setup to read data from the I²C bus as a receiver.
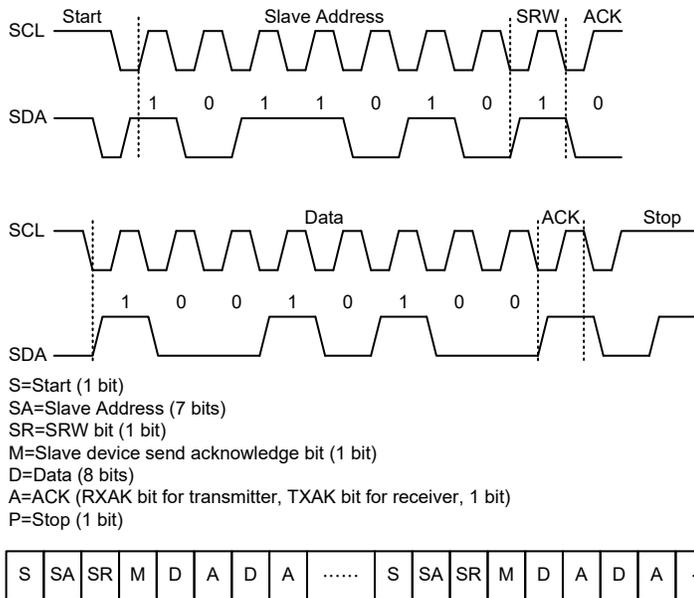
I²C Bus Slave Address Acknowledge Signal

After the master has transmitted a calling address, any slave device on the I²C bus, whose own internal address matches the calling address, must generate an acknowledge signal. The acknowledge signal will inform the master that a slave device has accepted its calling address. If no acknowledge signal is received by the master then a STOP signal must be transmitted by the master to end the communication. When the HAAS flag is high, the addresses have matched and the slave device must check the SRW flag to determine if it is to be a transmitter or a receiver. If the SRW flag is high, the slave device should be setup to be a transmitter so the HTX bit in the SIMC1 register should be set to "1". If the SRW flag is low, then the microcontroller slave device should be setup as a receiver and the HTX bit in the SIMC1 register should be set to "0".

I²C Bus Data and Acknowledge Signal

The transmitted data is 8-bit wide and is transmitted after the slave device has acknowledged receipt of its slave address. The order of serial bit transmission is the MSB first and the LSB last. After receipt of 8 bits of data, the receiver must transmit an acknowledge signal, level "0", before it can receive the next data byte. If the slave transmitter does not receive an acknowledge bit signal from the master receiver, then the slave transmitter will release the SDA line to allow the master to send a STOP signal to release the I²C Bus. The corresponding data will be stored in the SIMD register. If setup as a transmitter, the slave device must first write the data to be transmitted into the SIMD register. If setup as a receiver, the slave device must read the transmitted data from the SIMD register.

When the slave receiver receives the data byte, it must generate an acknowledge bit, known as TXAK, on the 9th clock. The slave device, which is setup as a transmitter will check the RXAK bit in the SIMC1 register to determine if it is to send another data byte, if not then it will release the SDA line and await the receipt of a STOP signal from the master.

S=Start (1 bit)
SA=Slave Address (7 bits)
SR=SRW bit (1 bit)
M=Slave device send acknowledge bit (1 bit)
D=Data (8 bits)
A=ACK (RXAK bit for transmitter, TXAK bit for receiver, 1 bit)
P=Stop (1 bit)

| S | SA | SR | M | D | A | D | A | ...... | S | SA | SR | M | D | A | D | A | ...... | P |

**I²C Communication Timing Diagram**

Note: When a slave address is matched, the device must be placed in either the transmit mode and then write data to the SIMD register, or in the receive mode where it must implement a dummy read from the SIMD register to release the SCL line.
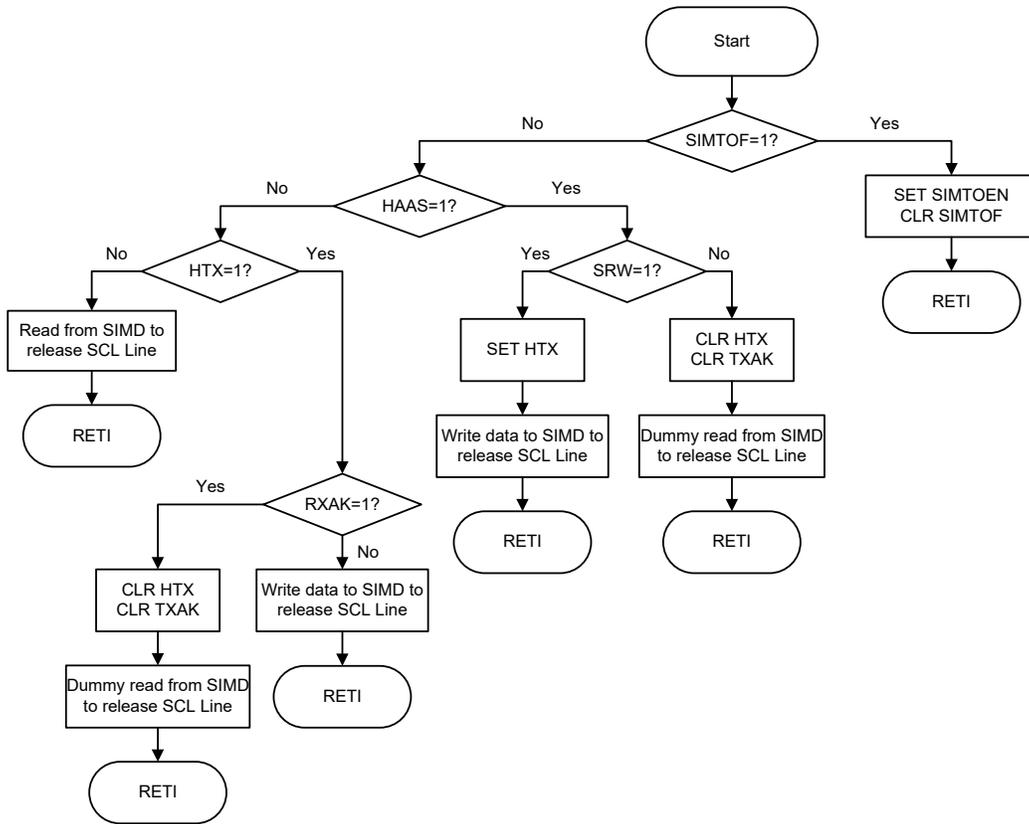
I²C Bus ISR Flow Chart

I²C Time-out Control

In order to reduce the problem of I²C lockup due to reception of erroneous clock sources, a time-out function is provided. If the clock source to the I²C is not received for a while, then the I²C circuitry and registers will be reset after a certain time-out period. The time-out counter starts counting on an I²C bus "START" & "address match" condition, and is cleared by an SCL falling edge. Before the next SCL falling edge arrives, if the time elapsed is greater than the time-out setup by the SIMTOC register, then a time-out condition will occur. The time-out function will stop when an I²C "STOP" condition occurs.
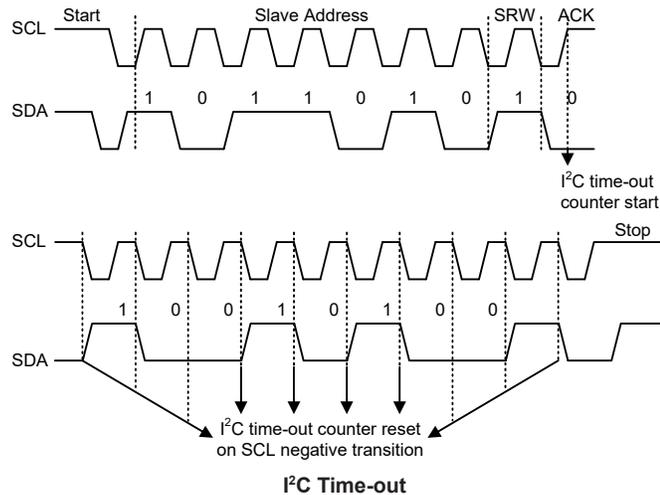
I²C Time-out

When an I²C time-out counter overflow occurs, the counter will stop and the SIMTOEN bit will be cleared to zero and the SIMTOF bit will be set high to indicate that a time-out condition has occurred. The time-out condition will also generate an interrupt which uses the USIM interrupt vector. When an I²C time-out occurs, the I²C internal circuitry will be reset and the registers will be reset into the following condition:

Registers	After I²C Time-out
SIMD, SIMA, SIMC0	No change
SIMC1	Reset to POR condition

I²C Registers after Time-out

The SIMTOF flag can be cleared by the application program. There are 64 time-out periods which can be selected using SIMTOS5~SIMTOS0 bits in the SIMTOC register. The time-out time is given by the formula: $((1{\sim}64){\times}32)/f_{SUB}$. This gives a time-out period which ranges from about 1ms to 64ms.

- **SIMTOC Register**

Bit	7	6	5	4	3	2	1	0
Name	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **SIMTOEN**: USIM I²C Time-out control
      0: Disable
      1: Enable

Bit 6   **SIMTOF**: USIM I²C Time-out flag
      0: No time-out occurred
      1: Time-out occurred
      This bit is set high when time-out occurs and can only be cleared by application program.

Bit 5~0   **SIMTOS5~SIMTOS0**: USIM I²C Time-out period selection
      I²C time-out clock source is $f_{SUB}/32$.
      I²C time-out time is equal to $(SIMTOS[5:0]+1){\times}(32/f_{SUB})$.
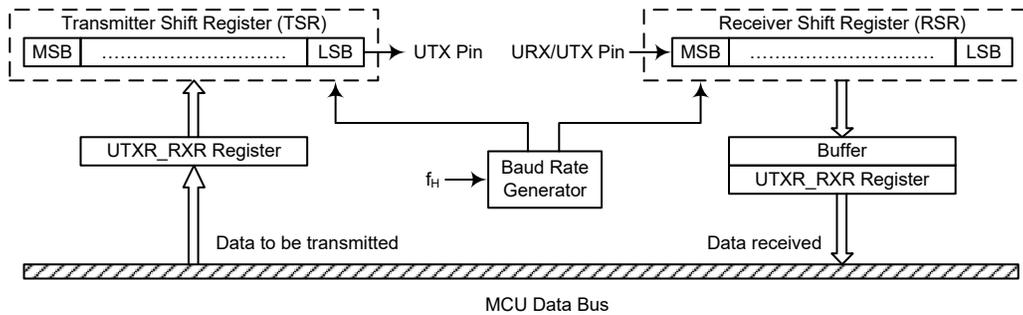
UART Interface

The device contains an integrated full-duplex or half-duplex asynchronous serial communications UART interface that enables communication with external devices that contain a serial interface. The UART function has many features and can transmit and receive data serially by transferring a frame of data with eight or nine data bits per transmission as well as being able to detect errors when the data is overwritten or incorrectly framed. The UART function shares the same internal interrupt vector with the SPI and I²C interfaces which can be used to indicate when a reception occurs or when a transmission terminates.

The integrated UART function contains the following features:

- Full-duplex or half-duplex (single wire mode) asynchronous communication

- 8 or 9 bits character length

- Even, odd or no parity options

- One or two stop bits

- Baud rate generator with 8-bit prescaler

- Parity, framing, noise and overrun error detection

- Support for interrupt on address detect (last character bit=1)

- Separately enabled transmitter and receiver
- 2-byte Deep FIFO Receive Data Buffer
- URX/UTX pin wake-up function
- Transmit and receive interrupts
- Interrupts can be triggered by the following conditions:
  - Transmitter Empty
  - Transmitter Idle
  - Receiver Full
  - Receiver Overrun
  - Address Mode Detect

UART Data Transfer Block Diagram – USWM=0
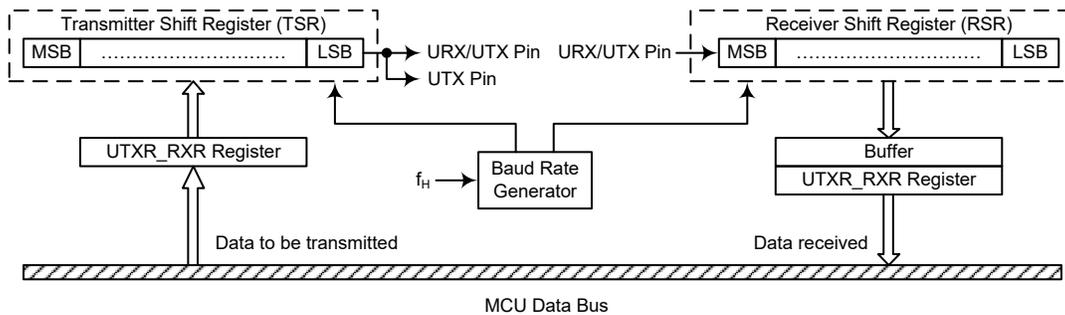
UART Data Transfer Block Diagram – USWM=1

UART External Pins

To communicate with an external serial interface, the internal UART has two external pins known as UTX pin and URX/UTX pin, which are pin-shared with I/O or other pin functions. The UTX and URX/UTX pin function should first be selected by the corresponding pin-shared function selection register before the UART function is used. Along with the UMD bit, the UREN bit, the UTXEN or URXEN bits, if set, will setup these pins to transmitter output and receiver input conditions. At this time the internal pull-high resistor related to the transmitter output pin will be disabled, while the internal pull-high resistor related to the receiver input pin is controlled by the corresponding I/O pull-high function control bit. When the UTX or URX/UTX pin function is disabled by clearing the UMD, UREN, UTXEN or URXEN bit, the UTX or URX/UTX pin will be set to a floating state. At this time whether the internal pull-high resistor is connected to the UTX or URX/UTX pin or not is determined by the corresponding I/O pull-high function control bit.

UART Single Wire Mode

The UART function also supports a Single Wire Mode communication which is selected using the USWM bit in the UUCR3 register. When the USWM bit is set high, the UART function will be in the single wire mode. In the single wire mode, a single URX/UTX pin can be used to transmit and receive data depending upon the corresponding control bits. When the URXEN bit is set high, the URX/UTX pin is used as a receiver pin. When the URXEN bit is cleared to zero and the UTXEN bit is set high, the URX/UTX pin will act as a transmitter pin.

It is recommended not to set both the URXEN and UTXEN bits high in the single wire mode. If both the URXEN and UTXEN bits are set high, the URXEN bit will have the priority and the UART will act as a receiver.

It is important to note that the functional description in this UART chapter, which is described from the full-duplex communication standpoint, also applies to the half-duplex (single wire mode) communication except the pin usage. In the single wire mode, the UTX pin mentioned in this chapter should be replaced by the URX/UTX pin to understand the whole UART single wire mode function.

In the single wire mode, the data can also be transmitted on the UTX pin in a transmission operation with proper software configurations. Therefore, the data will be output on the URX/UTX and UTX pins.

UART Data Transfer Scheme

The UART Data Transfer Block Diagram shows the overall data transfer structure arrangement for the UART. The actual data to be transmitted from the MCU is first transferred to the UTXR_RXR register by the application program. The data will then be transferred to the Transmit Shift Register from where it will be shifted out, LSB first, onto the UTX pin at a rate controlled by the Baud Rate Generator. Only the UTXR_RXR register is mapped onto the MCU Data Memory, the Transmit Shift Register is not mapped and is therefore inaccessible to the application program.

Data to be received by the UART is accepted on the external URX/UTX pin, from where it is shifted in, LSB first, to the Receiver Shift Register at a rate controlled by the Baud Rate Generator. When the shift register is full, the data will then be transferred from the shift register to the internal UTXR_RXR register, where it is buffered and can be manipulated by the application program. Only the UTXR_RXR register is mapped onto the MCU Data Memory, the Receiver Shift Register is not mapped and is therefore inaccessible to the application program.

It should be noted that the actual register for data transmission and reception only exists as a single shared register in the Data Memory. This shared register known as the UTXR_RXR register is used for both data transmission and data reception.

UART Status and Control Registers

There are seven control registers associated with the UART function. The UMD bit in the SIMC0 register can be used to select the UART interface. The USWM bit in the UUCR3 register is used to enable/disable the UART Single Wire Mode. The UUSR, UUCR1 and UUCR2 registers control the overall function of the UART, while the UBRG register controls the Baud rate. The actual data to be transmitted and received on the serial interface is managed through the UTXR_RXR data register. Note that UART related registers and their POR values are only available when the UART mode is selected by setting the UMD bit in the SIMC0 register to "1".

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	UMD	SIMDEB1	SIMDEB0	SIMEN	SIMICF
UUSR	UPERR	UNF	UFERR	UOERR	URIDLE	URXIF	UTIDLE	UTXIF
UUCR1	UREN	UBNO	UPREN	UPRT	USTOPS	UTXBRK	URX8	UTX8
UUCR2	UTXEN	URXEN	UBRGH	UADDEN	UWAKE	URIE	UTIIE	UTEIE
UUCR3	—	—	—	—	—	—	—	USWM
UTXR_RXR	UTXRX7	UTXRX6	UTXRX5	UTXRX4	UTXRX3	UTXRX2	UTXRX1	UTXRX0
UBRG	UBRG7	UBRG6	UBRG5	UBRG4	UBRG3	UBRG2	UBRG1	UBRG0

UART Register List

• **SIMC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	UMD	SIMDEB1	SIMDEB0	SIMEN	SIMICF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	0	0	0	0	0

Bit 7~5   **SIM2~SIM0**: USIM SPI/I^{2}C Operating Mode Control

When the UMD bit is cleared to zero, these bits setup the SPI or I^{2}C operating mode of the USIM function. Refer to the SPI or I^{2}C register section for more details.

Bit 4   **UMD**: UART mode selection bit

0: SPI or I^{2}C mode
1: UART mode

This bit is used to select the UART mode. When this bit is cleared to zero, the actual SPI or I^{2}C mode can be selected using the SIM2~SIM0 bits.

Bit 3~2   **SIMDEB1~SIMDEB0**: I^{2}C Debounce Time Selection

Refer to the I^{2}C register section.

Bit 1   **SIMEN**: USIM SPI/I^{2}C Enable Control

This bit is only available when the USIM is configured to operate in an SPI or I^{2}C mode with the UMD bit set low. Refer to the SPI or I^{2}C register section for more details.

Bit 0   **SIMICF**: USIM SPI Incomplete Flag

Refer to the SPI register section.

• **UUSR Register**

The UUSR register is the status register for the UART, which can be read by the program to determine the present status of the UART. All flags within the UUSR register are read only. Further explanation on each of the flags is given below:

Bit	7	6	5	4	3	2	1	0
Name	UPERR	UNF	UFERR	UOERR	URIDLE	URXIF	UTIDLE	UTXIF
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	1	0	1	1

Bit 7   **UPERR**: Parity error flag

0: No parity error is detected
1: Parity error is detected

The UPERR flag is the parity error flag. When this read only flag is "0", it indicates a parity error has not been detected. When the flag is "1", it indicates that the parity of the received word is incorrect. This error flag is applicable only if Parity mode (odd or even) is selected. The flag can also be cleared by a software sequence which involves a read to the status register UUSR followed by an access to the UTXR_RXR data register.

Bit 6   **UNF**: Noise flag

         0: No noise is detected

         1: Noise is detected

The UNF flag is the noise flag. When this read only flag is "0", it indicates no noise condition. When the flag is "1", it indicates that the UART has detected noise on the receiver input. The UNF flag is set during the same cycle as the URXIF flag but will not be set in the case of as overrun. The UNF flag can be cleared by a software sequence which will involve a read to the status register UUSR followed by an access to the UTXR_RXR data register.

Bit 5   **UFERR**: Framing error flag

         0: No framing error is detected

         1: Framing error is detected

The UFERR flag is the framing error flag. When this read only flag is "0", it indicates that there is no framing error. When the flag is "1", it indicates that a framing error has been detected for the current character. The flag can also be cleared by a software sequence which will involve a read to the status register UUSR followed by an access to the UTXR_RXR data register.

Bit 4   **UOERR**: Overrun error flag

         0: No overrun error is detected

         1: Overrun error is detected

The UOERR flag is the overrun error flag which indicates when the receiver buffer has overflowed. When this read only flag is "0", it indicates that there is no overrun error. When the flag is "1", it indicates that an overrun error occurs which will inhibit further transfers to the UTXR_RXR receive data register. The flag is cleared by a software sequence, which is a read to the status register UUSR followed by an access to the UTXR_RXR data register.

Bit 3   **URIDLE**: Receiver status

         0: Data reception is in progress (Data being received)

         1: No data reception is in progress (Receiver is idle)

The URIDLE flag is the receiver status flag. When this read only flag is "0", it indicates that the receiver is between the initial detection of the start bit and the completion of the stop bit. When the flag is "1", it indicates that the receiver is idle. Between the completion of the stop bit and the detection of the next start bit, the URIDLE bit is "1" indicating that the UART receiver is idle and the URX/UTX pin stays in logic high condition.

Bit 2   **URXIF**: Receive UTXR_RXR data register status

         0: UTXR_RXR data register is empty

         1: UTXR_RXR data register has available data

The URXIF flag is the receive data register status flag. When this read only flag is "0", it indicates that the UTXR_RXR read data register is empty. When the flag is "1", it indicates that the UTXR_RXR read data register contains new data. When the contents of the shift register are transferred to the UTXR_RXR register, an interrupt is generated if URIE=1 in the UUCR2 register. If one or more errors are detected in the received word, the appropriate receive-related flags UNF, UFERR, and/or UPERR are set within the same clock cycle. The URXIF flag will eventually be cleared when the UUSR register is read with URXIF set, followed by a read from the UTXR_RXR register, and if the UTXR_RXR register has no more new data available.

Bit 1   **UTIDLE**: Transmission idle

         0: Data transmission is in progress (Data being transmitted)

         1: No data transmission is in progress (Transmitter is idle)

The UTIDLE flag is known as the transmission complete flag. When this read only flag is "0", it indicates that a transmission is in progress. This flag will be set high when the UTXIF flag is "1" and when there is no transmit data or break character being transmitted. When UTIDLE is equal to "1", the UTX pin becomes idle with the pin state in logic high condition. The UTIDLE flag is cleared by reading the UUSR register with UTIDLE set and then writing to the UTXR_RXR register. The flag is not generated when a data character or a break is queued and ready to be sent.

Bit 0   **UTXIF**: Transmit UTXR_RXR data register status

  0: Character is not transferred to the transmit shift register

  1: Character has transferred to the transmit shift register (UTXR_RXR data register is empty)

  The UTXIF flag is the transmit data register empty flag. When this read only flag is "0", it indicates that the character is not transferred to the transmitter shift register. When the flag is "1", it indicates that the transmitter shift register has received a character from the UTXR_RXR data register. The UTXIF flag is cleared by reading the UART status register (UUSR) with UTXIF set and then writing to the UTXR_RXR data register. Note that when the UTXEN bit is set, the UTXIF flag bit will also be set since the transmit data register is not yet full.

• UUCR1 Register

The UUCR1 register together with the UUCR2 and UUCR3 registers are the three UART control registers that are used to set the various options for the UART function, such as overall on/off control, parity control, data transfer bit length, single wire mode communication etc. Further explanation on each of the bits is given below:

Bit	7	6	5	4	3	2	1	0
Name	UREN	UBNO	UPREN	UPRT	USTOPS	UTXBRK	URX8	UTX8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	W
POR	0	0	0	0	0	0	x	0

"x": unknown

Bit 7   **UREN**: UART function enable control

  0: Disable UART. UTX and URX/UTX pins are in a floating state

  1: Enable UART. UTX and URX/UTX pins function as UART pins

  The UREN bit is the UART enable bit. When this bit is equal to "0", the UART will be disabled and the URX/UTX pin as well as the UTX pin will be set in a floating state. When the bit is equal to "1", the UART will be enabled if the UMD bit is set and the UTX and URX/UTX pins will function as defined by the USWM mode selection bit together with the UTXEN and URXEN enable control bits.

  When the UART is disabled, it will empty the buffer so any character remaining in the buffer will be discarded. In addition, the value of the baud rate counter will be reset. If the UART is disabled, all error and status flags will be reset. Also the UTXEN, URXEN, UTXBRK, URXIF, UOERR, UFERR, UPERR and UNF bits will be cleared, while the UTIDLE, UTXIF and URIDLE bits will be set. Other control bits in UUCR1, UUCR2, UUCR3 and UBRG registers will remain unaffected. If the UART is active and the UREN bit is cleared, all pending transmissions and receptions will be terminated and the module will be reset as defined above. When the UART is re-enabled, it will restart in the same configuration.

Bit 6   **UBNO**: Number of data transfer bits selection

  0: 8-bit data transfer

  1: 9-bit data transfer

  This bit is used to select the data length format, which can have a choice of either 8-bit or 9-bit format. When this bit is equal to "1", a 9-bit data length format will be selected. If the bit is equal to "0", then an 8-bit data length format will be selected. If 9-bit data length format is selected, then bits URX8 and UTX8 will be used to store the 9th bit of the received and transmitted data respectively.

  Note that the 9th bit of data if UBNO=1, or the 8th bit of data if UBNO=0, which is used as the parity bit, does not transfer to URX8 or UTXRX7 respectively when the parity function is enabled.

Bit 5   **UPREN**: Parity function enable control

  0: Parity function is disabled

  1: Parity function is enabled

This is the parity enable bit. When this bit is equal to "1", the parity function will be enabled. If the bit is equal to "0", then the parity function will be disabled.

Bit 4   **UPRT**: Parity type selection bit

      0: Even parity for parity generator
      1: Odd parity for parity generator

This bit is the parity type selection bit. When this bit is equal to "1", odd parity type will be selected. If the bit is equal to "0", then even parity type will be selected.

Bit 3   **USTOPS**: Number of Stop bits selection for transmitter

      0: One stop bit format is used
      1: Two stop bits format is used

This bit determines if one or two stop bits are to be used for transmitter. When this bit is equal to "1", two stop bits are used. If this bit is equal to "0", then only one stop bit is used.

Bit 2   **UTXBRK**: Transmit break character

      0: No break character is transmitted
      1: Break characters transmit

The UTXBRK bit is the Transmit Break Character bit. When this bit is "0", there are no break characters and the UTX pin operates normally. When the bit is "1", there are transmit break characters and the transmitter will send logic zeros. When this bit is equal to "1", after the buffered data has been transmitted, the transmitter output is held low for a minimum of a 13-bit length and until the UTXBRK bit is reset.

Bit 1   **URX8**: Receive data bit 8 for 9-bit data transfer format (read only)

This bit is only used if 9-bit data transfers are used, in which case this bit location will store the 9th bit of the received data known as URX8. The UBNO bit is used to determine whether data transfers are in 8-bit or 9-bit format.

Bit 0   **UTX8**: Transmit data bit 8 for 9-bit data transfer format (write only)

This bit is only used if 9-bit data transfers are used, in which case this bit location will store the 9th bit of the transmitted data known as UTX8. The UBNO bit is used to determine whether data transfers are in 8-bit or 9-bit format.

• **UUCR2 Register**

The UUCR2 register is the second of the UART control registers and serves several purposes. One of its main functions is to control the basic enable/disable operation of the UART Transmitter and Receiver as well as enabling the various USIM UART mode interrupt sources. The register also serves to control the baud rate speed, receiver wake-up enable and the address detect enable. Further explanation on each of the bits is given below:

Bit	7	6	5	4	3	2	1	0
Name	UTXEN	URXEN	UBRGH	UADDEN	UWAKE	URIE	UTIIE	UTEIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **UTXEN**: UART Transmitter enabled control

      0: UART transmitter is disabled
      1: UART transmitter is enabled

The bit named UTXEN is the Transmitter Enable Bit. When this bit is equal to "0", the transmitter will be disabled with any pending data transmissions being aborted. In addition the buffers will be reset. In this situation the UTX pin will be set in a floating state.

If the UTXEN bit is equal to "1" and the UMD and UREN bit are also equal to "1", the transmitter will be enabled and the UTX pin will be controlled by the UART. Clearing the UTXEN bit during a transmission will cause the data transmission to be aborted and will reset the transmitter. If this situation occurs, the UTX pin will be set in a floating state.

Bit 6   **URXEN**: UART Receiver enabled control

0: UART receiver is disabled

1: UART receiver is enabled

The bit named URXEN is the Receiver Enable Bit. When this bit is equal to "0", the receiver will be disabled with any pending data receptions being aborted. In addition the receive buffers will be reset. In this situation the URX/UTX pin will be set in a floating state. If the URXEN bit is equal to "1" and the UMD and UREN bit are also equal to "1", the receiver will be enabled and the URX/UTX pin will be controlled by the UART. Clearing the URXEN bit during a reception will cause the data reception to be aborted and will reset the receiver. If this situation occurs, the URX/UTX pin will be set in a floating state.

Bit 5   **UBRGH**: Baud Rate speed selection

0: Low speed baud rate

1: High speed baud rate

The bit named UBRGH selects the high or low speed mode of the Baud Rate Generator. This bit, together with the value placed in the baud rate register UBRG, controls the Baud Rate of the UART. If this bit is equal to "1", the high speed mode is selected. If the bit is equal to "0", the low speed mode is selected.

Bit 4   **UADDEN**: Address detect function enable control

0: Address detect function is disabled

1: Address detect function is enabled

The bit named UADDEN is the address detect function enable control bit. When this bit is equal to "1", the address detect function is enabled. When it occurs, if the 8th bit, which corresponds to UTXRX7 if UBNO=0 or the 9th bit, which corresponds to URX8 if UBNO=1, has a value of "1", then the received word will be identified as an address, rather than data. If the corresponding interrupt is enabled, an interrupt request will be generated each time the received word has the address bit set, which is the 8th or 9th bit depending on the value of UBNO. If the address bit known as the 8th or 9th bit of the received word is "0" with the address detect function being enabled, an interrupt will not be generated and the received data will be discarded.

Bit 3   **UWAKE**: URX/UTX pin wake-up UART function enable control

0: URX/UTX pin wake-up UART function is disabled

1: URX/UTX pin wake-up UART function is enabled

This bit is used to control the wake-up UART function when a falling edge on the URX/UTX pin occurs. Note that this bit is only available when the UART clock (f_H) is switched off. There will be no URX/UTX pin wake-up UART function if the UART clock (f_H) exists. If the UWAKE bit is set to 1 as the UART clock (f_H) is switched off, a UART wake-up request will be initiated when a falling edge on the URX/UTX pin occurs. When this request happens and the corresponding interrupt is enabled, an URX/UTX pin wake-up UART interrupt will be generated to inform the MCU to wake up the UART function by switching on the UART clock (f_H) via the application program. Otherwise, the UART function cannot resume even if there is a falling edge on the URX/UTX pin when the UWAKE bit is cleared to 0.

Bit 2   **URIE**: Receiver interrupt enable control

0: Receiver related interrupt is disabled

1: Receiver related interrupt is enabled

This bit enables or disables the receiver interrupt. If this bit is equal to "1" and when the receiver overrun flag UOERR or receive data available flag URXIF is set, the USIM interrupt request flag USIMF will be set. If this bit is equal to "0", the USIM interrupt request flag USIMF will not be influenced by the condition of the UOERR or URXIF flags.

Bit 1   **UTIIE**: Transmitter Idle interrupt enable control

0: Transmitter idle interrupt is disabled

1: Transmitter idle interrupt is enabled

This bit enables or disables the transmitter idle interrupt. If this bit is equal to "1" and when the transmitter idle flag UTIDLE is set, due to a transmitter idle condition, the USIM interrupt request flag USIMF will be set. If this bit is equal to "0", the USIM interrupt request flag USIMF will not be influenced by the condition of the UTIDLE flag.

Bit 0   **UTEIE**: Transmitter Empty interrupt enable control
0: Transmitter empty interrupt is disabled
1: Transmitter empty interrupt is enabled

This bit enables or disables the transmitter empty interrupt. If this bit is equal to "1" and when the transmitter empty flag UTXIF is set, due to a transmitter empty condition, the USIM interrupt request flag USIMF will be set. If this bit is equal to "0", the USIM interrupt request flag USIMF will not be influenced by the condition of the UTXIF flag.

• UUCR3 Register

The UUCR3 register is used to enable the UART Single Wire Mode communication. As the name suggests in the single wire mode the UART communication can be implemented in one single line, URX/UTX, together with the control of the URXEN and UTXEN bits in the UUCR2 register.

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	USWM
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	0

Bit 7~1   Unimplemented, read as "0"

Bit 0   **USWM**: Single wire mode enable control
0: Disable, the URX/UTX pin is used as UART receiver function only
1: Enable, the URX/UTX pin can be used as UART receiver or transmitter function controlled by the URXEN and UTXEN bits

Note that when the Single Wire Mode is enabled, if both the URXEN and UTXEN bits are high, the URX/UTX pin will just be used as UART receiver input.

• UTXR_RXR Register

The UTXR_RXR register is the data register which is used to store the data to be transmitted on the UTX pin or being received from the URX/UTX pin.

Bit	7	6	5	4	3	2	1	0
Name	UTXRX7	UTXRX6	UTXRX5	UTXRX4	UTXRX3	UTXRX2	UTXRX1	UTXRX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": unknown

Bit 7~0   **UTXRX7~UTXRX0**: UART Transmit/Receive Data bit 7 ~ bit 0

• UBRG Register

Bit	7	6	5	4	3	2	1	0
Name	UBRG7	UBRG6	UBRG5	UBRG4	UBRG3	UBRG2	UBRG1	UBRG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	x	x	x	x	x	x	x	x

"x": unknown

Bit 7~0   **UBRG7~UBRG0**: Baud Rate values
By programming the UBRGH bit in UUCR2 Register which allows selection of the related formula described above and programming the required value in the UBRG register, the required baud rate can be setup.
Note: Baud rate=f_H/[64×(N+1)] if UBRGH=0.
Baud rate=f_H/[16×(N+1)] if UBRGH=1.

Baud Rate Generator

To setup the speed of the serial data communication, the UART function contains its own dedicated baud rate generator. The baud rate is controlled by its own internal free running 8-bit timer, the period of which is determined by two factors. The first of these is the value placed in the baud rate register UBRG and the second is the value of the UBRGH bit with the control register UUCR2. The UBRGH bit decides if the baud rate generator is to be used in a high speed mode or low speed mode, which in turn determines the formula that is used to calculate the baud rate. The value N in the UBRG register which is used in the following baud rate calculation formula determines the division factor. Note that N is the decimal value placed in the UBRG register and has a range of between 0 and 255.

UUCR2 UBRGH Bit	0	1
Baud Rate (BR)	$f_H/[64 (N+1)]$	$f_H/[16 (N+1)]$

By programming the UBRGH bit which allows selection of the related formula and programming the required value in the UBRG register, the required baud rate can be setup. Note that because the actual baud rate is determined using a discrete value, N, placed in the UBRG register, there will be an error associated between the actual and requested value. The following example shows how the UBRG register value N and the error value can be calculated.

Calculating the Baud Rate and Error Values

For a clock frequency of 4MHz, and with UBRGH cleared to zero determine the UBRG register value N, the actual baud rate and the error value for a desired baud rate of 4800.

From the above table the desired baud rate $BR=f_H/[64 (N+1)]$

Re-arranging this equation gives $N=[f_H/(BR \times 64)] - 1$

Giving a value for $N=[4000000/(4800 \times 64)] - 1 = 12.0208$

To obtain the closest value, a decimal value of 12 should be placed into the UBRG register. This gives an actual or calculated baud rate value of $BR=4000000/[64 \times (12+1)]=4808$

Therefore the error is equal to $(4808 - 4800)/4800=0.16\%$

UART Setup and Control

For data transfer, the UART function utilizes a non-return-to-zero, more commonly known as NRZ, format. This is composed of one start bit, eight or nine data bits, and one or two stop bits. Parity is supported by the UART hardware, and can be setup to be even, odd or no parity. For the most common data format, 8 data bits along with no parity and one stop bit, denoted as 8, N, 1, is used as the default setting, which is the setting at power-on. The number of data bits and stop bits, along with the parity, are setup by programming the corresponding UBNO, UPRT, UPREN, and USTOPS bits in the UUCR1 register. The baud rate used to transmit and receive data is setup using the internal 8-bit baud rate generator, while the data is transmitted and received LSB first. Although the UART transmitter and receiver are functionally independent, they both use the same data format and baud rate. In all cases stop bits will be used for data transmission.

Enabling/Disabling the UART Interface

The basic on/off function of the internal UART function is controlled using the UREN bit in the UUCR1 register. When the UART mode is selected by setting the UMD bit in the SIMC0 register to "1", if the UREN, UTXEN and URXEN bits are set, then these two UART pins will act as normal UTX output pin and URX/UTX input pin respectively. If no data is being transmitted on the UTX pin, then it will default to a logic high value.

Clearing the UREN bit will disable the UTX and URX/UTX pins and allow these two pins to be used as normal I/O or other pin-shared functional pins by configuring the corresponding pin-shared control bits. When the UART function is disabled the buffer will be reset to an empty condition, at the same time discarding any remaining residual data. Disabling the UART will also reset the error and status flags with bits UTXEN, URXEN, UTXBRK, URXIF, UOERR, UFERR, UPERR and UNF being cleared while bits UTIDLE, UTXIF and URIDLE will be set. The remaining control bits in the UUCR1, UUCR2, UUCR3 and UBRG registers will remain unaffected. If the UREN bit in the UUCR1 register is cleared while the UART is active, then all pending transmissions and receptions will be immediately suspended and the UART will be reset to a condition as defined above. If the UART is then subsequently re-enabled, it will restart again in the same configuration.

Data, Parity and Stop Bit Selection

The format of the data to be transferred is composed of various factors such as data bit length, parity on/off, parity type, address bits and the number of stop bits. These factors are determined by the setup of various bits within the UUCR1 register. The UBNO bit controls the number of data bits which can be set to either 8 or 9, the UPRT bit controls the choice of odd or even parity, the UPREN bit controls the parity on/off function and the USTOPS bit decides whether one or two stop bits are to be used. The following table shows various formats for data transmission. The address bit, which is the MSB of the data byte, identifies the frame as an address character or data if the address detect function is enabled. The number of stop bits, which can be either one or two, is independent of the data length and is only used for the transmitter. There is only one stop bit for the receiver.

Start Bit	Data Bits	Address Bit	Parity Bit	Stop Bit
Example of 8-bit Data Formats				
1	8	0	0	1
1	7	0	1	1
1	7	1	0	1
Example of 9-bit Data Formats				
1	9	0	0	1
1	8	0	1	1
1	8	1	0	1

Transmitter Receiver Data Format

The following diagram shows the transmit and receive waveforms for both 8-bit and 9-bit data formats.

8-bit Data Format

9-bit Data Format
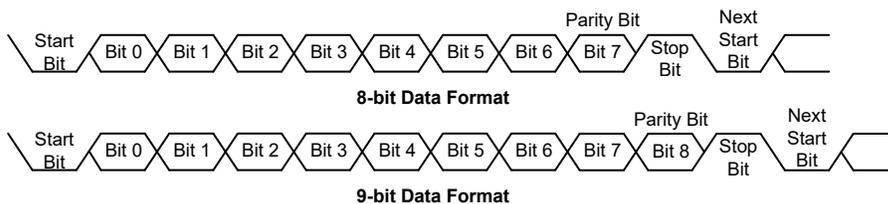
UART Transmitter

Data word lengths of either 8 or 9 bits can be selected by programming the UBNO bit in the UUCR1 register. When UBNO bit is set, the word length will be set to 9 bits. In this case the 9th bit, which is the MSB, needs to be stored in the UTX8 bit in the UUCR1 register. At the transmitter core lies the Transmitter Shift Register, more commonly known as the TSR, whose data is obtained from the transmit data register, which is known as the UTXR_RXR register. The data to be transmitted is loaded into this UTXR_RXR register by the application program. The TSR register is not written to with new data until the stop bit from the previous transmission has been sent out. As soon as this

stop bit has been transmitted, the TSR can then be loaded with new data from the UTXR_RXR register, if it is available. It should be noted that the TSR register, unlike many other registers, is not directly mapped into the Data Memory area and as such is not available to the application program for direct read/write operations. An actual transmission of data will normally be enabled when the UTXEN bit is set, but the data will not be transmitted until the UTXR_RXR register has been loaded with data and the baud rate generator has defined a shift clock source. However, the transmission can also be initiated by first loading data into the UTXR_RXR register, after which the UTXEN bit can be set. When a transmission of data begins, the TSR is normally empty, in which case a transfer to the UTXR_RXR register will result in an immediate transfer to the TSR. If during a transmission the UTXEN bit is cleared, the transmission will immediately cease and the transmitter will be reset. The UTX output pin can then be configured as the I/O or other pin-shared function by configuring the corresponding pin-shared control bits.

Transmitting Data

When the UART is transmitting data, the data is shifted on the UTX pin from the shift register, with the least significant bit first. In the transmit mode, the UTXR_RXR register forms a buffer between the internal bus and the transmitter shift register. It should be noted that if 9-bit data format has been selected, then the MSB will be taken from the UTX8 bit in the UUCR1 register. The steps to initiate a data transfer can be summarized as follows:

- Make the correct selection of the UBNO, UPRT, UPREN and USTOPS bits to define the required word length, parity type and number of stop bits.
- Setup the UBRG register to select the desired baud rate.
- Set the UTXEN bit to ensure that the UTX pin is used as a UART transmitter pin.
- Access the UUSR register and write the data that is to be transmitted into the UTXR_RXR register. Note that this step will clear the UTXIF bit.

This sequence of events can now be repeated to send additional data.

It should be noted that when UTXIF=0, data will be inhibited from being written to the UTXR_RXR register. Clearing the UTXIF flag is always achieved using the following software sequence:

    1. A UUSR register access

    2. A UTXR_RXR register write execution

The read-only UTXIF flag is set by the UART hardware and if set indicates that the UTXR_RXR register is empty and that other data can now be written into the UTXR_RXR register without overwriting the previous data. If the UTEIE bit is set then the UTXIF flag will generate an interrupt.

During a data transmission, a write instruction to the UTXR_RXR register will place the data into the UTXR_RXR register, which will be copied to the shift register at the end of the present transmission. When there is no data transmission in progress, a write instruction to the UTXR_RXR register will place the data directly into the shift register, resulting in the commencement of data transmission, and the UTXIF bit being immediately set. When a frame transmission is complete, which happens after stop bits are sent or after the break frame, the UTIDLE bit will be set. To clear the UTIDLE bit the following software sequence is used:

    1. A UUSR register access

    2. A UTXR_RXR register write execution

Note that both the UTXIF and UTIDLE bits are cleared by the same software sequence.

Transmitting Break

If the UTXBRK bit is set then and the state keeps for a time greater than $[(BRG+1) \times t_H]$ while UTIDLE=1, then break characters will be sent on the next transmission. Break character transmission consists of a start bit, followed by 13×N '0' bits and stop bits, where N=1, 2, etc. If a break character is to be transmitted then the UTXBRK bit must be first set by the application program, and then cleared to generate the stop bits. Transmitting a break character will not generate a transmit interrupt. Note that a break condition length is at least 13 bits long. If the UTXBRK bit is continually kept at a logic high level then the transmitter circuitry will transmit continuous break characters. After the application program has cleared the UTXBRK bit, the transmitter will finish transmitting the last break character and subsequently send out one or two stop bits. The automatic logic highs at the end of the last break character will ensure that the start bit of the next frame is recognized.

UART Receiver

The UART is capable of receiving word lengths of either 8 or 9 bits. If the UBNO bit is set, the word length will be set to 9 bits with the MSB being stored in the URX8 bit of the UUCR1 register. At the receiver core lies the Receive Serial Shift Register, commonly known as the RSR. The data which is received on the URX/UTX external input pin is sent to the data recovery block. The data recovery block operating speed is 16 times that of the baud rate, while the main receive serial shifter operates at the baud rate. After the URX/UTX pin is sampled for the stop bit, the received data in RSR is transferred to the receive data register, if the register is empty. The data which is received on the external URX/UTX input pin is sampled three times by a majority detect circuit to determine the logic level that has been placed onto the URX/UTX pin. It should be noted that the RSR register, unlike many other registers, is not directly mapped into the Data Memory area and as such is not available to the application program for direct read/write operations.

Receiving Data

When the UART receiver is receiving data, the data is serially shifted in on the external URX/UTX input pin, LSB first. In the read mode, the UTXR_RXR register forms a buffer between the internal bus and the receiver shift register. The UTXR_RXR register is a two-byte deep FIFO data buffer, where two bytes can be held in the FIFO while a third byte can continue to be received. Note that the application program must ensure that the data is read from UTXR_RXR before the third byte has been completely shifted in, otherwise this third byte will be discarded and an overrun error UOERR will be subsequently indicated. The steps to initiate a data transfer can be summarized as follows:

- Make the correct selection of UBNO, UPRT and UPREN bits to define the word length, parity type.
- Setup the UBRG register to select the desired baud rate.
- Set the URXEN bit to ensure that the URX/UTX pin is used as a UART receiver pin.

At this point the receiver will be enabled which will begin to look for a start bit.

When a character is received the following sequence of events will occur:

- The URXIF bit in the UUSR register will be set when the UTXR_RXR register has data available. There will be at most one more character available before an overrun error occurs.
- When the contents of the shift register have been transferred to the UTXR_RXR register, then if the URIE bit is set, an interrupt will be generated.
- If during reception, a frame error, noise error, parity error, or an overrun error has been detected, then the error flags can be set.

The URXIF bit can be cleared using the following software sequence:

1. A UUSR register access
2. A UTXR_RXR register read execution

Receiving Break

Any break character received by the UART will be managed as a framing error. The receiver will count and expect a certain number of bit times as specified by the values programmed into the UBNO bit plus one stop bit. If the break is much longer than 13 bit times, the reception will be considered as complete after the number of bit times specified by UBNO plus one stop bit. The URXIF bit is set, UFERR is set, zeros are loaded into the receive data register, interrupts are generated if appropriate and the URIDLE bit is set. A break is regarded as a character that contains only zeros with the UFERR flag set. If a long break signal has been detected, the receiver will regard it as a data frame including a start bit, data bits and the invalid stop bit and the UFERR flag will be set. The receiver must wait for a valid stop bit before looking for the next start bit. The receiver will not make the assumption that the break condition on the line is the next start bit. The break character will be loaded into the buffer and no further data will be received until stop bits are received. It should be noted that the URIDLE read only flag will go high when the stop bits have not yet been received. The reception of a break character on the UART registers will result in the following:

- The framing error flag, UFERR, will be set.

- The receive data register, UTXR_RXR, will be cleared.

- The UOERR, UNF, UPERR, URIDLE or URXIF flags will possibly be set.

Idle Status

When the receiver is reading data, which means it will be in between the detection of a start bit and the reading of a stop bit, the receiver status flag in the UUSR register, otherwise known as the URIDLE flag, will have a zero value. In between the reception of a stop bit and the detection of the next start bit, the URIDLE flag will have a high value, which indicates the receiver is in an idle condition.

Receiver Interrupt

The read only receive interrupt flag URXIF in the UUSR register is set by an edge generated by the receiver. An interrupt is generated if URIE=1, when a word is transferred from the Receive Shift Register, RSR, to the Receive Data Register, UTXR_RXR. An overrun error can also generate an interrupt if URIE=1.

Managing Receiver Errors

Several types of reception errors can occur within the UART module, the following section describes the various types and how they are managed by the UART.

Overrun Error – UOERR

The UTXR_RXR register is composed of a two-byte deep FIFO data buffer, where two bytes can be held in the FIFO register, while a third byte can continue to be received. Before this third byte has been entirely shifted in, the data should be read from the UTXR_RXR register. If this is not done, the overrun error flag UOERR will be consequently indicated.

In the event of an overrun error occurring, the following will happen:

- The UOERR flag in the UUSR register will be set.

- The UTXR_RXR contents will not be lost.

- The shift register will be overwritten.

- An interrupt will be generated if the URIE bit is set.

The UOERR flag can be cleared by an access to the UUSR register followed by a read to the UTXR_RXR register.

Noise Error – UNF

Over-sampling is used for data recovery to identify valid incoming data and noise. If noise is detected within a frame the following will occur:

- The read only noise flag, UNF, in the UUSR register will be set on the rising edge of the URXIF bit.

- Data will be transferred from the Shift register to the UTXR_RXR register.

- No interrupt will be generated. However this bit rises at the same time as the URXIF bit which itself generates an interrupt.

Note that the UNF flag is reset by a UUSR register read operation followed by a UTXR_RXR register read operation.

Framing Error – UFERR

The read only framing error flag, UFERR, in the UUSR register, is set if a zero is detected instead of stop bits. If two stop bits are selected, both stop bits must be high; otherwise the UFERR flag will be set. The UFERR flag and the received data will be recorded in the UUSR and UTXR_RXR registers respectively, and the flag is cleared in any reset.

Parity Error – UPERR

The read only parity error flag, UPERR, in the UUSR register, is set if the parity of the received word is incorrect. This error flag is only applicable if the parity is enabled, UPREN=1, and if the parity type, odd or even is selected. The read only UPERR flag and the received data will be recorded in the UUSR and UTXR_RXR registers respectively. It is cleared on any reset, it should be noted that the flags, UFERR and UPERR, in the UUSR register should first be read by the application program before reading the data word.

UART Interrupt Structure

Several individual UART conditions can trigger an USIM interrupt. When these conditions exist, a low pulse will be generated to get the attention of the microcontroller. These conditions are a transmitter data register empty, transmitter idle, receiver data available, receiver overrun, address detect and an URX/UTX pin wake-up. When any of these conditions are created, if the global interrupt enable bit and the USIM interrupt control bit are enabled and the stack is not full, the program will jump to its corresponding interrupt vector where it can be serviced before returning to the main program. Four of these conditions have the corresponding UUSR register flags which will generate an USIM interrupt if its associated interrupt enable control bit in the UUCR2 register is set. The two transmitter interrupt conditions have their own corresponding enable control bits, while the two receiver interrupt conditions have a shared enable control bit. These enable bits can be used to mask out individual USIM UART mode interrupt sources.

The address detect condition, which is also an USIM UART mode interrupt source, does not have an associated flag, but will generate an USIM interrupt when an address detect condition occurs if its function is enabled by setting the UADDEN bit in the UUCR2 register. An URX/UTX pin wake-up, which is also an USIM UART mode interrupt source, does not have an associated flag, but will generate an USIM interrupt if the UART clock (f_H) source is switched off and the UWAKE and URIE bits in the UUCR2 register are set when a falling edge on the URX/UTX pin occurs. Note that in the event of an URX/UTX wake-up interrupt occurring, there will be a certain period of delay, commonly known as the System Start-up Time, for the oscillator to restart and stabilize before the system resumes normal operation.

Note that the UUSR register flags are read only and cannot be cleared or set by the application program, neither will they be cleared when the program jumps to the corresponding interrupt servicing routine, as is the case for some of the other interrupts. The flags will be cleared automatically when certain actions are taken by the UART, the details of which are given in the UART register section. The overall UART interrupt can be disabled or enabled by the USIM interrupt enable control bit in the interrupt control register of the microcontroller to decide whether the interrupt requested by the UART module is masked out or allowed.
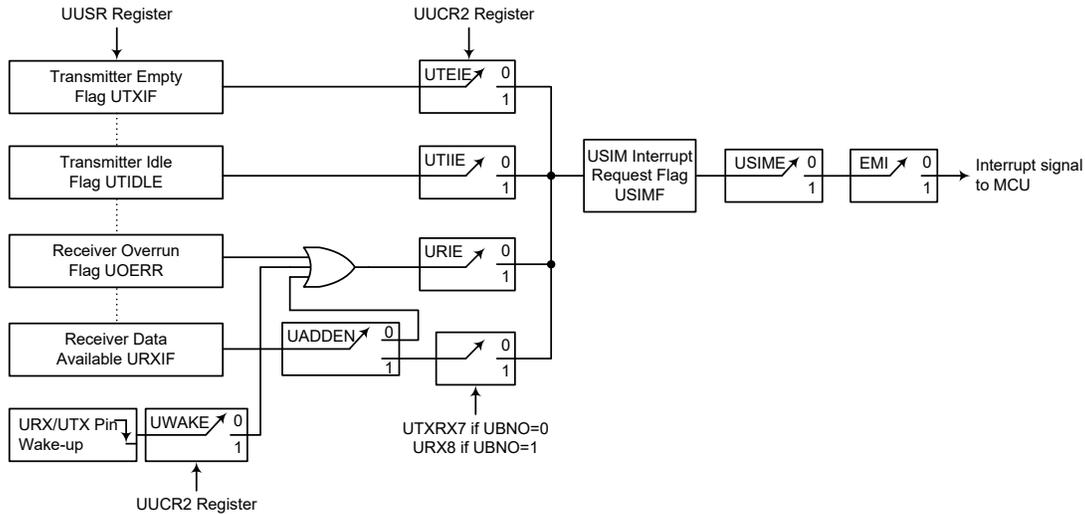
UART Interrupt Structure

Address Detect Mode

Setting the Address Detect Mode bit, UADDEN, in the UUCR2 register, enables this special mode. If this bit is enabled then an additional qualifier will be placed on the generation of a Receiver Data Available interrupt, which is requested by the URXIF flag. If the UADDEN bit is enabled, then when data is available, an interrupt will only be generated if the highest received bit has a high value. Note that the USIME and EMI interrupt enable bits must also be enabled for correct interrupt generation. This highest address bit is the 9th bit if UBNO=1 or the 8th bit if UBNO=0. If this bit is high, then the received word will be defined as an address rather than data. A Data Available interrupt will be generated every time the last bit of the received word is set. If the UADDEN bit is not enabled, then a Receiver Data Available interrupt will be generated each time the URXIF flag is set, irrespective of the data last bit status. The address detect mode and parity enable are mutually exclusive functions. Therefore if the address detect mode is enabled, then to ensure correct operation, the parity function should be disabled by resetting the parity enable bit UPREN to zero.

UADDEN	9th Bit if UBNO=1, 8th Bit if UBNO=0	USIM Interrupt Generated
0	0	√
	1	√
1	0	×
	1	√

UADDEN Bit Function

UART Power Down and Wake-up

When the UART clock (f_H) is off, the UART will cease to function, all clock sources to the module are shutdown. If the UART clock (f_H) is off while a transmission is still in progress, then the transmission will be paused until the UART clock source derived from the microcontroller is

activated. In a similar way, if the MCU enters the IDLE or SLEEP Mode while receiving data, then the reception of data will likewise be paused. When the MCU enters the IDLE or SLEEP Mode, note that the UUSR, UUCR1, UUCR2, UUCR3, UTXR_RXR, as well as the UBRG register will not be affected. It is recommended to make sure first that the UART data transmission or reception has been finished before the microcontroller enters the IDLE or SLEEP mode.

The UART function contains a receiver URX/UTX pin wake-up function, which is enabled or disabled by the UWAKE bit in the UUCR2 register. If this bit, along with the UART mode selection bit, UMD, the UART enable bit, UREN, the receiver enable bit, URXEN and the receiver interrupt bit, URIE, are all set when the UART clock (f_H) is off, then a falling edge on the URX/UTX pin will trigger an URX/UTX pin wake-up UART interrupt. Note that as it takes certain system clock cycles after a wake-up, before normal microcontroller operation resumes, any data received during this time on the URX/UTX pin will be ignored.

For a UART wake-up interrupt to occur, in addition to the bits for the wake-up being set, the global interrupt enable bit, EMI, and the USIM interrupt enable bit, USIME, must be set. If the EMI and USIME bits are not set then only a wake up event will occur and no interrupt will be generated. Note also that as it takes certain system clock cycles after a wake-up before normal microcontroller resumes, the USIM interrupt will not be generated until after this time has elapsed.

Buzzer Driver

Buzzer Driver Block Diagram
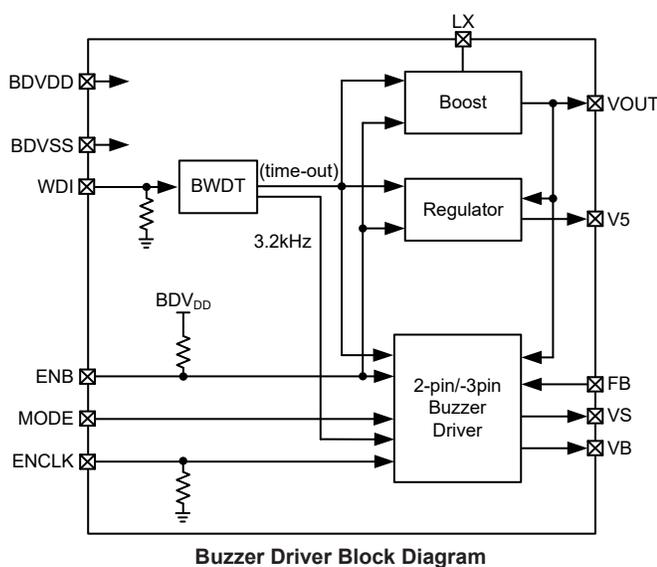
Functional Description

In order to reduce input voltage drop during startup, when ENB>V_{IH}, the boost convert of buzzer driver has a 250mA peak current limit monitoring for the internal switch, when the soft start current limit threshold is detected, the internal switch is turned off until next cycle, and the boost converter current is unlimited after 25ms.

The buzzer driver provides a Buzzer Watchdog Timer, BWDT, for MCU failure alarm function. It is required to toggle the WDI by inputting a pulse to WDI within the BWDT period, t_{WDI}, to reset the BWDT counter. Otherwise, when the BWDT times out, the internal TO flag will be set high to trigger the buzzer. The TO flag will not cleared to 0 until the MCU toggle the WDI again.

Truth Table

The truth table for the input signal is as follows: When BWDT does not time out, the TO flag is set to 0; when BWDT times out, the TO flag is set to 1. The TO flag has the highest priority.

TO flag	ENB	MODE	ENCLK	Function Description
0	0	0	0	Boost on, Regulator on, 3-pin buzzer mode
0	0	0	1	Boost on, Regulator on, Buzzer off
0	0	1	x	Boost on, Regulator on, 2-pin buzzer mode Buzzer signal provided by ENCLK
0	1	x	x	Boost off, Regulator off, Buzzer off
1	x	0	x	Boost on, Regulator on, 3-pin buzzer mode
1	x	1	x	Boost on, Regulator on, 2-pin buzzer mode Buzzer signal provided by BWDT

Timing Chart

WDI Timing
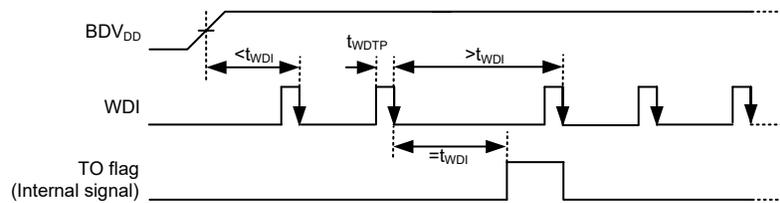
Timing
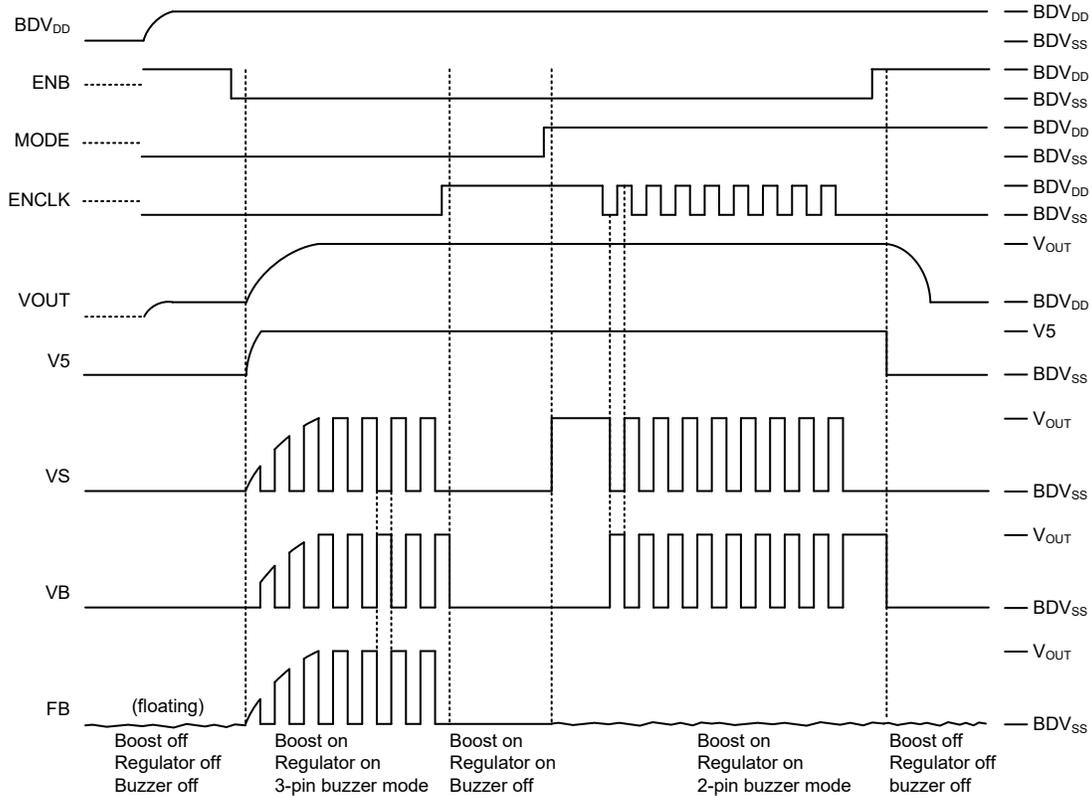
Low Voltage Detector – LVD

The device has a Low Voltage Detector function, also known as LVD. This enables the device to monitor the power supply voltage, V_{DD}, and provide a warning signal should it fall below a certain level. This function may be especially useful in battery applications where the supply voltage will gradually reduce as the battery ages, as it allows an early warning battery low signal to be generated. The Low Voltage Detector also has the capability of generating an interrupt signal.

LVD Register

The Low Voltage Detector function is controlled using a single register with the name LVDC. Three bits in this register, VLVD2~VLVD0, are used to select one of eight fixed voltages below which a low voltage condition will be determined. A low voltage condition is indicated when the LVDO bit is set. If the LVDO bit is low, this indicates that the V_{DD} voltage is above the preset low voltage value. The LVDEN bit is used to control the overall on/off function of the low voltage detector. Setting the bit high will enable the low voltage detector. Clearing the bit to zero will switch off the internal low voltage detector circuits. As the low voltage detector will consume a certain amount of power, it may be desirable to switch off the circuit when not in use, an important consideration in power sensitive battery powered applications.

• **LVDC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	LVDO	LVDEN	VBGEN	VLVD2	VLVD1	VLVD0
R/W	—	—	R	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6 Unimplemented, read as "0"

Bit 5 **LVDO**: LVD Output Flag
  0: No Low Voltage Detected
  1: Low Voltage Detected

Bit 4 **LVDEN**: Low Voltage Detector Control
  0: Disable
  1: Enable

Bit 3 **VBGEN**: Bandgap Buffer Control
  0: Disable
  1: Enable
  Note that the Bandgap circuit is enabled when the LVD or the LVR function is enabled or when the VBGEN bit is set high.

Bit 2~0 **VLVD2~VLVD0**: LVD Voltage Selection
  000: 2.0V
  001: 2.2V
  010: 2.4V
  011: 2.7V
  100: 3.0V
  101: 3.3V
  110: 3.6V
  111: 4.0V

LVD Operation

The Low Voltage Detector function operates by comparing the power supply voltage, V_{DD}, with a pre-specified voltage level stored in the LVDC register. This has a range of 2.0V~4.0V. When the power supply voltage, V_{DD}, falls below this pre-determined value, the LVDO bit will be set high indicating a low power supply voltage condition. When the device is in the SLEEP mode, the low

voltage detector will be disabled even if the LVDEN bit is high. After enabling the Low Voltage Detector, a time delay t_{LVDS} should be allowed for the circuitry to stabilise before reading the LVDO bit. Note also that as the V_{DD} voltage may rise and fall rather slowly, at the voltage near that of V_{LVD}, there may be multiple LVDO bit transitions.


LVD Operation
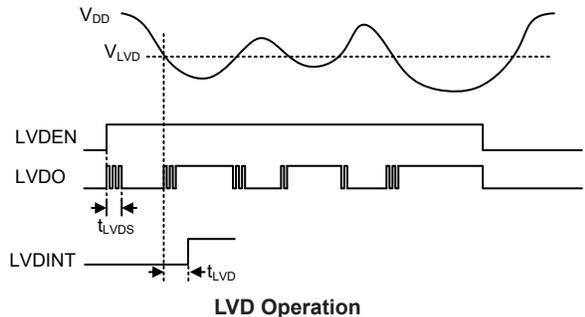
The Low Voltage Detector also has its own interrupt, providing an alternative means of low voltage detection, in addition to polling the LVDO bit. The interrupt will only be generated after a delay of t_{LVD} after the LVDO bit has been set high by a low voltage condition, i.e., V_{DD} falls below the preset LVD voltage. In this case, the LVF interrupt request flag will be set, causing an interrupt to be generated. This will cause the device to wake-up from the IDLE Mode, however if the Low Voltage Detector wake up function is not required then the LVF flag should be first set high before the device enters the IDLE Mode.

Cyclic Redundancy Check – CRC

The Cyclic Redundancy Check, CRC, calculation unit is an error detection technique test algorithm and uses to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as input and generates a 16-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described in the following section.

CRC Block Diagram
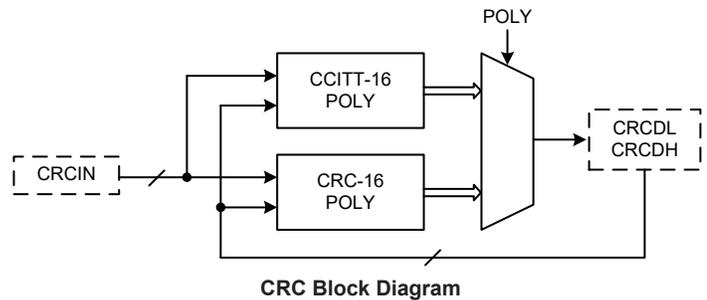
CRC Registers

The CRC generator contains an 8-bit CRC data input register, CRCIN, and a CRC checksum register pair, CRCDH and CRCDL. The CRCIN register is used to input new data and the CRCDH and CRCDL registers are used to hold the previous CRC calculation result. A CRC control register, CRCCR, is used to select which CRC generating polynomial is used.

Register	Bit							
Name	7	6	5	4	3	2	1	0
CRCIN	D7	D6	D5	D4	D3	D2	D1	D0
CRCDL	D7	D6	D5	D4	D3	D2	D1	D0
CRCDH	D15	D14	D13	D12	D11	D10	D9	D8
CRCCR	—	—	—	—	—	—	—	POLY

CRC Register List

• **CRCIN Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: CRC input data register

• **CRCDL Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D7~D0**: 16-bit CRC checksum low byte data register

• **CRCDH Register**

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0   **D15~D8**: 16-bit CRC checksum high byte data register

• **CRCCR Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	POLY
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	0

Bit 7~1   Unimplemented, read as "0"

Bit 0   **POLY**: 16-bit CRC generating polynomial selection
        0: CRC-CCITT: $X^{16}+X^{12}+X^5+1$
        1: CRC-16: $X^{16}+X^{15}+X^2+1$

CRC Operation

The CRC generator provides the 16-bit CRC result calculation based on the CRC16 and CCITT CRC16 polynomials. In this CRC generator, there are only these two polynomials available for the numeric values calculation. It can not support the 16-bit CRC calculations based on any other polynomials.

The following two expressions can be used for the CRC generating polynomial which is determined using the POLY bit in the CRC control register, CRCCR. The CRC calculation result is called as the CRC checksum, CRCSUM, and stored in the CRC checksum register pair, CRCDH and CRCDL.

• CRC-CCITT: $X^{16}+ X^{12}+X^5+1$

• CRC-16: $X^{16}+X^{15}+X^2+1$

CRC Computation

Each write operation to the CRCIN register creates a combination of the previous CRC value stored in the CRCDH and CRCDL registers and the new data input. The CRC unit calculates the CRC data register value is based on byte by byte. It will take one MCU instruction cycle to calculate the CRC checksum.

CRC Calculation Procedures:

1. Clear the checksum register pair, CRCDH and CRCDL.

2. Execute an "Exclusive OR" operation with the 8-bit input data byte and the 16-bit CRCSUM high byte. The result is called the temporary CRCSUM.

3. Shift the temporary CRCSUM value left by one bit and move a "0" into the LSB.

4. Check the shifted temporary CRCSUM value after procedure 3.

   If the MSB is 0, then this shifted temporary CRCSUM will be considered as a new temporary CRCSUM.

   Otherwise, execute an "Exclusive OR" operation with the shifted temporary CRCSUM in procedure 3 and a data "8005H". Then the operation result will be regarded as the new temporary CRCSUM.

   Note that the data to be perform an "Exclusive OR" operation is "8005H" for the CRC-16 polynomial while for the CRC-CCITT polynomial the data is "1021H".

5. Repeat the procedure 3 ~ procedure 4 until all bits of the input data byte are completely calculated.

6. Repeat the procedure 2 ~ procedure 5 until all of the input data bytes are completely calculated. Then, the latest calculated result is the final CRC checksum, CRCSUM.

CRC Calculation Examples:

• Write 1 byte input data into the CRCIN register and the corresponding CRC checksum are individually calculated as the following table shown.

CRC Data Input / CRC Polynomial	00H	01H	02H	03H	04H	05H	06H	07H
CRC-CCITT ($X^{16}+X^{12}+X^5+1$)	0000H	1021H	2042H	3063H	4084H	50A5H	60C6H	70E7H
CRC-16 ($X^{16}+X^{15}+X^2+1$)	0000H	8005H	800FH	000AH	801BH	001EH	0014H	8011H

Note: The initial value of the CRC checksum register pair, CRCDH and CRCDL, is zero before each CRC input data is written into the CRCIN register.

• Write 4 bytes input data into the CRCIN register sequentially and the CRC checksum are sequentially listed in the following table.

CRC Data Input / CRC Polynomial	CRCIN=78h→56h→34h→12h
CRC-CCITT ($X^{16}+X^{12}+X^5+1$)	(CRCDH, CRCDL)=FF9FH→BBC3H→A367H→D0FAH
CRC-16 ($X^{16}+X^{15}+X^2+1$)	(CRCDH, CRCDL)=0110h→91F1h→F2DEh→5C43h

Note: The initial value of the CRC checksum register pair, CRCDH and CRCDL, is zero before the sequential CRC data input operation.

Program Memory CRC Checksum Calculation Example:

1. Clear the checksum register pair, CRCDH and CRCDL.

2. Select the CRC-CCITT or CRC-16 polynomial as the generating polynomial using the POLY bit in the CRCCR register.

3. Execute the table read instruction to read the program memory data value.

4. Write the table data low byte into the CRCIN register and execute the CRC calculation with the current CRCSUM value. Then a new CRCSUM result will be obtained and stored in the CRC checksum register pair, CRCDH and CRCDL.

5. Write the table data high byte into the CRCIN register and execute the CRC calculation with the current CRCSUM value. Then a new CRCSUM result will be obtained and stored in the CRC checksum register pair, CRCDH and CRCDL.

6. Repeat the procedure 3 ~ procedure 5 to read the next program memory data value and execute the CRC calculation until all program memory data are read followed by the sequential CRC calculation. Then the value in the CRC checksum register pair is the final CRC calculation result.

Interrupts

Interrupts are an important part of any microcontroller system. When an external event or an internal function such as a Timer Module or an A/D converter requires microcontroller attention, their corresponding interrupt will enforce a temporary suspension of the main program allowing the microcontroller to direct attention to their respective needs. The device contains several external interrupt and internal interrupts functions. The external interrupts are generated by the action of the external INT0~INT1 pins, while the internal interrupts are generated by various internal functions including the TMs, Time Bases, LVD, EEPROM, USIM, Power Line Transceiver Comparators and the A/D converter.

Interrupt Registers

Overall interrupt control, which basically means the setting of request flags when certain microcontroller conditions occur and the setting of interrupt enable bits by the application program, is controlled by a series of registers, located in the Special Purpose Data Memory. The registers fall into two categories. The first is the INTC0~INTC3 registers which setup the primary interrupts, the second is the INTEG register which setup the external interrupt trigger edge type.

Each register contains a number of enable bits to enable or disable individual registers as well as interrupt flags to indicate the presence of an interrupt request. The naming convention of these follows a specific pattern. First is listed an abbreviated interrupt type, then the (optional) number of that interrupt followed by either an "E" for enable/disable bit or "F" for request flag.

Function	Enable Bit	Request Flag	Notes
Global	EMI	—	—
PLT Comparators	PLTCnE	PLTCnF	n=0~1
INTn Pin	INTnE	INTnF	n=0~1
USIM	USIME	USIMF	—
LVD	LVE	LVF	—
A/D Converter	ADE	ADF	—
EEPROM	DEE	DEF	—
STM	STMPE	STMPF	—
	STMAE	STMAF	

Function	Enable Bit	Request Flag	Notes
PTM	PTMPE	PTMPF	—
	PTMAE	PTMAF	
Time Bases	TBnE	TBnF	n=0~1

Interrupt Register Bit Naming Conventions

Register Name	Bit							
	7	6	5	4	3	2	1	0
INTEG	—	—	—	—	INT1S1	INT1S0	INT0S1	INT0S0
INTC0	—	INT1F	INT0F	PLTC0F	INT1E	INT0E	PLTC0E	EMI
INTC1	DEF	ADF	LVF	USIMF	DEE	ADE	LVE	USIME
INTC2	STMAF	STMPF	PTMAF	PTMPF	STMAE	STMPE	PTMAE	PTMPF
INTC3	—	PLTC1F	TB1F	TB0F	—	PLTC1E	TB1E	TB0E

Interrupt Register List

• **INTEG Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	INT1S1	INT1S0	INT0S1	INT0S0
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4   Unimplemented, read as "0"
Bit 3~2   **INT1S1~INT1S0**: Interrupt trigger edge selection for INT1 pin
                  00: Disable
                  01: Rising edge
                  10: Falling edge
                  11: Rising and falling edges
Bit 1~0   **INT0S1~INT0S0**: Interrupt trigger edge selection for INT0 pin
                  00: Disable
                  01: Rising edge
                  10: Falling edge
                  11: Rising and falling edges

• **INTC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	INT1F	INT0F	PLTC0F	INT1E	INT0E	PLTC0E	EMI
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	0	0	0	0	0	0	0

Bit 7   Unimplemented, read as "0"
Bit 6   **INT1F**: INT1 interrupt request flag
               0: No request
               1: Interrupt request
Bit 5   **INT0F**: INT0 interrupt request flag
               0: No request
               1: Interrupt request
Bit 4   **PLTC0F**: PLT Comparator 0 interrupt request flag
               0: No request
               1: Interrupt request
Bit 3   **INT1E**: INT1 interrupt control
               0: Disable
               1: Enable

Bit 2   **INT0E**: INT0 interrupt control
                 0: Disable
                 1: Enable

Bit 1   **PLTC0E**: PLT Comparator 0 interrupt control
                 0: Disable
                 1: Enable

Bit 0   **EMI**: Global interrupt control
                 0: Disable
                 1: Enable

• **INTC1 Register**

Bit	7	6	5	4	3	2	1	0
Name	DEF	ADF	LVF	USIMF	DEE	ADE	LVE	USIME
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **DEF**: EEPROM interrupt request flag
                 0: No request
                 1: Interrupt request

Bit 6   **ADF**: A/D converter interrupt request flag
                 0: No request
                 1: Interrupt request

Bit 5   **LVF**: LVD interrupt request flag
                 0: No request
                 1: Interrupt request

Bit 4   **USIMF**: USIM interrupt request flag
                 0: No request
                 1: Interrupt request

Bit 3   **DEE**: EEPROM interrupt control
                 0: Disable
                 1: Enable

Bit 2   **ADE**: A/D converter nterrupt control
                 0: Disable
                 1: Enable

Bit 1   **LVE**: LVD interrupt control
                 0: Disable
                 1: Enable

Bit 0   **USIME**: USIM interrupt control
                 0: Disable
                 1: Enable

• **INTC2 Register**

Bit	7	6	5	4	3	2	1	0
Name	STMAF	STMPF	PTMAF	PTMPF	STMAE	STMPE	PTMAE	PTMPF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7   **STMAF**: STM Comparator A match interrupt request flag
                 0: No request
                 1: Interrupt request

Bit 6   **STMPF**: STM Comparator P match interrupt request flag
                 0: No request
                 1: Interrupt request

Bit 5   **PTMAF**: PTM Comparator A match interrupt request flag
                 0: No request
                 1: Interrupt request

Bit 4   **PTMPF**: PTM Comparator P match interrupt request flag
                  0: No request
                  1: Interrupt request

Bit 3   **STMAE**: STM Comparator A match interrupt control
                  0: Disable
                  1: Enable

Bit 2   **STMPE**: STM Comparator P match interrupt control
                  0: Disable
                  1: Enable

Bit 1   **PTMAE**: PTM Comparator A match interrupt control
                  0: Disable
                  1: Enable

Bit 0   **PTMPE**: PTM Comparator P match interrupt control
                  0: Disable
                  1: Enable

• **INTC3 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	PLTC1F	TB1F	TB0F	—	PLTC1E	TB1E	TB0E
R/W	—	R/W	R/W	R/W	—	R/W	R/W	R/W
POR	—	0	0	0	—	0	0	0

Bit 7   Unimplemented, read as "0"

Bit 6   **PLTC1F**: PLT Comparator1 interrupt request flag
                  0: No request
                  1: Interrupt request

Bit 5   **TB1F**: Time Base 1 interrupt request flag
                  0: No request
                  1: Interrupt request

Bit 4   **TB0F**: Time Base 0 interrupt request flag
                  0: No request
                  1: Interrupt request

Bit 3   Unimplemented, read as "0"

Bit 2   **PLTC1E**: PLT Comparator 1 interrupt control
                  0: Disable
                  1: Enable

Bit 1   **TB1E**: Time Base 1 interrupt control
                  0: Disable
                  1: Enable

Bit 0   **TB0E**: Time Base 0 interrupt control
                  0: Disable
                  1: Enable
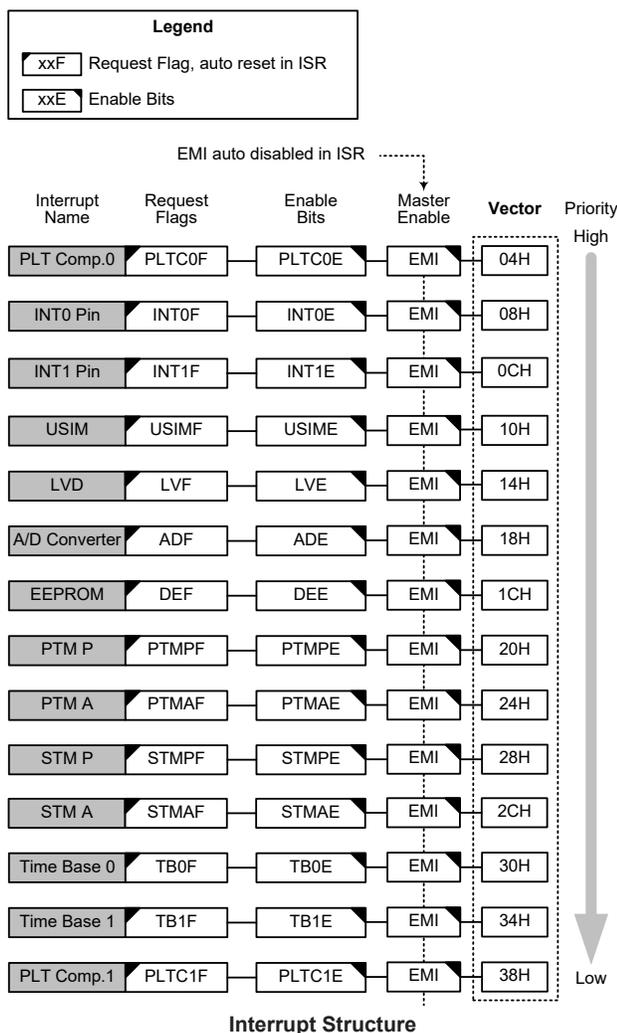
Interrupt Operation

When the conditions for an interrupt event occur, such as a TM Comparator P, Comparator A match or A/D conversion completion etc., the relevant interrupt request flag will be set. Whether the request flag actually generates a program jump to the relevant interrupt vector is determined by the condition of the interrupt enable bit. If the enable bit is set high, then the program will jump to its relevant vector; if the enable bit is zero then although the interrupt request flag is set an actual interrupt will not be generated and the program will not jump to the relevant interrupt vector. The global interrupt enable bit, if cleared to zero, will disable all interrupts.

When an interrupt is generated, the Program Counter, which stores the address of the next instruction to be executed, will be transferred onto the stack. The Program Counter will then be loaded with a new address which will be the value of the corresponding interrupt vector. The microcontroller will then fetch its next instruction from this interrupt vector. The instruction at this vector will usually be a "JMP"

which will jump to another section of program which is known as the interrupt service routine. Here is located the code to control the appropriate interrupt. The interrupt service routine must be terminated with a "RETI", which retrieves the original Program Counter address from the stack and allows the microcontroller to continue with normal execution at the point where the interrupt occurred.

The various interrupt enable bits, together with their associated request flags, are shown in the accompanying diagrams with their order of priority. All interrupt sources have their own individual vector. Once an interrupt subroutine is serviced, all the other interrupts will be blocked, as the global interrupt enable bit, EMI bit will be cleared automatically. This will prevent any further interrupt nesting from occurring. However, if other interrupt requests occur during this interval, although the interrupt will not be immediately serviced, the request flag will still be recorded.

If an interrupt requires immediate servicing while the program is already in another interrupt service routine, the EMI bit should be set after entering the routine, to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the Stack Pointer is decremented. If immediate service is desired, the stack must be prevented from becoming full. In case of simultaneous requests, the accompanying diagram shows the priority that is applied. All of the interrupt request flags when set will wake up the device if it is in SLEEP or IDLE Mode, however to prevent a wake-up from occurring the corresponding flag should be set before the device is in SLEEP or IDLE Mode.

Legend

xxF	Request Flag, auto reset in ISR
xxE	Enable Bits

EMI auto disabled in ISR

Interrupt Name	Request Flags	Enable Bits	Master Enable	**Vector**	Priority
PLT Comp.0	PLTC0F	PLTC0E	EMI	04H	High
INT0 Pin	INT0F	INT0E	EMI	08H	
INT1 Pin	INT1F	INT1E	EMI	0CH	
USIM	USIMF	USIME	EMI	10H	
LVD	LVF	LVE	EMI	14H	
A/D Converter	ADF	ADE	EMI	18H	
EEPROM	DEF	DEE	EMI	1CH	
PTM P	PTMPF	PTMPE	EMI	20H	
PTM A	PTMAF	PTMAE	EMI	24H	
STM P	STMPF	STMPE	EMI	28H	
STM A	STMAF	STMAE	EMI	2CH	
Time Base 0	TB0F	TB0E	EMI	30H	
Time Base 1	TB1F	TB1E	EMI	34H	
PLT Comp.1	PLTC1F	PLTC1E	EMI	38H	Low

Interrupt Structure

External Interrupts

The external interrupts are controlled by signal transitions on the pins INT0~INT1. An external interrupt request will take place when the external interrupt request flags, INT0F~INT1F, are set, which will occur when a transition, whose type is chosen by the edge select bits, appears on the external interrupt pins. To allow the program to branch to their respective interrupt vector addresses, the global interrupt enable bit, EMI, and respective external interrupt enable bit, INT0E~INT1E, must first be set. Additionally, the correct interrupt edge type must be selected using the INTEG register to enable the external interrupt function and to choose the trigger edge type. As the external interrupt pins are pin-shared with I/O pins, they can only be configured as external interrupt pins if their external interrupt enable bit in the corresponding interrupt register has been set and the external interrupt pin is selected by the corresponding pin-shared function selection bits. The pin must also be setup as an input by setting the corresponding bit in the port control register. When the interrupt is enabled, the stack is not full and the correct transition type appears on the external interrupt pin, a subroutine call to the external interrupt vector, will take place. When the interrupt is serviced, the external interrupt request flags, INT0F~INT1F, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts. Note that any pull-high resistor selections on the external interrupt pins will remain valid even if the pin is used as an external interrupt input.

The INTEG register is used to select the type of active edge that will trigger the external interrupt. A choice of either rising or falling or both edge types can be chosen to trigger an external interrupt. Note that the INTEG register can also be used to disable the external interrupt function.

PLT Comparator Interrupts

The PLT comparator interrupts are controlled by the Power Line Transceiver circuit internal comparators. A PLT comparator interrupt request will take place when the PLT comparator interrupt request flag, PLTCnF, is set, a situation that will occur when the PLT comparator output bit changes state. To allow the program to branch to their interrupt vector addresses, the global interrupt enable bit, EMI, and PLT comparator interrupt enable bit, PLTCnE, must first be set. When the interrupt is enabled, the stack is not full and the PLT comparator inputs generate a comparator output bit transition, a subroutine call to the PLT comparator interrupt vector, will take place. When the interrupt is serviced, the PLT comparator interrupt request flag, PLTCnF, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

USIM Interrupt

The Universal Serial Interface Module Interrupt, also known as the USIM interrupt, will take place when the USIM Interrupt request flag, USIMF, is set. As the USIM interface can operate in three modes which are SPI mode, I²C mode and UART mode, the USIMF flag can be set by different conditions depending on the selected interface mode.

If the SPI or I²C mode is selected, the USIM interrupt can be triggered when a byte of data has been received or transmitted by the USIM SPI or I²C interface, or an I²C slave address matches, or an I²C bus time-out occurs. If the UART mode is selected, several individual UART conditions including a transmitter data register empty, transmitter idle, receiver data available, receiver overrun, address detect and an URX/UTX pin wake-up, can generate an USIM interrupt with the USIMF flag bit set high.

To allow the program to branch to its interrupt vector address, the global interrupt enable bit, EMI and the Universal Serial Interface Module Interrupt enable bit, USIME, must first be set. When the interrupt is enabled, the stack is not full and any of the above described situations occurs, a subroutine call to the USIM Interrupt vector, will take place. When the interrupt is serviced, the USIM interrupt request flags will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

Note that if the USIM interrupt is triggered by the UART interface, after the interrupt has been servied, the UUSR register flags will be cleared automatically when certain actions are taken by the UART, the details of which are given in the UART section.

LVD Interrupt

An LVD Interrupt request will take place when the LVD Interrupt request flag, LVF, is set, which occurs when the Low Voltage Detector function detects a low power supply voltage. To allow the program to branch to its interrupt vector address, the global interrupt enable bit, EMI, and Low Voltage Interrupt enable bit, LVE, must first be set. When the interrupt is enabled, the stack is not full and a low voltage condition occurs, a subroutine call to the LVD Interrupt vector, will take place. When the Low Voltage Interrupt is serviced, the LVD Interrupt flag, LVF, will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

A/D Converter Interrupt

An A/D Converter Interrupt request will take place when the A/D Converter Interrupt request flag, ADF, is set, which occurs when the A/D conversion process finishes. To allow the program to branch to its interrupt vector address, the global interrupt enable bit, EMI and the A/D Interrupt enable bit, ADE, must first be set. When the interrupt is enabled, the stack is not full and the A/D conversion process has ended, a subroutine call to the A/D Converter Interrupt vector, will take place. When the interrupt is serviced, the A/D Converter Interrupt request flag, ADF, will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

EEPROM Interrupt

An EEPROM Interrupt request will take place when the EEPROM Interrupt request flag, DEF, is set, which occurs when an EEPROM Write cycle ends. To allow the program to branch to its interrupt vector address, the global interrupt enable bit, EMI and the EEPROM Interrupt enable bit, DEE, must first be set. When the interrupt is enabled, the stack is not full and an EEPROM Write cycle ends, a subroutine call to the EEPROM Interrupt vector will take place. When the EEPROM Interrupt is serviced, the DEF flag will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

TM Interrupts

The Standardand Periodic Type TMs each have two interrupts, one comes from the comparator A match situation and the other comes from the comparator P match situation. For all of the TM types there are two interrupt request flags and two enable control bits. A TM interrupt request will take place when any of the TM request flags are set, a situation which occurs when a TM comparator P or A match situation happens.

To allow the program to branch to their respective interrupt vector addresses, the global interrupt enable bit, EMI and the respective TM Interrupt enable bit, must first be set. When the interrupt is enabled, the stack is not full and a TM comparator match situation occurs, a subroutine call to the relevant TM Interrupt vector location, will take place. When the TM interrupt is serviced, the TM interrupt request flags will be automatically cleared. The EMI bit will also be automatically cleared to disable other interrupts.

Time Base Interrupts

The function of the Time Base Interrupts is to provide regular time signals in the form of an internal interrupt. They are controlled by the overflow signals from their respective timer functions. When these happens their respective interrupt request flags, TB0F or TB1F will be set. To allow the

program to branch to their respective interrupt vector addresses, the global interrupt enable bit, EMI and Time Base enable bits, TB0E or TB1E, must first be set. When the interrupt is enabled, the stack is not full and the Time Base overflows, a subroutine call to their respective vector locations will take place. When the interrupt is serviced, the respective interrupt request flag, TB0F or TB1F, will be automatically reset and the EMI bit will be cleared to disable other interrupts.

The purpose of the Time Base Interrupt is to provide an interrupt signal at fixed time periods. Its clock source, f_{PSC}, originates from the internal clock source f_{SYS}, $f_{SYS}/4$, f_{SUB} or f_{LXT} and then passes through a divider, the division ratio of which is selected by programming the appropriate bits in the TB0C or TB1C register to obtain longer interrupt periods whose value ranges. The clock source which in turn controls the Time Base interrupt period is selected using the CLKSEL1~CLKSEL0 bits in the PSCR register.

Time Base Interrupt
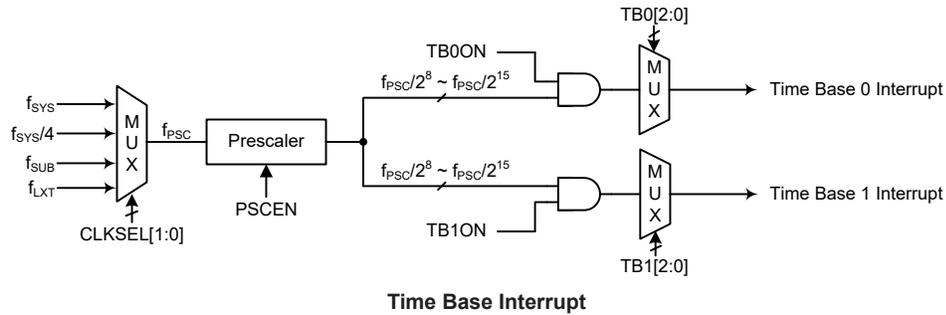
• **PSCR Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	PSCEN	CLKSEL1	CLKSEL0
R/W	—	—	—	—	—	R/W	R/W	R/W
POR	—	—	—	—	—	0	0	0

Bit 7~3   Unimplemented, read as "0"

Bit 2   **PSCEN**: Prescaler clock enable control
　　0: Disable
　　1: Enable

　　This PSCEN bit is the Prescaler clock enable or disable control bit. When the Prescale clock is disabled, it can reduce extra power consumption.

Bit 1~0   **CLKSEL1~CLKSEL0**: Prescaler clock source selection
　　00: f_{SYS}
　　01: $f_{SYS}/4$
　　10: f_{SUB}
　　11: f_{LXT}

• **TBnC Register (n=0~1)**

Bit	7	6	5	4	3	2	1	0
Name	TBnON	—	—	—	—	TBn2	TBn1	TBn0
R/W	R/W	—	—	—	—	R/W	R/W	R/W
POR	0	—	—	—	—	0	0	0

Bit 7   **TBnON**: Time Base n Control
　　0: Disable
　　1: Enable

Bit 6~3   Unimplemented, read as "0"

Bit 2~0   **TBn2~TBn0**: Time Base n Time-out Period Selection

         000: $2^8/f_{PSC}$
         001: $2^9/f_{PSC}$
         010: $2^{10}/f_{PSC}$
         011: $2^{11}/f_{PSC}$
         100: $2^{12}/f_{PSC}$
         101: $2^{13}/f_{PSC}$
         110: $2^{14}/f_{PSC}$
         111: $2^{15}/f_{PSC}$

Interrupt Wake-up Function

Each of the interrupt functions has the capability of waking up the microcontroller when in the SLEEP or IDLE Mode. A wake-up is generated when an interrupt request flag changes from low to high and is independent of whether the interrupt is enabled or not. Therefore, even though the device is in the SLEEP or IDLE Mode and its system oscillator stopped, situations such as external edge transitions on the external interrupt pins or a low power supply voltage may cause their respective interrupt flag to be set high and consequently generate an interrupt. Care must therefore be taken if spurious wake-up situations are to be avoided. If an interrupt wake-up function is to be disabled, then the corresponding interrupt request flag should be set high before the device enters the SLEEP or IDLE Mode. The interrupt enable bits have no effect on the interrupt wake-up function.

Programming Considerations

By disabling the relevant interrupt enable bits, a requested interrupt can be prevented from being serviced, however, once an interrupt request flag is set, it will remain in this condition in the interrupt register until the corresponding interrupt is serviced or until the request flag is cleared by the application program.

It is recommended that programs do not use the "CALL" instruction within the interrupt service subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately. If only one stack is left and the interrupt is not well controlled, the original control sequence will be damaged once a CALL subroutine is executed in the interrupt subroutine.

Every interrupt has the capability of waking up the microcontroller when it is in SLEEP or IDLE Mode, the wake up being generated when the interrupt request flag changes from low to high. If it is required to prevent a certain interrupt from waking up the microcontroller then its respective request flag should be first set high before enter SLEEP or IDLE Mode.

As only the Program Counter is pushed onto the stack, then when the interrupt is serviced, if the contents of the accumulator, status register or other registers are altered by the interrupt service program, their contents should be saved to the memory at the beginning of the interrupt service routine.

To return from an interrupt subroutine, either a RET or RETI instruction may be executed. The RETI instruction in addition to executing a return to the main program also automatically sets the EMI bit high to allow further interrupts. The RET instruction however only executes a return to the main program leaving the EMI bit in its present zero state and therefore disabling the execution of further interrupts.

Configuration Options

Configuration options refer to certain options within the MCU that are programmed into the device during the programming process. During the development process, these options are selected using the HT-IDE software development tools. All options must be defined for proper system function, the details of which are shown in the table.

No.	Options
Oscillator Option	
1	HIRC frequency selection – f_{HIRC}: 2MHz, 4MHz or 8MHz
Temperature Sensor Option	

2	Temperature Calibration Selection
	    1: Disable
	    2: Enable

Note: 1. When the HIRC has been configured at a frequency shown in this table, the HIRC1 and HIRC0 bits should also be set to select the same frequency to achieve the HIRC frequency accuracy specified in the A.C. Characteristics.

2. If it is required to implement temperature calibration and "Enable" has been selected, when using the writer for programming, it will detect whether the temperature module (EMDE001A) is connected or not. If the temperature module is not connected, the writer will indicate an error and cannot implement programming.

Application Circuits

2-pin Buzzer Mode

3-pin Buzzer Mode
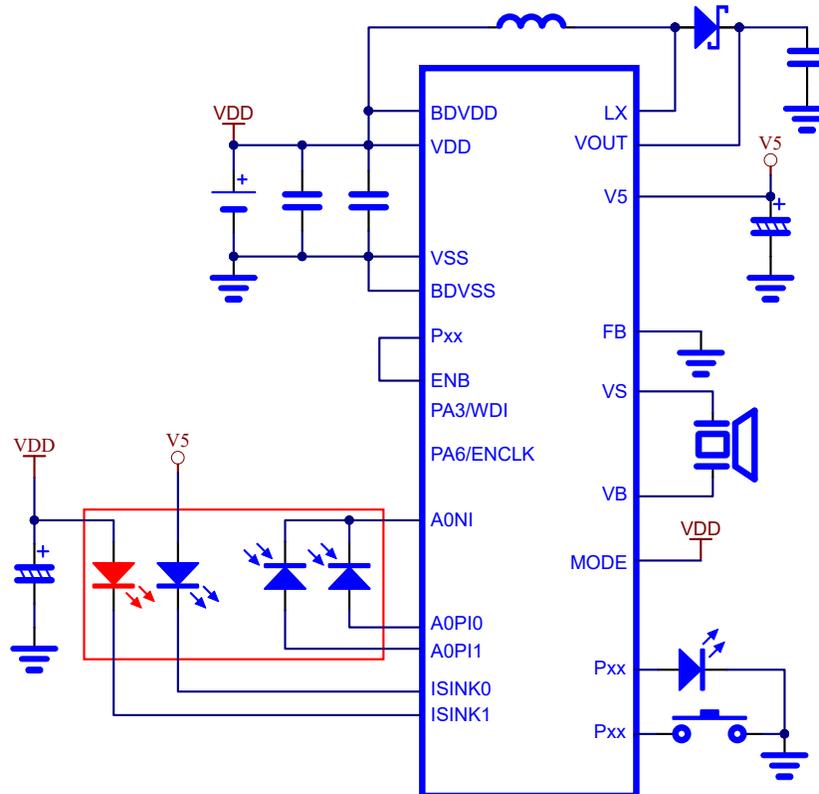
Instruction Set

Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontroller, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5μs and branch or call instructions would be implemented within 1μs. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be "CLR PCL" or "MOV PCL, A". For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of several kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions such as INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

Logical and Rotate Operation

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry bit from where it can be examined and the necessary serial bit set high or low. Another application which rotate data operations are used is to implement multiplication and division calculations.

Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction "RET" in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data bits.

Bit Operations

The ability to provide single bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port bit programming where individual bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-bit output port, manipulate the input data to ensure that other bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these bit operation instructions are used.

Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be setup as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

Instruction Set Summary

The instructions related to the data memory access in the following table can be used when the desired data memory is located in Data Memory sector 0.

Table Conventions

x: Bits immediate data

m: Data Memory address

A: Accumulator

i: 0~7 number of bits

addr: Program memory address

Mnemonic	Description	Cycles	Flag Affected
Arithmetic			
ADD A,[m]	Add Data Memory to ACC	1	Z, C, AC, OV, SC
ADDM A,[m]	Add ACC to Data Memory	1[Note]	Z, C, AC, OV, SC
ADD A,x	Add immediate data to ACC	1	Z, C, AC, OV, SC
ADC A,[m]	Add Data Memory to ACC with Carry	1	Z, C, AC, OV, SC
ADCM A,[m]	Add ACC to Data memory with Carry	1[Note]	Z, C, AC, OV, SC
SUB A,x	Subtract immediate data from the ACC	1	Z, C, AC, OV, SC, CZ
SUB A,[m]	Subtract Data Memory from ACC	1	Z, C, AC, OV, SC, CZ
SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	1[Note]	Z, C, AC, OV, SC, CZ
SBC A,x	Subtract immediate data from ACC with Carry	1	Z, C, AC, OV, SC, CZ
SBC A,[m]	Subtract Data Memory from ACC with Carry	1	Z, C, AC, OV, SC, CZ
SBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	1[Note]	Z, C, AC, OV, SC, CZ
DAA [m]	Decimal adjust ACC for Addition with result in Data Memory	1[Note]	C
Logic Operation			
AND A,[m]	Logical AND Data Memory to ACC	1	Z
OR A,[m]	Logical OR Data Memory to ACC	1	Z
XOR A,[m]	Logical XOR Data Memory to ACC	1	Z
ANDM A,[m]	Logical AND ACC to Data Memory	1[Note]	Z
ORM A,[m]	Logical OR ACC to Data Memory	1[Note]	Z
XORM A,[m]	Logical XOR ACC to Data Memory	1[Note]	Z
AND A,x	Logical AND immediate Data to ACC	1	Z
OR A,x	Logical OR immediate Data to ACC	1	Z
XOR A,x	Logical XOR immediate Data to ACC	1	Z
CPL [m]	Complement Data Memory	1[Note]	Z
CPLA [m]	Complement Data Memory with result in ACC	1	Z
Increment & Decrement			
INCA [m]	Increment Data Memory with result in ACC	1	Z
INC [m]	Increment Data Memory	1[Note]	Z
DECA [m]	Decrement Data Memory with result in ACC	1	Z
DEC [m]	Decrement Data Memory	1[Note]	Z
Rotate			
RRA [m]	Rotate Data Memory right with result in ACC	1	None
RR [m]	Rotate Data Memory right	1[Note]	None
RRCA [m]	Rotate Data Memory right through Carry with result in ACC	1	C
RRC [m]	Rotate Data Memory right through Carry	1[Note]	C
RLA [m]	Rotate Data Memory left with result in ACC	1	None
RL [m]	Rotate Data Memory left	1[Note]	None
RLCA [m]	Rotate Data Memory left through Carry with result in ACC	1	C
RLC [m]	Rotate Data Memory left through Carry	1[Note]	C

Mnemonic	Description	Cycles	Flag Affected
Data Move			
MOV A,[m]	Move Data Memory to ACC	1	None
MOV [m],A	Move ACC to Data Memory	1^{Note}	None
MOV A,x	Move immediate data to ACC	1	None
Bit Operation			
CLR [m].i	Clear bit of Data Memory	1^{Note}	None
SET [m].i	Set bit of Data Memory	1^{Note}	None
Branch Operation			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if Data Memory is zero	1^{Note}	None
SZA [m]	Skip if Data Memory is zero with data movement to ACC	1^{Note}	None
SZ [m].i	Skip if bit i of Data Memory is zero	1^{Note}	None
SNZ [m]	Skip if Data Memory is not zero	1^{Note}	None
SNZ [m].i	Skip if bit i of Data Memory is not zero	1^{Note}	None
SIZ [m]	Skip if increment Data Memory is zero	1^{Note}	None
SDZ [m]	Skip if decrement Data Memory is zero	1^{Note}	None
SIZA [m]	Skip if increment Data Memory is zero with result in ACC	1^{Note}	None
SDZA [m]	Skip if decrement Data Memory is zero with result in ACC	1^{Note}	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None
RETI	Return from interrupt	2	None
Table Read Operation			
TABRD [m]	Read table (specific page) to TBLH and Data Memory	2^{Note}	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory	2^{Note}	None
ITABRD [m]	Increment table pointer TBLP first and Read table (specific page) to TBLH and Data Memory	2^{Note}	None
ITABRDL [m]	Increment table pointer TBLP first and Read table (last page) to TBLH and Data Memory	2^{Note}	None
Miscellaneous			
NOP	No operation	1	None
CLR [m]	Clear Data Memory	1^{Note}	None
SET [m]	Set Data Memory	1^{Note}	None
CLR WDT	Clear Watchdog Timer	1	TO, PDF
SWAP [m]	Swap nibbles of Data Memory	1^{Note}	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC	1	None
HALT	Enter power down mode	1	TO, PDF

Note: 1. For skip instructions, if the result of the comparison involves a skip then two cycles are required, if no skip takes place only one cycle is required.

2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.

Extended Instruction Set

The extended instructions are used to support the full range address access for the data memory. When the accessed data memory is located in any data memory sector except sector 0, the extended instruction can be used to directly access the data memory instead of using the indirect addressing access. This can not only reduce the use of Flash memory space but also improve the CPU execution efficiency.

Mnemonic	Description	Cycles	Flag Affected
Arithmetic			
LADD A,[m]	Add Data Memory to ACC	2	Z, C, AC, OV, SC
LADDM A,[m]	Add ACC to Data Memory	2[Note]	Z, C, AC, OV, SC
LADC A,[m]	Add Data Memory to ACC with Carry	2	Z, C, AC, OV, SC
LADCM A,[m]	Add ACC to Data memory with Carry	2[Note]	Z, C, AC, OV, SC
LSUB A,[m]	Subtract Data Memory from ACC	2	Z, C, AC, OV, SC, CZ
LSUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	2[Note]	Z, C, AC, OV, SC, CZ
LSBC A,[m]	Subtract Data Memory from ACC with Carry	2	Z, C, AC, OV, SC, CZ
LSBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	2[Note]	Z, C, AC, OV, SC, CZ
LDAA [m]	Decimal adjust ACC for Addition with result in Data Memory	2[Note]	C
Logic Operation			
LAND A,[m]	Logical AND Data Memory to ACC	2	Z
LOR A,[m]	Logical OR Data Memory to ACC	2	Z
LXOR A,[m]	Logical XOR Data Memory to ACC	2	Z
LANDM A,[m]	Logical AND ACC to Data Memory	2[Note]	Z
LORM A,[m]	Logical OR ACC to Data Memory	2[Note]	Z
LXORM A,[m]	Logical XOR ACC to Data Memory	2[Note]	Z
LCPL [m]	Complement Data Memory	2[Note]	Z
LCPLA [m]	Complement Data Memory with result in ACC	2	Z
Increment & Decrement			
LINCA [m]	Increment Data Memory with result in ACC	2	Z
LINC [m]	Increment Data Memory	2[Note]	Z
LDECA [m]	Decrement Data Memory with result in ACC	2	Z
LDEC [m]	Decrement Data Memory	2[Note]	Z
Rotate			
LRRA [m]	Rotate Data Memory right with result in ACC	2	None
LRR [m]	Rotate Data Memory right	2[Note]	None
LRRCA [m]	Rotate Data Memory right through Carry with result in ACC	2	C
LRRC [m]	Rotate Data Memory right through Carry	2[Note]	C
LRLA [m]	Rotate Data Memory left with result in ACC	2	None
LRL [m]	Rotate Data Memory left	2[Note]	None
LRLCA [m]	Rotate Data Memory left through Carry with result in ACC	2	C
LRLC [m]	Rotate Data Memory left through Carry	2[Note]	C
Data Move			
LMOV A,[m]	Move Data Memory to ACC	2	None
LMOV [m],A	Move ACC to Data Memory	2[Note]	None
Bit Operation			
LCLR [m].i	Clear bit of Data Memory	2[Note]	None
LSET [m].i	Set bit of Data Memory	2[Note]	None

Mnemonic	Description	Cycles	Flag Affected
Branch			
LSZ [m]	Skip if Data Memory is zero	2[Note]	None
LSZA [m]	Skip if Data Memory is zero with data movement to ACC	2[Note]	None
LSNZ [m]	Skip if Data Memory is not zero	2[Note]	None
LSZ [m].i	Skip if bit i of Data Memory is zero	2[Note]	None
LSNZ [m].i	Skip if bit i of Data Memory is not zero	2[Note]	None
LSIZ [m]	Skip if increment Data Memory is zero	2[Note]	None
LSDZ [m]	Skip if decrement Data Memory is zero	2[Note]	None
LSIZA [m]	Skip if increment Data Memory is zero with result in ACC	2[Note]	None
LSDZA [m]	Skip if decrement Data Memory is zero with result in ACC	2[Note]	None
Table Read			
LTABRD [m]	Read table (specific page) to TBLH and Data Memory	3[Note]	None
LTABRDL [m]	Read table (last page) to TBLH and Data Memory	3[Note]	None
LITABRD [m]	Increment table pointer TBLP first and Read table (specific page) to TBLH and Data Memory	3[Note]	None
LITABRDL [m]	Increment table pointer TBLP first and Read table (last page) to TBLH and Data Memory	3[Note]	None
Miscellaneous			
LCLR [m]	Clear Data Memory	2[Note]	None
LSET [m]	Set Data Memory	2[Note]	None
LSWAP [m]	Swap nibbles of Data Memory	2[Note]	None
LSWAPA [m]	Swap nibbles of Data Memory with result in ACC	2	None

Note: 1. For these extended skip instructions, if the result of the comparison involves a skip then three cycles are required, if no skip takes place two cycles is required.

2. Any extended instruction which changes the contents of the PCL register will also require three cycles for execution.

Instruction Definition

ADC A,[m]	Add Data Memory to ACC with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC

ADCM A,[m]	Add ACC to Data Memory with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC

ADD A,[m]	Add Data Memory to ACC
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC

ADD A,x	Add immediate data to ACC
Description	The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + x$
Affected flag(s)	OV, Z, AC, C, SC

ADDM A,[m]	Add ACC to Data Memory
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC

AND A,[m]	Logical AND Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "AND" } [m]$
Affected flag(s)	Z

AND A,x	Logical AND immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bit wise logical AND operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \text{ "AND" } x$
Affected flag(s)	Z

ANDM A,[m]	Logical AND ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.
Operation	[m] ← ACC "AND" [m]
Affected flag(s)	Z

CALL addr	Subroutine call
Description	Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction.
Operation	Stack ← Program Counter + 1 Program Counter ← addr
Affected flag(s)	None

CLR [m]	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	[m] ← 00H
Affected flag(s)	None

CLR [m].i	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	[m].i ← 0
Affected flag(s)	None

CLR WDT	Clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF

CPL [m]	Complement Data Memory
Description	Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa.
Operation	[m] ← [m]
Affected flag(s)	Z

CPLA [m]	Complement Data Memory with result in ACC
Description	Each bit of the specified Data Memory is logically complemented (1′s complement).
	Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC ← [m]
Affected flag(s)	Z

DAA [m]	Decimal-Adjust ACC for addition with result in Data Memory
Description	Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.
Operation	$[m] \leftarrow ACC + 00H$ or $[m] \leftarrow ACC + 06H$ or $[m] \leftarrow ACC + 60H$ or $[m] \leftarrow ACC + 66H$
Affected flag(s)	C

DEC [m]	Decrement Data Memory
Description	Data in the specified Data Memory is decremented by 1.
Operation	$[m] \leftarrow [m] - 1$
Affected flag(s)	Z

DECA [m]	Decrement Data Memory with result in ACC
Description	Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] - 1$
Affected flag(s)	Z

HALT	Enter power down mode
Description	This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared.
Operation	$TO \leftarrow 0$ $PDF \leftarrow 1$
Affected flag(s)	TO, PDF

INC [m]	Increment Data Memory
Description	Data in the specified Data Memory is incremented by 1.
Operation	$[m] \leftarrow [m] + 1$
Affected flag(s)	Z

INCA [m]	Increment Data Memory with result in ACC
Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC \leftarrow [m] + 1$
Affected flag(s)	Z

JMP addr	Jump unconditionally
Description	The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction.
Operation	Program Counter ← addr
Affected flag(s)	None

MOV A,[m]	Move Data Memory to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	ACC ← [m]
Affected flag(s)	None

MOV A,x	Move immediate data to ACC
Description	The immediate data specified is loaded into the Accumulator.
Operation	ACC ← x
Affected flag(s)	None

MOV [m],A	Move ACC to Data Memory
Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	[m] ← ACC
Affected flag(s)	None

NOP	No operation
Description	No operation is performed. Execution continues with the next instruction.
Operation	No operation
Affected flag(s)	None

OR A,[m]	Logical OR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "OR" [m]
Affected flag(s)	Z

OR A,x	Logical OR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "OR" x
Affected flag(s)	Z

ORM A,[m]	Logical OR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC "OR" [m]
Affected flag(s)	Z

RET	Return from subroutine
Description	The Program Counter is restored from the stack. Program execution continues at the restored address.
Operation	Program Counter ← Stack
Affected flag(s)	None

RET A,x	Return from subroutine and load immediate data to ACC
Description	The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address.
Operation	Program Counter ← Stack ACC ← x
Affected flag(s)	None

RETI	Return from interrupt
Description	The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program.
Operation	Program Counter ← Stack EMI ← 1
Affected flag(s)	None

RL [m]	Rotate Data Memory left
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.
Operation	[m].(i+1) ← [m].i; (i=0~6) [m].0 ← [m].7
Affected flag(s)	None

RLA [m]	Rotate Data Memory left with result in ACC
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.(i+1) ← [m].i; (i=0~6) ACC.0 ← [m].7
Affected flag(s)	None

RLC [m]	Rotate Data Memory left through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.
Operation	[m].(i+1) ← [m].i; (i=0~6) [m].0 ← C C ← [m].7
Affected flag(s)	C

RLCA [m] Rotate Data Memory left through Carry with result in ACC

Description   Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation $ACC.(i+1) \leftarrow [m].i; (i=0\sim6)$
$ACC.0 \leftarrow C$
$C \leftarrow [m].7$

Affected flag(s)   C

RR [m]   Rotate Data Memory right

Description   The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.

Operation $[m].i \leftarrow [m].(i+1); (i=0\sim6)$
$[m].7 \leftarrow [m].0$

Affected flag(s)   None

RRA [m]   Rotate Data Memory right with result in ACC

Description   Data in the specified Data Memory is rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation $ACC.i \leftarrow [m].(i+1); (i=0\sim6)$
$ACC.7 \leftarrow [m].0$

Affected flag(s)   None

RRC [m]   Rotate Data Memory right through Carry

Description   The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.

Operation $[m].i \leftarrow [m].(i+1); (i=0\sim6)$
$[m].7 \leftarrow C$
$C \leftarrow [m].0$

Affected flag(s)   C

RRCA [m]   Rotate Data Memory right through Carry with result in ACC

Description   Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation $ACC.i \leftarrow [m].(i+1); (i=0\sim6)$
$ACC.7 \leftarrow C$
$C \leftarrow [m].0$

Affected flag(s)   C

SBC A,[m]   Subtract Data Memory from ACC with Carry

Description   The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation $ACC \leftarrow ACC - [m] - C$

Affected flag(s)   OV, Z, AC, C, SC, CZ

SBC A, x	Subtract immediate data from ACC with Carry
Description	The immediate data and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	ACC ← ACC − [m] − C
Affected flag(s)	OV, Z, AC, C, SC, CZ

SBCM A,[m]	Subtract Data Memory from ACC with Carry and result in Data Memory
Description	The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	[m] ← ACC − [m] − C
Affected flag(s)	OV, Z, AC, C, SC, CZ

SDZ [m]	Skip if decrement Data Memory is 0
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	[m] ← [m] − 1 Skip if [m]=0
Affected flag(s)	None

SDZA [m]	Skip if decrement Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	ACC ← [m] − 1 Skip if ACC=0
Affected flag(s)	None

SET [m]	Set Data Memory
Description	Each bit of the specified Data Memory is set to 1.
Operation	[m] ← FFH
Affected flag(s)	None

SET [m].i	Set bit of Data Memory
Description	Bit i of the specified Data Memory is set to 1.
Operation	[m].i ← 1
Affected flag(s)	None

SIZ [m]	Skip if increment Data Memory is 0
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$[m] \leftarrow [m] + 1$ Skip if [m]=0
Affected flag(s)	None

SIZA [m]	Skip if increment Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m] + 1$ Skip if ACC=0
Affected flag(s)	None

SNZ [m].i	Skip if bit i of Data Memory is not 0
Description	If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if $[m].i \neq 0$
Affected flag(s)	None

SNZ [m]	Skip if Data Memory is not 0
Description	The contents of the specified Data Memory are read out and then written back to the specified Data Memory again. If the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if $[m] \neq 0$
Affected flag(s)	None

SUB A,[m]	Subtract Data Memory from ACC
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - [m]$
Affected flag(s)	OV, Z, AC, C, SC, CZ

SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$[m] \leftarrow ACC - [m]$
Affected flag(s)	OV, Z, AC, C, SC, CZ

SUB A,x	Subtract immediate data from ACC
Description	The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - x$
Affected flag(s)	OV, Z, AC, C, SC, CZ

SWAP [m]	Swap nibbles of Data Memory
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged.
Operation	$[m].3\sim[m].0 \leftrightarrow [m].7\sim[m].4$
Affected flag(s)	None

SWAPA [m]	Swap nibbles of Data Memory with result in ACC
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC.3\sim ACC.0 \leftarrow [m].7\sim[m].4$ $ACC.7\sim ACC.4 \leftarrow [m].3\sim[m].0$
Affected flag(s)	None

SZ [m]	Skip if Data Memory is 0
Description	The contents of the specified Data Memory are read out and then written back to the specified Data Memory again. If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	Skip if [m]=0
Affected flag(s)	None

SZA [m]	Skip if Data Memory is 0 with data movement to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m]$ Skip if [m]=0
Affected flag(s)	None

SZ [m].i	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if [m].i=0
Affected flag(s)	None

TABRD [m]	Read table (specific page) to TBLH and Data Memory
Description	The low byte of the program code (specific page) addressed by the table pointer (TBLP and TBHP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

TABRDL [m]	Read table (last page) to TBLH and Data Memory
Description	The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

ITABRD [m]	Increment table pointer low byte first and read table (specific page) to TBLH and Data Memory Description Increment table pointer low byte, TBLP, first and then the program code (specific page) addressed by the table pointer (TBHP and TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte)
	TBLH ← program code (high byte)
Affected flag(s)	None

ITABRDL [m]	Increment table pointer low byte first and read table (last page) to TBLH and Data Memory
Description	Increment table pointer low byte, TBLP, first and then the low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte)
	TBLH ← program code (high byte)
Affected flag(s)	None

XOR A,[m]	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "XOR" [m]
Affected flag(s)	Z

XORM A,[m]	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC "XOR" [m]
Affected flag(s)	Z

XOR A,x	Logical XOR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "XOR" x
Affected flag(s)	Z

Extended Instruction Definition

The extended instructions are used to directly access the data stored in any data memory sections.

LADC A,[m]   Add Data Memory to ACC with Carry

Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC

LADCM A,[m]   Add ACC to Data Memory with Carry

Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m] + C$
Affected flag(s)	OV, Z, AC, C, SC

LADD A,[m]   Add Data Memory to ACC

Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC

LADDM A,[m]   Add ACC to Data Memory

Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.
Operation	$[m] \leftarrow ACC + [m]$
Affected flag(s)	OV, Z, AC, C, SC

LAND A,[m]   Logical AND Data Memory to ACC

Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	$ACC \leftarrow ACC \ "AND" \ [m]$
Affected flag(s)	Z

LANDM A,[m]   Logical AND ACC to Data Memory

Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.
Operation	$[m] \leftarrow ACC \ "AND" \ [m]$
Affected flag(s)	Z

LCLR [m]   Clear Data Memory

Description   Each bit of the specified Data Memory is cleared to 0.

Operation   [m] ← 00H

Affected flag(s)   None

LCLR [m].i   Clear bit of Data Memory

Description   Bit i of the specified Data Memory is cleared to 0.

Operation   [m].i ← 0

Affected flag(s)   None

LCPL [m]   Complement Data Memory

Description   Each bit of the specified Data Memory is logically complemented (1′s complement). Bits
                     which previously contained a 1 are changed to 0 and vice versa.

Operation   [m] ← [m]

Affected flag(s)   Z

LCPLA [m]   Complement Data Memory with result in ACC

Description   Each bit of the specified Data Memory is logically complemented (1′s complement).
                     Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result
                     is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation   ACC ← [m]

Affected flag(s)   Z

LDAA [m]   Decimal-Adjust ACC for addition with result in Data Memory

Description   Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value
                     resulting from the previous addition of two BCD variables. If the low nibble is greater than 9
                     or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble
                     remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6
                     will be added to the high nibble. Essentially, the decimal conversion is performed by adding
                     00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag
                     may be affected by this instruction which indicates that if the original BCD sum is greater than
                     100, it allows multiple precision decimal addition.

Operation   [m] ← ACC + 00H or
                     [m] ← ACC + 06H or
                     [m] ← ACC + 60H or
                     [m] ← ACC + 66H

Affected flag(s)   C

LDEC [m]   Decrement Data Memory

Description   Data in the specified Data Memory is decremented by 1.

Operation   [m] ← [m] − 1

Affected flag(s)   Z

LDECA [m]	Decrement Data Memory with result in ACC
Description	Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC ← [m] − 1
Affected flag(s)	Z

LINC [m]	Increment Data Memory
Description	Data in the specified Data Memory is incremented by 1.
Operation	[m] ← [m] + 1
Affected flag(s)	Z

LINCA [m]	Increment Data Memory with result in ACC
Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC ← [m] + 1
Affected flag(s)	Z

LMOV A,[m]	Move Data Memory to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	ACC ← [m]
Affected flag(s)	None

LMOV [m],A	Move ACC to Data Memory
Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	[m] ← ACC
Affected flag(s)	None

LOR A,[m]	Logical OR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC "OR" [m]
Affected flag(s)	Z

LORM A,[m]	Logical OR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC "OR" [m]
Affected flag(s)	Z

LRL [m] Rotate Data Memory left

Description   The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.

Operation $[m].(i+1) \leftarrow [m].i; (i=0\sim6)$
               $[m].0 \leftarrow [m].7$

Affected flag(s)   None

LRLA [m] Rotate Data Memory left with result in ACC

Description   The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.
               The rotated result is stored in the Accumulator and the contents of the Data Memory remain
               unchanged.

Operation $ACC.(i+1) \leftarrow [m].i; (i=0\sim6)$
               $ACC.0 \leftarrow [m].7$

Affected flag(s)   None

LRLC [m] Rotate Data Memory left through Carry

Description   The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7
               replaces the Carry bit and the original carry flag is rotated into bit 0.

Operation $[m].(i+1) \leftarrow [m].i; (i=0\sim6)$
               $[m].0 \leftarrow C$
               $C \leftarrow [m].7$

Affected flag(s)   C

LRLCA [m] Rotate Data Memory left through Carry with result in ACC

Description   Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces
               the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in
               theAccumulator and the contents of the Data Memory remain unchanged.

Operation $ACC.(i+1) \leftarrow [m].i; (i=0\sim6)$
               $ACC.0 \leftarrow C$
               $C \leftarrow [m].7$

Affected flag(s)   C

LRR [m] Rotate Data Memory right

Description   The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.

Operation $[m].i \leftarrow [m].(i+1); (i=0\sim6)$
               $[m].7 \leftarrow [m].0$

Affected flag(s)   None

LRRA [m]	Rotate Data Memory right with result in ACC
Description	Data in the specified Data Memory is rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.i \leftarrow [m].(i+1)$; (i=0~6) $ACC.7 \leftarrow [m].0$
Affected flag(s)	None

LRRC [m]	Rotate Data Memory right through Carry
Description	The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.
Operation	$[m].i \leftarrow [m].(i+1)$; (i=0~6) $[m].7 \leftarrow C$ $C \leftarrow [m].0$
Affected flag(s)	C

LRRCA [m]	Rotate Data Memory right through Carry with result in ACC
Description	Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	$ACC.i \leftarrow [m].(i+1)$; (i=0~6) $ACC.7 \leftarrow C$ $C \leftarrow [m].0$
Affected flag(s)	C

LSBC A,[m]	Subtract Data Memory from ACC with Carry
Description	The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$ACC \leftarrow ACC - [m] - C$
Affected flag(s)	OV, Z, AC, C, SC, CZ

LSBCM A,[m]	Subtract Data Memory from ACC with Carry and result in Data Memory
Description	The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	$[m] \leftarrow ACC - [m] - C$
Affected flag(s)	OV, Z, AC, C, SC, CZ

LSDZ [m]   Skip if decrement Data Memory is 0

Description   The contents of the specified Data Memory are first decremented by 1. If the result is 0 the
                     following instruction is skipped. As this requires the insertion of a dummy instruction while
                     the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program
                     proceeds with the following instruction.

Operation $[m] \leftarrow [m] - 1$
                     Skip if [m]=0

Affected flag(s)   None

LSDZA [m]   Skip if decrement Data Memory is zero with result in ACC

Description   The contents of the specified Data Memory are first decremented by 1. If the result is 0, the
                     following instruction is skipped. The result is stored in the Accumulator but the specified
                     Data Memory contents remain unchanged. As this requires the insertion of a dummy
                     instruction while the next instruction is fetched, it is a three cycle instruction. If the result is
                     not 0, the program proceeds with the following instruction.

Operation $ACC \leftarrow [m] - 1$
                     Skip if ACC=0

Affected flag(s)   None

LSET [m]   Set Data Memory

Description   Each bit of the specified Data Memory is set to 1.

Operation $[m] \leftarrow FFH$

Affected flag(s)   None

LSET [m].i   Set bit of Data Memory

Description   Bit i of the specified Data Memory is set to 1.

Operation $[m].i \leftarrow 1$

Affected flag(s)   None

LSIZ [m]   Skip if increment Data Memory is 0

Description   The contents of the specified Data Memory are first incremented by 1. If the result is 0, the
                     following instruction is skipped. As this requires the insertion of a dummy instruction while
                     the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program
                     proceeds with the following instruction.

Operation $[m] \leftarrow [m] + 1$
                     Skip if [m]=0

Affected flag(s)   None

LSIZA [m]   Skip if increment Data Memory is zero with result in ACC

Description   The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation   ACC ← [m] + 1
Skip if ACC=0

Affected flag(s)   None

LSNZ [m].i   Skip if bit i of Data Memory is not 0

Description   If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is 0 the program proceeds with the following instruction.

Operation   Skip if [m].i ≠ 0

Affected flag(s)   None

LSNZ [m]   Skip if Data Memory is not 0

Description   The contents of the specified Data Memory are read out and then written to the specified Data Memory again. If the content of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is 0 the program proceeds with the following instruction.

Operation   Skip if [m] ≠ 0

Affected flag(s)   None

LSUB A,[m]   Subtract Data Memory from ACC

Description   The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation   ACC ← ACC − [m]

Affected flag(s)   OV, Z, AC, C, SC, CZ

LSUBM A,[m]   Subtract Data Memory from ACC with result in Data Memory

Description   The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation   [m] ← ACC − [m]

Affected flag(s)   OV, Z, AC, C, SC, CZ

LSWAP [m]	Swap nibbles of Data Memory
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged.
Operation	$[m].3\sim[m].0 \leftrightarrow [m].7\sim[m].4$
Affected flag(s)	None

LSWAPA [m]	Swap nibbles of Data Memory with result in ACC
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	$ACC.3\sim ACC.0 \leftarrow [m].7\sim[m].4$ $ACC.7\sim ACC.4 \leftarrow [m].3\sim[m].0$
Affected flag(s)	None

LSZ [m]	Skip if Data Memory is 0
Description	The contents of the specified Data Memory are read out and then written to the specified Data Memory again. If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	Skip if [m]=0
Affected flag(s)	None

LSZA [m]	Skip if Data Memory is 0 with data movement to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	$ACC \leftarrow [m]$ Skip if [m]=0
Affected flag(s)	None

LSZ [m].i	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a three cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if [m].i=0
Affected flag(s)	None

LTABRD [m]	Read table (specific page) to TBLH and Data Memory
Description	The low byte of the program code (specific page) addressed by the table pointer (TBHP and TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	$[m] \leftarrow$ program code (low byte) $TBLH \leftarrow$ program code (high byte)
Affected flag(s)	None

LTABRDL [m]   Read table (last page) to TBLH and Data Memory

Description   The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved
                  to the specified Data Memory and the high byte moved to TBLH.

Operation   [m] ← program code (low byte)
                  TBLH ← program code (high byte)

Affected flag(s) None

LITABRD [m]   Increment table pointer low byte first and read table (specific page) to TBLH and Data
                  Memory

Description   Increment table pointer low byte, TBLP, first and then the program code (specific page)
                  addressed by the table pointer (TBHP and TBLP) is moved to the specified Data Memory and
                  the high byte moved to TBLH.

Operation   [m] ← program code (low byte)
                  TBLH ← program code (high byte)

Affected flag(s) None

LITABRDL [m] Increment table pointer low byte first and read table (last page) to TBLH and Data Memory

Description   Increment table pointer low byte, TBLP, first and then the low byte of the program code
                  (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and
                  the high byte moved to TBLH.

Operation   [m] ← program code (low byte)
                  TBLH ← program code (high byte)

Affected flag(s) None

LXOR A,[m]   Logical XOR Data Memory to ACC

Description   Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR
                  operation. The result is stored in the Accumulator.

Operation   ACC ← ACC "XOR" [m]

Affected flag(s) Z

LXORM A,[m]   Logical XOR ACC to Data Memory

Description   Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR
                  operation. The result is stored in the Data Memory.

Operation   [m] ← ACC "XOR" [m]

Affected flag(s) Z

Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)

- The Operation Instruction of Packing Materials

- Carton information

24-pin SSOP (150mil) Outline Dimensions
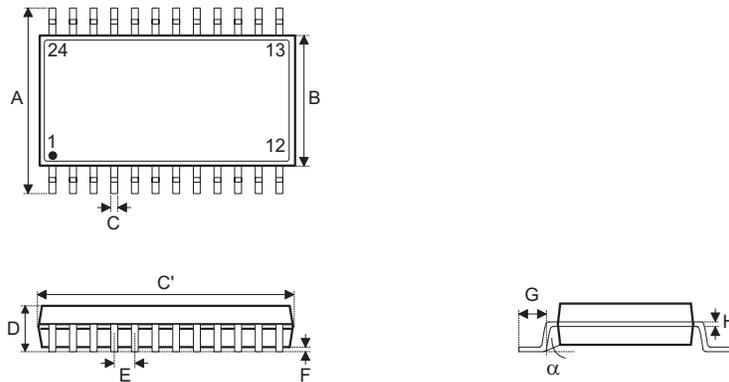
Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.236 BSC	
B		0.154 BSC	
C	0.008	—	0.012
C'		0.341 BSC	
D	—	—	0.069
E		0.025 BSC	
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		6.00 BSC	
B		3.90 BSC	
C	0.20	—	0.30
C'		8.66 BSC	
D	—	—	1.75
E		0.635 BSC	
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°

28-pin SSOP (150mil) Outline Dimensions
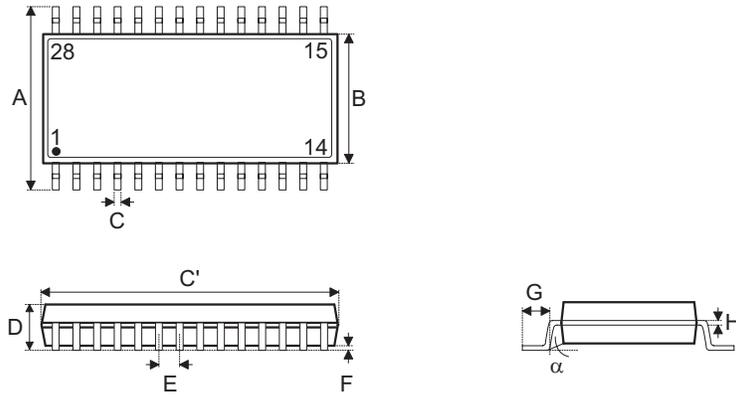
Symbol	Dimensions in inch		
	Min.	**Nom.**	**Max.**
A		0.236 BSC	
B		0.154 BSC	
C	0.008	—	0.012
C'		0.390 BSC	
D	—	—	0.069
E		0.025 BSC	
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	**Nom.**	**Max.**
A		6.00 BSC	
B		3.90 BSC	
C	0.20	—	0.30
C'		9.90 BSC	
D	—	—	1.75
E		0.635 BSC	
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°