PIR Controller

BA76220

Revision: V1.01 Date: January 13, 2026

www.holtek.com

Features

- Operating voltage: 2.2V~5.5V
- Standby current: 12μA (Typ.)
- CDS input
- High noise immunity
- 40-second warm-up or 10-second fast mode
- 6 hour adjustable PIR turn-on timing
- Output drive pin
- Low voltage detector
- Package type: 16-pin NSOP

Applications

- PIR light control
- Motion detectors
- Auto door bells

Development Tools

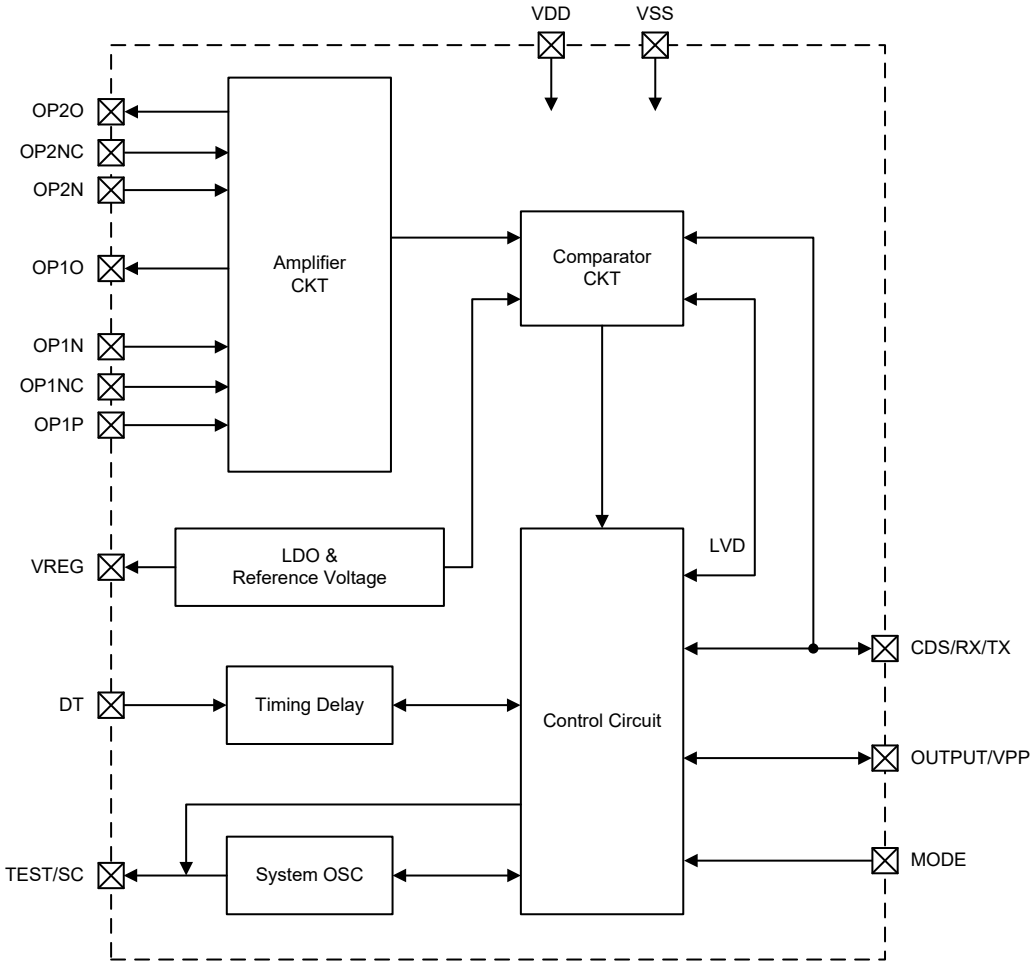
For rapid product development and to simplify device parameter setting, Holtek has provided relevant development tools which users can download from the following link:

https://www.holtek.com/page/tool-detail/dev_plat/security/PIR_Parameter_Platform

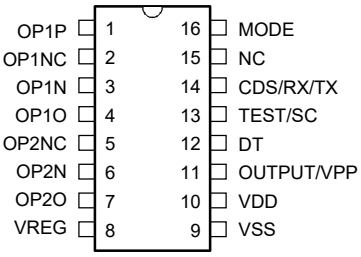
General Description

The BA76220 is a controller specifically designed for human infrared sensors (PIR Sensor), featuring high sensitivity, low power consumption and multi-functional output control, suitable for various smart sensing applications. It also supports OTP (One-Time Programmable) ROM, allowing customization of IC parameters to meet specific application requirements. The controller is available in low profile 16-pin NSOP package.

Block Diagram



Pin Assignment



BA76220
16 NSOP-A

Pin Description

Pin No.	Pin Name	Type	Internal Connection	Description
1	OP1P	AI	PMOS	OP1 non-inverting input
2	OP1NC	AI	PMOS	Capacitor connected to OP1 inverting input
3	OP1N	AI	PMOS	OP1 inverting input
4	OP1O	AO	CMOS	OP1 output
5	OP2NC	AI	PMOS	Capacitor connected to OP2 inverting input
6	OP2N	AI	PMOS	OP2 inverting input
7	OP2O	AO	CMOS	OP2 output
8	VREG	AO	NMOS	Regulator voltage
9	VSS	PWR	—	Negative power supply, ground
10	VDD	PWR	—	Positive power supply
11	OUTPUT/VPP	DO/PWR	CMOS	OUTPUT and VPP share the same pin ● Output to drive, active high ● Programming ROM power supply
12	DT	AI	PMOS	Delay time oscillator input. Connected to an external RC to adjust output duration
13	TEST/SC	DO	CMOS	TEST and SC share the same pin ● TEST is used to test the 32kHz system frequency ● SC is used to detect LVD and CDS
14	CDS/RX/TX	AI/DI/DO	CMOS	CDS and RX/TX share the same pin ● CDS is connected to a CDS voltage divider for daytime/night auto-detection. A low input to this pin can disable the PIR input ● Write data & read data
15	NC	—	—	Not connected
16	MODE	AI	CMOS	● Operating mode selection input VDD: Output is always ON VSS: Output is always OFF OPEN: Auto detection ● Input for Test mode

Legend: DI: Digital Input; DO: Digital Output; AI: Analog Input; AO: Analog Output; PWR: Power

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to 6.0V

Input Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature..... -60°C to 150°C

Operating Temperature..... -40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of the device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.2	3.3	5.5	V
V_{REG}(Note)	Regulator Voltage	—	C_{VREG}=0.1μF, VREG[1:0]=01B	-3%	2.0	3%	V
		—	C_{VREG}=0.1μF, VREG[1:0]=00B	-3%	2.2	3%	V
		—	C_{VREG}=0.1μF, VREG[1:0]=10/11B	-3%	2.4	3%	V
I_{REG}	Driving Current	5V	C_{VREG}=0.1μF, ΔV_{OUT}=-3%	1	—	—	mA
I_{STB}	Standby Current	5V	DT off, OPAMP on	—	17	23	μA
		3V		—	12	17	μA
I_{OH}	OUTPUT Source Current	5V/3V	V_{OH}=0.9V_{DD}	-5	-10	—	mA
I_{OL}	OUTPUT Sink Current	5V/3V	V_{OL}=0.1V_{DD}	10	20	—	mA
V_{IH}	MODE High Input Voltage	—	—	0.7V_{DD}	—	—	V
V_{IL}	MODE Low Input Voltage	—	—	—	—	0.3V_{DD}	V
V_{OS}	Operational Amplifier Input Offset Voltage	3V	—	-10	—	10	mV
f_{SYS}	System Oscillator Frequency	5V/3V	IRC	-2%	32	2%	kHz
f_{DT}	Delay Time Frequency	3V	ERC: V_{REG}, R_{DT}=30kΩ, C_{DT}=3000pF, @25°C	-10%	16	10%	kHz
A_{OL}	Operational Amplifier Open Loop Gain	3V	R_{LOAD}=1MΩ, C_{LOAD}=60pF	60	80	—	dB
GBW	Operational Amplifier Gain Band Bandwidth	3V	R_{LOAD}=1MΩ, C_{LOAD}=60pF	2	4	—	kHz
V_{PIRH}	Comparator Window High Level	—	(1/2)V_{REG}+(1/6)V_{REG}	-5%	1.33	5%	V
V_{PIRL}	Comparator Window Low Level	—	(1/2)V_{REG}-(1/6)V_{REG}	-5%	0.66	5%	V

Note: When V_{DD} is less than V_{REG}+0.1V, then the V_{REG} voltage will be equal to V_{DD}. If the V_{REG} voltage is less than the PIR operating voltage, then the PIR sensor will not operate normally.

Functional Description

TEST

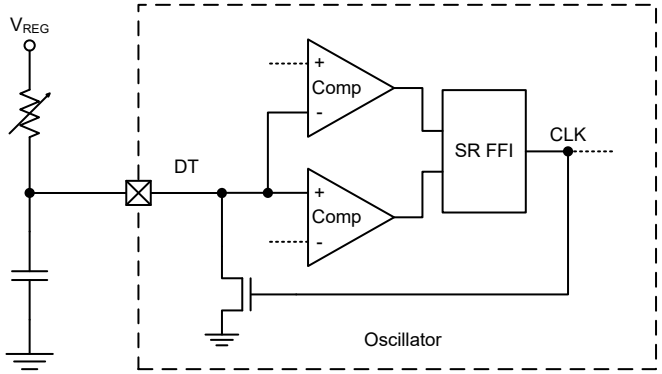
The TEST pin is an output which is used to test the 32kHz system frequency. The TEST/SC is a shared pin. The pin is used as TEST within 1 second after power-on.

SC

The SC pin is an output pin which is used to for LVD and CDS detection. The TEST/SC is a shared pin. The pin is used as SC after 1 second of power-on.

DT

The DT pin is a delay time oscillator input pin. It is connected to an external RC to obtain the desired output turn-on duration. Variable output turn-on durations can be achieved by selecting various values of RC or using a variable resistor. The DT structure is shown below.



DT Oscillator Structure

MODE

The MODE pin is a tristate input which is used to select the desired device operating mode.

MODE Status	Operating Mode	Description
VDD	ON	Output is always ON: OUTPUT pin activated
VSS	OFF	Output is always OFF: OUTPUT pin inactive
OPEN	AUTO	Outputs remain in the off state till activated by a valid PIR input trigger signal.

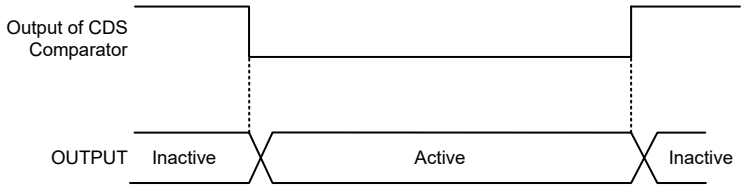
The device provides the following additional function:

If the pin is asserted a high pulse which is more than 400ms within 1 second after power-on, the device will be forced to enter the test mode, and when the device enters the test mode, the power-on delay time is changed from 40 seconds to 10 seconds.

CDS

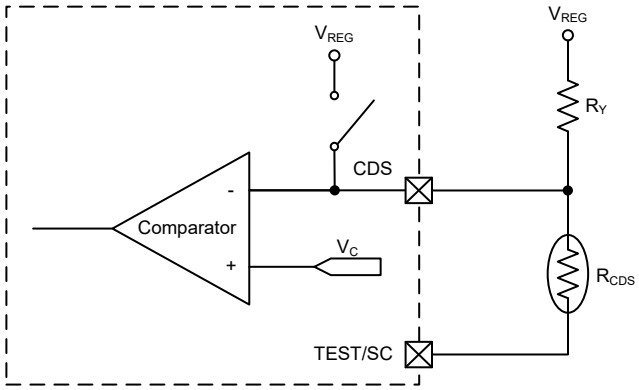
The CDS pin is connected to an internal comparator input. It is used to allow the device to distinguish between day and night conditions. When the CDS input voltage is less than V_C, the PIR amplifier circuit will be disabled and the outputs of OUTPUT pin is inactive. When the input voltage of the CDS is greater than V_C, the outputs are both active. The debounce time for the CDS pin for switching the output from an inactive to an active state is about less than 3 seconds. Connect this pin to V_{REG} when this function is not used. The CDS timing is shown below. The V_C comes from 6-bit DAC, the voltage changes is described in the following CDS register. The 6-bit DAC is shared with LVD.

CDS Pin	Status	Output
$V_{CDS}<V_C$	Day Time	Disabled
$V_{CDS}>V_C$	Night	Controlled by PIR



CDS Timing

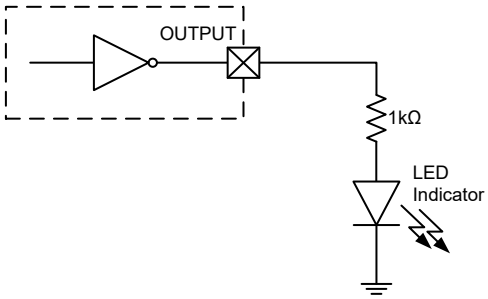
As shown below, R_{CDS} and R_Y can be adjusted to obtain the desired day time detection level.



CDS Application Example

OUTPUT

The OUTPUT is a CMOS structure, acting as a valid trigger indicator. The high duration is controlled by the delay time oscillator and the MODE pin. The OUTPUT pin structure is shown below.



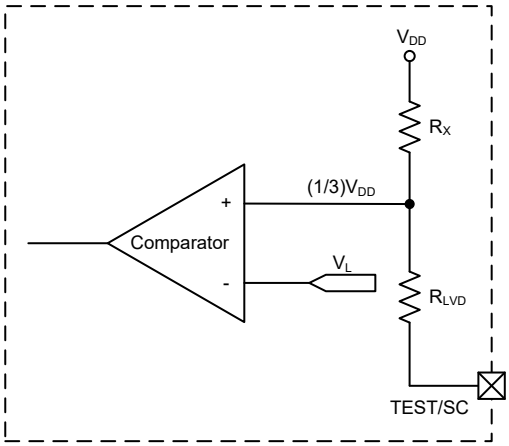
OUTPUT Pin Can Drive LED

LVD

The LVD is a low voltage detector. When the detected voltage is less than V_L, the OUTPUT will be toggled.

As shown below, assume R_X, R_{LVD} can be adjusted to obtain the desired voltage detection level.

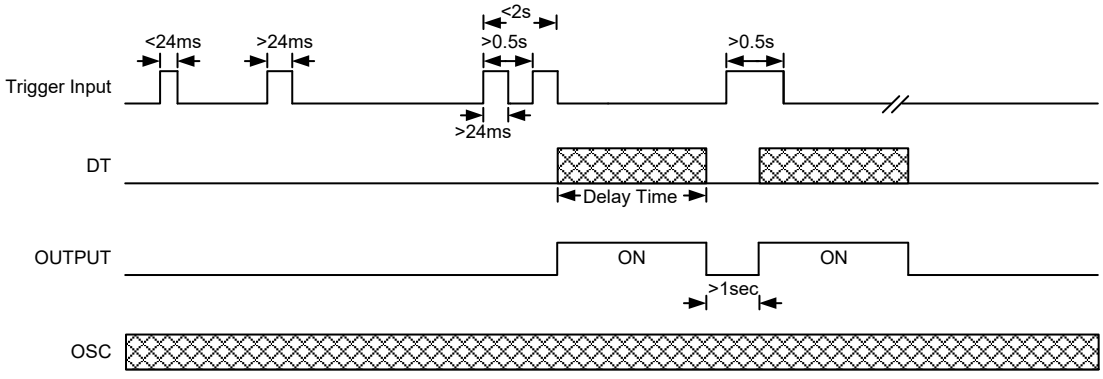
Users can select V_L by the LVD register.



LVD Application Example

Trigger Timing

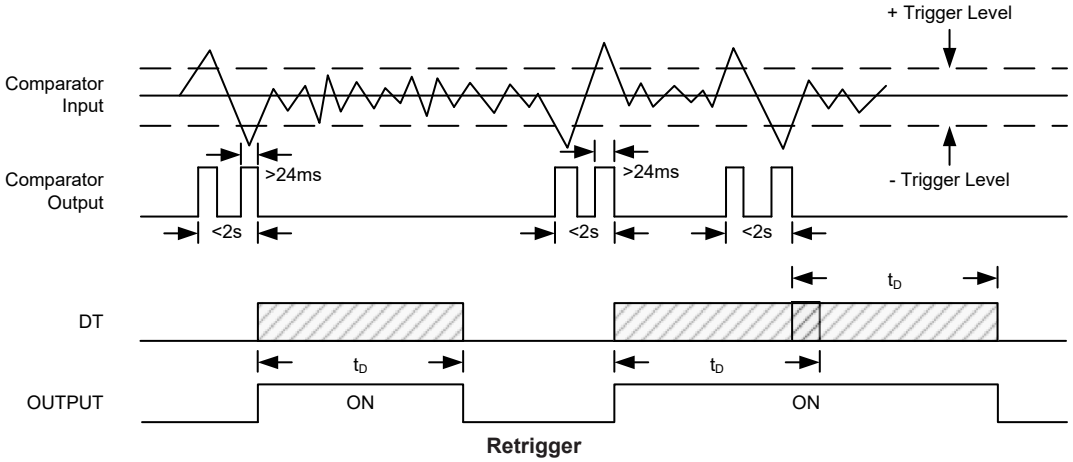
The effective input trigger signal width should be ≥ 24ms. The output is valid either with (1) trigger signal width ≥ 0.5 seconds or (2) more than 2 effective trigger inputs within 2 seconds (separation of 2 triggers ≥ 0.5s). And the separation time between two OUTPUT pin turn-on time must be more than 1 sec. The trigger timing is shown below.



Trigger Timing

Retrigger

When the output of the comparator is a valid signal, the OUTPUT pin will be activated and the active duration is controlled by the DT oscillating period. If the previous "Delay Time t_D" has not been over yet and the next valid signal occurs again, the active duration of the OUTPUT pin will be restarted to count. The timing is shown below.



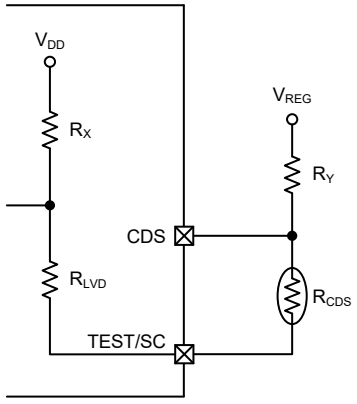
Retrigger

LVD & CDS Detect Circuit

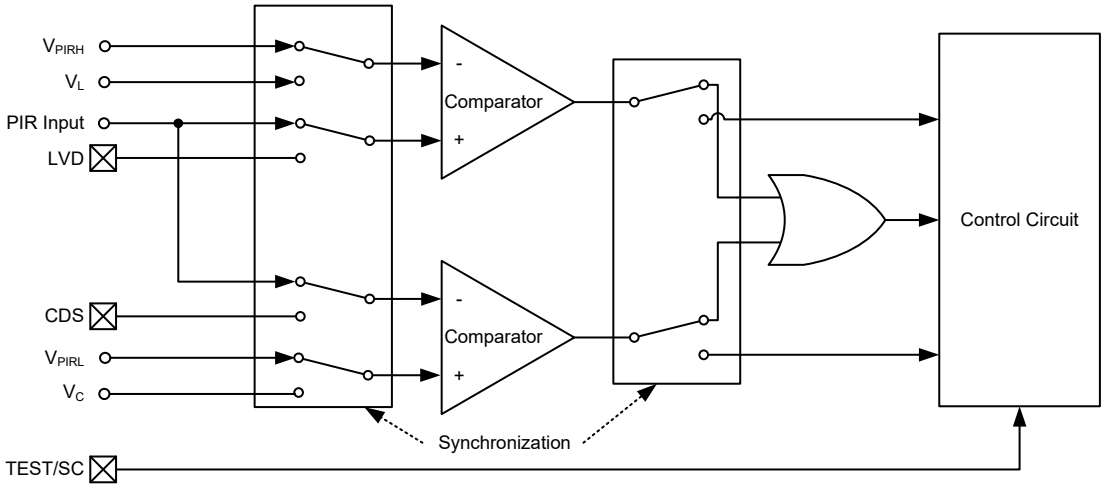
The external and internal detecting circuits for LVD and CDS are shown below respectively. When the input voltage V_{LVD} is less than V_L, the comparator outputs a low level and it means that the V_{DD} is less than minimum operating voltage (V_{MIN}). When the V_{CDS} is less than V_C, the comparator outputs high level and it means that it is daytime, otherwise it is night.

Where $V_{LVD} = \frac{R_{LVD}}{R_{LVD} + R_X} V_{DD}$

$V_{CDS} = \frac{R_{CDS}}{R_{CDS} + R_Y} V_{REG}$



CDS & LVD Application Circuit

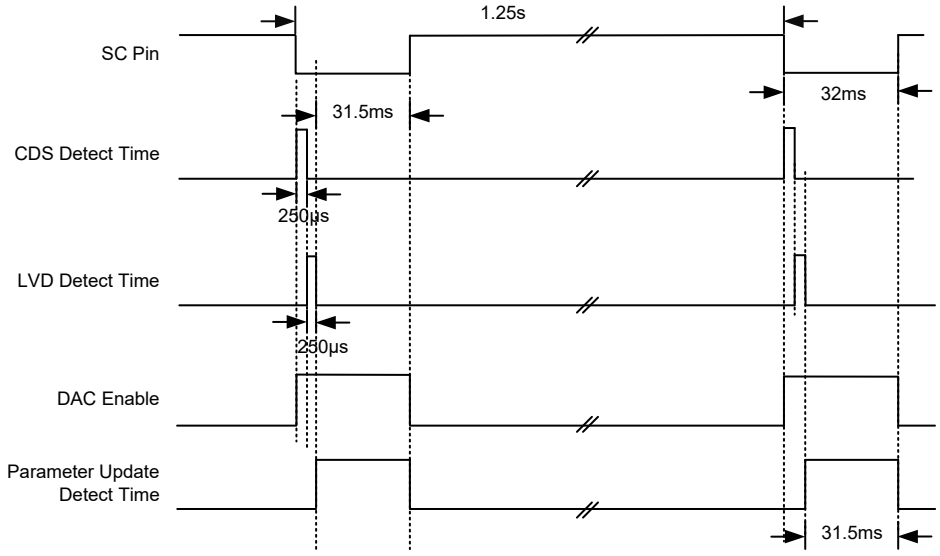


Internal Structure

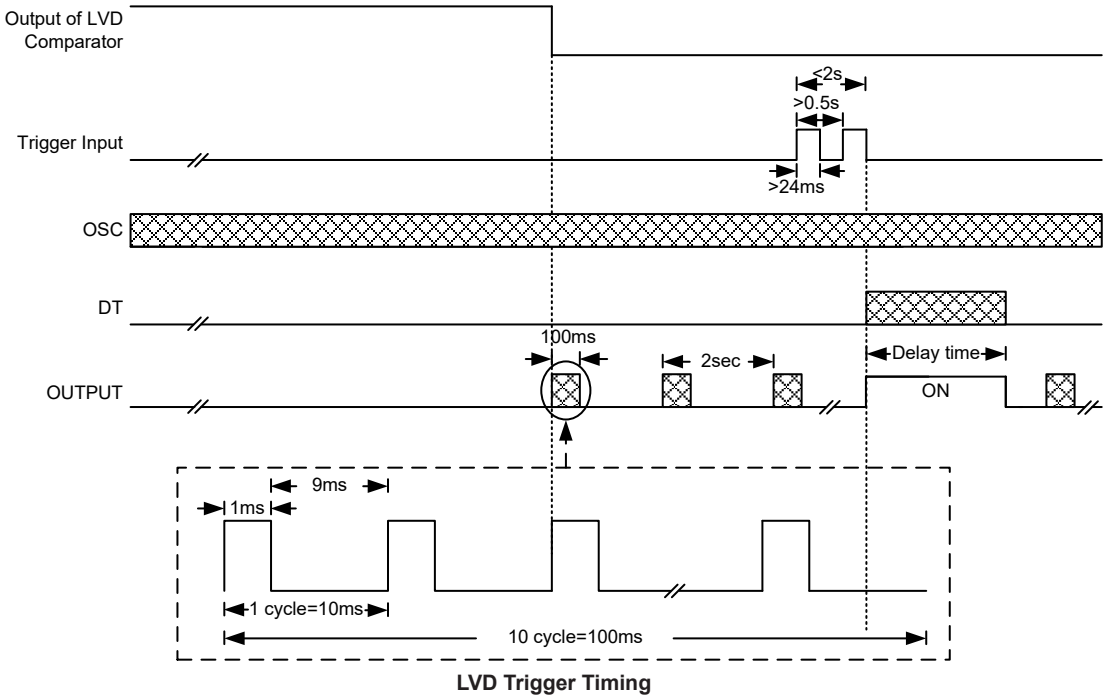
Note: When the input voltage of CDS is low, it means that daytime, the OUTPUT pin is inactive.

The Criterion of LVD and CDS

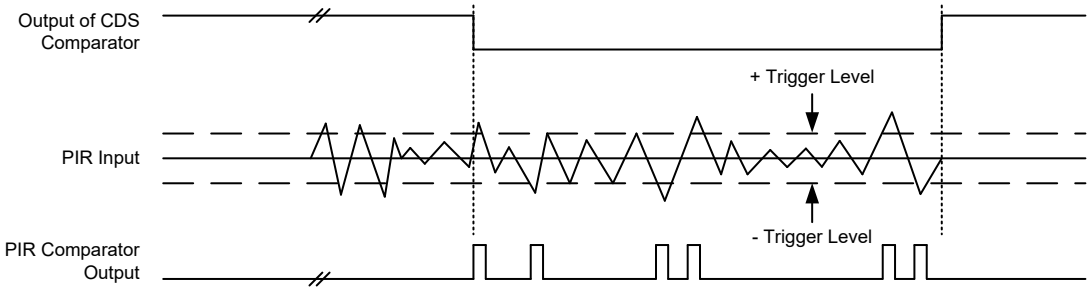
The criterion for detecting LVD and CDS are defined as following: the LVD and CDS are detected once per 1.25 seconds and the detecting time is 32ms. If the CDS signals are detected as the same state for 2 times continuously, the states of CDS is validated. If the LVD signals are detected as the same state for 4 times continuously, the states of LVD is validated. The LVD and CDS trigger timing are shown below. When the LVD condition occurs, the OUTPUT will be toggled, and neglecting any one valid trigger during 0.5 seconds after OUTPUT begins to flash. When the CDS is changed from high to low, the output of PIR is controlled by PIR, and when the CDS is changed from low to high, the output of PIR is disabled.



Detect Timing



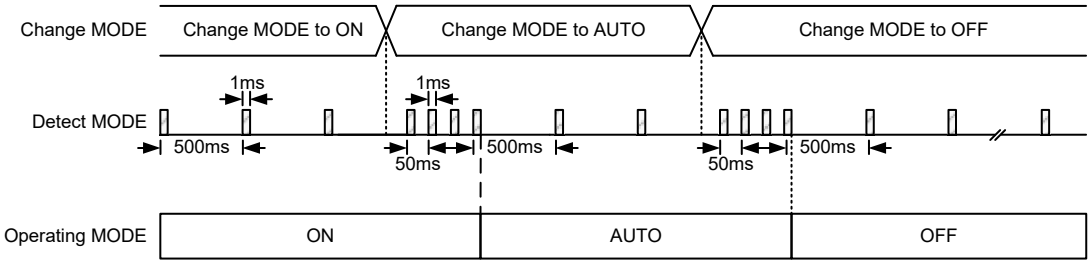
LVD Trigger Timing



CDS Trigger Timing

The Criterion of MODE

When the MODE is not changed, the MODE is detected once per 500ms, and when the MODE is changed, the MODE is detected once per 50ms. If the MODE signal is detected as the same state for 4 times continuously, the state of MODE is validated. The timing is shown below.



Detect Mode

Conditions for Disabling the PIR Amplifier Circuit

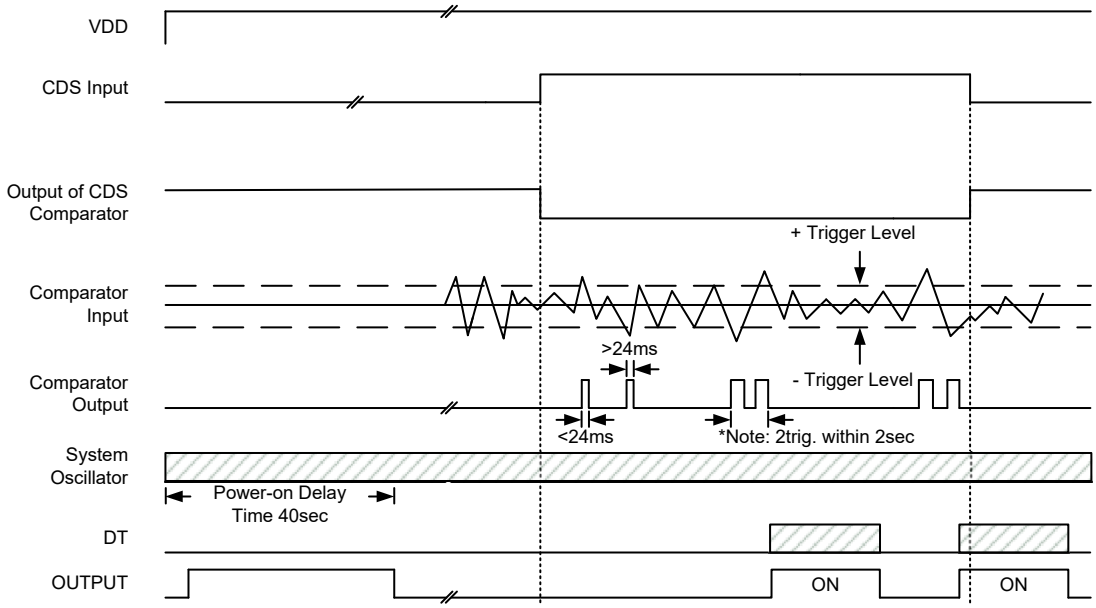
The device allows the PIR amplifier circuit to be disabled which is defined as follows:

- When the input voltage of V_{CDS} is less than V_C, it means that daytime, the circuit of PIR amplifier is disabled.

Selection of OSC or DT

The Delay time oscillation circuit is active and used only for the OUTPUT turn-on.

The OSC system frequency is always active and used for other conditions.



Trigger Timing

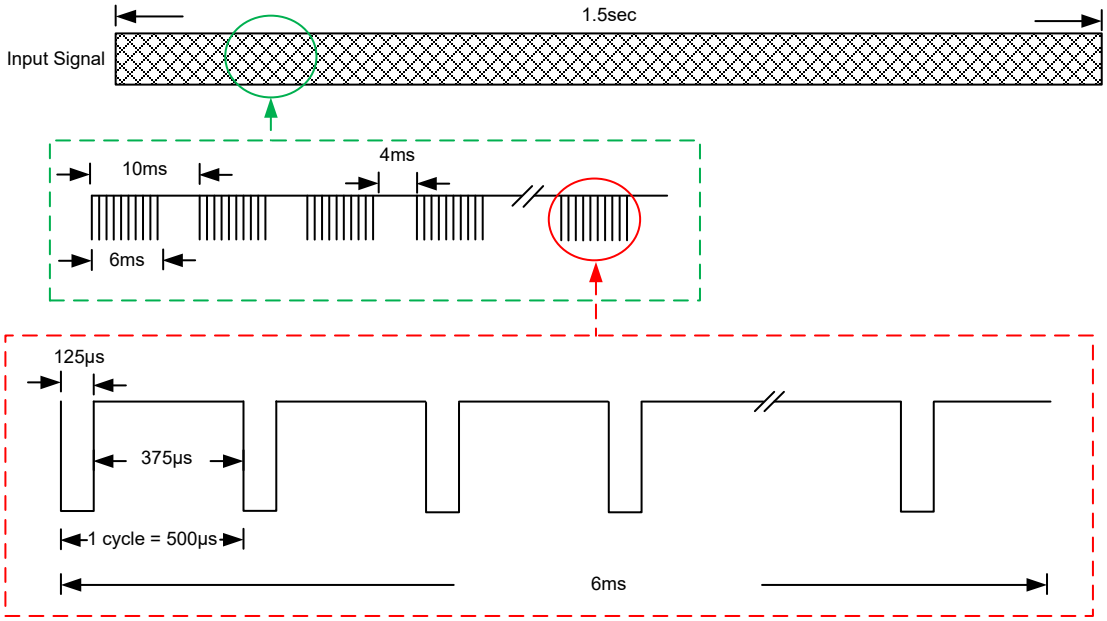
Note: The output is activated if the trigger signal conforms to the following criteria:

1. Two triggers occur within 2 seconds and the separation time between two triggers is more than 0.5sec.
2. The trigger signal sustains duration ≥ 0.5 seconds.

Write ROM & Data Updated

The device supports ROM programming and host computer parameter updating. When the device is powered on, the Buffer will read the parameters from ROM first, and if the host computer requires to modify the parameters, it will rewrite the values of the Buffer via the single-wire UART. The write ROM operation is implemented via a programming platform. After the ROM is written successfully, the Buffer will read the parameter values from the ROM.

When entering the host computer mode, a start signal should be input on the CDS pin, as shown below. A carrier signal is required for 1.5 seconds, during which there are carrier waves with a period of 10ms including a 6ms pulse wave and a 4ms high level. The 6ms pulse consists of 125μs low levels and 375μs high levels. When a two-cycle carrier signal is detected, the parameter modification mode is entered. If no falling edge is received for more than 10ms after entering the parameter modification mode, it will return to the normal mode.



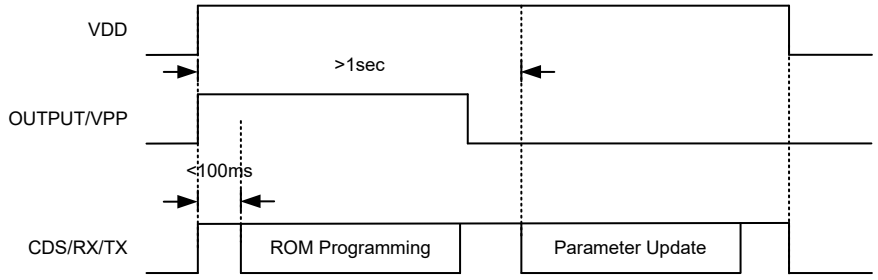
Host Computer Programming Start Pattern

Note: As the OUTPUT is pin-shared with the VPP, special attention should be made to the peripheral circuits above the OUTPUT when performing the OTP programming. Due to the high voltage involved in the OTP programming process, users must carefully check and ensure that all peripheral circuits connected to the OUTPUT pin can safely handle this high voltage. The peripheral circuits could include resistors, capacitors, transistors and other components, which may cause short circuit, over voltage, voltage drop or signal interference during the programming process, thus affecting the programming reliability and accuracy. And confirm whether the voltage withstand of all components is satisfied. Therefore, before the OTP programming, it should ensure that the peripheral circuits are properly configured and meet the programming requirements to avoid any factors that may affect the programming quality.

Communication Write/Read Value Protocol

After entering the host computer mode, the parameter values can be written to Buffer. Each item requires to transmit 4 bytes to be valid, namely ID byte, DATA byte, $\overline{\text{DATA}}$ byte, and check byte. The transmission communication uses single-wire UART with baud rate of 2400.

Timing Point	Function		ID	DATA Byte	$\overline{\text{DATA}}$ Byte	Check Byte
After 1s of power-on	Write Buffer	Sensitivity	1011 1001	DATA	$\overline{\text{DATA}}$	1100 1100
		CDS	1011 0110			
		LVD	1011 1010			
		DT1	1011 0101			
		DT2	1011 1100			
After 1s of power-on	Read Buffer	Sensitivity	0110 1001			
		CDS	0110 0110			
		LVD	0110 1010			
		DT1	0110 0101			
		DT2	0110 1100			
Unlimited	Exit		1010 0101	—	—	—



ROM Programming & Parameter Update Timing

Registers

• OPA Register

Bit	7	6	5	4	3	2	1	0
Name	—	FWUEN	OPA1SW	PGAC4	PGAC3	PGAC2	PGAC1	PGAC0
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	0	0	0	0	0	0	0

Bit 7 Unimplemented, read as "0"

Bit 6 **FWUEN**: Fast warm-up enable bit
0: Disable
1: Enable

Bit 5 **OPA1SW**: OPA1 short switch between inverting input and output control bit
0: Off
1: On

Bit 4 **PGAC4**: OPA1 basic gain control
0: Basic gain=256
1: Basic gain=128

Bit 3~0 **PGAC3~PGAC0**: OPA1 gain control
PGAC4=0:
Gain=256+(PAGC[3:0]×8), V_{DD} @ 2.2V~5.5V
PGAC4=1:
Gain=128+(PAGC[3:0]×8), V_{DD} @ 2.2V~5.5V

• **CDS Register**

Bit	7	6	5	4	3	2	1	0
Name	CDSEN	—	CDS5	CDS4	CDS3	CDS2	CDS1	CDS0
R/W	R/W	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	—	0	0	0	0	0	0

Bit 7 **CDSEN**: CDS enable bit
0: Disable
1: Enable
If the CDS is disabled, the CDS pin will be pulled high internally.

Bit 6 Unimplemented, read as "0"

Bit 5~0 **CDS5~CDS0**: CDS comparison voltage
$V_C=V_{REG}/64\times CDS[5:0]$

• **LVD Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	LVD5	LVD4	LVD3	LVD2	LVD1	LVD0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7~6 Unimplemented, read as "0"

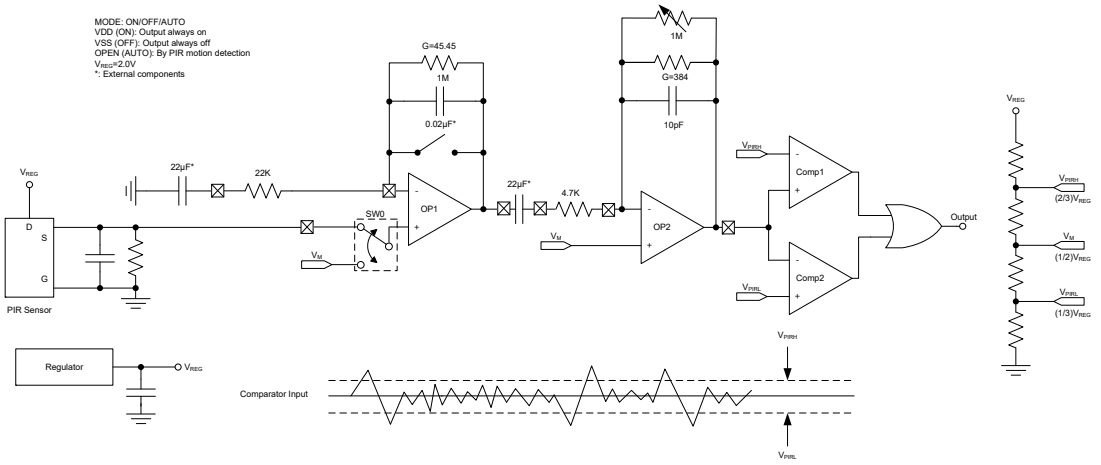
Bit 5~0 **LVD5~LVD**: LVD comparison voltage
$V_L=V_{REG}/64\times LVD[5:0]$

• **DT1 & DT2 Register**

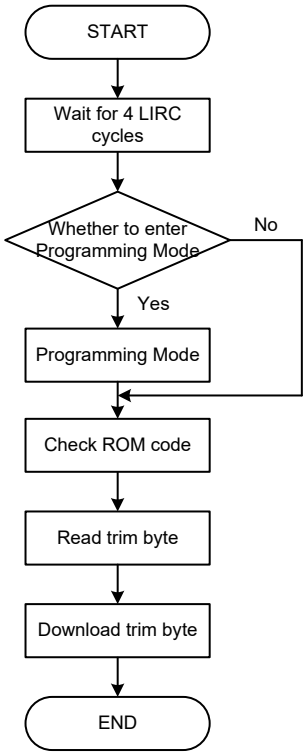
Register	DT2								DT1							
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Name	DT15	DT14	DT13	DT12	DT11	DT10	DT9	DT8	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DT15~DT0: Time delay control
0: Peripheral circuit control
0xFFFF: OUTPUT always high
Others: DT[15:0]×0.5s, upper limit 6 hours

PIR Amplifier

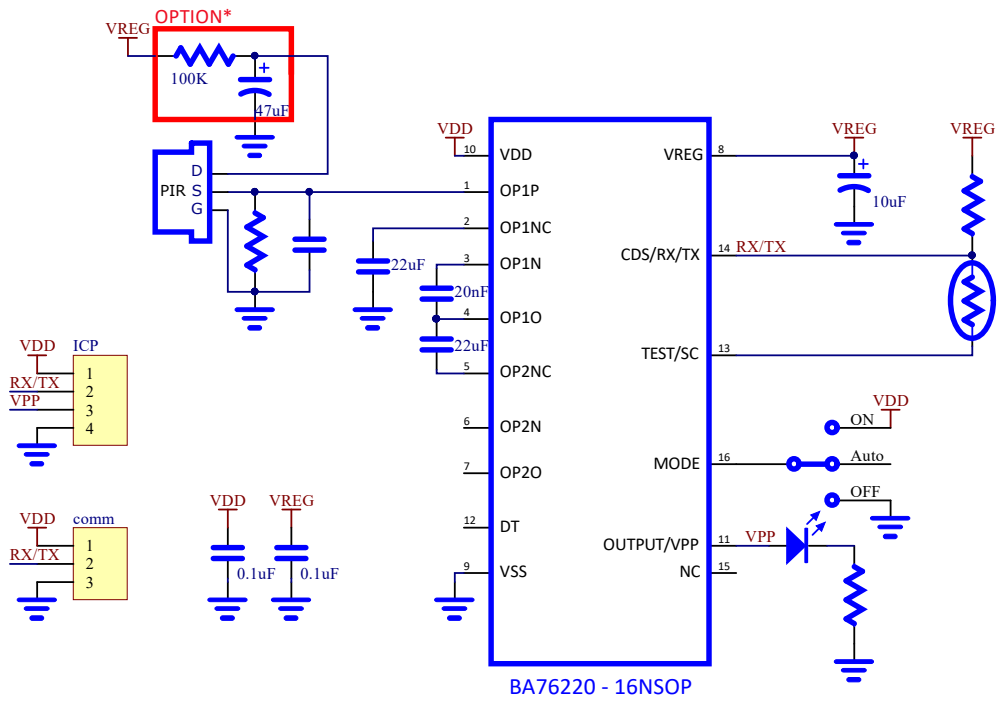


Power-on Flow



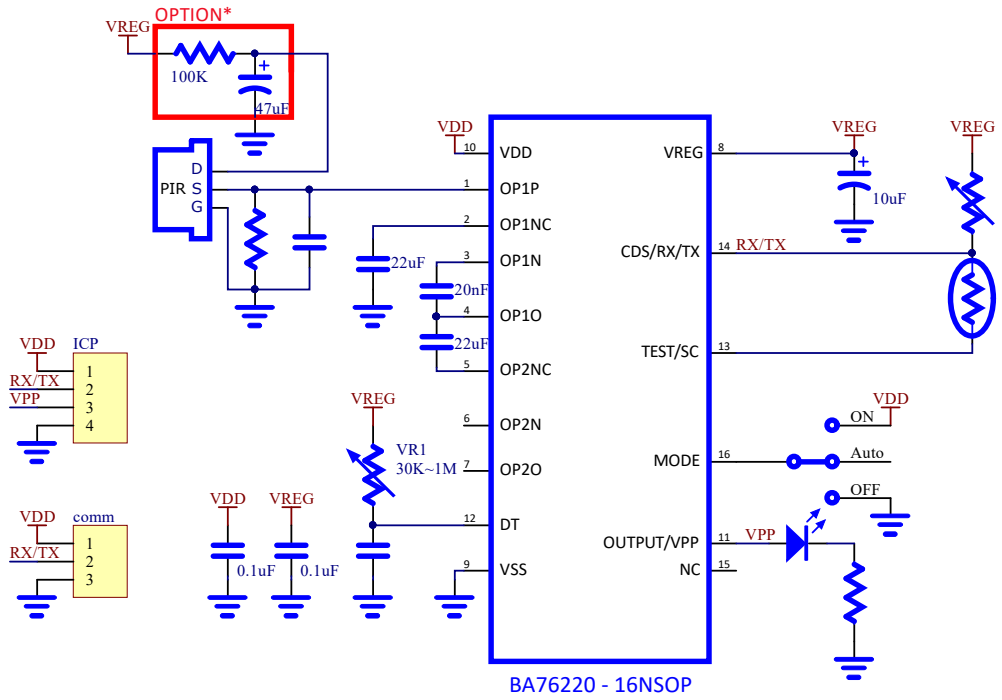
Application Circuits

OTP-based Application Circuit



*: Associated with the system's sensitivity and stability

RC-based Application Circuit



*: Associated with the system's sensitivity and stability

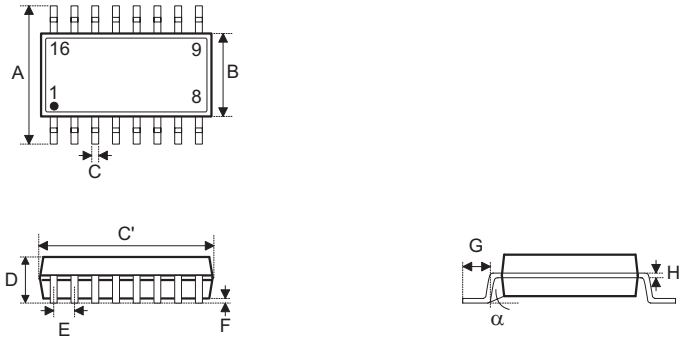
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

16-pin NSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.236 BSC	
B		0.154 BSC	
C	0.012	—	0.020
C’		0.390 BSC	
D	—	—	0.069
E		0.050 BSC	
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		6.00 BSC	
B		3.90 BSC	
C	0.31	—	0.51
C’		9.90 BSC	
D	—	—	1.75
E		1.27 BSC	
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°