Mix-Signal FPGA

Datasheet

Part Number：BAF1000

中国航天

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1. PRODUCT SUMMARIZE

BAF1000 is a mix-signal FPGA device developed by Beijing Microelectronics Technology Institute (BMTI).Based on SIP (System in Package) technology, BAF1000 achieve FPGA, PROM, ADC and DAC circuit connection.BAF1000 can realize analog-to-digital conversion, digital-to-analog conversion and bit stream storage, also common FPGA function. BAF1000 can be applied to data acquisition, signal processing and control field.

BAF1000 support LVTTL/LVCMOS standard for 3.3V application platform. The package is BGA256 in standard fine pitches (1.00 mm). BAF1000 is suitable for temperature range -40℃~85℃.

2. PRODUCT STRUCTURE

BQ2V1000 (FPGA, which is compatible with Virtex-II series XQ2V1000 of Xilinx) is working as control center of BAF1000. BAF1000 integrates a 12 bit D/A module, a 14 bit A/D module and a 4M bit Flash based FPGA configuration module.

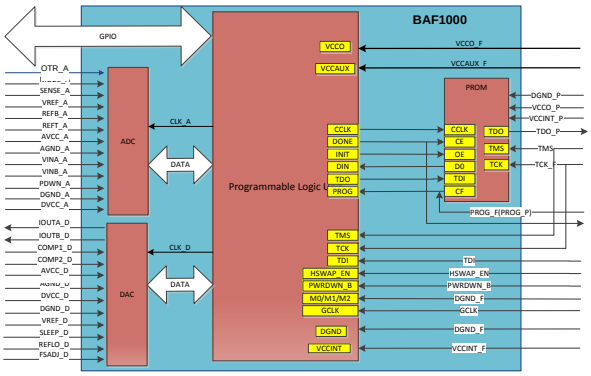


Figure 1 BAF1000 Block Diagram

Figure 2 BAF1000

2.1 Programmable Logic Unit

Programmable Logic Unit is 1M system gates SRAM-based FPGA（BQ2V1000）, As shown in Table 1. BQ2V1000 includes various configurable elements. The architecture is optimized for high-density and high-performance logic designs. As shown in Figure 3, the programmable device is comprised of input/output blocks (IOBs) and internal configurable logic blocks (CLBs).Programmable I/O blocks provide the interface between package pins and the internal configurable logic. Most popular and leading-edge I/O standards are supported by the programmable IOBs.

The internal configurable logic includes four major elements organized in a regular array:

- Configurable Logic Blocks (CLBs) provide functional elements for combinatorial and synchronous logic, including basic storage elements. BUFTs (3-state buffers) associated with each CLB element drive dedicated segmentable horizontal routing resources.
- Block SelectRAM memory modules provide large 18 Kbit storage elements of dual-port RAM.
- Multiplier blocks are 18-bit x 18-bit dedicated multipliers.
- DCM (Digital Clock Manager) blocks provide self-calibrating, fully digital solutions for clock distribution delay compensation, clock multiplication and division, coarse- and

fine-grained clock phase shifting.

A new generation of programmable routing resources called Active Interconnect Technology interconnects all of these elements. The general routing matrix (GRM) is an array of routing switches. Each programmable element is tied to a switch matrix, allowing multiple connections to the general routing matrix. The overall programmable interconnection is hierarchical and designed to support high-speed designs.

All programmable elements, including the routing resources, are controlled by values stored in static memory cells. These values are loaded in the memory cells during configuration and can be reloaded to change the functions of the programmable elements.

Table 1: **Programmable Logic Unit**

System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs
	Array Row xCol.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)	
1M	40 x 32	5,120	160	40	40	720	8

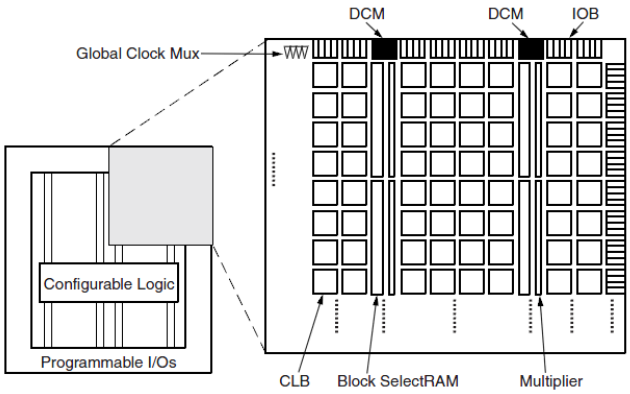


Figure 3 Programmable Logic Unit Architecture Overview

CELL FEATURES

- 1 million equivalent system gate
  - 1.5V (VCCINT) Core Power Supply, Dedicated 3.3V VCCAUX Auxiliary and VCCO I/O Power Supplies
  - 300 MHz internal clock speed (Advance Data)
  - 600 Mb/s I/O (Advance Data)
  - 720Kbit dual-port RAM in 18 Kbit block SelectRAM resources
- SelectIO Technology
  - 19 single-ended and six differential standards
  - Programmable sink current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
- High-Performance Clock Management Circuitry
  - 8 DCM (Digital Clock Manager) modules
    --- Precise clock de-skew
    --- Flexible frequency synthesis

--- High-resolution phase shifting

- 16 global clock multiplexer buffers

■ Arithmetic Functions
- Dedicated 18-bit x 18-bit multiplier blocks
- Fast look-ahead carry logic chains

■ SRAM-Based In-System Configuration
- Unlimited reprogram ability
- Partial reconfiguration
- Readback capability
- IEEE 1149.1 Compatible Boundary-Scan Logic Support

■ Supported by Xilinx ISE

2.2 Configuration And Memory Unit

Configuration and memory unit is a in-system programmable configuration PROM. This 4-megabit PROM provides an easy-to-use, cost-effective method for reprogramming and storing programmable Logic Unit configuration bit streams.

When the Programmable Logic Unit is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after CE and OE are enabled, data is available on the PROM DATA (D0) pin that is connected to the Programmable Logic Unit DIN pin. New data is available in a short access time after each rising clock edge. The Programmable Logic Unit generates the appropriate number of clock pulses to complete the configuration.

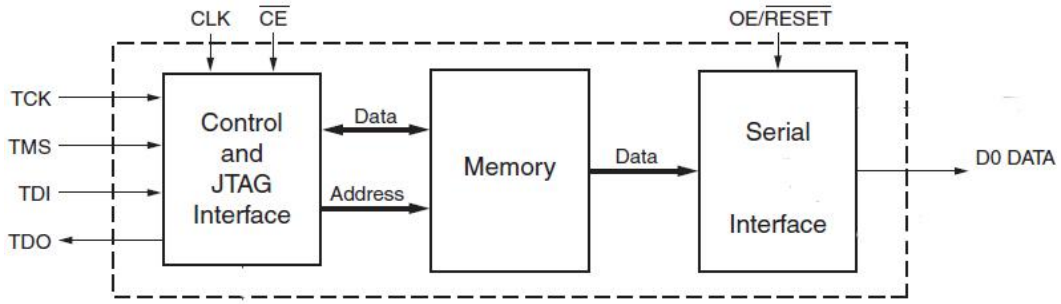


Figure 4 Configuration And Memory Unit Block Diagram

CELL FEATURES

■ In-System Programmable 3.3V PROMs for Configuration of Programmable Logic Unit
- Endurance of 20,000 Program/Erase Cycles
- Program/Erase Over Full Industrial Voltage and Temperature Range (–40 ℃ to +85 ℃)

■ IEEE Std 1149.1 Boundary-Scan (JTAG) Support

■ Low-Power Advanced CMOS FLASH Process

■ Serial Configuration Modes (up to 33MHz)

■ 3.3V Signals and Output Capability

■ Design Support Using the Xilinx ISE Software Packages

2.3 A/D conversion unit

A/D conversion unit is a single 3.3V supply, 12-bit, 30MSPS analog-to-digital converters(ADC). This ADC cell features a high performance sample-and-hold amplifier (SHA)

and voltage reference. The ADC cell uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 30MSPS data rates guaranteed no missing codes over the full operating temperature range.

The wide bandwidth truly differential SHA allows a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage level in successive channels and for sampling single-channel inputs at frequencies which well beyond the Nyquist rate.

A single-ended clock input is used to control all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance. The digital output data is presented in straight binary or twos complement formats. An out-of-range (OTR) signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

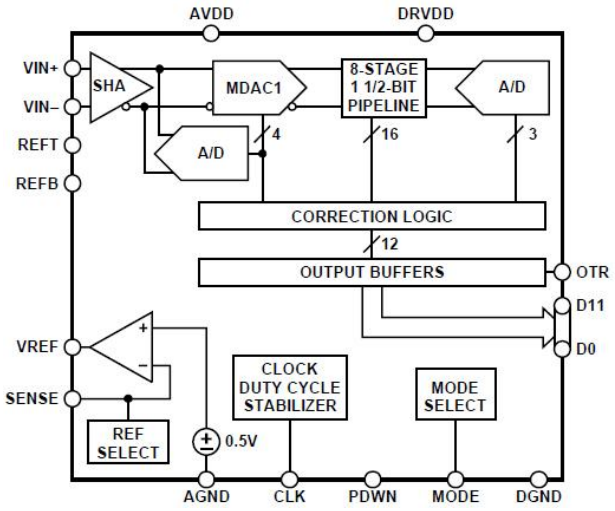


Figure 5 A/D Conversion Unit Functional Block Diagram

CELL FEATURES

- Single 3.3V supply operation (3.0V to 3.6V)
- Differential input with 500MHz bandwidth
- On-chip reference and SHA
- DNL = ±1 LSB
- Flexible analog input: 1V p-p to 2V p-p range
- Offset binary or twos complement data format
- Clock duty cycle stabilizer
- SNR = 52 dBc to Nyquist at 20MSPS
- SFDR = 61 dBc to Nyquist at 20MSPS

2.4 D/A conversion unit

D/A conversion unit is a single 3.3V supply, 14-bit resolution, low power digital-to-analog converter (DAC). This DAC offers exceptional ac and dc performance while supporting update rates up to 50 MSPS.

This DAC cell flexible single-supply operating range of 3.3V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced

to a mere 45mW with a slight degradation in performance by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 25mW.

This DAC cell is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2V temperature compensated band gap reference have been integrated to provide a complete monolithic DAC solution. Flexible supply options support +3.3V CMOS logic families.

This DAC cell is a current-output DAC with a nominal full-scale output current of 20mA and > 100k output impedance. Differential current outputs are provided to support single ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer.

The on-chip reference and control amplifier are configured for maximum accuracy and flexibility. This DAC cell can be driven by the on-chip reference or by a variety of external reference voltages. The internal control amplifier, which provides a wide (>10:1) adjustment span, allows full-scale current to be adjusted over a 2mA to 20mA range while maintaining excellent dynamic performance. Thus, This DAC cell may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

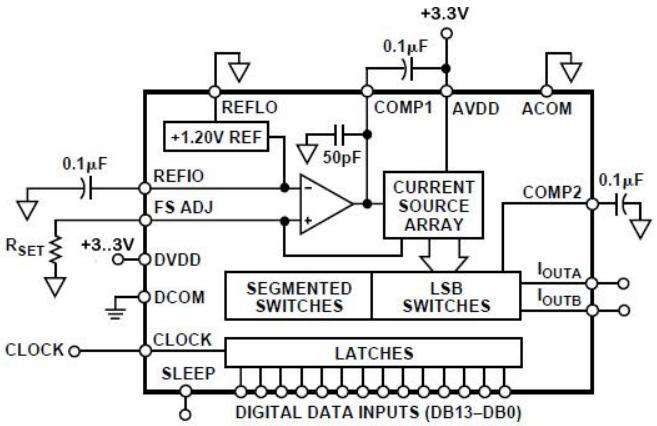
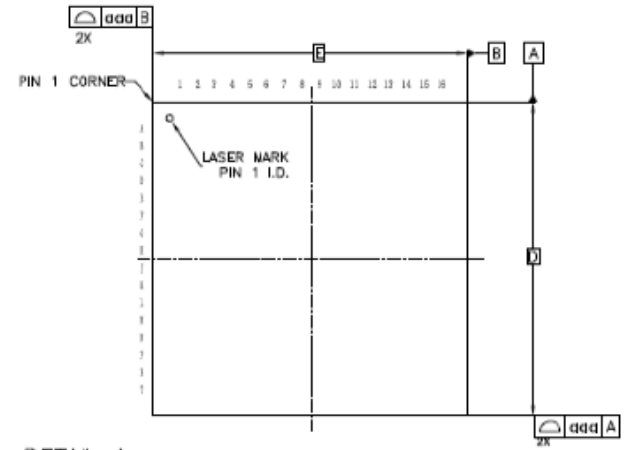


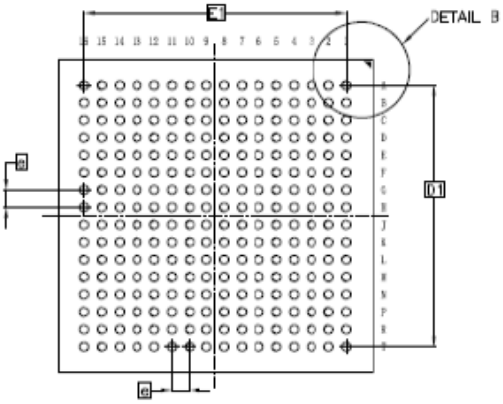
Figure 6 D/A Conversion Unit Functionnal Block Diagram

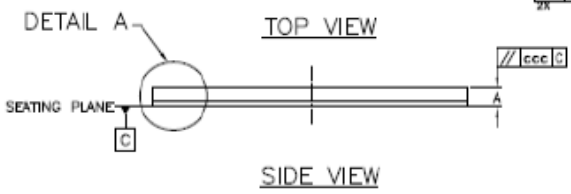
CELL FEATURES

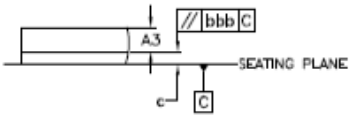
- 50 MSPS Update Rate
- 14-Bit Resolution
- Excellent SFDR and IMD
- Differential Current Outputs: 2mA to 20mA
- On-Chip 1.20 V Reference
- Single +3.3 V Supply Operation
- Edge-Triggered Latches

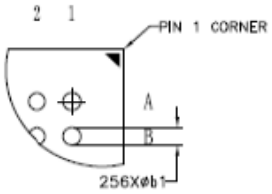
3 BAF1000 Package Specifications











SYMBCL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.12
A3	0.70BASIC		
c	0.32	0.36	0.4
D	17.90	18.00	18.10
D1	15.00BASIC		
E	17.90	18.00	18.10
E1	15.00BASIC		
e	1.00BASIC		
b1	0.47	0.50	0.53
aaa	0.10		
bbb	0.15		
ccc	0.20		

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