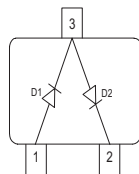
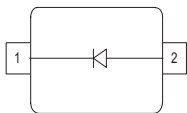


Silicon PIN Diode

- For low loss RF switches and attenuators
- Very low capacitance at zero volt reverse bias at frequencies above 1 GHz (typ. 0.25 pF)
- Low forward resistance (typ. 1.5 Ω @ 5mA)
- Low harmonics
- Pb-free (RoHS compliant) package


BAR67-02V
BAR67-04


Type	Package	Configuration	L_S (nH)	Marking
BAR67-02V	SC79	single	0.6	T
BAR67-04	SOT23	series	1.8	PMs

Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Diode reverse voltage	V_R	150	V
Forward current	I_F	200	mA
Total power dissipation	P_{tot}		mW
$T_S \leq 118^\circ\text{C}$, BAR67-02V		250	
$T_S \leq 25^\circ\text{C}$, BAR67-04		250	
Junction temperature	T_j	150	$^\circ\text{C}$
Operating temperature range	T_{op}	-55 ... 125	
Storage temperature	T_{stg}	-55 ... 150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}		K/W
BAR67-02V		≤ 115	
BAR67-04		≤ 290	

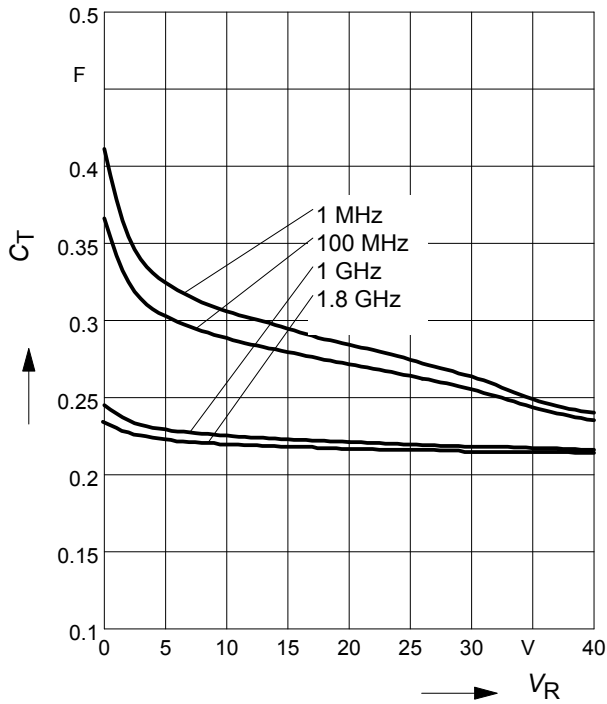
¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Breakdown voltage $I_{(BR)} = 5 \mu\text{A}$	$V_{(BR)}$	150	-	-	V
Reverse current $V_R = 100 \text{ V}$	I_R	-	-	20	nA
Forward voltage $I_F = 50 \text{ mA}$	V_F	-	0.95	1.2	V
AC Characteristics					
Diode capacitance $V_R = 5 \text{ V}, f = 1 \text{ MHz}$ $V_R = 0 \text{ V}, f = 100 \text{ MHz}$ $V_R = 0 \text{ V}, f = 1 \text{ GHz}$ $V_R = 0 \text{ V}, f = 1.8 \text{ GHz}$	C_T	-	0.35	0.55	pF
Reverse parallel resistance $V_R = 0 \text{ V}, f = 100 \text{ MHz}$ $V_R = 0 \text{ V}, f = 1 \text{ GHz}$ $V_R = 0 \text{ V}, f = 1.8 \text{ GHz}$	R_P	-	25	-	k Ω
Forward resistance $I_F = 5 \text{ mA}, f = 100 \text{ MHz}$ $I_F = 10 \text{ mA}, f = 100 \text{ MHz}$	r_f	-	1.5	1.8	Ω
Charge carrier life time $I_F = 10 \text{ mA}, I_R = 6 \text{ mA}$, measured at $I_R = 3 \text{ mA}$, $R_L = 100 \Omega$	τ_{rr}	-	700	-	ns
I-region width	W_I	-	13	-	μm

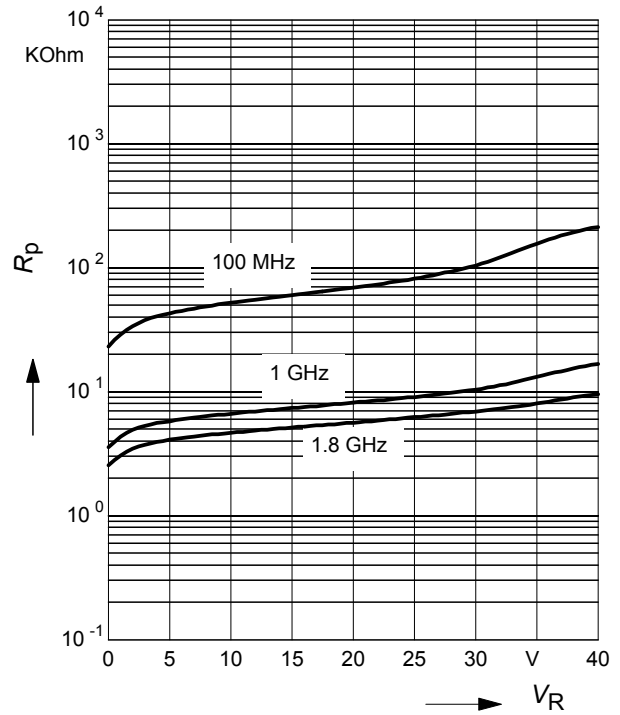
Diode capacitance $C_T = f(V_R)$

$f = \text{Parameter}$



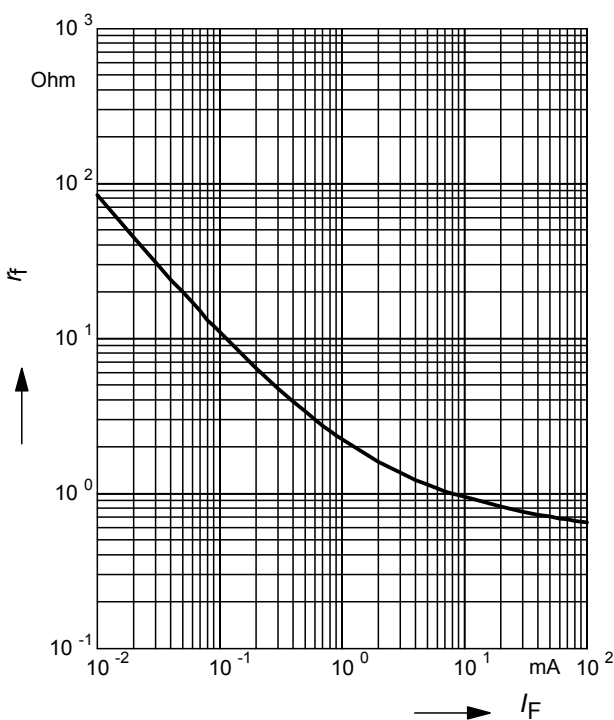
Reverse parallel resistance $R_P = f(V_R)$

$f = \text{Parameter}$



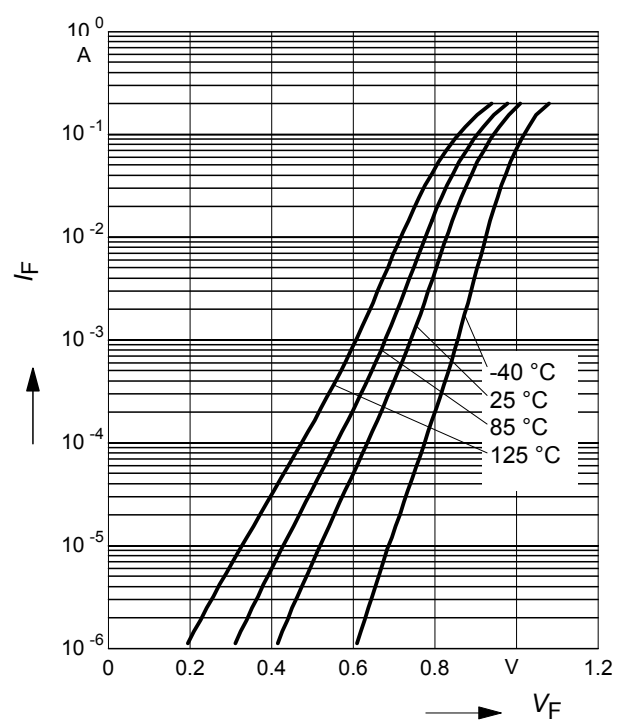
Forward resistance $r_f = f(I_F)$

$f = 100\text{MHz}$



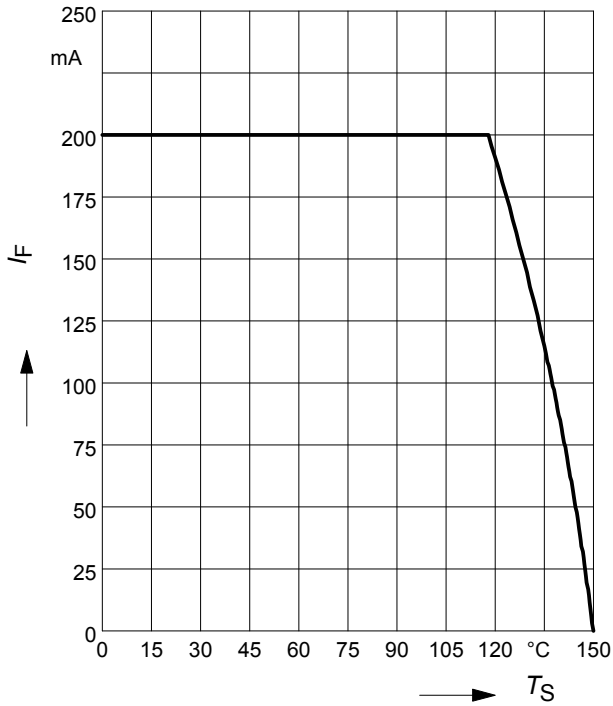
Forward current $I_F = f(V_F)$

$T_A = \text{Parameter}$



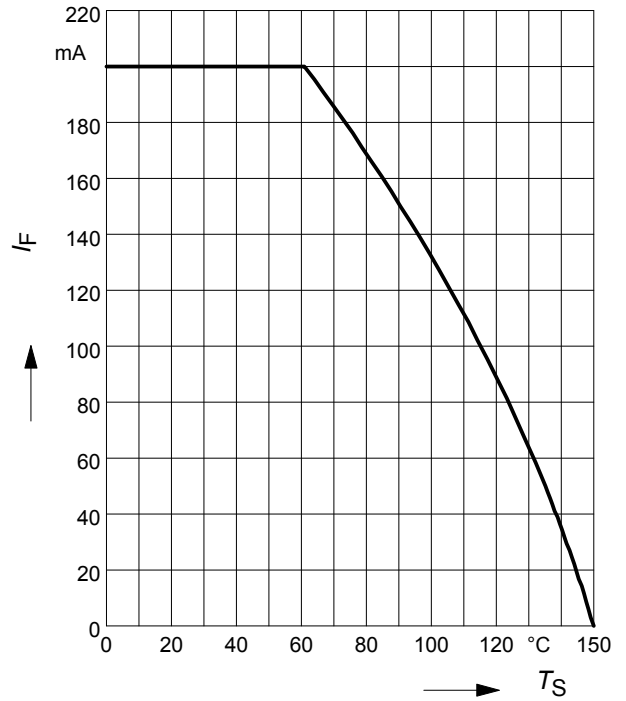
Forward current $I_F = f(T_S)$

BAR67-02V



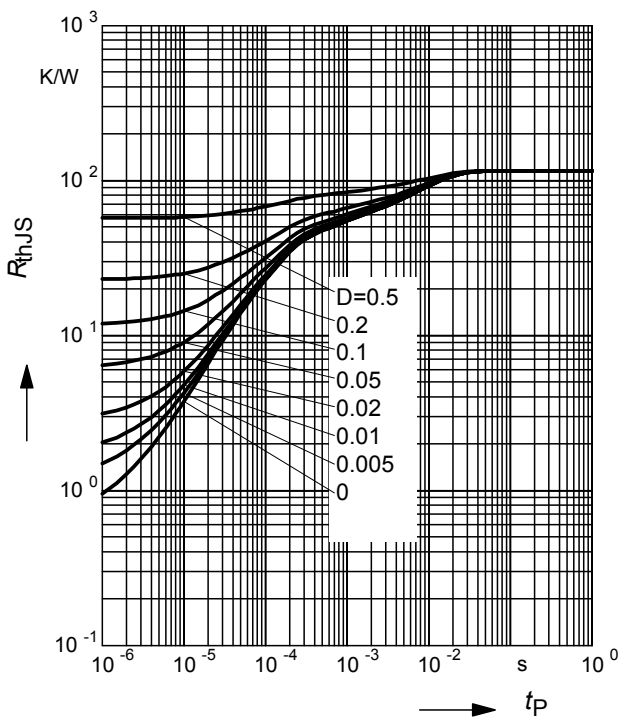
Forward current $I_F = f(T_S)$

BAR67-04



Permissible Puls Load $R_{thJS} = f(t_p)$

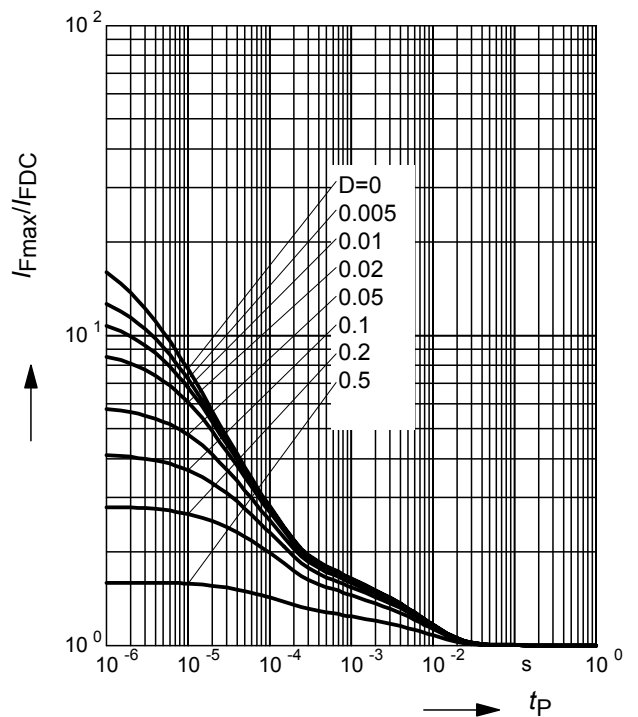
BAR67-02V



Permissible Pulse Load

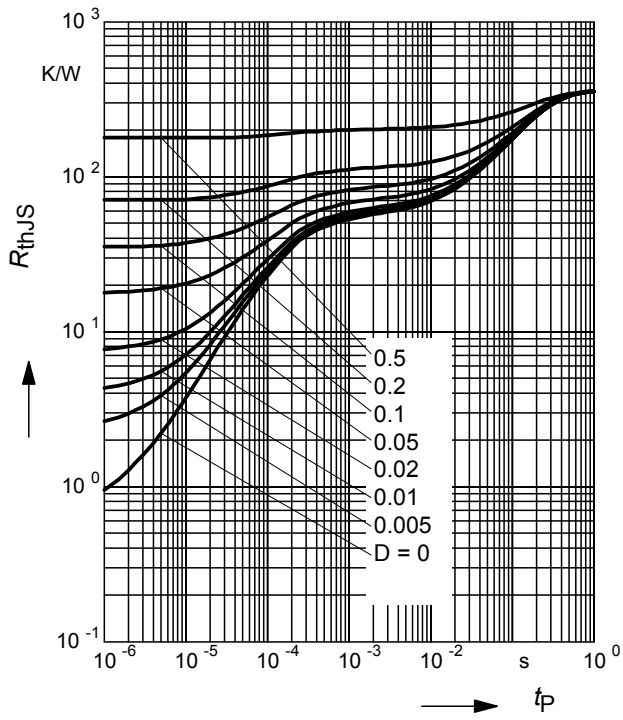
$I_{Fmax} / I_{FDC} = f(t_p)$

BAR67-02V



Permissible Puls Load $R_{thJS} = f(t_p)$

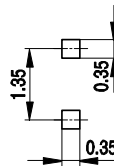
BAR67-04



Package Outline



Foot Print

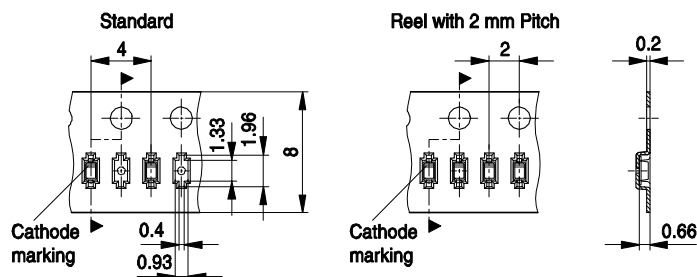


Marking Layout (Example)



Standard Packing

- Reel \varnothing 180 mm = 3.000 Pieces/Reel
- Reel \varnothing 180 mm = 8.000 Pieces/Reel (2 mm Pitch)
- Reel \varnothing 330 mm = 10.000 Pieces/Reel



Date Code marking for discrete packages with one digit (SCD80, SC79, SC75¹⁾) CES-Code

Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

1) New Marking Layout for SC75, implemented at October 2005.

Package Outline



1) Lead width can be 0.6 max. in dambar area

Foot Print



Marking Layout (Example)



Standard Packing

Reel \varnothing 180 mm = 3.000 Pieces/Reel
 Reel \varnothing 330 mm = 10.000 Pieces/Reel



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