BC2161
Sub-1GHz OOK/GFSK Transmitter with Encoder

Features

- Operating voltage: V_{DD}=2.2V~3.6V
- Complete Sub-1GHz OOK/GFSK (BT=0.5) modulation transmitter
- Key input function
  - 2 key inputs for the 8-pin SOP-EP package type
  - 8 key inputs for the 16-pin NSOP-EP package type
- Frequency bands: 315MHz, 433MHz, 868MHz, 915MHz
- Integrated 320-bit FUSE data memory
- Output power of up to 13dBm
- Low sleep current of 0.1μA
- TX current consumption @ 433MHz:
  - TYP. 18.5mA(GFSK, 10dBm)/TYP. 11.2mA (OOK, 10dBm, 50% duty cycle)
- Programmable symbol rate from 1.5ksps to 24ksps for OOK modulation
- Programmable data rate from 2kbps to 125kbps for GFSK modulation
- Integrated full range VCO, loop filter and Fractional-N PLL synthesizer
- Supports 16MHz crystal
- 4-step programmable TX Power: 0/5/10/13 dBm
- FCC / ETSI Compliant
- Small size package types: 8-pin SOP-EP/16-pin NSOP-EP

Abbreviation Notes

TX: RF Transmitter

SX: Synthesizer

PA: Power Amplifier

OOK: On-Off Keying

GFSK: Gaussian Frequency Shift Keying

PLL: Phase Lock Loop

MMD: Multi-Mode Divider

XTAL: External Crystal

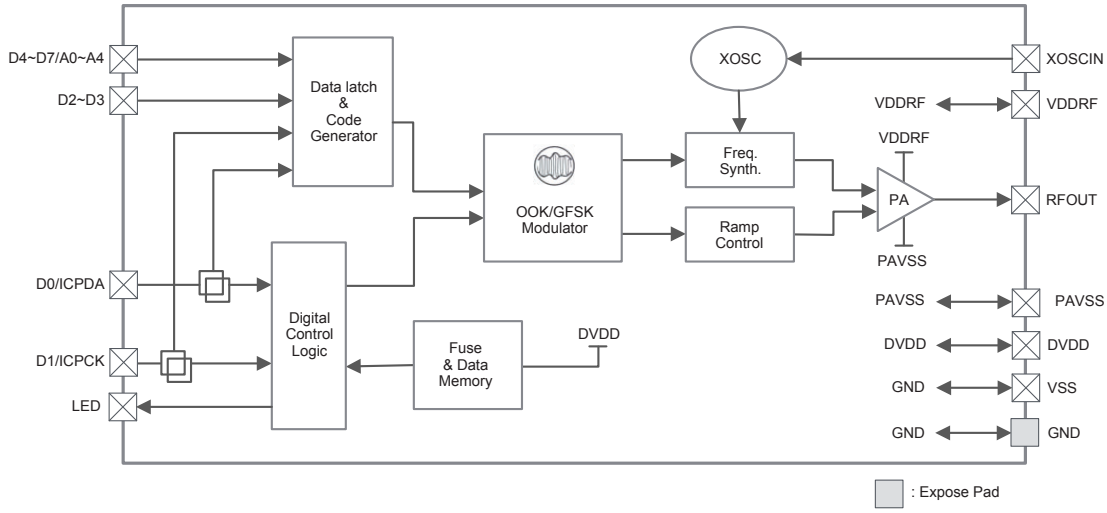
General Description

The BC2161 is a highly integrated OOK/GFSK transmitter for remote wireless applications. The transmitter is a true "data-in, antenna-out" monolithic device making it very easy for users to implement wireless systems.

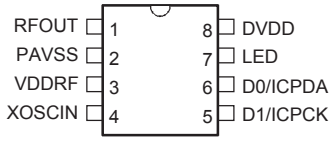
The BC2161 can operate at the 315MHz, 433MHz, 868MHz and 915MHz frequency bands. It supports both OOK and GFSK modulation schemes and can operate with symbol rate of up to 24ksps and data rate of up to 125kbps respectively.

The BC2161 offers a programmable output power level. It is capable of delivering +13dBm maximum power into a 50Ω load. The BC2161 adopts agile state machines to ease the control and minimize the power consumption. With an external crystal and a few external components, the BC2161 can implement a complete solution for an effective RF transmitter.

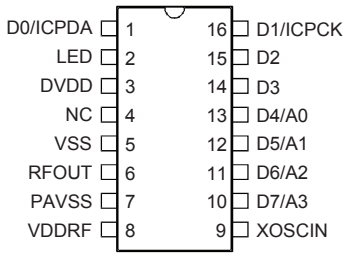
Block Diagram



Pin Assignment



BC2161
8 SOP-EP-A



BC2161
16 NSOP-EP-A

Pin Description

The function of each pin is listed in the following table. Note that where more than one package type exists the table will reflect the situation for the larger package type.

Pin No.	Pin Name	Function	Type	Description
1	D0/ICPDA	D0	I	Data input
		ICPDA	I/O	ICP Data pin
2	LED	LED	O	LED Indicator
3	DVDD	DVDD	PWR	RF Digital positive power supply
4	NC	No connection	—	—
5	VSS	Ground	PWR	Ground
6	RFOUT	PA_OUT	AO	RF output signal from Power Amplifier - Connect to matching circuit
7	PAVSS	VSSRF_PA	PWR	RF ground
8	VDDRF	VDDRF	PWR	Analog positive power supply
9	XOSCIN	Crystal	AI	Crystal input
10~13	D4/A0~D7/A3	D4/A0~D7/A3	I	Compound Pin Data / Address / Key Trigger input
14,15	D2, D3	D2, D3	I	Data input
16	D1/ICPCK	D1	I	Data input
		ICPCK	I	ICP Clock pin
17	GND	Ground	PWR	Expose Pad

Legend: I: Digital Input O: Digital Output
AI: Analog Input AO: Analog Output
PWR: Power

Absolute Maximum Ratings

Supply Voltage .....V_{SS}-0.3V to V_{SS}+3.6V

Voltage on I/O Pins….....V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature .....-55°C to 150°C

Operating Temperature.....-40°C to 85°C

ESD HBM..... ±2kV

* Devices being ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883H Method 3015.8.

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those has listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=3.3V, f_{XTAL}=16MHz, OOK/GFSK modulation with Matching circuit, PAOUT is powered by V_{DD}=3.3V, unless otherwise noted.

Symbol	Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	—	2.2	3.3	3.6	V
T_A	Operating Temperature	—	-40	—	85	°C
T_{FP}	FUSE Program Temperature	—	—	25	—	°C
V_{IH}	High Level Input Voltage	—	$0.7V_{DD}$	—	V_{DD}	V
V_{IL}	Low Level Input Voltage	—	0	—	$0.3V_{DD}$	V
V_{OH}	High Level Output Voltage	@I_{OH}=-5mA	$0.8V_{DD}$	—	V_{DD}	V
V_{OL}	Low Level Output Voltage	@I_{OL}=5mA	0	—	$0.2V_{DD}$	V
	Current Consumptions	I_{Sleep} in the Deep Sleep Mode	—	0.1	—	μA
		I_L Data low & PA off current	—	6.0	—	mA
I_H	Current Consumption @ 315MHz Band (Data=1)	P_{OUT}=0dBm	—	10.5	—	mA
		P_{OUT}=10dBm	—	18.5	—	
		P_{OUT}=13dBm	—	24.5	—	
	Current Consumption @ 433MHz Band (Data=1)	P_{OUT}=0dBm	—	11.0	—	mA
		P_{OUT}=10dBm	—	18.5	—	
		P_{OUT}=13dBm	—	25.0	—	
	Current Consumption @ 868MHz Band (Data=1)	P_{OUT}=0dBm	—	13.5	—	mA
		P_{OUT}=10dBm	—	20.0	—	
		P_{OUT}=13dBm	—	24.5	—	
	Current Consumption @ 915MHz Band (Data=1)	P_{OUT}=0dBm	—	12.5	—	mA
		P_{OUT}=10dBm	—	19	—	
		P_{OUT}=13dBm	—	24	—	

A.C. Characteristics

RF Characteristics

Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
RF						
f_{RF}	RF Operating Frequency Range	—	—	315 433 868 915	—	MHz
XTAL						
f_{XTAL}	RF Operating XTAL Frequency	General case	—	16	—	MHz
ESR	XTAL Equivalent Series Resistance	—	—	—	100	Ω
C_L	XTAL Capacitor Load	—	—	16	—	pF
	XTAL Tolerance[1]	—	—	±20	—	ppm
$t_{Startup}$	XTAL Startup Time[2]	—	—	1	—	ms
PLL						
f_{STEP}	RF Frequency Synthesizer Step	—	—	0.5	—	kHz
PN_{PLL}	PLL Phase Noise @ 433MHz	Phase Noise @ 100k offset	—	-78	—	dBc/Hz
		Phase Noise @ 1M offset		-105		
	PLL Phase noise @ 868MHz	Phase Noise @ 100k offset	—	-68	—	
		Phase Noise @ 1M offset		-100		
f_{DEV}	Frequency Deviation	f_{XTAL}=16MHz	—	50	—	kHz

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
TX						
	Symbol Rate	OOK modulation	1.5	24	—	ksps
	Data Rate	GFSK modulation(@f_{DEV}=12.5kHz)	2	125	—	kbps
P_{OUT}	RF Transmitter Output Power	@ 433MHz	0	—	13	dBm
		@ 868MHz	0	—	13	
ER_{OOK}	OOK Extinction Ratio	OOK Modulation depth	—	70	—	dB
	Occupied Bandwidth (OOK, -20dBc)	@ 315MHz	—	400	—	kHz
		@ 433MHz				
		@ 868MHz				
		@ 915MHz				
SE_{TX}	Transmitter Spurious Emission (P_{OUT}=10dBm)	f < 1GHz	—	—	-36	dBm
		47MHz < f < 74MHz 87.5 MHz < f < 118MHz 174MHz < f < 230MHz 470MHz < f < 790MHz	—	—	-54	
		2^{nd}, 3^{rd} Harmonic	—	—	-30	

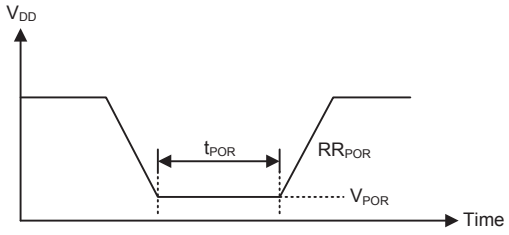
Note: 1. This is the total tolerance including (1)Initial tolerance (2)Crystal loading (3)Aging and (4)Temperature dependence.

2. Depend on crystal property.

Power on Reset Electrical Characteristics

Operating Temperature:-40°C to 85°C Ta=25°C Typical

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{POR}	VDD start voltage to ensure power-on reset	—	—	—	—	100	mV
RR_{POR}	VDD rising rate to ensure power-on reset	—	—	0.035	—	—	V/ms
t_{POR}	Minimum time for VDD stays at VPOR to ensure power-on reset	—	—	1	—	—	ms



Functional Description

This fully integrated RF transmitter can operate in the 315MHz, 433MHz, 868MHz and 915MHz frequency bands. The additional of a crystal and a limited number of external components are all that is required to create a complete and versatile RF transmitter system. The device includes an internal power amplifier and is capable of delivering up to +13dBm. Such a power level enables a small form factor transmitter to operate near the maximum transmission regulation limits. The device can operate with OOK and GFSK receiver types. The GFSK data rate is up to 125kbps, allowing the device to support more complicated control protocols.

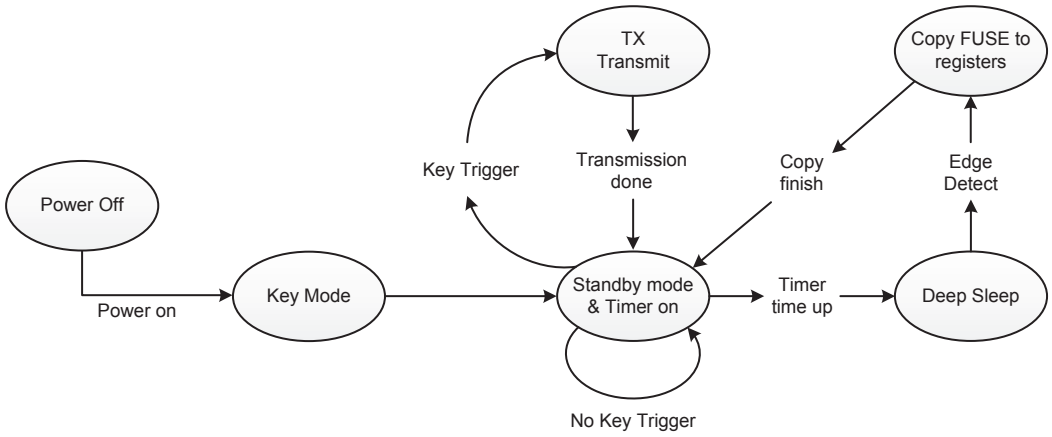
To provide extra user flexibility, the device contains an area of FUSE memory, which is a kind of one-time programmable non-volatile memory. For devices whose FUSE are already programmed, the FUSE memory contents will be copied to the relevant registers automatically. However, the registers will be reset to their initial state when the device is powered off. Note that the Fuse must been programmed before using the IC.

State Control

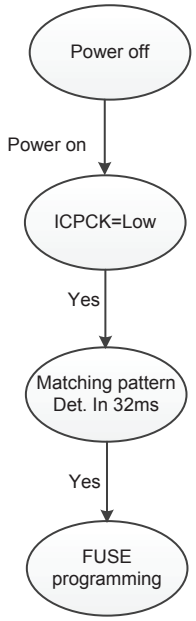
The device has integrated state machines that control the state transition between the different modes.

Key Mode

If users want to enter the key mode, the Fuse must be programmed. During the Standby mode, if there is no key trigger event, the device will enter the Deep Sleep Mode after a 2ms delay. When a key trigger event occurs, which is a level trigger generated by pressing a button for more than 1ms, the transmitter will start to transfer data. The interval between data frames can be figured out using the following equation: 2ms × (FRAME_GAP[2:0]). The transmission will end when the Frame counter stops. The device will then enter the Deep Sleep Mode after a fixed delay time of 2ms. In the Deep Sleep Mode, the clock stops and register configurations from 0x00 to 0x27 will all be reset. The device can only be woken up by an edge detection, which is implemented by pulling the Key pins from high to low. After this happens the FUSE memory will be automatically copied to the relevant registers and the device will enter the Standby mode.



FUSE ICP Mode



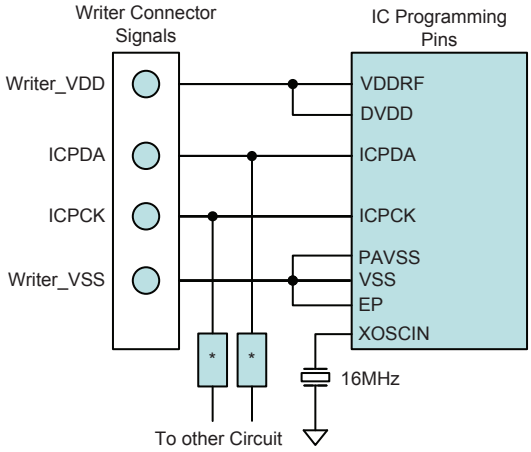
After powering on, the device checks the ICPCK pin state, which is active low but which will be pulled high by the internal pull high function. By adding this procedure, the device can still enter the programming interface to check the programmed value even if it has been programmed. For the 8-pin package applications, it is recommended that the D0 pin should be used as a Key. As the device clock frequency is 16MHz, the device will enter the ICP Mode for FUSE programming after a delay time of 32ms. Note that the FUSE can only be programmed once.

Programming Methodology

The device programming interface should utilise an adaptor with an integrated 16MHz crystal.

Program Function	Pin Name	Pin Description
ICPCK	ICPCK	ICP clock
ICPDA	ICPDA	ICP data /address
VDD	VDDRF, DVDD	Power supply
VSS, EP	PAVSS, VSS, Exposed-Pad	Ground
XTAL IN (Adaptor)	XOSCIN	IC system clock

When programming the device needs to be located on a Socket with a 16MHz crystal connected between pin XOSCIN and ground. Holtek provides an e-link or e-WriterPro tool for communication with the PC. Between the e-link and the device there are four interconnecting lines, namely VDD, VSS, ICPCK and ICPDA pins.



Note: * may be resistor or capacitor - the resistance of * must be greater than 1kΩ and the capacitance of * must be less than 1nF.

Encoder Packet Example – OOK Modulation

Packet Structure:

In the above structure, the procedures enclosed in brackets mean optional and can therefore be disabled. The rest are leading code, address and data, which are necessary parts of the packet. These parameters can be configured but can never be disabled.

Example 1: HT6P20B

Format:

Pilot(24 λ)	Address(22-bit)	Data(2-bit)	End(4-bit)

Pilot code is 24λ → LEAD_CODE[2:0]=000b;

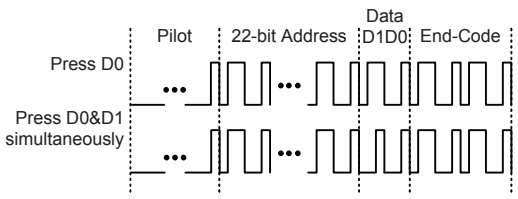
Address: [155555h], Address Length is 22-bit → ADDR_LEN[2:0]=100b;

DATA: 2 Keys (D1/D0) → KEY_SEL[1:0]=00b;

End code is 4-bit → END_CODE[1:0]=01b;

Bit format: Low to High → Waveform=0b ;

→ 1λ low + 2λ high (Data=Zero) / 2λ low + 1λ high (Data=One)



Example 2: HT6P20D

Format:

Pilot(24 λ)	Address(20-bit)	Data(4-bit)	End(4-bit)

Pilot code is 24λ → LEAD_CODE[2:0]=000b;

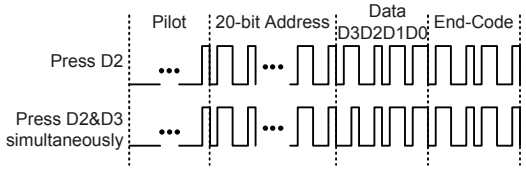
Address: [55555h];Address Length is 20-bit → ADDR_LEN[2:0]=011b;

DATA: 4 Keys (D3/D2/D1/D0) → KEY_SEL[1:0]=01b;

End code is 4-bit → END_CODE[1:0]=01b;

Bit format: Low to High → Waveform=0b;

→ 1λ low + 2λ high (Data=Zero) / 2λ low + 1λ high (Data=One)



Example 3: HT6P427A

Format:

Pilot(32 λ)	Address(20-bit)	Data(4-bit)

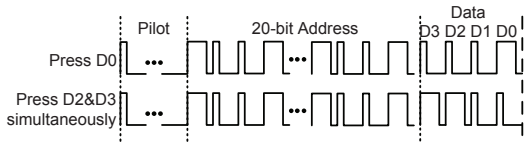
Pilot code is 32λ → LEAD_CODE[2:0]=001b;

Address: [99999h]; Address Length is 20-bit → ADDR_LEN[2:0]=011b;

DATA: 4 Keys (D3/D2/D1/D0) → KEY_SEL[1:0]=01b;

Bit format: High to Low → Waveform=1b;

→ 1λ high + 3λ low (Data=Zero) / 3λ high + 1λ low (Data=One)



Example 4: HT6P437A

Format:

Pilot(32 λ)	Internal Address(20-bit)	External Address(4-bit)	Data(4-bit)

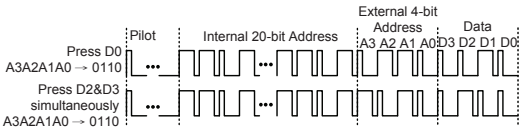
Pilot code is 32λ → LEAD_CODE[2:0]=001b;

Address: [DDDDDh] + Dipswitch; Address Length is 20-bit → ADDR_LEN[2:0]=011b;

DATA: 4 Dipswitches (A3/A2/A1/A0) + 4 Keys (D3/D2/D1/D0) → KEY_SEL[1:0]=10b;

Bit format: High to Low → Waveform=1b;

→ 1λ high + 3λ low (Data=Zero) / 3λ high + 1λ low (Data=One)



Example 5: HT6P237A

Format:

Pilot(24 λ)	Address(22-bit)	Data(2-bit)	End(4-bit)

Pilot code is 24λ → LEAD_CODE[2:0]=000b;

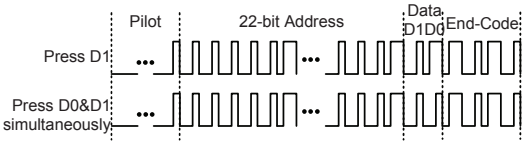
Address: [3EEEEEh]; Address Length is 22-bit → ADDR_LEN[2:0]=100b;

DATA: 2 Keys (D1/D0) → KEY_SEL[1:0]=00b;

End code is 4-bit → END_CODE[1:0]=01b;

Bit format: Low to High → Waveform=0b;

→ 1λ low + 2λ high (Data=Zero) / 2λ low + 1λ high (Data=One)



Example 6: HT6P247A

Format:

Pilot(24 λ)	Address(24-bit)	Data(4-bit)	End(4-bit)

Pilot code is 24λ → LEAD_CODE[2:0]=000b;

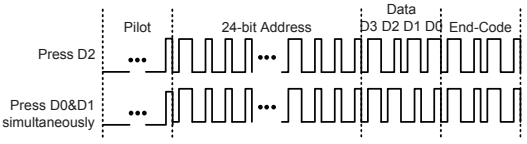
Address: [777777h]; Address Length is 24-bit → ADDR_LEN[2:0]=101b;

DATA: 4 Keys (D3/D2/D1/D0) → KEY_SEL[1:0]=01b;

End code is 4-bit → END_CODE[1:0]=01b;

Bit format: Low to High → Waveform=0b;

→ 1λ low + 2λ high (Data=Zero) / 2λ low + 1λ high (Data=One)



Example 7: HT12E

Format:

Pilot(37 λ)	Address(8-bit)	Data(4-bit)

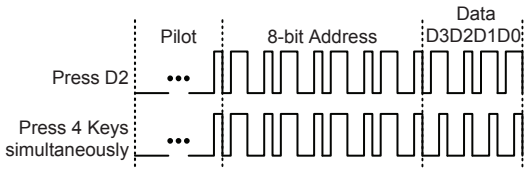
Pilot code is 37λ → LEAD_CODE[2:0]=010b;

Address: [55h]; Address Length is 8-bit → ADDR_LEN[2:0]=000b;

DATA: 4 Keys (D3/D2/D1/D0) → KEY_SEL[1:0]=01b;

Bit format: Low to High → Waveform=0b;

→ 1λ low + 2λ high (Data=Zero) / 2λ low + 1λ high (Data=One)



Example 8: Custom Format

Format:

Preamble (16 λ)	Start (6 λ)	Address (8-bit)	Data (4-bit)	CRC (8-bit)	End (4 λ)

Preamble code is 16λ → LEAD_CODE[2:0]=100b;

Start code is 6λ → START_BIT[1:0]=01b;

Address: [93h]; Address Length is 8-bit → ADDR_LEN[2:0]=000b;

DATA: 4 Keys (D3/D2/D1/D0) → KEY_SEL[1:0]=01b;

CRC: 8-bit → CRC[1:0]=10b;

End Code is 4λ → END_CODE[1:0]=10b;

Bit format: High to Low → Waveform=1b;

→ 1λ high + 3λ low (Data=Zero) / 3λ high + 1λ low (Data=One)

Encoder Packet Example – GFSK Modulation

The BC2161 transmitter can operates together with the BC3601 receiver.

Packet Format:

Preamble	SyncWord	Trailer	Data (1Byte)	CRC

The packet contains 76-bits in total, in which only the SyncWord occupies the FUSE memory space. The data is sourced from the keys.

Functional	Bit	Description	Compare the BC3601
Preamble	16 (Default)	Does not occupy the FUSE space	Preamble
Syncword	32	Occupies the FUSE space	Syncword
Trailer	4	Does not occupy the FUSE space	Trailer
Data	8	Does not occupy the FUSE space	Data
CRC	16	Does not occupy the FUSE space	CRC

Preamble:

The transmission format is fixed by repeating the data "10101010…", the wave ratio of DATA "1" and DATA "0" is 1:1. The preamble bit number can be determined by the FSK_PRMB_SE[1:0] bits in the CFG16 register, it is preset to 2 bytes by default.

Syncword:

Users can setup the Syncword using the FUSE, the bit number is fixed at 32-bits.

Trailer:

The Trailer is an internal fixed format in the device, users do not have to setup this part.

CRC:

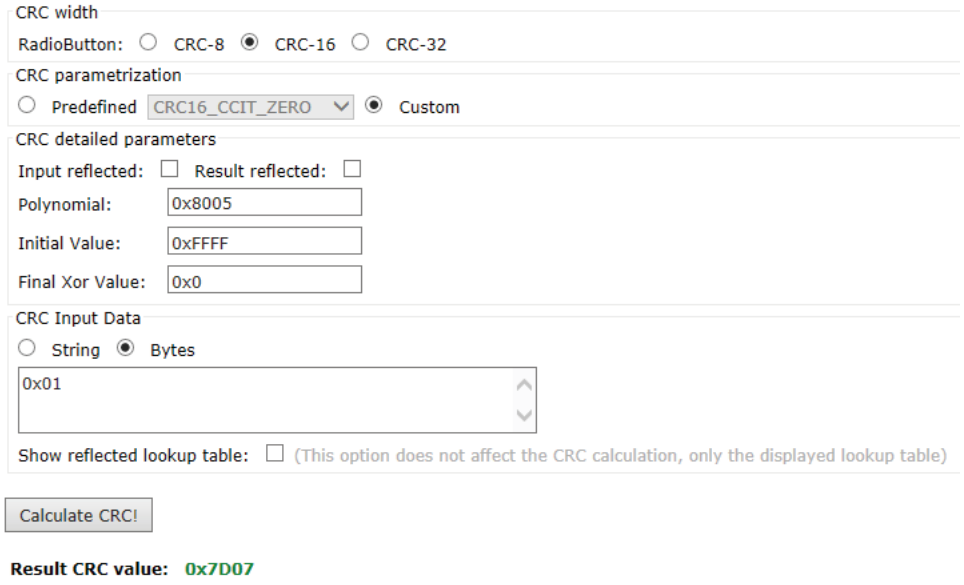
The CRC on-line calculator can be accessed by the following website : http://www.sunshine2k.de/coding/javascript/crc/crc_js.html

For example GFSK Data(1 byte) is 0x01

The on-line calculator should be setup with the following configuration:

1. CRC width : select CRC-16
2. CRC parametrization : select “Custom”
3. Polynomial : 0x8005
4. Initial Value : 0xFFFF
5. Final Xor Value : 0x0
6. CRC Input Data : select Bytes, and fill in data
7. Click on “Calculate CRC!”
8. Result CRC Value : 0x7D07

As the following on-line calculator web interface screenshot shows:



Note:

Preamble	Sync_wordL	Sync_wordM	Sync_wordH	Sync_wordU	Trailer
1010···10	Bit7~Bit0	Bit7~Bit0	Bit7~Bit0	Bit7~Bit0	1010

Preamble format will follow Sync_wordL bit 7 to inverse.

If bit 7=0, Preamble format=0101…01

If bit 7=1, Preamble format=1010…10

Trailed format will follow Sync_wordU bit 0 to inverse.

If bit 0=0, Trailer format=1010

If bit 1=1, Trailer format=0101

Fuse Register Map

This list provides a summary of all internal registers. Their detailed operation is described under their relevant section in the functional description.

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
00h	CFG0	Reserved	EFPGM	XO_TRIM[5:0]					
01h	CFG1	FRAME_GAP[2:0]			Reserved				
02h	CFG2	FDEV[7:0]							
03h	CFG3	FSK_EN	Reserved						
04h	CFG4	Reserved							
05h	CFG5	Reserved							
06h	CFG6	Reserved							
07h	CFG7	Reserved							
08h	CFG8	Reserved							
09h	CFG9	Reserved							
0Ah	CFG10	D_K[3:0]				TXPWR[3:0]			
0Bh	CFG11	D_N[5:0]						BAND_SEL[1:0]	
0Ch	CFG12	D_K[11:4]							
0Dh	CFG13	D_K[19:12]							
0Eh	CFG14	BIT_WIDTH[4:0]					LEAD_CODE[2:0]		
0Fh	CFG15	ADDR_LEN[2:0]			END_CODE[1:0]		START_BIT[1:0]		Waveform
10h	CFG16	Reserved		FSK_PRMB_SEL[1:0]		CRC_SEL[1:0]		KEY_SEL[1:0]	
11h	CFG17	SYNC_WORDL[7:0]							
12h	CFG18	SYNC_WORDM[7:0]							
13h	CFG19	SYNC_WORDH[7:0]							
14h	CFG20	SYNC_WORDU[7:0]							
15h	CFG21	ENCODR_ADDRL[7:0]							
16h	CFG22	ENCODR_ADDRM[7:0]							
17h	CFG23	ENCODR_ADDRH[7:0]							
18h	CFG24	ENCODR_ADDRU[7:0]							
19h	CFG25	FRAME_CNTR[7:0]							
1Ah	CFG26	DTR[7:0]							
1Bh	CFG27	Reserved						DTR[9:8]	
1Ch	CFG28	Reserved	TXD_INV	TXD_REV	LED_SWD	Reserved			
1Dh	CFG29	Reserved							
1Eh	CFG30	MAX_FCNT[7:0]							
1Fh	CFG31	EFCRC_L[7:0]							
20h	CFG32	EFCRC_H[7:0]							
21h	CFG33	Reserved							TX_FLAG
22h	CFG34	Reserved							
23h	CFG35	Reserved							
24h	CFG36	Reserved							
25h	CFG37	Reserved							
26h	CFG38	Reserved							
27h	CFG39	Reserved							

If the Fuse is un-programmed, the BC2161 device will have a default state, determined by register initial values.

Modulation Mode: OOK

Operating Frequency: 433.92MHz

TX Output Power: 10dBm

XTAL Capacitor Load: 16.32pF

Encoding Format: HT6P427A

Symbol Rate: 4ksps

- **CFG0: Configuration Control Register 0**

Address	Bit	7	6	5	4	3	2	1	0
00h	Name	Reserved	EFPGM	XO_TRIM[5:0]					
	R/W	R/W	R	R/W					
	Initial Value	1	0	1	0	1	0	0	1

Bit 7 Reserved, must be [0b1]

Bit 6 **EFPGM**: FUSE programmed, read only by the Holtek RF Tool

0: Fuse is not programmed – FUSE data is not mapped to the configuration registers

1: Fuse is programmed – FUSE data is mapped to the configuration registers

Bit 5~0 **XO_TRIM[5:0]**: Trim the internal capacitor load value for the crystal

XO_TRIM[5:0]	Equiv. C_L (pF)
0	9.87
4	10.00
8	10.12
12	11.44
16	12.16
17	12.33
18	12.49
20	12.83
24	13.50
28	14.15

XO_TRIM[5:0]	Equiv. C_L (pF)
32	14.85
36	15.48
40	16.16
44	16.81
48	17.49
52	18.07
56	18.67
60	19.20
63	19.61

- **CFG1: Configuration Control Register 1**

Address	Bit	7	6	5	4	3	2	1	0
01h	Name	FRAME_GAP[2:0]			Reserved	Reserved			
	R/W	R/W			R/W	R/W			
	Initial Value	0	0	0	0	0	0	0	1

Bit 7~5 **FRAME_GAP[2:0]**: TX frame interval time

t=2ms × (FRAME_GAP[2:0])

000: 0ms

001: 2ms

010: 4ms

011: 6ms

100: 8ms

101: 10ms

110: 12ms

111: 14ms

This configuration is applied to OOK and GFSK modulation simultaneously.

Bit 4 Reserved bit

Bit 3~0 Reserved, must be [0b0001]

- **CFG2: Configuration Control Register 2**

Address	Bit	7	6	5	4	3	2	1	0
02h	Name	FDEV[7:0]							
	R/W	R/W							
	Initial Value	1	0	1	1	0	1	1	0

Bit 7~0 **FDEV[7:0]**: Frequency Deviation for FSK (Follow the BC3601 receiver)
This bit filed value can be calculated using the equation FDEV[7:0]=round [(h × fs × 2^{15})/f_{XTAL}], where h=(2×f_{DEV})/fs, fs means data rate.
For example: If data rate=10kbps, $f_{DEV=}$25kHz, then h=(2×25k)/10k=5,
FDEV[7:0]=round [(5 × 10k× 2^{15})/16M]=102=0x66

- **CFG3: Configuration Control Register 3**

Address	Bit	7	6	5	4	3	2	1	0
03h	Name	FSK_EN	Reserved						
	R/W	R/W	R/W						
	Initial Value	0	1	0	0	0	0	0	1

Bit 7 **FSK_EN**: GFSK modulation mode enable control
0: OOK modulation
1: GFSK modulation

Bit 6~0 Reserved, must be [0b1000001]

- **CFG4: Configuration Control Register 4**

Address	Bit	7	6	5	4	3	2	1	0
04h	Name	Reserved							
	R/W	R/W							
	Initial Value	0	1	0	0	0	0	1	0

Bit 7~0 Reserved, must be [0b01000010]

- **CFG5: Configuration Control Register 5**

Address	Bit	7	6	5	4	3	2	1	0
05h	Name	Reserved							
	R/W	R/W							
	Initial Value	0	0	0	1	0	1	0	1

Bit 7~0 Reserved, must be [0b00010101]

- **CFG6: Configuration Control Register 6**

Address	Bit	7	6	5	4	3	2	1	0
06h	Name	Reserved							
	R/W	R/W							
	Initial Value	1	0	0	1	1	0	0	1

Bit 7~0 Reserved, must be [0b10011001]

- **CFG7: Configuration Control Register 7**

Address	Bit	7	6	5	4	3	2	1	0
07h	Name	Reserved							
	R/W	R/W							
	Initial Value	1	1	0	1	0	1	0	0

Bit 7~0 Reserved, must be [0b11010100]

- **CFG8: Configuration Control Register 8**

Address	Bit	7	6	5	4	3	2	1	0
08h	Name	Reserved							
	R/W	R/W							
	Initial Value	1	0	1	0	0	0	1	0

Bit 7~0 Reserved, must be [0b10100010]

- **CFG9: Configuration Control Register 9**

Address	Bit	7	6	5	4	3	2	1	0
09h	Name	Reserved							
	R/W	R/W							
	Initial Value	0	1	0	1	0	1	0	1

Bit 7~0 Reserved, must be [0b01010101]

- **CFG10: Configuration Control Register10**

Address	Bit	7	6	5	4	3	2	1	0
0Ah	Name	D_K[3:0]				TXPWR[3:0]			
	R/W	R/W				R/W			
	Initial Value	0	0	1	1	1	0	0	0

Bit 7~4 **D_K[3:0]**: Fractional of dividend for MMD, which will be described later.

Bit 3~0 **TXPWR[3:0]**: RF output power stage selection

The device has several output power values which are 0, 5, 10 and 13dBm.

TXPWR[3:0]	RF Output Power (Typ.)
0000	0dBm
0100	5dBm
1000	10dBm
1100	13dBm

TXPWR[3:0]	Fine Tune Level (Typ.)
XX00	0
XX01	1
XX10	2
XX11	3

Note that the adjust range: Level 3 > Level 2 > Level 1 > Level 0

- **CFG11: Configuration Control Register11**

Address	Bit	7	6	5	4	3	2	1	0
0Bh	Name	D_N[5:0]						BAND_SEL[1:0]	
	R/W	R/W						R/W	
	Initial Value	0	1	0	1	1	0	0	1

Bit 7~2 **D_N[5:0]**: Integer of dividend for MMD

Bit 1~0 **BAND_SEL[1:0]**: Band Frequency Coarse Selection

BAND_SEL	Frequency	Divider
00	315MHz	2
01	433MHz	2
10	868MHz	1
11	915MHz	1

Note that the BAND_SEL only selects an approximate frequency range while the exact frequency value is determined by the D_N and D_K bit fields. For example, the 433.92MHz belongs to 433MHz frequency band in the BAND_SEL setting.

- **CFG12: Configuration Control Register12**

Address	Bit	7	6	5	4	3	2	1	0
0Ch	Name	D_K[11:4]							
	R/W	R/W							
	Initial Value	0	1	1	1	0	0	0	0

- **CFG13: Configuration Control Register13**

Address	Bit	7	6	5	4	3	2	1	0
0Dh	Name	D_K[19:12]							
	R/W	R/W							
	Initial Value	0	0	1	1	1	1	0	1

D_K[19:0]: 20-bit fractional of dividend for MMD

For example: XO=16MHz and TX frequency band=433MHz

1. For D_N field, (433M×Divider)/16M=54.125,

   Take the integer part → D_N[5:0]=54-32=22=010110b

2. For D_K field, (433M×Divider)/16M=54.125,

   Take the fractional part → D_K[19:0]=0.125 × 2^{20}=131072=0010-0000-0000-0000-0000b

Frequency	Divider	X'TAL	D_N[5:0]	D_K[19:4]	D_K[3:0]
315MHz	2	16MHz	000111	0110-0000-0000-0000	0000
433MHz	2	16MHz	010110	0010-0000-0000-0000	0000
433.92MHz	2	16MHz	010110	0011-1101-0111-0000	1010
868MHz	1	16MHz	010110	0100-0000-0000-0000	0000
915MHz	1	16MHz	011001	0011-0000-0000-0000	0000

- **CFG14: Configuration Control Register14**

Address	Bit	7	6	5	4	3	2	1	0
0Eh	Name	OOK Bit Rate[4:0]					LEAD_CODE[2:0]		
	R/W	R/W					R/W		
	Initial Value	0	0	1	0	1	0	0	1

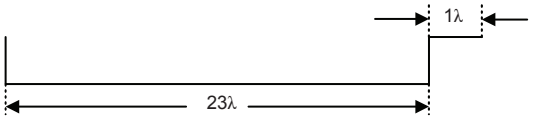
Bit 7~3 **OOK Bit Rate[4:0]**: Define the data bit rate (0.5k~6kbps)

OOK Bit Rate	Data Rate	t_{DW}
00000	0.5kbps	2ms
00001	0.6kbps	1.67ms
00010	0.7kbps	1.43ms
00011	0.8kbps	1.25ms
00100	0.9kbps	1.11ms
00101	1.0kbps	1ms
00110	1.1kbps	0.91ms
00111	1.2kbps	0.83ms
01000	1.3kbps	0.77ms
01001	1.4kbps	0.72ms
01010	1.5kbps	0.667ms
01011	1.6kbps	0.625ms
01100	1.7kbps	0.59ms
01101	1.8kbps	0.55ms
01110	1.9kbps	0.53ms
01111	2.0kbps	0.5ms

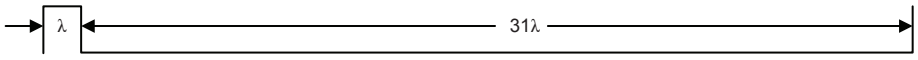
OOK Bit Rate	Data Rate	t_{DW}
10000	2.1kbps	0.476ms
10001	2.2kbps	0.454ms
10010	2.3kbps	0.434ms
10011	2.4kbps	0.416ms
10100	2.5 kbps	0.4ms
10101	2.6kbps	0.384ms
10110	2.7kbps	0.37ms
10111	2.8kbps	0.357ms
11000	2.9kbps	0.344ms
11001	3.0kbps	0.333ms
11010	3.5kbps	0.285ms
11011	4.0kbps	0.25ms
11100	4.5kbps	0.222ms
11101	5.0kbps	0.2ms
11110	5.5kbps	0.181ms
11111	6.0kbps	0.166ms

Bit 2~0 **LEAD_CODE[2:0]**: Define the lead code

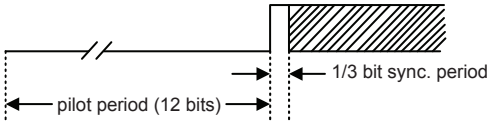
000: 23λLow + 1λHigh (HT6P20B/HT6P2x7A)



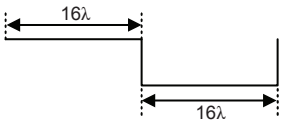
001: 1λHigh + 31λLow (HT6P4x7A)



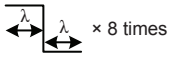
010: 36λLow + 1λHigh (HT12E)



011: 16λHigh+ 16λLow



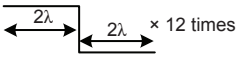
100: (1λHigh + 1λLow) × 8 times, 16 symbols in total



101: (2λHigh + 2λLow) × 8 times, 16 symbols in total

110: (1λHigh + 1λLow) × 12 times, 24 symbols in total

111: (2λHigh + 2λLow) × 12 times, 24 symbols in total



- **CFG15: Configuration Control Register15**

Address	Bit	7	6	5	4	3	2	1	0
0Fh	Name	ADDR_LEN[2:0]			END_CODE[1:0]		START_BIT[1:0]		Waveform
	R/W	R/W			R/W		R/W		R/W
	Initial Value	0	1	1	0	0	0	0	1

Bit 7~5 **ADDR_LEN[2:0]**: Define the address length

ADDR_LEN	Format
000 (HT12E)	8 bits
001	12 bits
010	16 bits
011 (HT6P427A)	20 bits
100 (HT6P20B, HT6P237A)	22 bits
101 (HT6P247A, HT6P437A)	24 bits
110	28 bits
111	32 bits

Bit 4~3 **END_CODE[1:0]**: Define the End code

END_CODE	Format
00	Disable
01 (HT6P20B, HT6P237A, HT6P247A)	(1λ Low + 2λ High + 2λ Low + 1λ High) × 2=(12λ)
10	4λ (Note 1)
11	2λ + 2λ (Note 2)

Notes:

1. The high or low level of the 4λ END_CODE is the opposite of the previous symbol level.
   - Example 1: Clear the Waveform to "0", no matter that whether the data is "1" or "0", the last symbol will be High, here the 4λ must be 4λ Low.

Pilot(24 λ)	Address(22-bit)	Data(2-bit)	End(4 λ)

Pilot code is 24λ → LEAD_CODE[2:0]=000b;

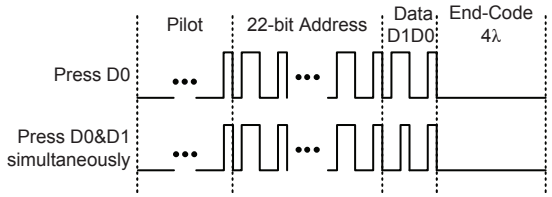
Address: [155555h]; Address length is 22-bit → ADDR_LEN[2:0]=100b;

DATA: 2 Keys (D1/D0) → KEY_SEL[1:0]=00b;

End code is 4-bit → END_CODE[1:0]=10b;

Bit format: Low to High → Waveform=0b;

1λ Low + 2λ High (Data=Zero) / 2λ Low + 1λ High (Data=One)



- Example 2: Set the Waveform to "1", no matter whether the data is "1" or "0", the last symbol will be Low, here the 4λ must be 4λ High.

2. 2λ + 2λ: these two 2λ are opposite to each other, while the high or low level of the first 2λ is opposite to the previous symbol level.

- Example 1: Clear the Waveform to "0", no matter whether the data is "1" or "0", the last symbol will be High, and here the 2λ + 2λ must be 2λ Low + 2λ High.

Pilot(24 λ)	Address(22-bit)	Data(2-bit)	End(2 λ+2 λ)

Pilot code is 24λ → LEAD_CODE[2:0]=000b;

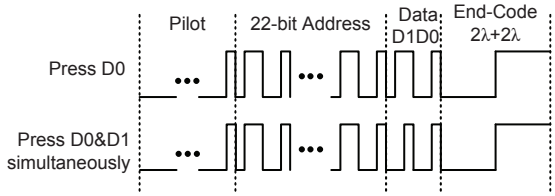
Address: [155555h]; Address length is 22-bit → ADDR_LEN[2:0]=100b;

DATA: 2 Keys (D1/D0) → KEY_SEL[1:0]=00b;

End code is 4-bit → END_CODE[1:0]=11b;

Bit format: Low to High → Waveform=0b;

1λ Low + 2λ High (Data=Zero) / 2λ Low + 1λ High (Data=One)

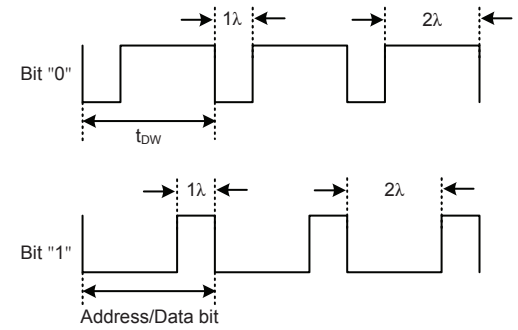


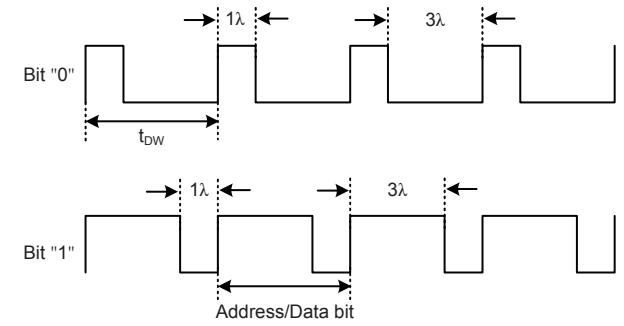
- Example 2: Set the Waveform to "1", no matter that the data is "1" or "0", the last symbol will be Low, and here the 2λ + 2λ must be 2λ High + 2λ Low.

Bit 2~1 **START_BIT[1:0]**: Only for OOK Encoder

START_BIT	Format
00	Disable
01	(2λ Low + 4λ High)
10	(4λ High + 2λ Low)
11	6λ Low

Bit 0 **Waveform**:

Waveform	Format
0 (HT6P20B, HT12E, HT6P2x7A)	Low to High  1λ low + 2λ high (data=Zero) 2λ low + 1λ high (data=One)

Waveform	Format
1 (HT6P4x7A)	High to Low  1λ high + 3λ low (data=Zero) 3λ high + 1λ low (data=One)

- **CFG16: Configuration Control Register16**

Address	Bit	7	6	5	4	3	2	1	0
10h	Name	Reserved		FSK_PRMB_SE[1:0]		CRC_SEL[1:0]		KEY_SEL[1:0]	
	R/W	R/W		R/W		R/W		R/W	
	Initial Value	0	1	0	0	0	0	0	1

Bit 7~6 Reserved, must be [0b01]

Bit 5~4 **FSK_PRMB_SE[1:0]**: Only for GFSK mode

00: 2 bytes

01: 4 bytes

10: 6 bytes

11: 8 bytes

Bit 3~2 **CRC_SEL[1:0]**: Select the address + data for CRC processing

The unit is Bit (not λ), the address is used as the high order of CRC polynomial and the data is used as the low order.

CRC_SEL	Format	Polynomial	Initial Value	Note
00	Disable	—	—	OOK/GFSK
01	4 Bits → Take the low nibble of the CRC8 calculated result	—	—	OOK
10	8 Bits → $X^8 + X^5 + X^4 + 1$	0x31	0x00	OOK
11	16 Bits → $X^{16} + X^{15} + X^2 + 1$	0x8005	0xFFFF	GFSK

Bit 1~0 **KEY_SEL[1:0]**

KEY_SEL	Format	Data bits
00	2 Keys	2 bits
01	4 Keys	4 bits
10	4 Dipswitches + 4 Keys	4 bits (4-bit extended address + 4-bit data)
11	8 Keys	8 bits

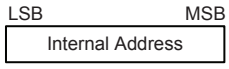
For the 16-pin package type, in the Key mode:

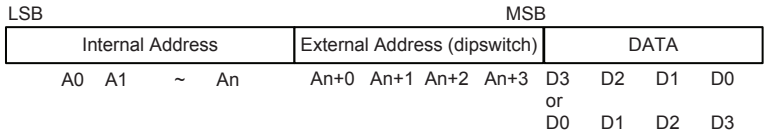
1. If this bit field is set as "00" then to select Keys D0~D1, the other 6 keys D2~D7 have no trigger function;
2. If the value is "01" then to select Keys D0~D3, the other 4 keys D4~D7 have no trigger function;
3. If the value is "10" then to select 4 Dipswitches + 4 Keys, the 4 dipswitch I/O status will be latched after power on, the dipswitches will maintain a pull-high or pull low status according to the latched high or low level to avoid current leakage in the Deep Sleep mode. These four dipswitches D4~D7 have no trigger function but will affect the address.
4. If dipswitch ever been changed, it is recommended to re-power on.

In the Key Mode, the TX transmitting data is determined by the keys while the transmitting data bit format is determined by the KEY_SEL bit field. The Data bit formats is shown as below:

Key Mode	OOK	GFSK
2 Keys	xx	111111xx
4 Keys	xxxx	1111xxxx
4 + 4 Keys	AAAAxxxx	AAAAxxxx
8 Keys	xxxx_xxxx	xxxx_xxxx

For the GFSK modulation, the transmitting data is fixed at 8 bits, bits without configurations are fixed at "1". As the above table shows, if the KEY_SEL bit field is set as "10" to select 4 Dipswitches + 4 Keys, the value of "A" is determined by Dipswitches and have no TX transmit trigger function. In the OOK modulation mode, data bit format can be 2 bits, 4 bits and 8 bits when the KEY_SEL bit field is configured to select 2 keys, 4 keys and 8 keys respectively. When the bit field is set to select 4 Dipswitches + 4 Keys, then the low nibble, bit 3~bit 0, is regarded as data and the 4-bit Dipswitches values is regarded as address.





- HT6P427A

Pilot-code	A0~A19	D0~D3

- HT6P437A

Pilot-code	A0~A23	D0~D3

- HT6P237A

Pilot-code	A0~A21	D1~D0	"0101"

- HT6P247A

Pilot-code	A0~A23	D3~D0	"0101"

- HT6P20B

Pilot-code	A0~A21	D1~D0	"0101"

- HT12E2Tx

Pilot-code	A0~A7	D0~D3

- **CFG17: Configuration Control Register17**

Address	Bit	7	6	5	4	3	2	1	0
11h	Name	SYNC_WORDL[7:0]							
	R/W	R/W							
	Initial Value	1	0	1	1	0	0	0	0

- **CFG18: Configuration Control Register18**

Address	Bit	7	6	5	4	3	2	1	0
12h	Name	SYNC_WORDM[7:0]							
	R/W	R/W							
	Initial Value	1	0	1	1	0	0	0	1

- **CFG19: Configuration Control Register19**

Address	Bit	7	6	5	4	3	2	1	0
13h	Name	SYNC_WORDH[7:0]							
	R/W	R/W							
	Initial Value	1	0	1	1	0	0	1	0

- **CFG20: Configuration Control Register20**

Address	Bit	7	6	5	4	3	2	1	0
14h	Name	SYNC_WORDU[7:0]							
	R/W	R/W							
	Initial Value	1	0	1	1	0	0	1	1

The CFG17~CFG20 is the 32-bit SYNC-WORD whose default values are 0xB0, 0xB1, 0xB2 and 0xB3 respectively, which follow the BC3601 receiver.

Preamble	Sync_wordL	Sync_wordM	Sync_wordH	Sync_wordU	Trailer
1010 ... 10	Bit 7 ~ Bit 0	Bit 7 ~ Bit 0	Bit 7 ~ Bit 0	Bit 7 ~ Bit 0	1010

- **CFG21: Configuration Control Register21**

Address	Bit	7	6	5	4	3	2	1	0
15h	Name	ENCODR_ADDRL[7:0]							
	R/W	R/W							
	Initial Value	0	0	0	0	0	0	0	0

- **CFG22: Configuration Control Register22**

Address	Bit	7	6	5	4	3	2	1	0
16h	Name	ENCODR_ADDRM[7:0]							
	R/W	R/W							
	Initial Value	0	0	0	0	0	0	0	0

- **CFG23: Configuration Control Register23**

Address	Bit	7	6	5	4	3	2	1	0
17h	Name	ENCODR_ADDRH[7:0]							
	R/W	R/W							
	Initial Value	0	0	0	0	0	0	0	0

- **CFG24: Configuration Control Register24**

Address	Bit	7	6	5	4	3	2	1	0
18h	Name	ENCODR_ADDRU[7:0]							
	R/W	R/W							
	Initial Value	0	0	0	0	0	0	0	0

The CFG21~CFG24 define the encoder address.

- **CFG25: Configuration Control Register25**

Address	Bit	7	6	5	4	3	2	1	0
19h	Name	FRAME_CNTR[7:0]							
	R/W	R/W							
	Initial Value	0	0	0	0	0	0	0	0

Bit 7~0 **FRAME_CNTR[7:0]**

The Frame Counter calculates the frame numbers using the following equation:

CNTR=FRAME_CNTR[7:0] + 1

0000: Transmit 1 complete frame

0001: Transmit 2 complete frames

0010: Transmit 3 complete frames

:

1111: Transmit 16 complete frames

- **CFG26: Configuration Control Register26**

Address	Bit	7	6	5	4	3	2	1	0
1Ah	Name	DTR[7:0]							
	R/W	R/W							
	Initial Value	0	0	0	0	0	1	1	1

Bit 7~0 **DTR[7:0]**: GFSK Data Rate setting parameter

- **CFG27: Configuration Control Register27**

Address	Bit	7	6	5	4	3	2	1	0
1Bh	Name	Reserved						DTR[9:8]	
	R/W	R/W						R/W	
	Initial Value	0	0	0	0	1	0	0	0

Bit 7~2 Reserved, must be [0b000010]

Bit 1~0 **DTR [9:8]**: GFSK Data Rate setting parameter

The GFSK Data Rate is calculated using the following equation:

Decimal value of the DTR[9:0]=[XTAL/(DR×16)]-1

DR (kbps)	DTR[9:0] Field Hexadecimal Value	DTR[9:0] Field Bbinary Value
2	1F3h	01-1111-0011b
10	63h	00-0110-0011b
50	13h	00-0001-0011b
100	09h	00-0000-1001b
125	07h	00-0000-0111b

- **CFG28 : Configuration Control Register28**

Address	Bit	7	6	5	4	3	2	1	0
1Ch	Name	Reserved	TXD_INV	TXD_REV	LED_SWD	Reserved			
	R/W	R/W	R/W	R/W	R/W	R/W			
	Initial Value	0	0	0	0	0	0	0	0

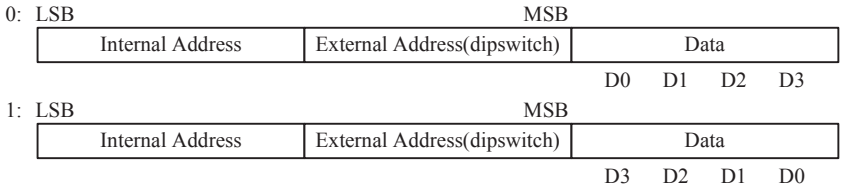
Bit 7 Reserved, must be [0b0]

Bit 6 **TXD_INV**: data inverse

0: No inverse

1: DATA "0" will be inversed as "1" and vice versa

Bit 5 **TXD_REV**: OOK mode Data MSB and LSB reverse control



Bit 4 **LED_SWD**: LED switch

0: LED follows the TX

1: LED follows the symbol high

Bit 3~0 Reserved, must be [0b0000]

- **CFG30: Configuration Control Register30**

Address	Bit	7	6	5	4	3	2	1	0
1Eh	Name	MAX_FCNT[7:0]							
	R/W	R/W							
	Initial Value	0	0	0	0	0	0	0	0

Bit 7~0 **MAX_FCNT[7:0]**

The TX will be disabled when the Frame Counter stops. However this bit field is used for the counted frames multiplication. This function is disabled when the bit field value is "0", otherwise the keys should be pressed and hold for a maximum waiting time to disable the TX, where the maximum waiting time=FRAME_CNTR[7:0] × MAX_FCNT[7:0]

- **CFG31: Configuration Control Register31**

Address	Bit	7	6	5	4	3	2	1	0
1Fh	Name	EFCRC_L[7:0]							
	R/W	R/W							
	Initial Value	0	0	0	0	0	0	0	0

- **CFG32: Configuration Control Register32**

Address	Bit	7	6	5	4	3	2	1	0
20h	Name	EFCRC_H[7:0]							
	R/W	R/W							
	Initial Value	0	0	0	0	0	0	0	0

EFCRC field: for FUSE CRC calculation

The address range of the CRC calculation is from 00h to 1Eh, which contains 31 bytes in total. The input order is LSB first, the CRC polynomial is $X^{16} + X^{15} + X^2 + 1$. The CRC on-line calculator can be accessed by the following website: http://www.sunshine2k.de/coding/javascript/crc/crc_js.html

For example:

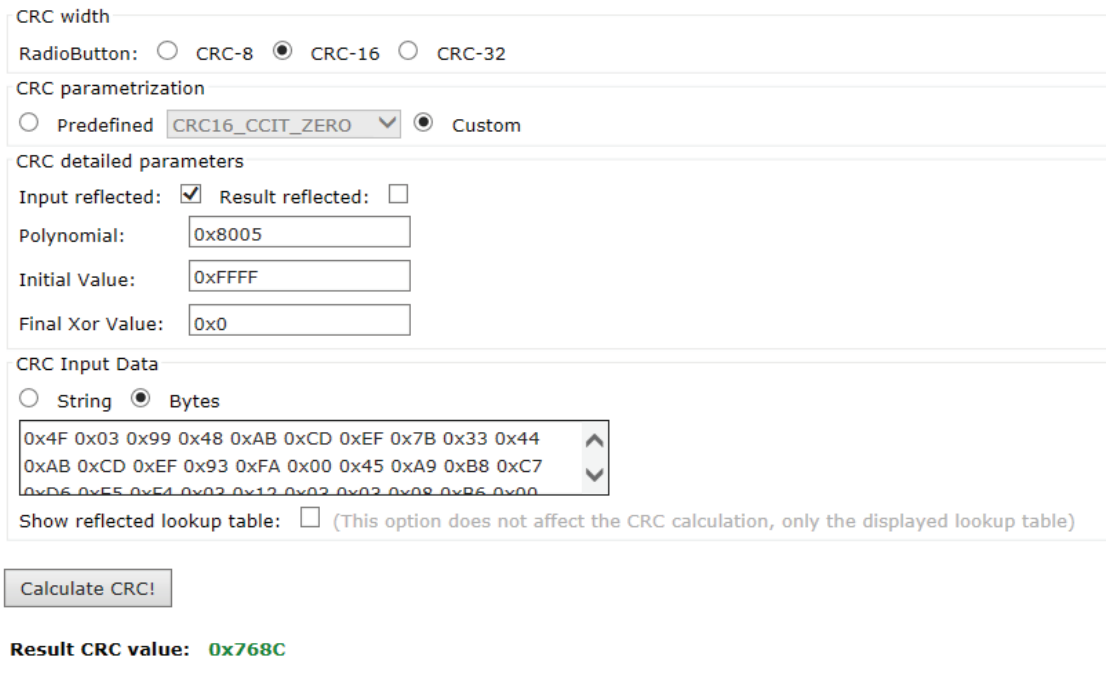
Data filled in the address range of 00h~1Eh are listed below:

0x4F 0x03 0x99 0x48 0xAB 0xCD 0xEF 0x7B 0x33 0x44 0xAB 0xCD 0xEF 0x93 0xFA 0x00 0x45 0xA9 0xB8 0xC7 0xD6 0xE5 0xF4 0x03 0x12 0x03 0x03 0x08 0xB6 0x00 0x00

The online calculator should be setup with the following configuration:

1. CRC width: select "CRC-16"
2. CRC parametrization: select "Custom"
3. CRC detailed parameters: select "Input reflected"
4. Polynomial: 0x8005
5. Initial Value: 0xFFFF
6. Final Xor Value: 0x0
7. CRC Input Data: select "Bytes" and fill in the data
8. Click on "Calculate CRC!"
9. Result CRC Value: 0x768C

As the following on-line calculator web interface screenshot shows:



- **CFG33: Configuration Control Register33**

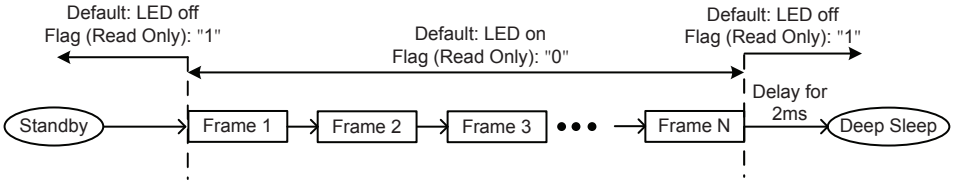
Address	Bit	7	6	5	4	3	2	1	0
21h	Name	Reserved							TX_FLAG
	R/W	Reserved							R
	Initial Value	0	0	0	0	0	0	0	1

Bit 7~1 Reserved, must be [0b0000000]

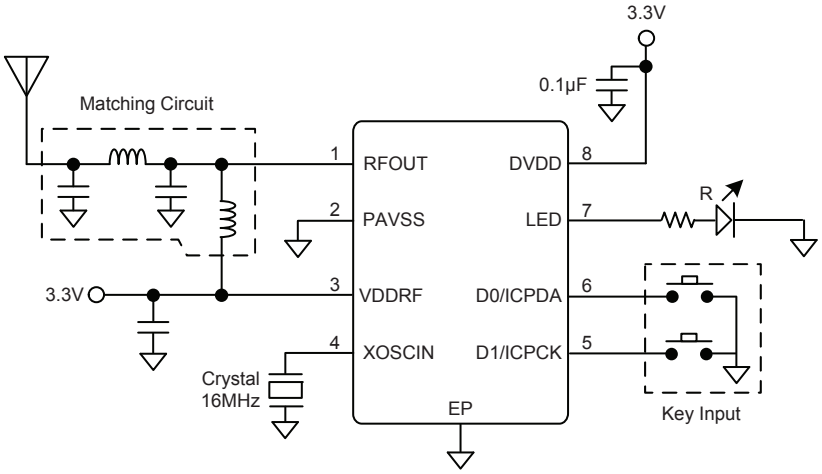
Bit 0 **TX_FLAG**: Transmission flag

0: Transmission is in progress, LED on

1: No transmission, LED off



Application Circuits



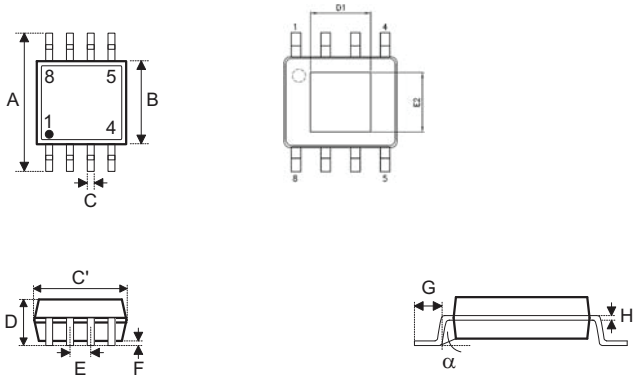
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

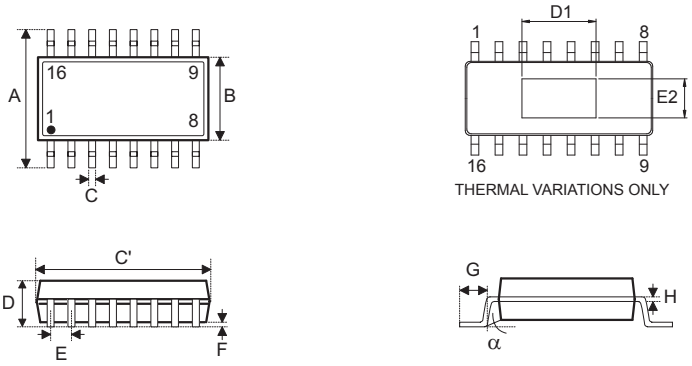
8-pin SOP (150mil) Outline Dimension (Exposed Pad)



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C'	—	0.193 BSC	—
D	—	—	0.069
D1	0.059	—	—
E	—	0.050 BSC	—
E2	0.039	—	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C'	—	4.90 BSC	—
D	—	—	1.75
D1	1.50	—	—
E	—	1.27 BSC	—
E2	1.00	—	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

16-pin NSOP (150mil) Outline Dimension (Exposed Pad)



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
D1	0.059	—	—
E2	0.039	—	—
C	0.012	—	0.020
C’	—	0.390 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
D1	1.50	—	—
E2	1.00	—	—
C	0.31	—	0.51
C’	—	9.90 BSC	—
D	—	—	1.75
E	—	1.27 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°