



Sub-1GHz Low-IF OOK/FSK RF Receiver

BC2502C/BC2502D

Revision: V1.10 Date: May 30, 2024

www.holtek.com

Features

- Frequency bands
 - ♦ BC2502C: 315MHz, 433MHz
 - ♦ BC2502D: 315MHz, 433MHz, 868MHz, 915MHz
- Operating voltage range: 2.4V~5.5V
- 0.5 μ A deep sleep current with data retention
- Low RX current
 - ♦ 4.5mA @ 433MHz
 - ♦ 5.8mA @ 868MHz
- Supports OOK/FSK modulation
 - ♦ OOK support up to 40ksps symbol rate
 - ♦ FSK support up to 50ksps symbol rate
- Good reception sensitivity under 0.1% BER (BW=93.6k)
 - ♦ -110dBm@25kbps, 433MHz, OOK
 - ♦ -107dBm@25kbps, 433MHz, FSK
 - ♦ -108dBm@25kbps, 868MHz, OOK
 - ♦ -104dBm@25kbps, 868MHz, FSK
- Wide RF input power range: from sensitivity to +10dBm
- Support 2-wire I²C interface for operation configuration
- On-chip VCO and Fractional-N synthesizer with integrated loop filter
- Supports low cost 16MHz crystal
- FCC/ETSI Compliant
- Package type: 10-pin SOP-EP

Applications

- Iron rolling doors
- Ceiling lamps
- Wireless switches
- Drying racks
- Wireless doorbells
- Integrated ceilings
- Other wireless products

General Description

The BC2502x receiver devices adopt a fully-integrated, low-IF OOK/FSK receiver with an automatic gain control (AGC) function and a fully-integrated OOK/FSK demodulator. The synthesizer is formed by an integrated VCO and a fractional-N PLL to support the 315, 433, 868, and 915MHz frequency bands. The devices only require a crystal and a minimum number of passive components to fully implement an OOK/FSK receiver. With this high level of functional integration, these devices provide excellent solutions for low-cost, low power wireless applications.

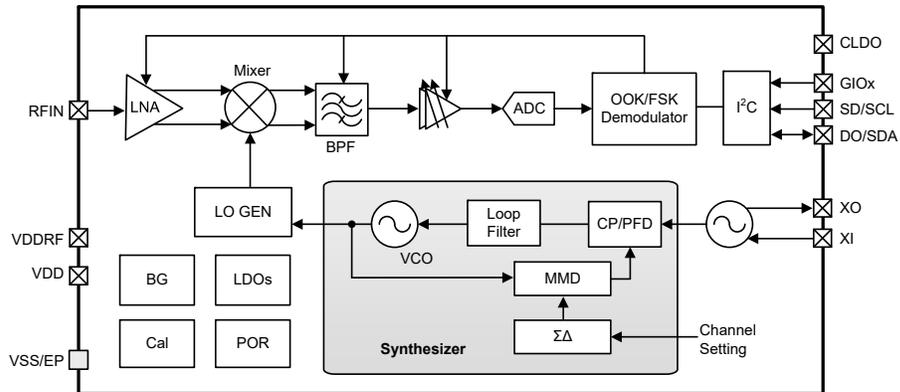
The devices achieve -112dBm sensitivity for the 433.92MHz bands. They operate from a supply voltage of 2.4V to 5.5V and typically require 4.5mA at 433.92MHz. There are two operation modes, one of which is the Auto RX mode. By properly setting certain PCB wirings, they can directly enter the RX mode. The devices also support a sniff RX mode, where the on/off RX mode function can be controlled by an MCU to achieve a lower than average power consumption using duty RX mode operation.

The BC2502 series offers two types of ICs. One is the BC2502C which covers the 315 and 433MHz bands while the BC2502D offers a choice of four frequency bands.

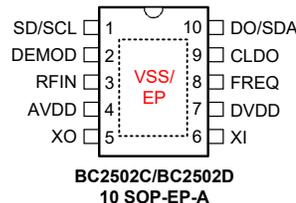
Selection Table

Part Number	Frequency Band
BC2502C	315MHz, 433MHz
BC2502D	315MHz, 433MHz, 868MHz, 915MHz

Block Diagram



Pin Assignment



Pin Description

Pin No.	Pin Name	I/O	Description
1	SD/SCL ⁽¹⁾	DI	RX mode shut-down control, should be pulled low in RX Mode
		DI	I ² C clock input line in Configuration Mode
2	DEMODO	—	Pin option for demodulation selection: <ul style="list-style-type: none"> • VDD: FSK • GND: OOK
3	RFIN ⁽⁴⁾	AI	RF LNA input
4	AVDD	PWR	Analog power supply
5	XO	AO	Crystal oscillator output
6	XI	AI	Crystal oscillator input
7	DVDD	PWR	Digital power supply
8	FREQ	DI	Pin option for frequency selection: <ul style="list-style-type: none"> • GND: 315MHz • Floating: 433.92MHz • VDD: 868.35MHz (BC2502D only)
9	CLDO	PWR	LDO output, connected to a bypass capacitor
10	DO/SDA ⁽¹⁾	DO	Demodulated data output in RX Mode
		DI/DO	I ² C data line in Configuration Mode
—	VSS/EP ⁽²⁾	PWR	Exposed pad, must be connected to ground

Legend: DI: Digital Input; DO: Digital Output; AI: Analog Input;
 AO: Analog Output; PWR: Power.

Note: 1. The DO/SDA & SD/SCL pins are default connected to a pull-high resistor after a power on reset. After entering the RX mode, these pull-high resistors are disconnected automatically. An analog debounce function is added to these two pins.

2. The VSS/EP pin located at the exposed pad.

3. The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.

4. Please refer to application note for RFIN pin connect external LNA circuit

Absolute Maximum Ratings

Supply Voltage	V _{SS} -0.3V to 5.5V
Input Digital Voltage	V _{SS} -0.3V to V _{DD} +0.3V
Input Analog Voltage	V _{SS} -0.3V to 2.1V
Storage Temperature.....	-60°C to 150°C
Operating Temperature.....	-40°C to 85°C
ESD HBM	±2kV

* Devices being ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, VDD=5.0V, fXTAL=16MHz, OOK/FSK demodulation with matching circuit, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T _{OP}	Operating Temperature	—	-40	—	85	°C
V _{DD}	Operating Voltage	—	2.4	5.0	5.5	V
Current Consumption						
I _{DeepSleep}	Current Consumption, Deep Sleep Mode	—	—	0.5	—	μA
I _{LightSleep}	Current Consumption, Light Sleep Mode	X'tal on	—	0.5	—	mA
I _{RX}	Current Consumption, RX Mode	@315MHz, OOK	—	4.7	—	mA
		@315MHz, FSK	—	4.7	—	
		@433MHz, OOK	—	4.5	—	
		@433MHz, FSK	—	4.5	—	
		@868MHz, OOK	—	5.8	—	
		@868MHz, FSK	—	5.8	—	
		@915MHz, OOK	—	5.8	—	
		@915MHz, FSK	—	5.8	—	
R _{PH}	Pull-high Resistance for I/O Ports	—	—	100	—	kΩ

A.C. Characteristics

Ta=25°C, VDD=5.0V, fXTAL=16MHz, OOK/FSK demodulation with matching circuit, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Receiver Characteristics						
f _{RF}	RF Frequency Range	BC2502C/BC2502D	—	315	—	MHz
		BC2502C/BC2502D	—	433.92	—	
		BC2502D only	—	868.35	—	
		BC2502D only	—	915	—	
SR	Symbol Rate	OOK modulation	0.5	—	40	ksps
DR	Data Rate	FSK modulation	1	—	50	ksps
f _{DEV}	Frequency Deviation	FSK modulation	4	—	25	kHz
P _{SENS} ⁽¹⁾	RX Sensitivity – 315MHz (Instrument: Keysight E4438C)	SR=1ksps, BER=0.1%	—	-111	—	dBm
		SR=10ksps, BER=0.1%	—	-111	—	
		DR=1ksps, BER=0.1% (@f _{DEV} =8kHz)	—	-105	—	
		DR=10ksps, BER=0.1% (@f _{DEV} =20kHz)	—	-109	—	
		DR=30ksps, BER=0.1% (@f _{DEV} =15kHz)	—	-109	—	
	RX Sensitivity – 433.92MHz (Instrument: Keysight E4438C)	SR=1ksps, BER=0.1%	—	-110	—	
		SR=10ksps, BER=0.1%	—	-110	—	
		DR=1ksps, BER=0.1% (@f _{DEV} =8kHz)	—	-105	—	
		DR=10ksps, BER=0.1% (@f _{DEV} =20kHz)	—	-108	—	
		DR=30ksps, BER=0.1% (@f _{DEV} =15kHz)	—	-107	—	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
P _{SENS} ⁽¹⁾	RX Sensitivity – 868.35MHz (Instrument: Keysight E4438C)	SR=1ksps, BER=0.1%	—	-108	—	dBm
		SR=10ksps, BER=0.1%	—	-108	—	
		DR=10ksps, BER=0.1% (@f _{DEV} =20kHz)	—	-104	—	
		DR=30ksps, BER=0.1% (@ f _{DEV} =15kHz)	—	-104	—	
	RX Sensitivity – 915MHz (Instrument: Keysight E4438C)	SR=1ksps, BER=0.1%	—	-107	—	
		SR=10ksps, BER=0.1%	—	-108	—	
		DR=10ksps, BER=0.1% (@f _{DEV} =20kHz)	—	-102	—	
		DR=30ksps, BER=0.1% (@ f _{DEV} =15kHz)	—	-102	—	
SE _{RX}	Receiver Spurious Emission	25MHz~1GHz	—	—	-57	dBm
		Above 1GHz	—	—	-47	
	Blocking Immunity	±2MHz offset	—	40	—	dBc
		±10MHz offset	—	64	—	
Receiver Characteristics						
Cof _{ST}	Configure Mode Settling Time (Deep Sleep to Configure Mode)	49US XO	—	1.5	—	ms
		SMD3225 XO	—	2.5	—	ms
RX _{ST}	RX Mode Settling Time (Deep Sleep Mode to RX Mode Data Out)	49US XO	—	1.5	—	ms
		SMD3225 XO	—	2.5	—	ms
LO Characteristics						
f _{LO}	Frequency Coverage Range	BC2502C/BC2502D	300	—	360	MHz
		BC2502C/BC2502D	390	—	450	
		BC2502D only	800	—	950	
f _{STEP}	Frequency Resolution	—	—	—	0.1	kHz
	Synthesizer Locking Time	—	—	130	—	µs
Crystal Oscillator Characteristics						
f _{XTAL}	Crystal Frequency	General case	—	16	—	MHz
t _{SU}	X'tal Startup Time ⁽²⁾	49US XO	—	0.5	—	ms
		SMD3225 XO	—	1.5	—	ms
ESR	X'tal Equivalent Series Resistance	—	—	—	100	Ω
C _L	X'tal Load Capacitance	—	—	16	—	pF
TOL	X'tal Tolerance ⁽³⁾	—	-20	—	+20	ppm

Note: 1. 315/433MHz Bands Digital Filter BW = 93.6kHz

868/915MHz Bands Digital Filter BW = 187.2kHz

2. The X'tal startup time depends on crystal property.

3. This is the total tolerance including (1) Initial tolerance (2) Crystal loading (3) Aging (4) Temperature dependence.

4. Max input power = 0dBm(@2.4V)

I²C Characteristics

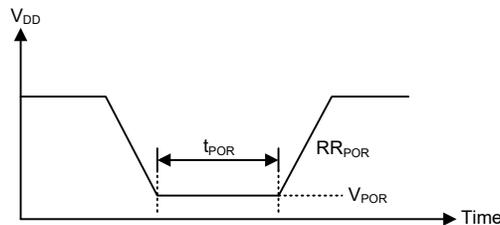
Ta=25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f _{SCL}	Serial Clock Frequency	—	—	—	1	MHz
t _{BUF}	Bus Free Time between Stop and Start Condition	SCL=1MHz	250	—	—	ns
t _{LOW}	SCL Low Time	SCL=1MHz	500	—	—	ns
t _{HIGH}	SCL High Time	SCL=1MHz	500	—	—	ns
t _{SU(DAT)}	Data Setup Time	SCL=1MHz	100	—	—	ns
t _{SU(STA)}	Start Condition Setup Time	SCL=1MHz	250	—	—	ns
t _{SU(STO)}	Stop Condition Setup Time	SCL=1MHz	250	—	—	ns
t _{H(DAT)}	Data Hold Time	SCL=1MHz	100	—	—	ns
t _{H(STA)}	Start Condition Hold Time	SCL=1MHz	250	—	—	ns
t _{r(SCL)}	Rise Time of SCL Signal	SCL=1MHz	—	—	100	ns
t _{f(SCL)}	Fall Time of SCL Signal	SCL=1MHz	—	—	100	ns
t _{r(SDA)}	Rise Time of SDA Signal	SCL=1MHz	—	—	100	ns
t _{f(SDA)}	Fall Time of SDA Signal	SCL=1MHz	—	—	100	ns

Power on Reset Characteristics

Ta=25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V _{POR}	V _{DD} Start Voltage to Ensure Power-on Reset	—	—	—	100	mV
RR _{POR}	V _{DD} Rising Rate to Ensure Power-on Reset	—	0.035	—	—	V/ms
t _{POR}	Minimum Time for V _{DD} Stays at V _{POR} to Ensure Power-on Reset	—	1	—	—	ms



Functional Description

The BC2502x devices are ultra-low power, high performance, low-cost OOK/FSK receivers suitable for use in wireless applications with a frequency of 315, 433, 868, 915MHz respectively. The devices are formed by a low-IF receiver, followed by an OOK/FSK demodulator and a fractional-N synthesizer. They only require a crystal and a minimum number of passive components to implement an OOK/FSK receiver.

OOK/FSK RF Receiver

The BC2502x devices adopt a fully-integrated, low-IF receiver architecture. The received RF signal is first amplified by a low noise amplifier (LNA), after which the frequency is reduced to an intermediate frequency (IF). The IF signal is filtered by a channel-selected filter which rejects the unwanted out-of-band interference signals and image signal. After the BPF stage, the desired IF signal is amplified by the limiter amplifier which generates a received-signal-strength-indicator (RSSI) signal.

The devices feature an automatic gain control (AGC) unit which adjusts the front-end gain according to the RSSI. The AGC can increase the dynamic range of the RSSI and enable the devices to receive a wide dynamic range RF signal.

The OOK/FSK one/zero type data is generated by comparing the RSSI signal to a manipulated threshold. This threshold is crucial to the performance of OOK/FSK demodulation. The agile threshold detection mechanism can reduce glitches when there is no RF signal or when long zero data streams are received. It also includes a fast tracking threshold to offer good immunity from co-channel interferences.

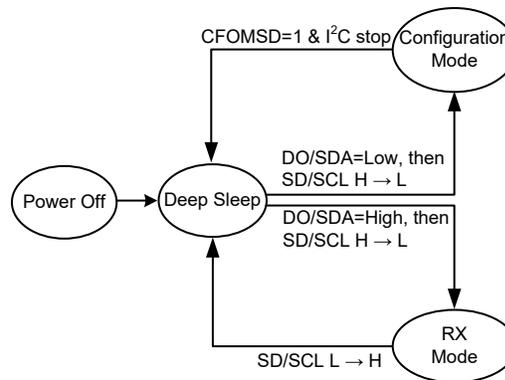
Operating Mode

The devices provide four operation modes, power off mode, deep sleep mode, RX mode and configuration mode.

In the deep sleep mode, there is less than 1µA of sleep mode leakage current with register data retention.

In the RX Mode, the devices execute normal RX operations that receive incoming RF signals from the antenna and then output the demodulated data onto the DO/SDA pin. There are two types of RX mode, one is the Auto RX mode and the other is the sniff RX mode.

In the Configuration Mode, the devices are operated as I²C slaves and are programmed by an external MCU. Users can select the desired RX channel by configuring the internal registers. After the configuration has completed, the devices will return to the deep sleep mode by setting the CFOMSD bit high.



Operation Mode Switching

Note: The CFOMSD bit will be cleared to zero automatically when the device leaves the configuration mode.

Auto RX Mode

The devices provide an Auto RX Mode. After power-on, the devices will enter the RX mode after a 30ms delay from the power-on reset. In this mode, frequency selection is achieved using a pin option together with external PCB wirings as shown in the following table.

FREQ Pin	Selected Frequency for BC2502C	Selected Frequency for BC2502D
GND	315MHz	315MHz
Floating	433.92MHz	433.92MHz
V _{DD}	Unavailable	868.35MHz

To directly enter this mode, the SD/SCL pin should be connected to ground and the FREQ pin should be connected to the required level before power is applied. Note that there is only one method for the device to leave the RX mode which is to remove the power.

Sniff RX Mode

The devices also provide a Sniff RX mode as it is controlled by an MCU. The SD/SCL pin defaults to a pull-high state. After power-on the devices will enter the deep sleep mode. An MCU could control the SD/SCL pin to make it enter or leave the RX mode. With additional SD/SCL control, users can optimize the average power consumption based on their applications.

It is not recommended to use the sniff RX mode if the frequency is less than or equal to 5ksp/s.

Configuration Mode

The devices include an I²C serial interface, which is used for bidirectional, two-line communication between multiple I²C devices. The two lines of this interface are the serial data line, SDA, and the serial clock line, SCL. Both lines are equipped with de-bounce functions. After a power on reset, these two pins are pulled to DVDD by default using internal pull-high resistors. When entering the RX mode, the pull-high resistors are disconnected.

The devices support the I²C format for byte write, page write, byte read and page read formats. Every byte placed onto the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.

It should be noted that the I²C is a non-standard I²C interface, which only supports a single device for connection.

Byte Write



Page Write



Byte Read



Page Read



Bus Direction:  : Host to device;  : Device to host;

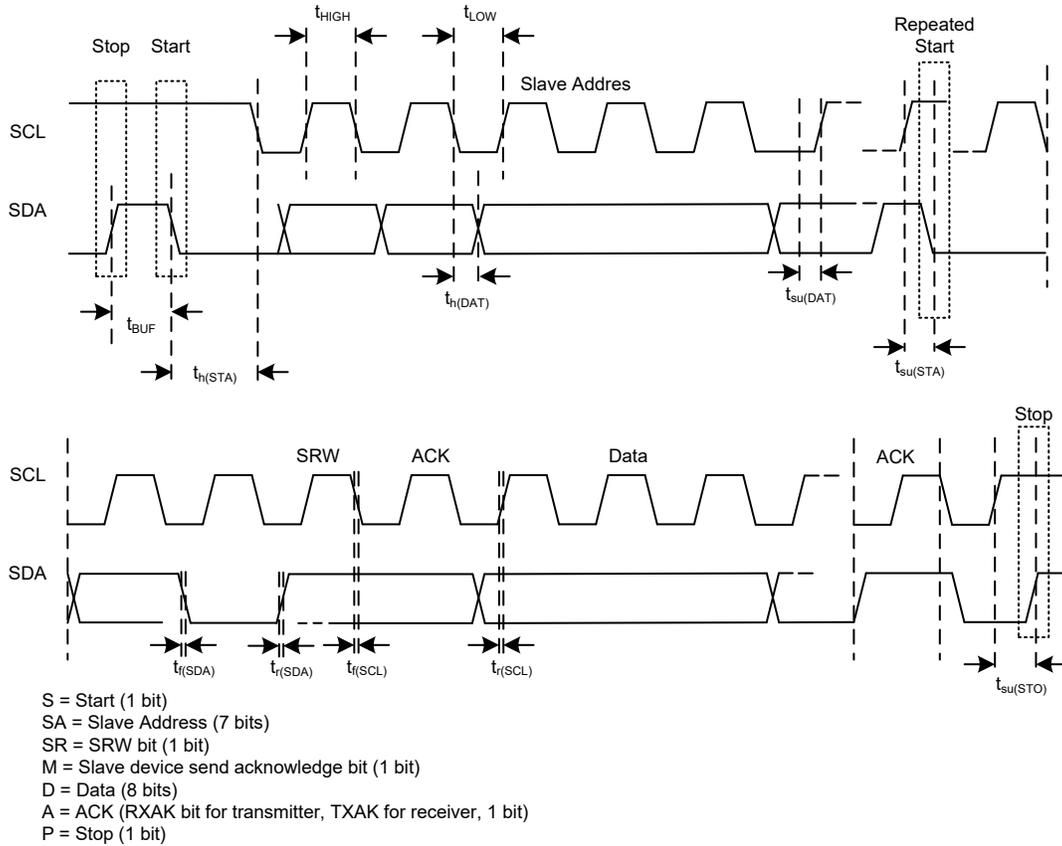
Symbol Definitions: S: Start; RS: Repeated Start; P: Stop;

DADDR[6:0]: Device Address, 25h;

R:Read(1); W: Write(0);

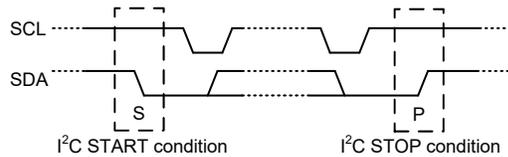
RADDR[7:0]: register address;

A: ACK(0); NA: NAK(1)



I²C Communication Timing Diagram

I²C START and STOP Conditions

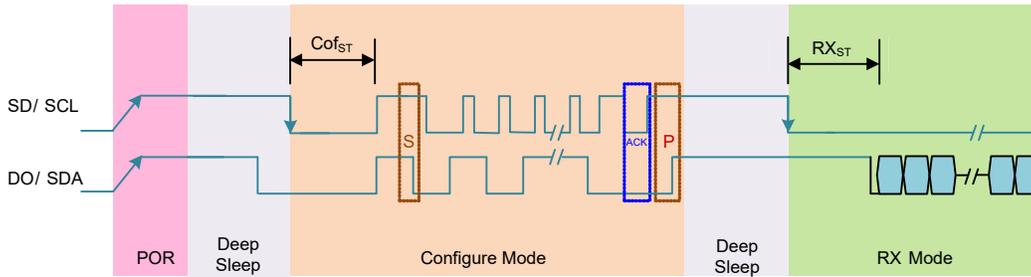


- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus remains busy if a Repeated START (RS) is generated instead of a STOP condition. The START (S) and Repeated START (RS) conditions are functionally identical.

Configuration Mode Switching and Timing

As shown in the following diagram, when SDA is low and a SCL falling edge occurs, the device changes from the Deep Sleep Mode to the Configuration Mode after a 1.5ms delay time. If the SCL level remains high for a time greater than or equal to 20ms, the device will be forced to leave the Configuration Mode.

If the devices are connected to an MCU through an I²C interface, users can set the CFOMSD bit of the register, at address 40h, to leave the Configuration Mode.



Entering and Leaving Configuration Mode Timing Diagram

Register Map

When connected to an external MCU, the device’s RF frequency can be setup using a series of internal registers in the Configuration Mode. The register data is written to and read from the devices using their internal I²C interface. The following provides a summary of all internal registers and their detailed descriptions.

Address	Register Name	Bit								
		7	6	5	4	3	2	1	0	
05h	FSKDM1	MODE_SEL	Reserved				MDIV_SEL[1:0]			
10h	OM	PWR_SOFT	BAND_SEL[1:0]		Reserved					
12h	SX1	Reserved	D_N[6:0]							
13h	SX2	D_K[7:0]								
14h	SX3	D_K[15:8]								
15h	SX4	Reserved				D_K[19:16]				
32h	T3	Reserved					CR_SEL	Reserved		
40h	I2C1	Reserved							CFOMSD	

• **FSKDM1 – FSK De-Modulator Control Register 1 (Addr: 05H)**

Bit	7	6	5	4	3	2	1	0
Name	MODE_SEL	—	—	—	—	—	MDIV_SEL [1:0]	
R/W	R/W	—	—	—	—	—	R/W	
POR	1	0	0	0	0	0	0	1

- Bit 7 **MODE_SEL**: Selection of demodulation type
 0: OOK mode
 1: FSK mode
- Bit 6~2 Reserved bit, cannot be changed
- Bit 1~0 **MDIV_SEL[1:0]**: Demodulator operation clock divider selection
 00: 187.2kHz
 01: 93.6kHz
 10: 46.8kHz
 11: reserved

• **OM – Operation Mode Control Register (Addr: 10H)**

Bit	7	6	5	4	3	2	1	0
Name	—	BAND_SEL[1:0]		—	—	—	—	—
R/W	—	R/W		—	—	—	—	—
POR	0	0	1	0	0	0	0	0

- Bit 7 Reserved bit, cannot be changed
 Bit 6~5 **BAND_SEL[1:0]**: Band selection
 00: 300~360MHz Band
 01: 390~450MHz Band
 10: Reserved
 11: 850~935MHz Band (BC2502D Only)
 Bit 4~0 Reserved bit, cannot be changed

• **SX1 – Fractional-N Synthesizer Control Register 1 (Addr: 12H)**

Bit	7	6	5	4	3	2	1	0
Name	—	D_N[6:0]						
R/W	—	R/W						
POR	1	0	0	0	0	1	0	1

- Bit 7 Reserved bit, must be set “1”
 Bit 6~0 **D_N[6:0]**: RF channel frequency integer number code
 $D_N[6:0] = \text{Floor} \left(\frac{f_{RF} - f_{IF}}{f_{XTAL}} \times 0.8 \right) \times M$, (315MHz: M=2, Other Bands: M=1)
 For example:
 $f_{XTAL}=16\text{MHz}$, RF channel frequency(f_{RF})=315MHz, Intermediate Frequency (f_{IF})=200kHz
 $\rightarrow (315\text{MHz} - 0.2\text{MHz}) / (16\text{MHz}) \times 0.8 \times 2 = 31.48$
 $\rightarrow D_N = 31$
 $\rightarrow \text{Dec2Bin}(31) = 001_1111$
 $f_{XTAL}=16\text{MHz}$, RF channel frequency(f_{RF})=433.92MHz, Intermediate Frequency (f_{IF})=200kHz
 $\rightarrow (433.92\text{MHz} - 0.2\text{MHz}) / (16\text{MHz}) \times 0.8 = 21.686$
 $\rightarrow D_N = 21$
 $\rightarrow \text{Dec2Bin}(21) = 001_0101$

• **SX2 – Fractional-N Synthesizer Control Register 2 (Addr: 13H)**

Bit	7	6	5	4	3	2	1	0
Name	D_K[7:0]							
R/W	R/W							
POR	1	1	0	1	1	0	1	1

- Bit 7~0 **D_K[7:0]**: RF channel frequency fractional number code lowest byte

• **SX3 – Fractional-N Synthesizer Control Register 3 (Addr: 14H)**

Bit	7	6	5	4	3	2	1	0
Name	D_K[15:8]							
R/W	R/W							
POR	1	1	1	1	1	0	0	1

- Bit 7~0 **D_K[15:8]**: RF channel frequency fractional number code medium byte

• **SX4 – Fractional-N Synthesizer Control Register 4 (Addr: 15H)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	D_K[19:16]			
R/W	—	—	—	—	R/W			
POR	0	1	1	0	1	0	1	0

Bit 7~4 Reserved bit, cannot be changed

Bit 3~0 **D_K[19:16]**: RF channel frequency fractional number code highest byte

$$D_K[19:0]=\text{Floor} \left\{ \left(\frac{f_{RF} - f_{IF}}{f_{XTAL}} \times 0.8 \times M - D_N[6:0] \times 2^{20} \right), (315\text{MHz: } M=2, \text{ Other Bands: } M=1) \right.$$

For example:

$f_{XTAL}=16\text{MHz}$, RF channel frequency(f_{RF})=315MHz, Intermediate Frequency (f_{IF})=200kHz

$$\rightarrow (315\text{MHz}-0.2\text{MHz})/(16\text{MHz}) \times 0.8 \times 2 = 31.48$$

$$\rightarrow D_K = 0.48 \times 2^{20} = 503316$$

$$\rightarrow \text{Dec2Bin}(503316) = 0111_1010_1110_0001_0100$$

$f_{XTAL}=16\text{MHz}$, RF channel frequency(f_{RF})=433.92MHz, Intermediate Frequency (f_{IF})=200kHz

$$\rightarrow (433.92\text{MHz}-0.2\text{MHz})/(16\text{MHz}) \times 0.8 = 21.686$$

$$\rightarrow D_K = 0.686 \times 2^{20} = 719323$$

$$\rightarrow \text{Dec2Bin}(719323) = 1010_1111_1001_1101_1011$$

• **T3 – Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CR_SEL	—
R/W	—	—	—	—	—	—	R/W	—
POR	1	0	0	0	0	0	0	0

Bit 7~2 Reserved bit, cannot be changed

Bit 1 **CR_SEL**: Control registers selection

0: From Default setting

1: From control register setting

Bit 0 Reserved bit, cannot be changed

• **I2C1 – I²C Control Register 1 (Addr: 40H)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	CFOMSD
R/W	—	—	—	—	—	—	—	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~1 Reserved bit, cannot be changed

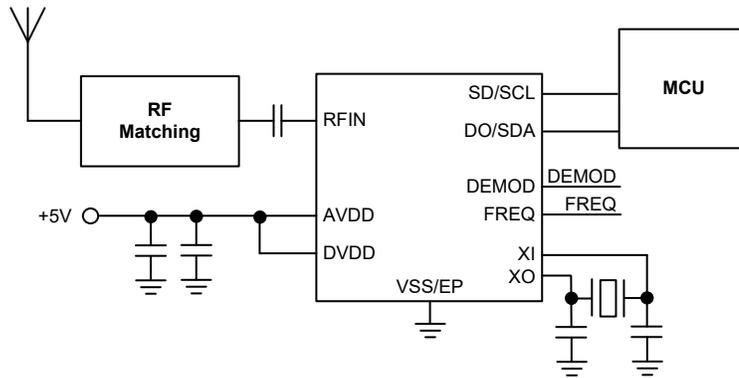
Bit 0 **CFOMSD**: Configuration Mode shut down control

0: No operation

1: Exit Configuration Mode

In the configuration mode the devices can be forced to leave this mode by first setting the CFOMSD bit high and then followed by an I²C stop condition. After leaving the Configuration Mode the CFOMSD bit will be reset to zero automatically.

Application Circuits



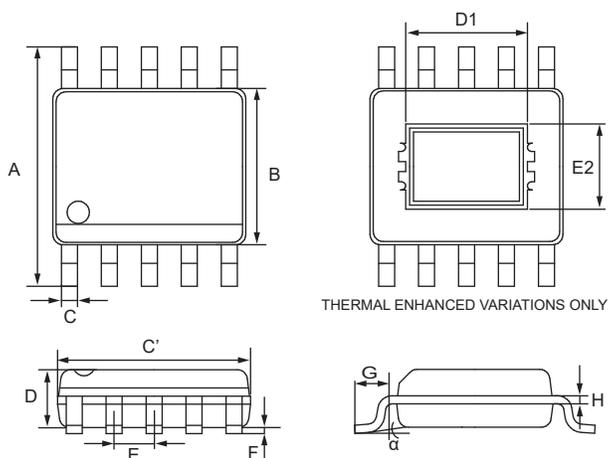
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package/Carton Information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- [Package Information \(include Outline Dimensions, Product Tape and Reel Specifications\)](#)
- [The Operation Instruction of Packing Materials](#)
- [Carton information](#)

10-pin SOP-EP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.236 BSC		
B	0.154 BSC		
C	0.012	—	0.018
C'	0.193 BSC		
D	—	—	0.069
D1	0.102	—	0.126
E	0.039 BSC		
E2	0.071	—	0.090
F	0.000	—	0.006
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	6.00 BSC		
B	3.90 BSC		
C	0.30	—	0.45
C'	4.90 BSC		
D	—	—	1.75
D1	2.59	—	3.20
E	1.00 BSC		
E2	1.81	—	2.28
F	0.00	—	0.15
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°

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