BC32F7611
32-bit Arm® Cortex®-M0+ MCU with BLE Transparent Transmission Controller

Features

- Operating Voltage: 3.3V (Typical)
- Core
  - 32-bit Arm® Cortex®-M0+ processor core
  - 0.93 DMIPS/MHz (Dhrystone v2.1)
  - Up to 40MHz operating frequency
- On-chip Memory
  - 64KB Flash Memory
  - 8KB SRAM
- Clock Control Unit
  - External 4~16MHz crystal oscillator
  - External 32.768kHz crystal oscillator
  - Internal 8MHz (±2%) RC oscillator
  - Internal 32kHz RC oscillator
- Peripherals
  - GPIO: 22 GPIOs pin-shared with other alternative functions
  - ADC: 6 external channels 1MSPS 12-bit SAR ADC
  - two I^2C interfaces with a speed up to 1MHz
  - One Universal Synchronous/Asynchronous Receiver/Transmitter – USART
  - Two Universal Asynchronous Receiver/Transmitters – UART
  - Master/Slave SPI controller with FIFO
  - One 16-bit General-Purpose Counter/Timers with 4 independent input channels
  - One 16-bit up-counter Single-Channel Timer with 6 input channels
  - Motor Control Timer
  - CRC-16/32 generator
  - Real-time Clock (RTC) with alarm function
  - Watchdog Timer
- Debug Support
  - Serial Wire Debug Port – SW-DP
- BLE
  - Integrated high performance RF and MODEM for BLE (Bluetooth Low Energy) applications
  - On-chip capacitors for BLE 32MHz crystal oscillator
  - Integrated DC/DC converter and LDOs allowing a wider supply range with a single power supply
  - Over 75dB RX gain and programmable gain steps
  - Sleep, Deep-Sleep and Power-Down modes for low power consumption
  - Few external components required for BLE applications
- Power Management
  - Multiple power saving modes: Sleep, Deep-Sleep1 and Deep-Sleep2 for low power consumption
- Package type: 46-pin QFN – 6.5mm×4.5mm

Applications

- Health care products
- Smart home appliances
- Beacons

General Description

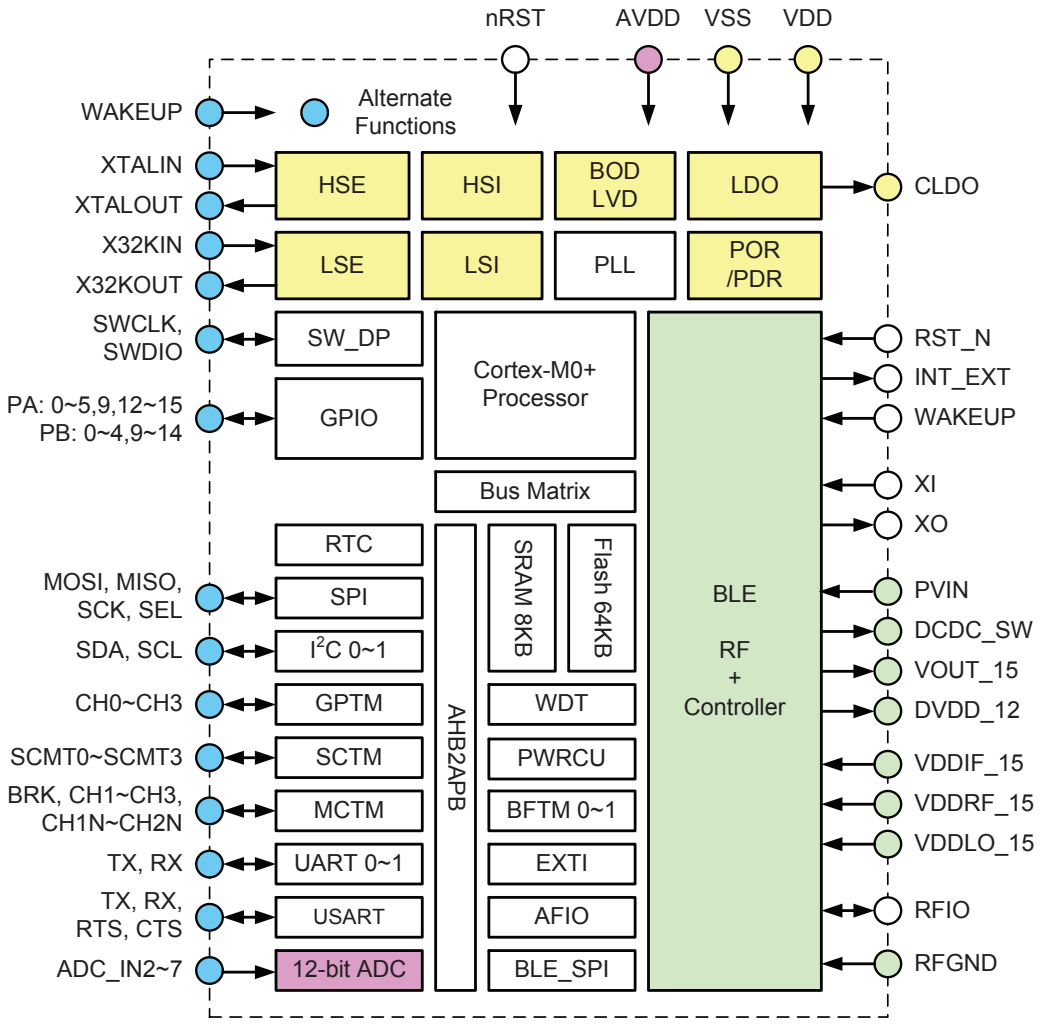
The BC32F7611 device is a fully-integrated, single-chip BLE SoC (System on Chip) microcontroller based around a high performance, low power consumption 32-bit Arm® Cortex®-M0+ processor core. The BLE function is designed to act as a BLE slave controller in accordance with the Bluetooth specification v4.1.

The device operates at a frequency of up to 40MHz with a Flash accelerator to obtain maximum efficiency. It provides 64KB of embedded Flash memory for code/data storage and 8KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, USART, UART, SPI, GPTM, SCTM, MCTM, CRC-16/32, RTC, WDT, SW-DP (Serial Wire Debug Port), etc., are also implemented in this device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

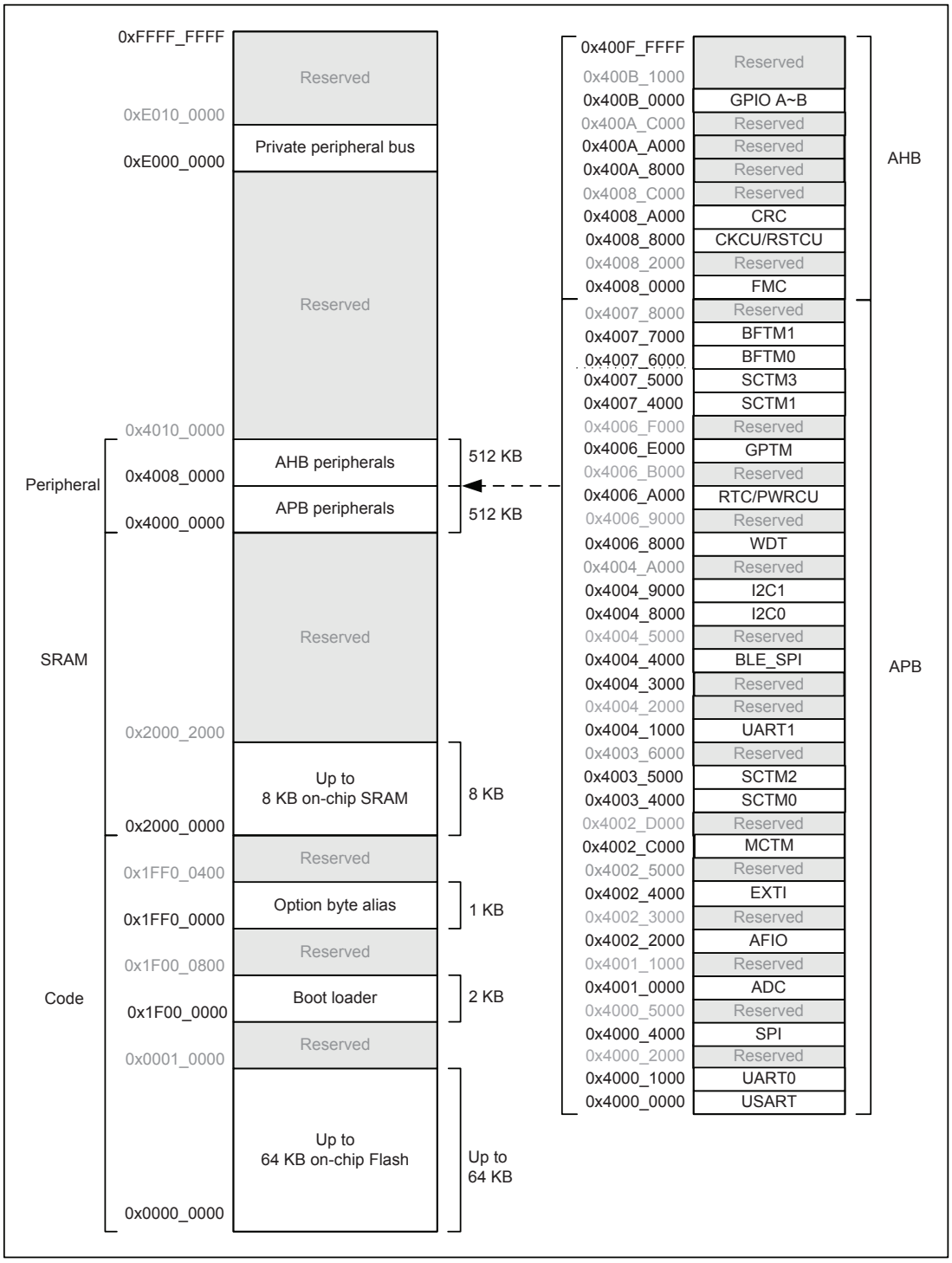
The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, health care products, smart home and so on.

Moreover, during the intervals with no active BLE RF connection, The BC32F7611 works in the sleep mode which can furtherly reduce power consumption.

Block Diagram



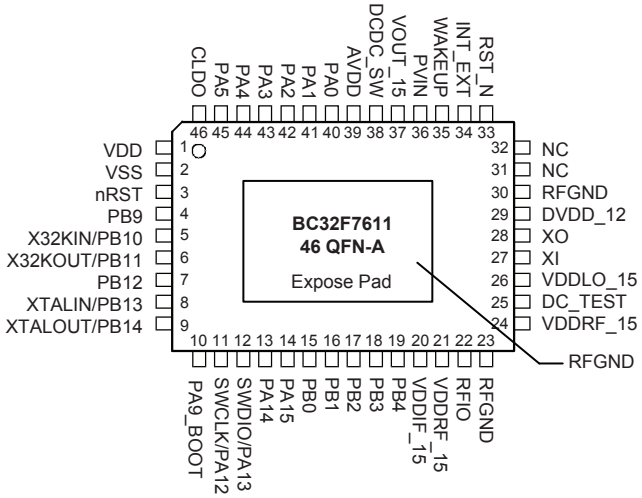
Memory Map


0xFFFF_FFFF
Reserved
0xE010_0000
Private peripheral bus
0xE000_0000
Reserved
0x4010_0000
AHB peripherals
512 KB
0x4008_0000
APB peripherals
512 KB
0x4000_0000
Reserved
0x2000_2000
Up to
8 KB on-chip SRAM
8 KB
0x2000_0000
Reserved
0x1FF0_0400
Option byte alias
1 KB
0x1FF0_0000
Reserved
0x1F00_0800
Boot loader
2 KB
0x1F00_0000
Reserved
0x0001_0000
Up to
64 KB on-chip Flash
Up to
64 KB
0x0000_0000
Peripheral
SRAM
Code
0x400F_FFFF
Reserved
0x400B_1000
0x400B_0000 GPIO A~B
0x400A_C000 Reserved
0x400A_A000 Reserved
0x400A_8000 Reserved
0x4008_C000 Reserved
0x4008_A000 CRC
0x4008_8000 CKCU/RSTCU
0x4008_2000 Reserved
0x4008_0000 FMC
0x4007_8000 Reserved
0x4007_7000 BFTM1
0x4007_6000 BFTM0
0x4007_5000 SCTM3
0x4007_4000 SCTM1
0x4006_F000 Reserved
0x4006_E000 GPTM
0x4006_B000 Reserved
0x4006_A000 RTC/PWRCU
0x4006_9000 Reserved
0x4006_8000 WDT
0x4004_A000 Reserved
0x4004_9000 I2C1
0x4004_8000 I2C0
0x4004_5000 Reserved
0x4004_4000 BLE_SPI
0x4004_3000 Reserved
0x4004_2000 Reserved
0x4004_1000 UART1
0x4003_6000 Reserved
0x4003_5000 SCTM2
0x4003_4000 SCTM0
0x4002_D000 Reserved
0x4002_C000 MCTM
0x4002_5000 Reserved
0x4002_4000 EXTI
0x4002_3000 Reserved
0x4002_2000 AFIO
0x4001_1000 Reserved
0x4001_0000 ADC
0x4000_5000 Reserved
0x4000_4000 SPI
0x4000_2000 Reserved
0x4000_1000 UART0
0x4000_0000 USART
AHB
APB

Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4001_9FFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4003_5FFF	SCTM2	
0x4003_6000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_2FFF	Reserved	
0x4004_3000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	BLE_SPI	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I2C0	
0x4004_9000	0x4004_9FFF	I2C1	
0x4004_A000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC/PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	SCTM3	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU/RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x400A_7FFF	Reserved	
0x400A_8000	0x400A_BFFF	Reserved	
0x400A_C000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400B_5FFF	Reserved	
0x400B_6000	0x400F_FFFF	Reserved	

Pin Assignment



Note: Not all pin-shared functions are shown in the pin assignment, refer to the Pin Alternate Function Mapping table for more details.

Pin Description

Pin Name	Pin No.	I/O	Description
VDD	1	P	Digital power supply; 2.2V~3.6V
VSS	2	P	Connect to ground
nRST	3	DI	MCU core reset input
PB9	4	IO	General Purpose I/O / MT_CH3
X32KIN/PB10	5	IO	X32KIN / General Purpose I/O / GT_CH0 / USR_TX / SCTM2
X32KOUT/PB11	6	IO	X32KOUT / General Purpose I/O / GT_CH1 / USR_RX / SCTM3
PB12	7	IO	PB12 / SPI_MISO / UR0_RX / SCTM0 / WAKEUP
XTALIN/PB13	8	AIO	Crystal Input / PB13 / UR0_TX / I2C0_SCL
XTALOUT/PB14	9	AIO	Crystal Output / PB14 / UR0_RX / I2C0_SDA
PA9_BOOT	10	DI	General Purpose I/O / Boot mode selections / SPI_MOSI / SCTM3 / CKOUT
SWCLK/PA12	11	DIO	Serial-Wired debug clock input / PA12
SWDIO/PA13	12	DIO	Serial-Wired debug data pin / PA13
PA14	13	IO	General Purpose I/O / MT_CH0 / USR_RTS / I2C1_SCL
PA15	14	IO	General Purpose I/O / MT_CH0N / USR_CTS / I2C1_SDA / SCTM1
PB0	15	IO	General Purpose I/O / MT_CH1 / USR_TX / I2C0_SCL
PB1	16	IO	General Purpose I/O / MT_CH1N / USR_RX / I2C0_SDA / SCTM2
PB2	17	IO	General Purpose I/O / MT_CH2 / SPI_SEL / UR1_TX
PB3	18	IO	General Purpose I/O / MT_CH2N / SPI_SCK / UR1_RX / SCTM1
PB4	19	IO	General Purpose I/O / MT_BRK / SPI_MOSI / UR1_TX / SCTM0
VDDIF_15	20	P	Analog power for IF part, connect to VOUT_15
VDDRF_15	21	P	Analog power for RF part, connect to VOUT_15
RFIO	22	AIO	RF input or output
RFGND	23	P	RF Power Ground
VDDRF_15	24	P	Analog power for RF part, connect to VOUT_15
DC_TEST	25	AO	Test pin for RF function
VDDLO_15	26	P	Analog power for RF part, connect to VOUT_15

Pin Name	Pin No.	I/O	Description
XI	27	AI	BLE 32MHz Crystal oscillator input
XO	28	AO	BLE 32MHz Crystal oscillator output
DVDD_12	29	P	Internal digital power 1.2V, require a 0.1μF capacitor to RFGND
RFGND	30	P	RF Power Ground
NC	31	—	Connect to ground
NC	32	—	Connect to ground
RST_N	33	DI	BLE hardware reset input
INT_EXT	34	DO	BLE External Interrupt
WAKEUP	35	DI	BLE Wakeup pin
PVIN	36	DI	BLE Power-supply; 2.2V~3.6V
VOUT_15	37	P	1.5V power output
DCDC_SW	38	P	Switching Output. Connect this pin to the switching end of the inductor
AVDD	39	P	+3.3V Analog Power supply
PA0	40	AIO	General Purpose I/O / ADC_IN2 / GT_CH0 / USR_RTS / I2C1_SCL
PA1	41	AIO	General Purpose I/O / ADC_IN3 / GT_CH1 / USR_CTS / I2C1_SDA
PA2	42	AIO	General Purpose I/O / ADC_IN4 / GT_CH2 / USR_TX
PA3	43	AIO	General Purpose I/O / ADC_IN5 / GT_CH3 / USR_RX
PA4	44	AIO	General Purpose I/O / ADC_IN6 / GT_CH0 / SPI_SCK / UR1_TX / I2C0_SCL
PA5	45	AIO	General Purpose I/O / ADC_IN7 / GT_CH1 / SPI_MISO / UR1_RX / I2C0_SDA
CLDO	46	P	MCU Core power LDO 1.5V output. It is recommended to connect a 1μF capacitor as close as possible between this pin and VSS.
RFGND	EP	P	Exposed Pad on the bottom of the package. Internally connected to RFGND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

Legend: AI=Analog Input; AO=Analog Output; AIO=Analog Input/Output, DI=Digital Input; DO=Digital Output; P=Power

Pin Alternate Function Mapping

The BC32F7611 uses the same architecture as the Coretex-M0+ 32-bit Standard MCU (http://www.holtek.com.tw/producthome/-/pid/35/164/165), for the MCU file please directly refer to the HT32F52241 related documents (http://www.holtek.com.tw/productdetail/-/vg/HT32F52231-41_HT32F52331-41).

The following table is the Pin Alternate Function Mapping of the BC32F7611, note the difference between the BC32F7611 and HT32F52241 when using the HT32F52241 related documents.

	AF0	AF1	AF2	AF4	AF5	AF6	AF7	AF13	AF15
Pin No.	System Default	GPIO	ADC	GPTM /MCTM	SPI	USART /UART	I^2C	SCTM	System Other
4	PB9			MT_CH3					
5	X32KIN	PB10		GT_CH0		USR_TX		SCTM2	
6	X32KOUT	PB11		GT_CH1		USR_RX		SCTM3	
7	PB12				SPI_MISO	UR0_RX		SCTM0	WAKEUP
8	XTALIN	PB13				UR0_TX	I2C0_SCL		
9	XTALOUT	PB14				UR0_RX	I2C0_SDA		
10	PA9_BOOT				SPI_MOSI			SCTM3	CKOUT
11	SWCLK	PA12							
12	SWDIO	PA13							
13	PA14			MT_CH0		USR_RTS	I2C1_SCL		
14	PA15			MT_CH0N		USR_CTS	I2C1_SDA	SCTM1	
15	PB0			MT_CH1		USR_TX	I2C0_SCL		
16	PB1			MT_CH1N		USR_RX	I2C0_SDA	SCTM2	
17	PB2			MT_CH2	SPI_SEL	UR1_TX			
18	PB3			MT_CH2N	SPI_SCK	UR1_RX		SCTM1	
19	PB4			MT_BRK	SPI_MOSI	UR1_TX		SCTM0	
40	PA0		ADC_IN2	GT_CH0		USR_RTS	I2C1_SCL		
41	PA1		ADC_IN3	GT_CH1		USR_CTS	I2C1_SDA		
42	PA2		ADC_IN4	GT_CH2		USR_TX			
43	PA3		ADC_IN5	GT_CH3		USR_RX			
44	PA4		ADC_IN6	GT_CH0	SPI_SCK	UR1_TX	I2C0_SCL		
45	PA5		ADC_IN7	GT_CH1	SPI_MOSI	UR1_RX	I2C0_SDA		

Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage ..... V_{IN}-0.3V to V_{IN}+3.6V

Input Voltage ..... V_{IN}-0.3V to V_{IN}+0.3V

Storage Temperature ..... -50°C to 125°C

Operating Temperature .....0°C to 70°C

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

BLE D.C. Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Supply Voltage(Note)	—	2.2	3.3	3.6	V
Digital Inputs						
V_{IH}	High Level Input Voltage	—	0.7×V_{IN}	—	—	V
V_{IL}	Low Level Input Voltage	—	—		0.2×V_{IN}	V
I_{IH}	High Level Input Current	—	—	10	—	μA
I_{IL}	Low Level Input Current	—	—	10	—	μA
C_I	Input Capacitance	—	—	5	—	pF
Digital Outputs						
V_{OH}	High Level Output Voltage	I_{OH} = 1mA	V_{IN}-0.5	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 1mA	—	—	0.5	V
I_{OZ}	High Impedance Output Current	—	—	—	1	μA
Supply Current (Ta=25°C, V_{IN}=3.3V, unless otherwise specified)						
I_{RX}		RX Mode	—	14.5	—	mA
I_{TX}		TX Mode, 0dBm Output Power	—	9	—	mA
I_{SLEEP}		Idle Mode when MCU sleep	—	13	20	μA
I_{ACT}		Idle Mode when MCU active	—	2	—	mA
I_{PDN}		Power-Down	—	280	360	μA

Note: If the BC32F7611 device is operating under the condition where V_{IN}<2.2V, the LDO mode must be selected. However it will consume more power.

BLE A.C. Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter		Min.	Typ.	Max.	Unit
Crystal Oscillator						
	Frequency		—	32	—	MHz
	Frequency Accuracy Requirement		-40	—	40	ppm
ESR	Equivalent Series Resistance		—	—	100	Ω
C0	Crystal Shunt Capacitance		1.5	7	—	pF
CL	Crystal Load Capacitance		8	12	16	pF
RX Characteristics						
P_{SENS}	Sensitivity		—	-90	—	dBm
	Sensitivity(Dirty On)		—	-88	—	dBm
P_{IN}	Maximum Input Power		—	-5	—	dBm
CI0	In-band Blocking	Co-channel interference	—	12	—	dB
CI1		Interfere at f_{OFFS} = +/- 1MHz	—	-2/4	—	dB
CI2		Interfere at f_{OFFS} = +/- 2MHz	—	-25/-35	—	dB
CI3		Interfere at f_{OFFS} = +/- 3MHz	—	-40/-40	—	dB
CI4		Interfere at f_{IMAGE}	—	-35	—	dB
CI5		Interfere at f_{IMAGE} +/- 1MHz	—	4/-38	—	dB
	Out-of-band Blocking	f = 30 ~ 2000MHz	—	-20	—	dBm
		f = 2000 ~ 2399MHz	—	-25	—	dBm
		f = 2484 ~ 3000MHz	—	-25	—	dBm
		f = 3000 ~ 12750MHz	—	-30	—	dBm
	Intermodulation performance for wanted signal at -64dBm and 1 Mbps BLE, 3rd, 4th and 5th offset channel		—	-40	—	dBm
			—	—	—	—

Symbol	Parameter		Min.	Typ.	Max.	Unit
TX Characteristic						
P_{TX}	Output Power		-18	—	+3	dBm
	TX RF Output Steps		—	6	—	dB
ΔF2AVG	Average Frequency Deviation for 10101010 Pattern		—	230	—	kHz
ΔF1AVG	Average Frequency Deviation for 11110000 Pattern		—	260	—	kHz
EO	Eye Opening = ΔF2AVG/ΔF1AVG		—	0.88	—	
	Frequency Accuracy		-50	—	+50	kHz
	Maximum Frequency Drift		—	30	—	kHz
	Initial Frequency Drift		—	10	—	kHz
FDR	Drift Rate		—	0.2	—	kHz/50μs
	Spurious Emissions	Frequency < 2.4GHz	—	-50	—	dBm
		Frequency in 2.4 ~ 12GHz	—	-40	—	dBm
	In-band Emissions	< f ± 2MHz (f = 2400 ~ 2483.5MHz, P_{TX} = 0dBm)	—	-51	—	dBm
		> f ± 3MHz (f = 2400 ~ 2483.5MHz, P_{TX} = 0dBm)	—	-55	—	dBm

CLDO Voltage Regulator Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.0V regulator input @ I_{LDO} = 35mA, voltage variant = ±5% after trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0V regulator input @ V_{LDO} = 1.5V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	—	1	—	μF

Power Consumption

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current (Run Mode)	V_{DD} = 3.3V, HSE = 8MHz, PLL = 40MHz, f_{HCLK} = 40MHz, f_{PCLK} = 40MHz, all peripherals enabled	—	12	—	mA
		V_{DD} = 3.3V, HSE = 8MHz, PLL = 40MHz, f_{HCLK} = 40MHz, f_{PCLK} = 40MHz, all peripherals disabled	—	7	—	mA
		V_{DD} = 3.3V, HSE off, PLL off, LSI on, f_{HCLK} = 32kHz, f_{PCLK} = 32kHz, all peripherals enabled	—	45	—	μA
		V_{DD} = 3.3V, HSE off, PLL off, LSI on, f_{HCLK} = 32kHz, f_{PCLK} = 32kHz, all peripherals disabled	—	40	—	μA
	Supply Current (Sleep Mode)	V_{DD} = 3.3V, HSE = 8MHz, PLL = 40MHz, f_{HCLK} = 0MHz, f_{PCLK} = 40MHz, all peripherals enabled	—	7.5	—	mA
		V_{DD} = 3.3V, HSE = 8MHz, PLL = 40MHz, f_{HCLK} = 0MHz, f_{PCLK} = 40MHz, all peripherals disabled	—	2	—	mA
	Supply Current (Deep-Sleep1 Mode)	V_{DD} = 3.3V, all clock off (HSE/PLL/f_{HCLK}), LDO in low power mode, LSI on, RTC on	—	35	—	μA
	Supply Current (Deep-Sleep2 Mode)	V_{DD} = 3.3V, all clock off (HSE/PLL/f_{HCLK}), LDO off DMOS on, LSI on, RTC on	—	5	—	μA

Notes: 1. HSE means high speed external oscillator; HSI means 8MHz high speed internal oscillator.

2. LSE means 32.768kHz low speed external oscillator; LSI means 32kHz low speed internal oscillator.

3. RTC means real time clock.

4. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power-On Reset Threshold (Rising Voltage on V_{DD})	Ta = 0°C ~ 70°C	1.66	1.79	1.90	V
V_{PDR}	Power-Down Reset Threshold (Falling Voltage on V_{DD})		1.49	1.64	1.78	V
$V_{PORHYST}$	POR Hysteresis	—	—	150	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3V	—	0.1	0.2	ms

Notes: 1. Data based on characterization results only, not tested in production.

2. Guaranteed by design, not tested in production.

3. If the LDO is turned on, the VDD POR has to be in the de-assertion condition. When the VDD POR is in the assertion state then the LDO will be turned off.

LVD/BOD Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Brown Out Detection Voltage	Ta = 0°C ~ 70°C after factory-trimmed (V_{DD} falling edge)		2.02	2.1	2.18	V
V_{LVD}	Low Voltage Detection Voltage	Ta = 0°C ~ 70°C (V_{DD} falling edge)	LVDS = 000	2.17	2.25	2.33	V
			LVDS = 001	2.32	2.4	2.48	V
			LVDS = 010	2.47	2.55	2.63	V
			LVDS = 011	2.62	2.7	2.78	V
			LVDS = 100	2.77	2.85	2.93	V
			LVDS = 101	2.92	3.0	3.08	V
			LVDS = 110	3.07	3.15	3.23	V
			LVDS = 111	3.22	3.3	3.38	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 3.3V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3V	—	—	—	—	μs
I_{DDLVD}	Operation Current (3)	V_{DD} = 3.3V	—	—	5	15	μA

Notes: 1. Data based on characterization results only, not tested in production.

2. Guaranteed by design, not tested in production.

3. Bandgap current is not included.

4. The LVDS field is in the PWRCU LVDCSR register

External Clock Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High Speed External Clock (HSE) Characteristics						
V_{DD}	Operation Range	—	2.0	—	3.6	V
f_{HSE}	High Speed External Oscillator Frequency (HSE)	—	4	—	16	MHz
C_{LHSE}	Load Capacitance	V_{DD} = 3.3V, R_{ESR} = 100Ω @ 16MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT Pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3V, C_L = 12pF @16MHz, HSEDR= 0	—	—	160	Ω
		V_{DD} = 2.4V, C_L = 12pF @16MHz, HSEDR = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3V @ 16MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power-Down Current	V_{DD} = 3.3V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3V	—	—	4	ms
Low Speed External Clock (LSE) Characteristics						
V_{BAK}	Operation Range	—	2.0	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{BAK} = 2.0V ~ 3.6V	—	32.768	—	KHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{BAK} = 3.3V	30	—	TBD	kΩ
C_L	Recommended Load Capacitance	V_{BAK} = 3.3V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768kHz, R_{ESR} = 50kΩ, C_L ≥ 7pF, V_{BAK} = 2.0V ~ 2.7V, Ta = 0°C ~ 70°C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768kHz, R_{ESR} = 50kΩ, C_L < 7pF, V_{BAK} = 2.0V ~ 3.6V, Ta = 0°C ~ 70°C	—	1.8	3.3	μA
	Power-Down Current	—	—	—	0.01	μA
t_{suLSE}	Startup Time (Low Current Mode)	f_{CK_LSI} = 32.768kHz, V_{BAK} = 2.0V ~ 3.6V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the HSE/LSE crystal circuits in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
High Speed Internal Clock (HSI) Characteristics						
V_{DD}	Operation Range	—	2.0	—	3.6	V
f_{HSI}	HSI Frequency	V_{DD} = 3.3V @ 25°C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3V, Ta = 25°C	-2	—	2	%
		V_{DD} = 2.5V ~ 3.6V, Ta = 0°C ~ 70°C	-3	—	3	%
		V_{DD} = 2.0V ~ 3.6V, Ta = 0°C ~ 70°C	-4	—	4	%
Duty	Duty Cycle	f_{HSI} = 8MHz	35	—	65	%
I_{DDHSI}	Oscillator Supply Current	f_{HSI} = 8MHz	—	300	500	μA
	Power-Down Current		—	—	0.05	μA
t_{suHSI}	Startup Time	f_{HSI} = 8MHz	—	—	10	μs
Low Speed Internal Clock (LSI) Characteristics						
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	V_{DD} = 3.3V, Ta = 0°C ~ 70°C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3V, Ta = 25°C	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3V, Ta = 25°C	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3V, Ta = 25°C	—	—	100	μs

PLL Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	PLL Output Clock	—	16	—	40	MHz
t_{LOCK}	PLL Lock Time	—	—	200	—	μs

Flash Memory Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program/Erase Cycles before Failure (Endurance)	Ta = 0°C ~ 70°C	10	—	—	K cycles
t_{RET}	Data Retention Time	Ta = 0°C ~ 70°C	10	—	—	Years
t_{PROG}	Word Programming Time	Ta = 0°C ~ 70°C	20	—	—	μs
t_{ERASE}	Page Erase Time	Ta = 0°C ~ 70°C	2	—	—	ms
t_{MERASE}	Mass Erase Time	Ta = 0°C ~ 70°C	10	—	—	ms

I/O Ports Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3V I/O	$V_I = V_{SS}$, On-chip pull-up resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	3.3V I/O	$V_I = V_{DD}$, On-chip pull-down resister disabled	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	3.3V I/O		-0.5	—	V_{DD}×0.35	V
		Reset pin		-0.5	—	V_{DD}×0.35	V
V_{IH}	High Level Input Voltage	3.3V I/O		V_{DD}×0.65	—	V_{DD}+0.5	V
		Reset pin		V_{DD}×0.65	—	V_{DD}+0.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3V I/O		—	0.12×V_{DD}	—	mV
		Reset pin		—	0.12×V_{DD}	—	mV
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3V I/O 4mA drive, V_{OL} = 0.4V		4	—	—	mA
		3.3V I/O 8mA drive, V_{OL} = 0.4V		8	—	—	mA
		3.3V I/O 12mA drive, V_{OL} = 0.4V		12	—	—	mA
		3.3V I/O 16mA drive, V_{OL} = 0.4V		16	—	—	mA
		Backup Domain I/O drive @ V_{DD} = 3.3V, V_{OL} = 0.4V, PB10, PB11, PB12		4	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	3.3V I/O 4mA drive, V_{OH} = V_{DD} - 0.4V		4	—	—	mA
		3.3V I/O 8mA drive, V_{OH} = V_{DD} - 0.4V		8	—	—	mA
		3.3V I/O 12mA drive, V_{OH} = V_{DD} - 0.4V		12	—	—	mA
		3.3V I/O 16mA drive, V_{OH} = V_{DD} - 0.4V		16	—	—	mA
		Backup Domain I/O drive @ V_{DD} = 3.3V, V_{OL} = V_{DD} - 0.4V, PB10, PB11, PB12		—	—	2	mA
V_{OL}	Low Level Output Voltage	3.3V 4mA drive I/O, I_{OL} = 4mA		—	—	0.4	V
		3.3V 8mA drive I/O, I_{OL} = 8mA		—	—	0.4	V
		3.3V 12mA drive I/O, I_{OL} = 12mA		—	—	0.4	V
		3.3V 16mA drive I/O, I_{OL} = 16mA		—	—	0.4	V
V_{OH}	High Level Output Voltage	3.3V 4mA drive I/O, I_{OH} = 4mA		V_{DD}-0.4	—	—	V
		3.3V 8mA drive I/O, I_{OH} = 8mA		V_{DD}-0.4	—	—	V
		3.3V 12mA drive I/O, I_{OL} = 12mA		V_{DD}-0.4	—	—	V
		3.3V 16mA drive I/O, I_{OL} = 16mA		V_{DD}-0.4	—	—	V
R_{PU}	Internal Pull-up Resistor	3.3V I/O		—	46	—	kΩ
R_{PD}	Internal Pull-down Resistor	3.3V I/O		—	46	—	kΩ

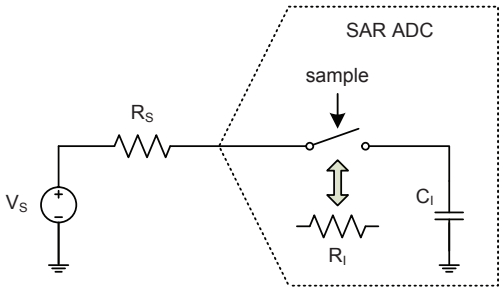
ADC Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.7	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3V	—	1	TBD	mA
I_{ADC_DN}	Power-Down Current Consumption	V_{DDA} = 3.3V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	MHz
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	—	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup Up Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750kHz, V_{DDA} = 3.3V	—	±2	±5	LSB
DNL	Differential Non-linearity Error	f_S = 750kHz, V_{DDA} = 3.3V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Notes: 1. Guaranteed by design, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately equal to $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.



ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} \quad R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

SCTM/GPTM/MCTM Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for GPTM	—	—	—	40	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	f_{TM}
f_{EXT}	External Single Frequency on Channel 1~4	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time	0	—	0	—	0	—	ns
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

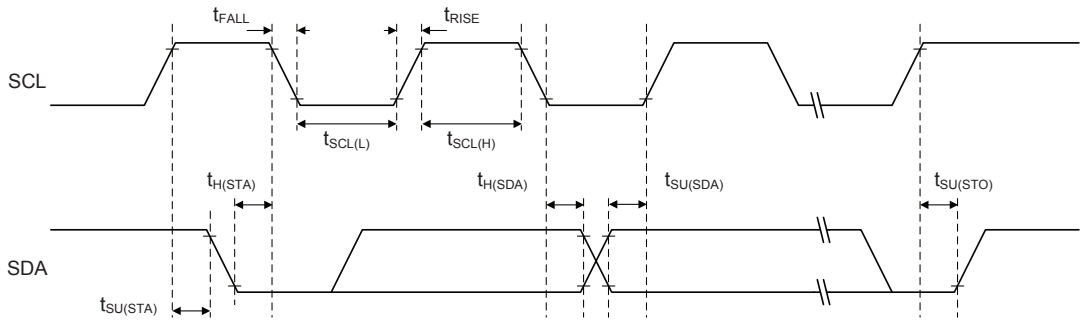
Notes: 1. Guaranteed by design, not tested in production.

2. To achieve 100kHz standard mode, the peripheral clock frequency must be higher than 2MHz.

3. To achieve 400kHz fast mode, the peripheral clock frequency must be higher than 8MHz.

4. To achieve 1MHz fast mode plus, the peripheral clock frequency must be higher than 20MHz.

5. The above characteristic parameters of the I²C bus timing are based on: SEQ_FILTER = 01 and COMB_FILTER_En is disabled.



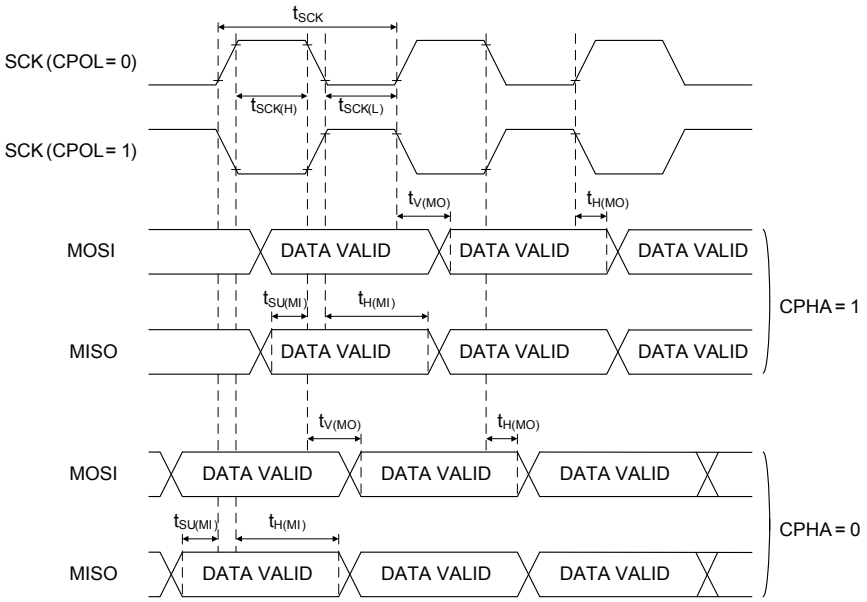
I²C Timing Diagram

SPI Characteristics

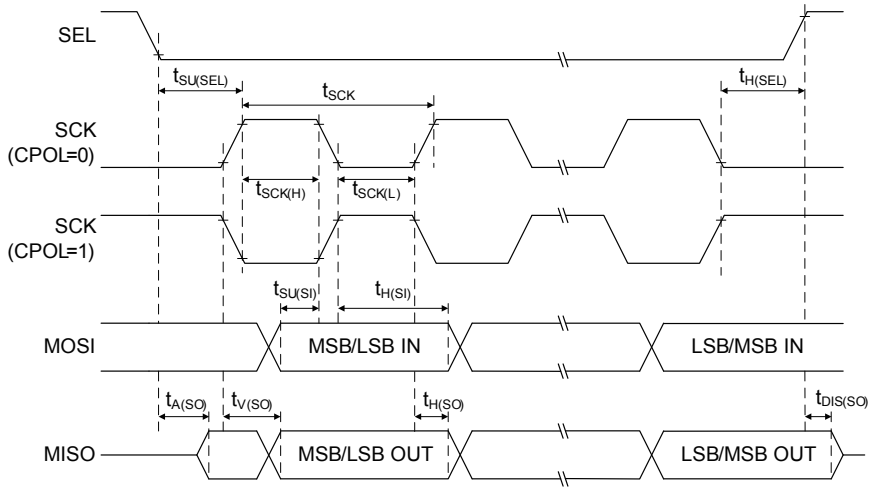
Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK} ($1/t_{SCK}$)	SPI Master Output SCK Clock Frequency	Master mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2-2$	—	$t_{SCK}/2+1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK} ($1/t_{SCK}$)	SPI Slave Input SCK Clock Frequency	Slave mode SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3\times t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2\times t_{PCLK}$	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3\times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: $t_{SCK} = 1/f_{SCK}$; $t_{PCLK} = 1/f_{PCLK}$. f_{SCK}: SPI output (input) clock frequency; f_{PCLK}: SPI peripheral clock frequency.



SPI Timing Diagram – SPI Master Mode



SPI Timing Diagram – SPI Slave Mode with CPHA=1

Functional Description

MCU Core

The Cortex®-M0+ core is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O port, hardware multiplier and low latency interrupt respond time.

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 40MHz operating frequency
- 0.93 DMIPS/MHz (Dhrystone v2.1)
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

Bluetooth Low Energy controller – BLE

It is designed to act as a BLE slave according to the Bluetooth specification v4.1.

- On-chip capacitors in the 32MHz crystal circuit to reduce the BOM
- On-chip DC/DC converter for a wide power range of the BLE controller
- 75dB RX gain and the gain step is programmable
- Support Sleep and Power-Down mode for low power consumption
- Embedded patch memory to reduce system effort and cost

On-Chip Memory

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripheral. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. The Memory Map chapter shows the memory map of the BC32F7611 device, including code, SRAM, peripheral, and other pre-defined regions.

- 64KB on-chip Flash memory for instruction/data and options storage
- 8KB on-chip SRAM
- Supports multiple boot modes

Flash Memory Controller – FMC

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program / page erase functions are also provided.

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

Reset Control Unit – RSTCU

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

- Supply supervisor
  - Power On Reset/Power-Down Reset – POR/PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

MCU Clock Control Unit – CKCU

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source.

- External 4 to 16MHz crystal oscillator
- External 32.768kHz crystal oscillator
- Internal 8MHz RC oscillator trimmed to ±2 % accuracy at 3.3V operating voltage and 25°C operating temperature
- Internal 32kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

Power Management – PWRCU

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in this device provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

- Single V_{DD} power supply: 2.0V to 3.6V
- Integrated 1.5V LDO regulator for CPU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- Two power domains: V_{DD}, 1.5V
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

External Interrupt/Event Controller – EXTI

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

- 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

Analog to Digital Converter – ADC

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 6 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

- 12-bit SAR ADC engine
- Up to 1Msps conversion rate
- 6 external analog input channels

I/O Ports – GPIO

There are 22 General Purpose I/O pins, GPIO, named from Port A ~ B for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

- 22 GPIOs
- Port A and B are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have a configurable output driving current

Motor Control Timer – MCTM

The Motor Control Timer consists of a single 16-bit up/down counter, four 16-bit CCRs (Capture/Compare Registers), single one 16-bit counter-reload register (CRR), single 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

- One 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Supports 3-phase motor control and hall sensor interface
- Break input to force the timer's output signals into a reset or fixed condition

PWM Generation and Capture Timers – GPTM

The General Purpose Timer consists of one 16-bit up/down counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

- One 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

Single Channel Generation and Capture Timers – SCTM

The Single-Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output.

- One 16-bit up and auto-reload counter
- One channel for each timer
- 16-bit programmable prescaler allowing counter clock frequency division by any factor between 1 and 65536
- Compare Match Output
- PWM waveform generation with Edge-aligned
- Single Pulse Mode Output

Basic Function Timer – BFTM

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

- One 32-bit compare/match count-up counter – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restart counter after a match condition

Watchdog Timer – WDT

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

- 12-bit down counter with 3-bit prescaler
- Reset event for the system
- Programmable watchdog timer window function
- Register write protection function

Real Time Clock – RTC

The Real Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the VDD15 power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the VDD15 power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

Inter-integrated Circuit – I^2C

The I^2C is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides three data transfer rates: 100kHz in the Standard mode, 400kHz in the Fast mode and 1MHz in the Fast Plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I^2C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

- Supports both master and slave modes with a frequency of up to 1MHz
- Provide an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

Serial Peripheral Interface – SPI

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

- Supports both master and slave mode
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

Universal Synchronous Asynchronous Receiver Transmitter – USART

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, (TX_FIFO) and receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud rate up to (f_{PCLK}/16) MHz and synchronous operating rate up to (f_{PCLK}/8) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8×9 bits for both receiver and transmitter

Universal Asynchronous Receiver Transmitter – UART

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

- Asynchronous serial communication operating baud-rate up to f_{PCLK}/16 MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error

Cyclic Redundancy Check – CRC

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, then this means that the data stream contains a data error.

- Support CRC16 polynomial: 0x8005, $X^{16}+X^{15}+X^2+1$
- Support CCITT CRC16 polynomial: 0x1021, $X^{16}+X^{12}+X^5+1$
- Support IEEE-802.3 CRC32 polynomial: 0x04C11DB7, $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum.
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

BLE Application Controller Interface

The BC32F7611 BLE function is set by the internal SPI interface. For the BLE protocol, the Write FIFO command must be sent first for each CMD from the host to the BLE controller and the read FIFO command must be sent first for each Return operation. Data follows the little-endian format. Commands are shown below.

Abbreviation	Explanation
BD	Bluetooth Device
BD_Addr	Bluetooth Device Address
BD_Name	Bluetooth Device Name

Opcode	Read Command	Write Command	Description
0x30	IntvRead		Read connection interval setting (only valid when connected)
0x31	BDNameRead	BDNameWrite	Read / write Bluetooth device name
0x32	BaudRateRead	BaudRateWrite	Read / write UART baud rate
0x33	BDAddrRead	BDAddrWrite	Read / write Bluetooth device address
0x35	AdvIntvRead	AdvIntvWrite	Read / write Bluetooth device advertising interval
0x36	AdvDataRead	AdvDataWrite	Read / write manufacturer specific data field of advertising packet
0x37	WhiteListRead	WhiteListWrite	Read / write white list, devices which are not in white list will be rejected
0x38	TxPowerRead	TxPowerWrite	Read / write RF TX power
0x3B		BatteryLevelWrite	Update Battery level let cell phone to read it
0x3F		BaudRateUpdate	Update new baud rate (baud rate must be set by BaudRateWrite first)
0x40		IntvLatencyWrite2	Write connection interval setting
0x50		AdvDataWrite2	Write whole advertising packet
0x51		ScanResDataWrite	Write whole scan response packet
0x5F		DisconnectWrite	Force to disconnect

Type	Dir.	Header	Payload										
		1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	...	Nth
Read Command	M→S	0x20	Opcode (byte×1)										
Read Event	M←S	0x21	Opcode (byte×1)	Length (byte×1)	Data (byte×Length, MSB)								
Payload Packet Command	M↔S	0x22	Length (byte×1 max=200)	RF Payload (byte×Length, MSB)									
Write Command	M→S	0x25	Opcode (byte×1, unit=byte×1)	Length (byte×1)	Data (byte×Length, MSB)								
Write Event / Payload Packet Event	M←S	0x26	Opcode (byte×1, unit=byte×1)	Result (byte×1)									
Write Physical Address	M→S	0x55	Length (byte×1, unit=byte×4, max=60)	Reserved (byte×2)		Address (byte×4,LSB)				Data (byte×Length×4,LSB)			
Read Physical Address	M→S	0x56	Length (byte×1, unit=byte×4, max=60)	Address (byte×4)									
Read Physical Address Return	M←S	0x57	Length (byte×1, unit=byte×4, max=60)	Reserved (byte×2)		Address (byte×4,LSB)				Data (byte×Length×4,LSB)			

BLE ACI Protocol

Notes: 1. "Dir." Means the transfer detection.

2. "M→S": from Master to Slave;
   "M←S": from Slave to Master;
   where "M" is the MCU and "S" is the BLE device.

3. "Reserved" means 0x00.

BLE Control Interface

The inner connection between the MCU and BLE controller is described as below. The device includes a 5-wire, 8-bit, MSB-first, Motorola-compatible with CPOL = 0 and CPHA = 0 SPI interface. The interface has the following features.

- Clock speed up to 10MHz
- Supports Mode 0 only
- Integrated 32 bytes RX/TX FIFOs for continuous bursts.

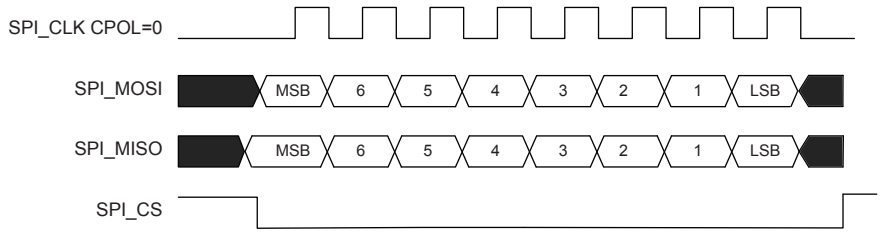
BLE SPI Signal name

BLE Signal Name	In/Out	BLE SPI Description
SPI_CLK	In	Clock
SPI_MOSI	In	Master output slave input
SPI_MISO	Out	Master input slave output
SPI_CS	In	Enable
SPI_INT	Out	Interrupt request

BLE SPI Signal Function

Protocol and Timing

The BLE SPI timing diagram is shown below.



BLE SPI Timing Diagram

BLE Command Format and Timing

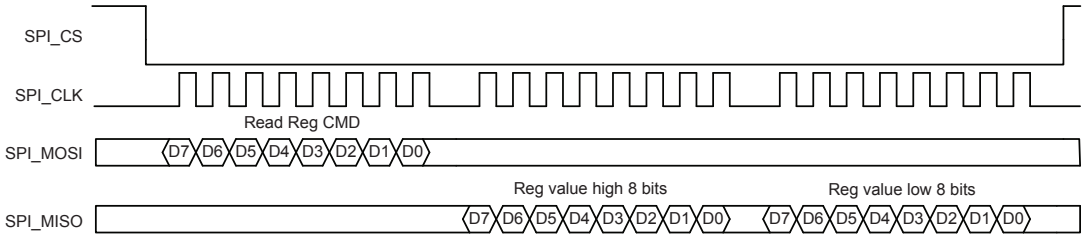
The BLE registers can be accessed by both the host and controller for getting or configuring the status of BLE controller.

BLE Register name	BLE Register Address	Parameter Value Description
Threshold	0x00	Bit[11:6]: BLE TX FIFO threshold Bit[5:0]: BLE RX FIFO threshold
Int_status	0x01	Interrupt status: Bit[4]: BLE RX FIFO not empty Bit[3]: BLE RX FIFO overflow Bit[2]: BLE RX FIFO over threshold Bit[1]: BLE RX FIFO empty Bit[0]: BLE RX FIFO under threshold
Int_Set	0x02	Interrupt Enable: For detail bits definition, refer to Int_status. Set 1 to enable INT
Int_Clr	0x03	Interrupt clear, write only For detail definition, refer to Int_status. Set 1 to clear the status bit
FIFOCount	0x04	Bit[11:6]: BLE TX FIFO count Bit[5:0]: BLE RX FIFO count

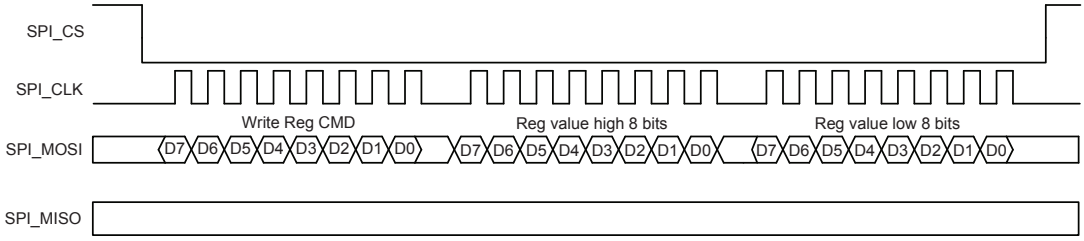
BLE SPI Interface Register Description

BLE CMD FORMAT		
CMD Name	Bit[7:5]	Bit[4:0]
Read Register	000b	Bit[4:1]: BLE Register address, bit[0] =1
Write Register	001b	Bit[4:1]: BLE Register address, bit[0] =1
Read FIFO	011b	Bit[4:0]=data length, 0 means 32 bytes, 1 means 1 byte
Write FIFO	101b	Bit[4:0]=data length, 0 means 32 bytes, 1 means 1 byte

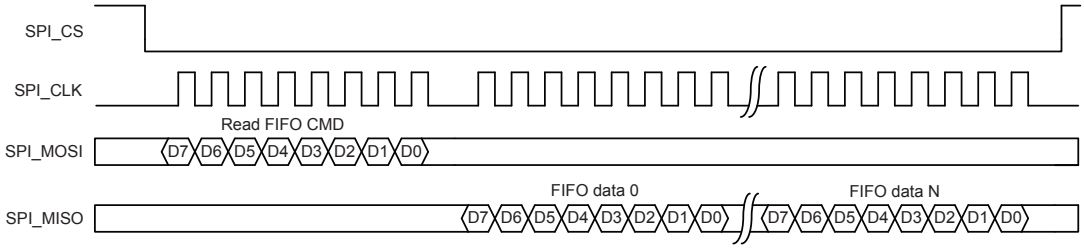
BLE SPI Register and FIFO Operation List



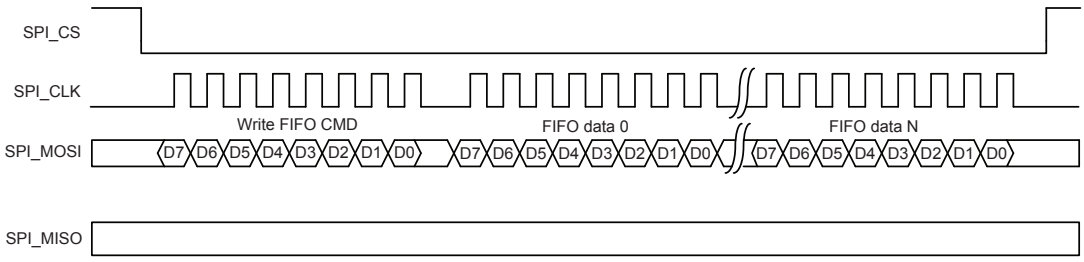
Read BLE Register Operation



Write BLE Register Operation



Read BLE FIFO Operation



Write BLE FIFO Operation

Sleep and Wake-up

The WAKEUP pin is used for the BC32F7611 operation mode setting. When the WAKEUP pin is low, the BLE can enter the sleep mode and the BC32F7611 can check the operation mode by monitoring the STATE pin. When the BLE controller is in Sleep mode, it can be woken up by the internal BLE_SPI or the WAKEUP pin.

Power-Down Mode

The PDN pin is used for the BLE power-down mode setting. If the PDN pin pulled low, the BLE controller will enter the power-down mode and all internal clocks will be disabled.

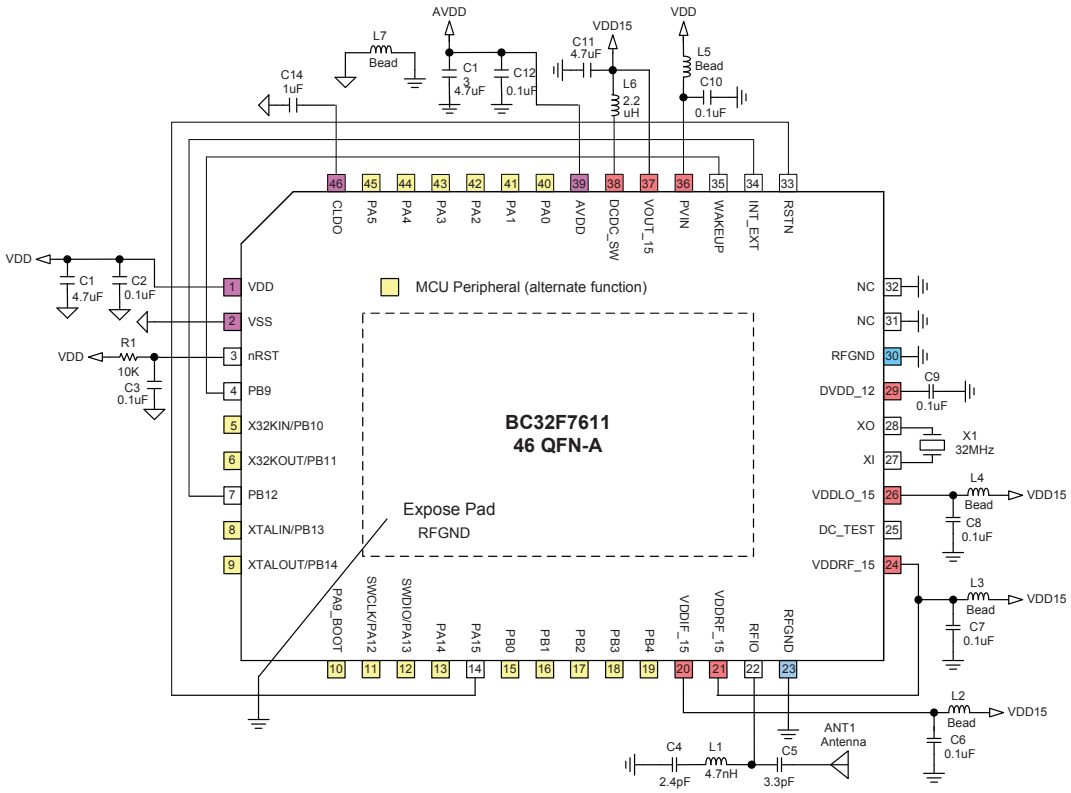
External Interrupt

The BLE controller provides an INT_EXT pin to output the interrupt signal of the microcontroller. If the INT_EXT pin is low, it means the valid data is ready.

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code/literal patch
- 2 comparators for hardware watch points

Application Circuits



Note: All decoupling capacitors should be located as close to the device pins as possible.

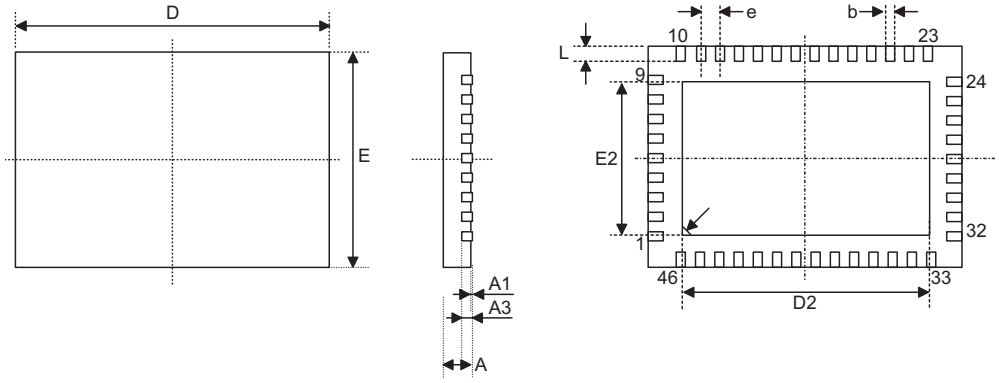
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

SAW Type 46-pin (6.5mm×4.5mm) QFN Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.031	0.033	0.035
A1	0.000	0.001	0.002
A3	—	0.008 BSC	—
b	0.006	0.008	0.010
D	0.254	0.256	0.258
E	0.175	0.177	0.179
e	—	0.016 BSC	—
D2	0.197	0.201	0.205
E2	0.118	0.122	0.126
L	0.012	0.016	0.020
K	—	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	0.020	0.040
A3	—	0.200 BSC	—
b	0.150	0.200	0.250
D	6.450	6.500	6.550
E	4.450	4.500	4.550
e	—	0.40 BSC	—
D2	5.00	5.10	5.20
E2	3.00	3.10	3.20
L	0.30	0.40	0.50
K	—	—	—