RFID NFC Type 2 Tag IC with I²C Interface and Energy Harvesting

BC45B4211

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Features

- Compatible with ISO/IEC 14443A standard
- NFC Forum Type 2 Tag compliant
- Cascaded two level 7-byte serial number
- Get Version command supported
- 50pF resonant capacitance
- I²C slave
- Configurable FD (Field Detector) pin for open drain output
- Pass-through mode with 64-byte SRAM buffer
- FWRITE and FREAD commands for NFC higher data throughput
- Full access, read only or no read/write access configured by setting AUTH0 and 32-bit password and related protection bits
- Energy harvesting from NFC field, also provide DC supply output to external logic devices
- 13.56MHz operating frequency
- 100% ASK demodulator from NFC
- 106kbps data rate from NFC
- Manchester encoding TX data output from NFC
- ECC based originality check signature

Memory

- 1K bytes of EEPROM none-volatile memory
- 64 bytes of SRAM buffer for data transfer between NFC and I²C
- 4 bytes of OTP user memory in Page 03 from NFC interface
- Each page is organized in 4 bytes for NFC interface
- Each block is organized in 16 bytes for I²C interface
- Data retention up to 20 years
- Write endurance time is up to 100,000 cycles

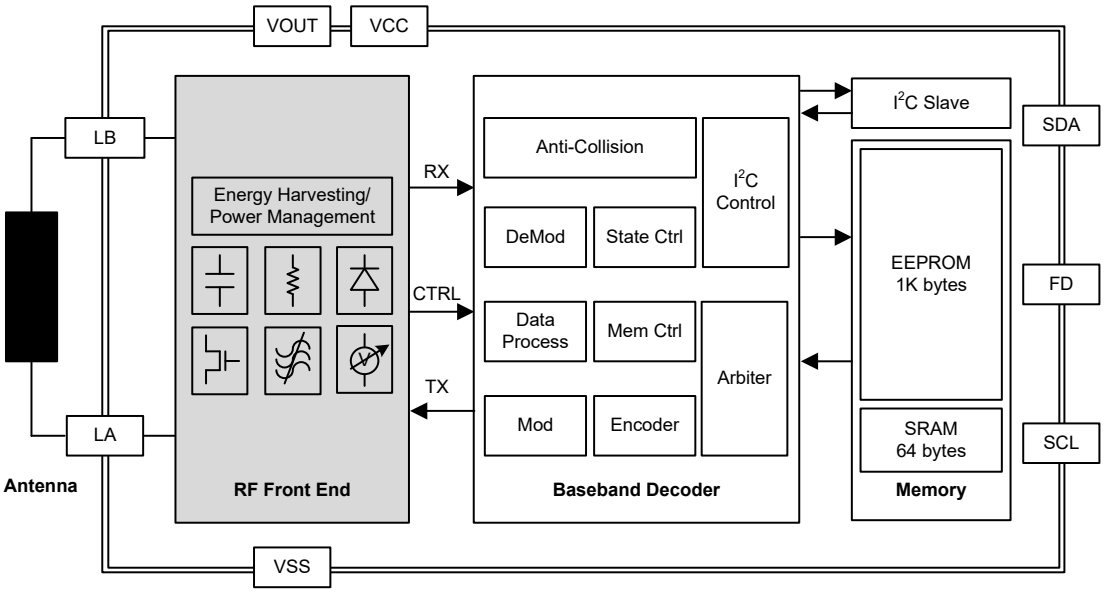
I²C Interface

- I²C slave interface supports up to 400kHz
- 7-bit slave address
- Default slave address is 55h

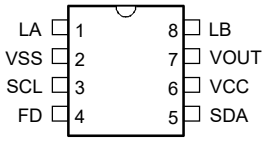
General Description

The BC45B4211 is a contactless RFID Tag IC, for use with NFC application devices according to ISO/IEC 14443A standard and NFC Forum Type 2 tag. The communication protocol complies with parts 2 and 3 of the ISO/IEC 14443A specification. Target applications include retail, smart poster, Wi-Fi or Bluetooth auto-pairing, product anti-fake and product authentication, etc.

Block Diagram



Pin Assignment



BC45B4211
8 SOP-A

Pin Description

Pin Name	Type	Description
LA	AN	Antenna connection
LB	AN	Antenna connection
VOUT	O	Energy harvesting voltage output
VCC	PWR	External power supply input
SDA	I/O	I²C serial data
FD	O	Field detector
SCL	I	I²C serial clock
VSS	PWR	Ground

Legend: I: Input; O: Output; AN: Analog signal; PWR: Power

Absolute Maximum Rating

Symbol	Parameter	Condition	Min.	Max.	Unit
T_{sto}	Storage Temperature	—	-55	125	°C
T_j	Junction Temperature	—	—	105	°C
V_{ESD}	Electrostatic Discharge Voltage (Human Body Model)	—	—	2	kV
V_{ESD}	Electrostatic Discharge Voltage (Charge Device Model)	—	—	200	V
V_{DD}	Supply Voltage	On pin VCC	-0.5	4.6	V
V_i	Input Voltage	On pins FD, SDA, SCL	-0.5	4.6	V
I_i	Maximum Input Peak Current	$I_{Max\ LA-LB}$	—	40	mA
$V_{i(RF)}$	RF Input Voltage	$V_{Max\ LA-LB}$	—	4.6	V_{peak}

D.C. Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
C_{in}	Input Capacitance	LA-LB, on-chip C_{IC}, f=13.56MHz, V_{LA-LB}=2.4V_{RMS}	44	50	56	pF
f_{OP}	Operating Frequency	—	—	13.560	—	MHz
T_{amb}	Operating Ambient Temperature	—	-40	25	105	°C
R_{TH_JA}	Thermal Resistance	JEDEC 2s2p board and 8-pin SOP package	—	115	—	K/W
Energy Harvesting Characteristics						
$V_{out,max}$	Output Voltage	Generated at the VOUT pin, Class 5 antenna, 14A/m, load current 1mA	—	—	3	V
I²C Interface Characteristics						
V_{CC}	Supply Voltage	Supply via V_{CC} only	2.0	—	3.6	V
I_{DD}	Supply Current	V_{CC}=1.8V I²C, Idle bus	—	160	—	μA
		V_{CC}=3.3V I²C, Idle bus	—	195	—	μA
		V_{CC}=1.8V I²C @ 400kHz	—	—	185	μA
		V_{CC}=2.5V I²C @ 400kHz	—	—	210	μA
		V_{CC}=3.3V I²C @ 400kHz	—	—	240	μA
I²C Pin Characteristics						
V_{OL}	Low Level Output Voltage	I_{OL}=3mA, V_{CC}>2V	—	—	0.4	V
		I_{OL}=2mA, V_{CC}<2V	—	—	0.2V_{CC}	V
V_{IH}	High Level Input Voltage	—	0.7V_{CC}	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	0.3V_{CC}	V
C_i	Input Capacitance	SCL and SDA pins	—	2.4	—	pF
I_L	Leakage Current	0V and $V_{CC,max}$	—	—	10	μA
t_{HIGH}	SCL High Time	Fast mode 400kHz	950	—	—	ns
FD Pin Characteristics						
V_{OL}	Low Level Output Voltage	I_{OL}=4mA, V_{CC}>2V	—	—	0.4	V
		I_{OL}=3mA, V_{CC}<2V	—	—	0.2V_{CC}	V
I_L	Leakage Current	—	—	1.5	10	μA
EEPROM Characteristics						
t_{ret}	Data Retention	T_{amb}	—	10	—	Years
n_{wr}	Write Endurance	—	—	100,000	—	Cycles

Functional Description

Anti-collision

The BC45B4211's anti-collision function allows multiple RFID tags operating in reader's magnetic field simultaneously. The anti-collision function enables the detection and operation of the BC45B4211 when other BC45B4211 equipped tags are also present.

Cascaded Unique Identification Number

The BC45B4211's unique identification number (UID) is 7 bytes long and supports cascade level 2 format according to ISO/IEC 14443A-3.

Memory Mapping

• NFC interface:

Page		Byte 0	Byte 1	Byte 2	Byte 3	
Dec	Hex					
0	00	UID0	UID1	UID2	UID3	R
1	01	UID4	UID5	UID6	SAK	R
2	02	ATQA0	ATQA1	Lock0	Lock1	R, R/W
3	03	OTP0(E1)	OTP1(10)	OTP2(6D)	OTP3(00)	R/W
4	04	Data0(03)	Data1(00)	Data2(FE)	Data3(00)	R/W
:	:	:	:	:	:	:
:	:	:	:	:	:	:
225	E1	Data884	Data885	Data886	Data887	R/W
226	E2	DLOCK0	DLOCK1	DLOCK2	RFU(0x00)	R/W
227	E3	RFU	RFU	RFU	AUTH0	R/W
228	E4	ACCESS	RFU	RFU	RFU	R/W
229	E5	PWD00	PWD01	PWD02	PWD03	R/W
230	E6	PACK0	PACK1	RFU	RFU	R/W
231	E7	PT_I2C	RFU	RFU	RFU	R/W
232	E8	CFG00 (NC_REG)	CFG01 (LAST_NDEF_BLOCK)	CFG02 (SRAM_MIRROR_BLOCK)	CFG03 (WDT_LS)	R/W
233	E9	CFG04 (WDT_MS)	CFG05 (I2C_CLOCK_STR)	CFG06 (REG_LOCK)	CFG07 (RFU)	R/W
234	EA	Invalid	Invalid	Invalid	Invalid	—
235	EB	Invalid	Invalid	Invalid	Invalid	—
236	EC	SR00 (NC_REG)	SR01 (LAST_NDEF_BLOCK)	SR02 (SRAM_MIRROR_BLOCK)	SR02 (WDT_LS)	R
237	ED	SR03 (WDT_MS)	SR04 (I2C_CLOCK_STR)	SR05 (NS_REG)	SR06 (RFU)	R
238	EE	Invalid	Invalid	Invalid	Invalid	—
:	:	:	:	:	:	:
:	:	:	:	:	:	:
255	FF	Invalid	Invalid	Invalid	Invalid	—

Memory Mapping Table from NFC

• **I²C interface:**

Block			Byte 0	Byte 1	Byte 2	Byte 3	
Sector	Dec	Hex					
0	0	00	UID0	UID1	UID2	UID3	R/W
			UID4	UID5	UID6	SAK	
			ATQA0	ATQA1	Lock0	Lock1	
			CC0(E1)	CC1(10)	CC2(6D)	CC3(00)	
	1	01	Data0(03)	Data1(00)	Data2(FE)	Data3(00)	R/W
	:	:	:	:	:	:	:
	:	:	:	:	:	:	:
	56	38	Data880	Data881	Data882	Data883	R/W
			Data884	Data885	Data886	Data887	
			DLOCK0	DLOCK1	DLOCK2	RFU(0x00)	
			RFU	RFU	RFU	AUTH0	
	57	39	ACCESS	RFU	RFU	RFU	R/W
			PWD00	PWD01	PWD02	PWD03	
			PACK0	PACK1	RFU	RFU	
			PT_I2C	RFU	RFU	RFU	
	58	3A	CFG00 (NC_REG)	CFG01 (LAST_NDEF_BLOCK)	CFG02 (SRAM_MIRROR_BLOCK)	CFG03 (WDT_LS)	R/W
			CFG04 (WDT_MS)	CFG05 (I2C_CLOCK_STR)	CFG06 (REG_LOCK)	CFG07 (RFU)	
			00	00	00	00	
			00	00	00	00	
	59	3B	SR00 (NC_REG)	SR01 (LAST_NDEF_BLOCK)	SR02 (SRAM_MIRROR_BLOCK)	SR03 (WDT_LS)	R/W
			SR04 (WDT_MS)	SR05 (I2C_CLOCK_STR)	SR06 (NS_REG)	SR07 (RFU)	
			00	00	00	00	
			00	00	00	00	
	60	3C	Invalid	Invalid	Invalid	Invalid	—
	:	:	:	:	:	:	:
	:	:	:	:	:	:	:
	63	3F	Invalid	Invalid	Invalid	Invalid	—
1	64	40	Invalid	Invalid	Invalid	Invalid	—
	:	:	:	:	:	:	:
	:	:	:	:	:	:	:
	127	7F	Invalid	Invalid	Invalid	Invalid	—
2	128	80	Invalid	Invalid	Invalid	Invalid	—
	:	:	:	:	:	:	:
	:	:	:	:	:	:	:
	191	BF	Invalid	Invalid	Invalid	Invalid	—
3	192	C0	Invalid	Invalid	Invalid	Invalid	—
	:	:	:	:	:	:	:
	:	:	:	:	:	:	:
	247	F7	Invalid	Invalid	Invalid	Invalid	—
	248	F8	SRAM00	SRAM01	SRAM02	SRAM03	R/W

Block			Byte 0	Byte 1	Byte 2	Byte 3	
Sector	Dec	Hex					
3	:	:	:	:	:	:	:
	:	:	:	:	:	:	:
	251	FB	SRAM60	SRAM61	SRAM62	SRAM63	R/W
	252	FC	Invalid	Invalid	Invalid	Invalid	—
	253	FD	Invalid	Invalid	Invalid	Invalid	—
	254	FE	SR00 (NC_REG)	SR01 (LAST_NDEF_BLOCK)	SR02 (SRAM_MIRROR_BLOCK)	SR03 (WDT_LS)	R/W
			SR04 (WDT_MS)	SR05 (I2C_CLOCK_STR)	SR06 (NS_REG)	SR07 (RFU)	R/W
			00	00	00	00	—
			00	00	00	00	—
	255	FF	Invalid	Invalid	Invalid	Invalid	—

Memory Mapping Table from I²C

Version Table

Byte	Name	Code	Description
0	Fixed Header	0x00	—
1	Vendor ID	0x7E	Holtek
2	Product type	0x04	NFC Tag
3	Product subtype	0x05	50pF capacitance, I²C, Field detection
4	Major product version	0x01	Version 1.x
5	Minor product version	0x00	Version x.0
6	Storage size	0x13	888 bytes: 2^9~2^{10}
7	Protocol type	0x03	ISO/IEC 14443A-3 compliant

Version Table

Unique Identifier (UID)

The UID, in ISO/IEC 14443A format, is programmed by IC manufacturer during production process and cannot be changed afterwards.

56 9	8 1
IC Manufacturer Serial Number	IC Mfg Code (0x7E)

Bit 56~Bit 9: 48-bit unique serial number

Bit 8~Bit 1: IC manufacturer code for Holtek

Capability Container (CC Bytes)

Page 03 (Default value is 00 00 00 00):

Byte 00	Byte 01	Byte 02	Byte 03
0xE1	0x10	0x6D	0x00

Byte 00: 0xE1, Magic number, to indicate that NFC Forum defined data is stored in the data area.

Byte 01: 0x10, Version number of NFC document supported by the Type 2 Tag Platform. "1" indicates the major version number and the "0" indicates the minor version number.

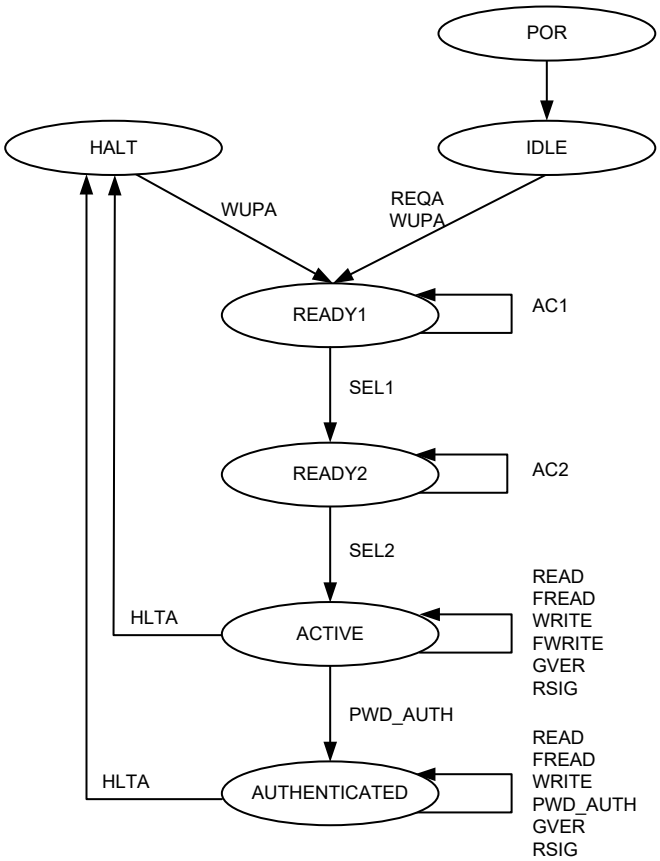
Byte 02: 0x6D, indicates the memory size of the data area of the Type 2 Tag Platform.

Byte 03: 0x00, indicates the read and write access capability of the data area and CC area of the Type 2 Tag Platform.

- The most significant nibble (the 4 most significant bits) indicates the read access condition:
  - The value 0h indicates read access granted without any security.
  - The values from 1h to 7h and Fh are reserved for future use.
  - The values from 8h to Eh are proprietary.
- The least significant nibble (the 4 least significant bits) indicates the write access condition:
  - The value 0h indicates write access granted without any security.
  - The values from 1h to 7h are reserved for future use.
  - The values from 8h to Eh are proprietary.
  - The value Fh indicates no write access granted at all.

State Diagram

The state diagram shown below describes the operation of the BC45B4211. For detailed explanation of state definition, please refer to ISO/IEC 14443A-3 documents.



Important Notice: The BC45B4211 does not support ISO/IEC 14443A-4.

Command List

	Command	Command Code	Description
1	REQA	0x26	Request Type A
2	WUPA	0x52	Wake-up Type A
3	AC1/SEL1	0x93	Anti-collision and select for 1st layer anti-collision
4	AC2/SEL2	0x95	Anti-collision and select for 2nd layer anti-collision
5	HLTA	0x50	Halt Type A
6	GVER	0x60	Get version
7	READ	0x30	Read page data
8	FREAD	0x3A	Fast read
9	WRITE	0xA2	Write page data
10	FWRITE	0xA6	Fast write page data
11	SEC_SEL	0xc2	Sector select
12	PWD_AUTH	0x1B	Password authentication
13	RSIG	0x3C	Read signature

Command Table

Static Lock Control Registers

Page 02: (Byte 2 and Byte 3)

Lock0								Lock1							
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
L	L	L	L	L	BL	BL	BL	L	L	L	L	L	L	L	L
7	6	5	4	OTP	15~10	9~4	OTP	15	14	13	12	11	10	9	8

Static Lock Bytes

In Page 2 data, Byte 2 and Byte 3 are lock control and status of the user's memory Page 3~Page 15. Lock Byte 0 (Lock0) is used for Page 3~Page 7 and Block Lock Control. Lock Byte 1 (Lock1) is used for Page 8~Page 15.

In the table above, L means lock control and lock status of the relative Page data. The data value cannot be changed afterward after the relative Lock bit is set to "1" and become a read-only Page. BL in Lock0 bit 0~bit 2 means Block Locking of the Lock byte. As soon as BL is set to "1", the relative block control bit (L, in Lock0 and Lock1) would become write inhibited, and cannot be changed afterward. These two Lock bytes are one time programmed bytes.

Note: 1. The data contents of byte 0 and byte 1 in Page 2 would be not affected by write command to Page 2.

2. These bytes can be reset to 0 by I²C interface.

Dynamic Lock Control Registers

Page E2h: (Byte 0, Byte 1 and Byte 2)

DLOCK0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L128~143	L112~127	L96~111	L80~95	L64~79	L48~63	L32~47	L16~31

Dynamic Lock Byte 0

DLOCK1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	L224~225	L208~223	L192~207	L176~191	L160~175	L144~159

Dynamic Lock Byte 1

DLOCK2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	BL208~225	BL176~207	BL144~175	BL112~143	BL80~111	BL48~79	BL16~47

Dynamic Lock Byte 2

In Page E2 data, Byte 0, Byte 1 and Byte 2 are lock control and status of the user's memory Page 16~Page 225. Byte 0 (DLOCK0) is used for Page 16~Page 143, Byte 1 (DLOCK1) is used for Page 144~Page 225, Byte 2 (DLOCK2) is used for Block Lock Control.

In the three tables above, L means lock control and lock status of the relative Page data. The data value cannot be changed afterward after the relative Lock bit set to "1" and become a read-only Page. BL in DLOCK2 means Block Locking of the Lock byte. As soon as BL set to "1", the relative block control bit (L, in DLOCK0 and DLOCK1) would become write inhibited, and cannot be changed afterward. These three DLOCK bytes are one time programmed bytes.

Note: 1. The RFU bit would be always read as 0x00.
2. These bytes can be reset to 0 by I²C interface.

OTP (One Time Program Data Byte)

Page 03 is the OTP area of the user memory. This page can be bitwise modified using the WRITE, which means as the bits had been set to "1", they cannot be reset to "0" afterward. The data contain meaning, please refer to the Memory Mapping Table from NFC.

Data Pages

Page 04~Page 225 are reserved as the user's read/write memory.

Page 03~Page 04 data content to be in the initialized state:

Page	Byte 0	Byte 1	Byte 2	Byte 3
03h	0xE1	0x10	0x6D	0x00
04h	0x03	0x00	0xFE	0x00

Page 03h~04h

Configuration Pages

Page	Byte 0	Byte 1	Byte 2	Byte 3
E3h	00	00	00	AUTH0
E4h	ACCESS	00	00	00
E5h	PWD0	PWD1	PWD2	PWD3
E6h	PACK0	PACK1	00	00
E7h	PT_I2C	00	00	00
E8h	NC_REG	LAST_NDEF_BLOCK	SRAM_MIRROR_BLOCK	WDT_LS
E9h	WDT_MS	I2C_CLOCK_STR	REG_LOCK	00

Configuration Pages

Configuration Registers

ACCESS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NFC_PROT	RFU	NFC_DIS_SEC1	RFU	RFU	AUTHLIM		

ACCESS Byte

PT_I2C							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	RFU	RFU	2K_PROT	SRAM_PROT	I2C_PROT	

PT_I2C Byte

NC_REG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NFCS_I2C_RST_ON_OFF	PTHRU_ON_OFF	FD_OFF		FD_ON		SRAM_MIRROR_ON_OFF	TRANSFER_DIR

NC_REG Byte

REG_LOCK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU						REG_LOCK_I2C	REG_LOCK_NFC

REG_LOCK Byte

I2C_CLOCK_STR (CFG05)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU							I2C_CLK_STR

I2C_CLOCK_STR Byte (Configuration Register 05)

Name	Bit	NFC Access	I²C Access	Default	Description
Authentication Pointer (AUTH0)					
AUTH0	7~0	R/W	R/W	FFh	Define the beginning page from which the password authenticated verification is required If the AUTH0 is set to a page address which is greater than the user memory page address, the password protection is disabled. (DLOCK page is in memory page address area, so it is also protected by AUTH0.)
Access Condition (ACCESS)					
NFC_PROT	7	R/W	R/W	0b	NFC protection bit 0b: Write access is protected by password verification 1b: Read and write access is protected by password verification
RFU	6~3	R/W	R/W	0000b	RFU, should be set to 0
AUTHLIM	2~0	R/W	R/W	000b	Authentication password verify attempt count limit Limitation of the negative password verification attempt. The value is 000b to 111b. If this value is set greater than 000b, the limitation will start. An incorrect password authentication flow will increase the negative password verification counter number; if this number is greater than the $2^{AUTHLIM}$ value, the password verification will be disabled forever even if a correct password authentication is occurred after that. Before the incorrect password verification counter is greater than the $2^{AUTHLIM}$ value, a success correct password authentication flow will reset the incorrect password verification counter value.
Password (PWD)					
PWD	31~0	R/W	R/W	FFFFFFFFh	32-bit password for authentication Reading this page will always respond all 0s
Password Acknowledge (PACK)					
PACK	15~0	R/W	R/W	0000h	16-bit password acknowledge Reading this page will always respond all 0s

Name	Bit	NFC Access	I²C Access	Default	Description
Protection Bit (PT_I2C)					
RFU	7~3	R/W	R/W	00000b	RFU, should be set to 0
SRAM_PROT	2	R/W	R/W	0b	Password protection for pass-through mode 0b: Disable 1b: Enable
I2C_PROT	1~0	R/W	R/W	00b	I²C interface memory access protection 00b: Disable 01b: Enable write protection in protected memory area 1xb: Enable read and write protection in protected memory area Note: I²C is always R/W permit in below area: 1. Session Register 2. SRAM area 3. Configuration blocks in Block39 and Block 3a, configuration byte access is depended on REG_LOCK_I2C bit
Configuration Registers					
NC_REG					
NFCS_I2C_RST_ON_OFF	7	R/W	R/W	0b	NFC interface silent and I²C interface soft reset function enable 0b: Disable 1b: Enable
PTHRU_ON_OFF	6	R/W	R/W	0b	Pass-through mode enable 0b: Disable 1b: Enable
FD_OFF	5~4	R/W	R/W	00b	Define the FD pin signal release condition (FD go to high if pull-up) 2'b00: Field is off 2'b01: Field is off or tag is in HLTA state 2'b10: Field is off or last page of NDEF message is read 2'b11: FD_ON=2'b11: Field is off or last SRAM data is read by I²C FD_ON=2'b00, 01 or 10: Field is off
FD_ON	3~2	R/W	R/W	00b	Define the FD pin signal set condition (FD go to low if pull-up) 2'b00: Field is on 2'b01: First valid NFC SOF (Start of frame) 2'b10: Tag is in SELECT state 2'b11: In PTHRU mode NFC → I²C: SRAM data is ready to be read by I²C I²C → NFC: SRAM data is read by NFC
SRAM_MIRROR_ON_OFF	1	R/W	R/W	0b	Enable SRAM mirror function 0b: Disable 1b: Enable
TRANSFER_DIR	0	R/W	R/W	1b	Set the data transfer direction when pass-through mode enabled 0b: I²C to NFC 1b: NFC to I²C
LAST_NEDF_BLOCK					
LAST_NEDF_BLOCK	7~0	R/W	R/W	00h	Define the block address of last NDEF data byte contained storage block Valid value range: 01h~37h
SRAM_MIRROR_BLOCK					
SRAM_MIRROR_BLOCK	7~0	R/W	R/W	F8h	Define the block address of beginning of SRAM mirrored block Valid value range: 01h~34h

Name	Bit	NFC Access	I²C Access	Default	Description
Watchdog Timer Least Significant Byte (WDT_LS)					
WDT_LS	7~0	R/W	R/W	48h	Define the least significant byte of watchdog timer timeout value
Watchdog Timer Most Significant Byte (WDT_MS)					
WDT_MS	7~0	R/W	R/W	08h	Define the most significant byte of watchdog timer timeout value
I2C_CLOCK_STR					
RFU	7~0	R/W	R/W	0000000b	RFU – all 7 bits should be 0b
I2C_CLK_STR	0	R/W	R/W	1b	Reserved for future use
REG_LOCK					
RFU	7~2	R/W	R/W	000000b	Reserved for future use
REG_LOCK_I2C	1	R/W	R/W	0b	I²C configuration lock bit, once set to 1b, it cannot change back to 0b 0b: Not lock 1b: Lock
REG_LOCK_NFC	0	R/W	R/W	0b	NFC configuration lock bit, once set to 1b, it cannot change back to 0b 0b: Not lock 1b: Lock

Configuration Table

Session Pages

Page	Byte 0	Byte 1	Byte 2	Byte 3
ECh	NC_REG	LAST_NDEF_BLOCK	SRAM_MIRROR_BLOCK	WDT_LS
EDh	WDT_MS	I2C_CLOCK_STR	NS_REG	00

Session Pages

Session Registers

I2C_CLOCK_STR (SR05)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RFU						NEG_AUTH_REACHED	I2C_CLK_STR

I2C_CLOCK_STR Byte (Session Register 05)

NS_REG							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
NDEF_DATA_READ	I2C_LOCKED	RF_LOCKED	SRAM_I2C_READY	SRAM_RF_READY	EEPROM_WR_ERR	EEPROM_WR_BUSY	RF_FIELD_PRESENT

NS_REG Byte

Name	Bit	NFC Access	I²C Access	Default	Description
Session Registers					
NC_REG					
NFCS_I2C_RST_ON_OFF	7	R	R/W	0b	NFC interface silent and I²C interface soft reset function enable 0b: Disable 1b: Enable
PTHRU_ON_OFF	6	R	R/W	0b	Pass-through mode enable 0b: Disable 1b: Enable This bit is auto-cleared as one of NFC or I²C interface off.

Name	Bit	NFC Access	I²C Access	Default	Description
FD_OFF	5~4	R	R/W	00b	Define the FD pin signal release condition (FD go to high if pull-up) 2'b00: Field is off 2'b01: Field is off or tag is in HLTA state 2'b10: Field is off or last page of NDEF message is read 2'b11: FD_ON=2'b11: Field is off or last SRAM data is read by I²C FD_ON=2'b00, 01 or 10: Field is off
FD_ON	3~2	R	R/W	00b	Define the FD pin signal set condition (FD go to low if pull-up) 2'b00: Field is on 2'b01: First valid NFC SOF (Start of frame) 2'b10: Tag is in SELECT state 2'b11: In PTHRU mode NFC → I²C: SRAM data is ready to be read by I²C I²C → NFC: SRAM data is read by NFC
SRAM_MIRROR_ON_OFF	1	R	R/W	0b	Enable SRAM mirror function 0b: Disable 1b: Enable
TRANSFER_DIR	0	R	R/W	1b	Set the data transfer direction when pass-through mode enabled 0b: I²C to NFC 1b: NFC to I²C
LAST_NEDF_BLOCK					
LAST_NEDF_BLOCK	7~0	R	R/W	00h	Define the block address of last NDEF data byte contained storage block Valid value range: 01h~37h
SRAM_MIRROR_BLOCK					
SRAM_MIRROR_BLOCK	7~0	R	R/W	F8h	Define the block address of beginning of SRAM mirrored block Valid value range: 01h~34h
Watchdog Timer Least Significant Byte (WDT_LS)					
WDT_LS	7~0	R	R/W	48h	Define the least significant byte of watchdog timer timeout value
Watchdog Timer Most Significant Byte (WDT_MS)					
WDT_MS	7~0	R	R/W	08h	Define the most significant byte of watchdog timer timeout value The WDT updated value will be active as this byte has been written.
I2C_CLOCK_STR (SR05)					
RFU	7~2	R	R	000000b	Reserved for future use
NEG_AUTH_REACHED	1	R	R	0b	Status of limited counter overflow for negative PWD_AUTH attempt
I2C_CLK_STR	0	R	R	1b	Reserved for future use
NS_REG					
NDEF_DATA_READ	7	R	R	0b	After all data is read from the block address specified by the LAST_NDEF_BLOCK byte, this bit will be set to 1b. After the NS_REG byte is read by I²C, this bit will be reset to 0b.
I2C_LOCKED	6	R	R/W	0b	1b: Memory access is locked to I²C
RF_LOCKED	5	R	R	0b	1b: Memory access is locked to NFC
SRAM_I2C_READY	4	R	R	0b	In pass-through mode, 1b: data is ready in SRAM to be read by I²C
SRAM_RF_READY	3	R	R	0b	In pass-through mode, 1b: data is ready in SRAM to be read by NFC

Name	Bit	NFC Access	I²C Access	Default	Description
EEPROM_ WR_ERR	2	R	R/W	0b	EEPROM write error status bit 1b: write error This bit should be cleared by I²C.
EEPROM_ WR_BUSY	1	R	R	0b	EEPROM write in progress status bit
RF_FIELD_ PRESENT	0	R	R	0b	NFC RF field present status bit

Field Detection Function

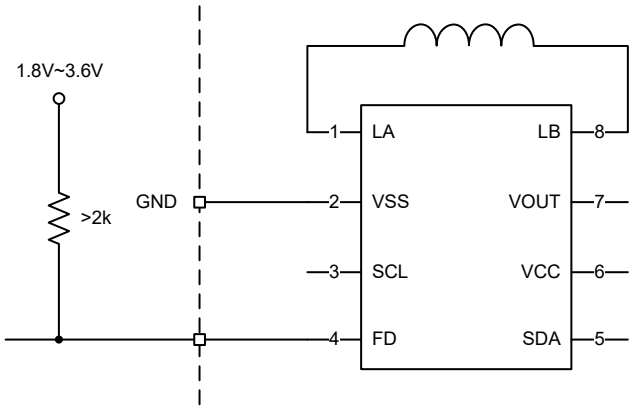
The FD pin is based on open-drain output implementation, used for configurable output signal to trigger the external logic device such as MCU or other controller.

The FD pin pulled down condition is: (FD_ON)

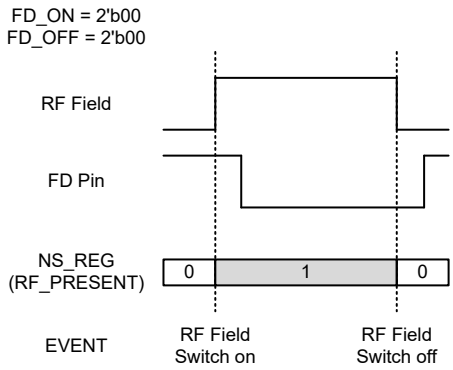
- NFC field is present. (in-field).
- The detection of first valid NFC start of frame.
- Enter the Selection state of tag.

The FD pin released from the pulled down condition is: (FD_OFF)

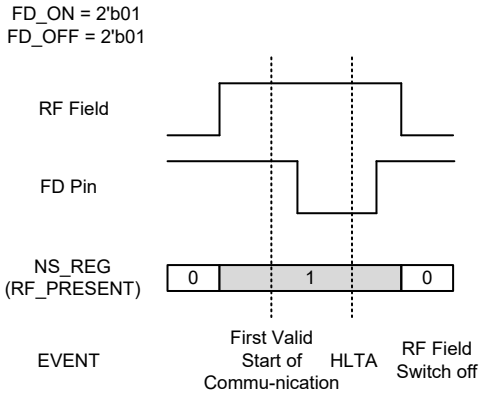
- NFC field is absent. (off-field)
- Enter the HLTA state of tag.
- The NFC interface has read the last message of NDEF defined in LAST_NDEF_BLOCK.



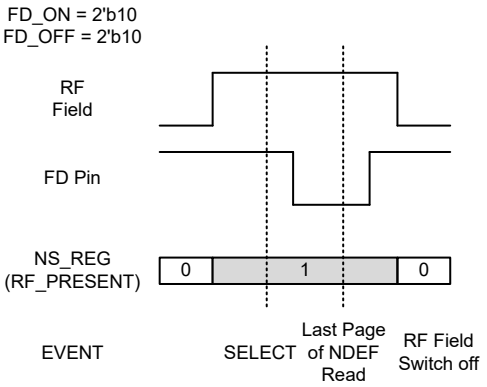
FD Pin Application Circuit



Configuration of FD_OFF and FD_ON is 0000b



Configuration of FD_OFF and FD_ON is 0101b



Configuration of FD_OFF and FD_ON is 1010b

Password Verification Function

The BC45B4211 provides the user to control the memory access authority. As soon as the AUTH0 in Page E3h of NFC interface is set, and the value is not greater than the highest user page address (Page EBh), the password authentication is enabled in NFC interface. With a success correct password verification flow, the BC45B4211 will respond the user defined PACK bytes to reader. Under this condition, users can access the memory page address greater than AUTH0 value. If no success correct password verification flow happened, the BC45B4211 is not enter the authentication state, the memory page which is greater than AUTH0 is limited to read only or read/write inhibit depending on the NFC_PROT bit setting.

Whether PWD_AUTH verification is done or not, the I²C interface memory access depends on AUTH0 and PT_I2C setting only.

PWD and PACK

The Passwords and PACK value are programmable in the Page E5 and Page E6 of NFC interface which are in the Block 39 of I²C interface. For security issue, reading these data will always respond all 00h.

Limitation of Negative Authentication Attempt

To prevent brute-force attacks on the password, the BC45B4211 sets the limitation of negative authentication attempt counts depending on the AUTHLIM bits. If the AUTHLIM bits are set to 000b, the limitation is disabled. If the AUTHLIM bits are not equal to 000b, each negative authentication attempt would make the internal counter increment. As soon as the internal counter value is greater than $2^{AUTHLIM}$, the BC45B4211 is permanently locked to the un-authentication state. Before the maximum limitation is reached, one successful password verification authentication will reset the internal counter to all 0s.

Watchdog Timer

The BC45B4211 embedded one 16-bit counter for watchdog timer used. In order to allowed I²C execute a fully Read/Write procedure, the I2C_LOCKED bit is stay at 1b as I²C Read/Write memory beginning till the watchdog timer timeout. The I2C_LOCKED bit can be cleared to 0b by the I²C interface before the watchdog timer timeout while the I²C Read/Write had done.

The default value of watchdog timer is about 20ms (0848h), the timeout value can be set from 0001h (about 9.44μs) to FFFFh (about 618ms) on WDT_MS and WDT_LS byte. As soon as the WDT_MS byte set, the new value is active.

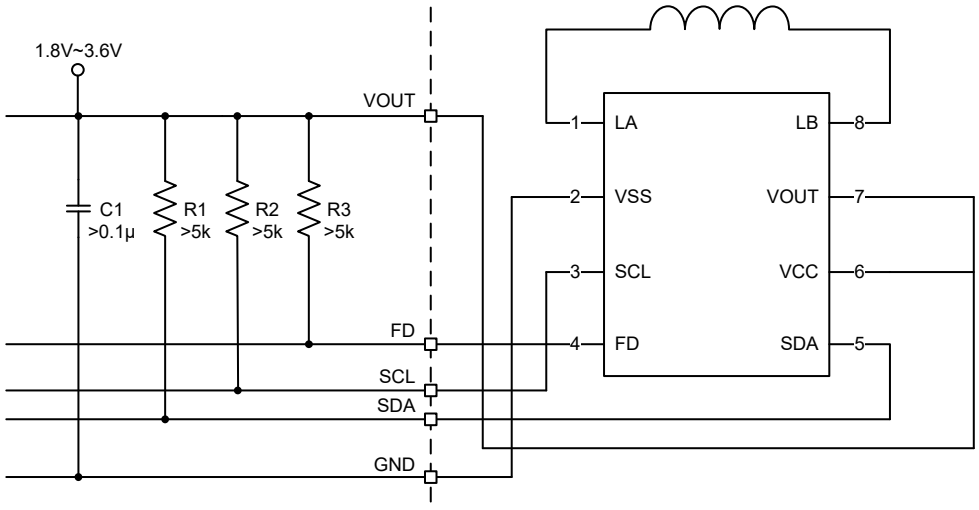
If the watchdog timer is timeout and the I²C Read/Write is still in progress, the I2C_LOCKED bit will hold on 1b until the Read/Write access done.

Energy Harvesting Feature

The BC45B4211 provides the power source by energy harvested from NFC RF field for external low power device used.

The voltage and current supply value is depended on the power strength harvested from RF field which is associated to Reader power and antenna or Tag antenna size or the distance of communication.

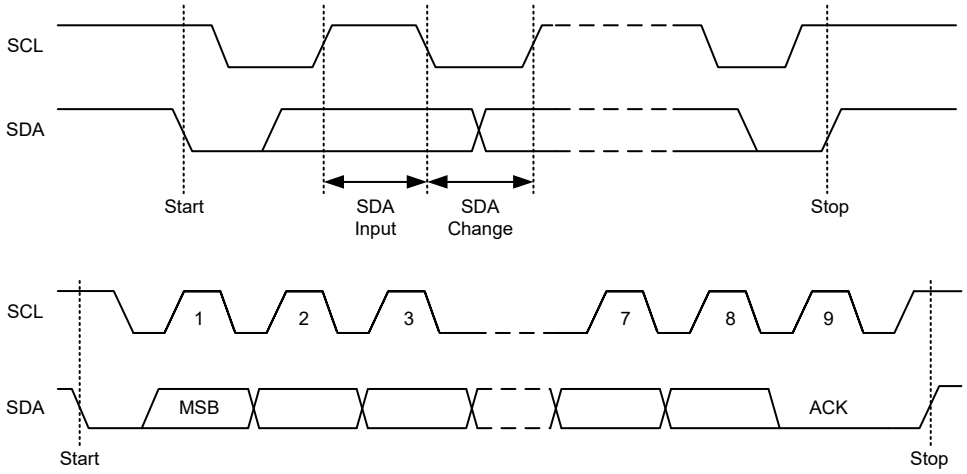
The typical application circuit is illustrated below, the capacitor C1 should be connected between VOUT and GND and located as close to the VOUT pin as possible.



Typical Application Circuit

Commands

I²C Commands



I²C Bus Protocol

The BC45B4211 provides I²C slave mode feature, the protocol is complied with standard I²C protocol.

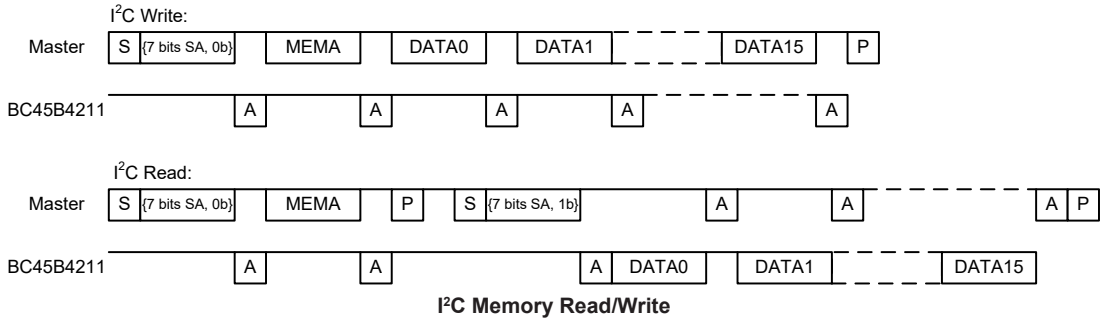
The Start bit is found as a falling edge of SDA while the SCL is stable in the high state. The Start bit is followed by 7-bit SA (Slave Address) and 1-bit R/W access command.

The default SA value is 55h (1010101b), to change the SA value, users should write the most 7-bit value to the first byte of I²C Block 0 from I²C interface. Reading the first byte of I²C Block 0 will always respond the value of UID0.

Each I²C packet should have one Stop bit. The Stop bit is found as the rising edge of SDA while the SCL is stable in high state.

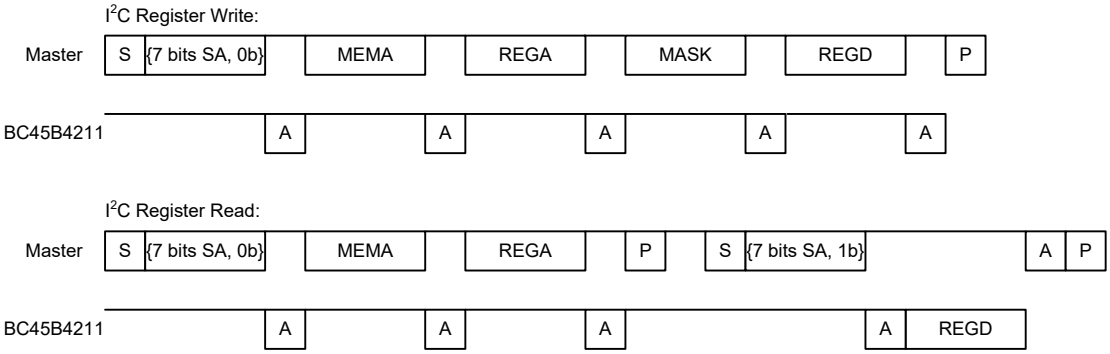
Command Format

- Memory read and write:



I²C Memory Read/Write

- Register read and write:



I²C Register Read/Write

I²C Memory Write

To execute the I²C memory write command, the I²C master should transmit the write MEMA with 16 bytes of data to be written to the block address which is assigned in MEMA bytes.

I²C Memory Read

The I²C memory read command procedure is divided by two steps. First, the I²C master should transmit the write MEMA command to assign the MEMA byte as the block address from which the data would be read out. Second, after the write MEMA command, the I²C master should ready to receive 16 bytes of data from the BC45B4211.

I²C Register Write

To execute the I²C register write command, the I²C master should transmit the write command with one MEMA byte, one REGA byte, one MASK byte and one register data byte REGD. The MEMA byte is the block address of the register to be written, and the REGA byte is the byte address of the block of MEMA. To be bit address write issue, one MASK byte is needed. Only the bit position with value 1b in MASK byte is the bit in REGD to be written and modified. The bit position with value 0b in MASK byte will not be written in REGD byte.

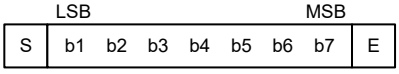
I²C Register Read

The I²C register read command procedure is divided by two steps like I²C memory read command. First, the I²C master should transmit the write MEMA with REGA command to assign the register block and byte address from which the REGD byte would be read out. Second, after the write MEMA and REGA command, the I²C master should ready to receive the REGD byte from the BC45B4211.

NFC Commands

Command Format

Short Frame: 7-bit



- **REQA Command**

  The REQA command is send by the reader when the BC45B4211 is in the IDLE state. Upon receiving this command, the BC45B4211 responds with ATQA and enters the ready state according to ISO/IEC 14443A-3 standard.

Reader Command

Command Code	Parameter	Data	CRC Check
0x26	—	—	—

BC45B4211 Response

BC45B4211 Response
ATQA0 + ATQA1 (0x44 0x00)

- **WUPA Command**

  The WUPA command is send by the reader when the BC45B4211 is in the IDLE or HALT state. Upon receiving this command, the BC45B4211 responds with ATQA and enters the ready state according to ISO/IEC 14443A-3 standard.

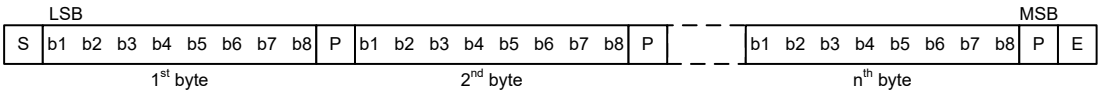
Reader Command

Command Code	Parameter	Data	CRC Check
0x52	—	—	—

BC45B4211 Response

BC45B4211 Response
ATQA0 + ATQA1 (0x44 0x00)

Standard Frame



n × (8 data bits + odd parity bit) with n ≥ 1.

Each byte is followed by an odd parity bit and the parity bit P is set to "1" such that the number of 1s in (b1to b8, P) is odd.

- **Anti-collision and Select Commands**

  The following commands are used during an anti-collision and select loop. The anti-collision and select commands are divided into two cascade levels. These commands are based on the same command code and differ only for Parameter. These commands consist of select code and number of valid bits of UID.

  - **Anti-collision of Cascade Level 1**

    Reader Command

Command Code	Parameter	Data	CRC Check
0x93	0x20~0x67	Part of the UID	—

    BC45B4211 Response

BC45B4211 Response
CT + UID0 + UID1 + UID2 + BCC0 (0x88 + UID0 + UID1 + UID2 + BCC0)

    Note: BCC0=CT ⊕ UID0 ⊕ UID1 ⊕ UID2

  - **Select of Cascade Level 1**

    Reader Command

Command Code	Parameter	Data	CRC Check
0x93	0x70	CT + UID0 + UID1 + UID2 + BCC0	CRC

BC45B4211 Response

BC45B4211 Response
SAK + CRC (0x04 + CRC)

- **Anti-collision of Cascade Level 2**

Reader Command

Command Code	Parameter	Data	CRC Check
0x95	0x20~0x67	Part of the UID	—

BC45B4211 Response

BC45B4211 Response
UID3 + UID4 + UID5 + UID6 + BCC1

Note: BCC1=UID3 ⊕ UID4 ⊕ UID5 ⊕ UID6

- **Select of Cascade Level 2**

Reader Command

Command Code	Parameter	Data	CRC Check
0x95	0x70	UID3 + UID4 + UID5 + UID6 + BCC1	CRC

BC45B4211 Response

BC45B4211 Response
SAK + CRC (0x00 + CRC)

- **HLTA Command**

The HLTA command consists of two bytes followed by CRC check and the tag returns nothing if the HLTA command is acknowledged.

Reader Command

Command Code	Parameter	Data	CRC Check
0x50	0x00	—	CRC

BC45B4211 Response

BC45B4211 Response
None

- **READ Command**

The READ command would read 4 pages of data per command. The data 00 is the content of the initial address.

Reader Command

Command Code	Parameter	Data	CRC Check
0x30	address	—	CRC

BC45B4211 Response

BC45B4211 Response
D0 + D1 + D2+ ……+ D15 + CRC0 + CRC1 or NAK (4-bit 0x0) if address is outside read range

- **WRITE Command**

The WRITE command is used to program the user accessible memory space one page at a time. Each memory page consists of 4-byte data. The reader issues a write command and specifies the memory page address, corresponding memory page data and 2-byte CRC to the BC45B4211. The BC45B4211 would respond ACK (4-bit 0xa) to the reader or NAK (4-bit 0x0) if an error happened.

Reader Command

Command Code	Parameter	Data	CRC Check
0xA2	address	4-Byte (D0, D1, D2, D3)	CRC

BC45B4211 Response

BC45B4211 Response
ACK (4-bit 0xA) or NAK (4-bit 0x0)

- **Fast Write Command**

The Fast Write command is used as the Pass-Through mode is enabled. When the reader issues the FWRITE command to the BC45B4211, the BC45B4211 will write the 64-byte data to embedded SRAM buffer. As the last byte of SRAM data written, an MCU can read these SRAM data from the I²C interface. To issue the FWRITE command, the reader should send the FWRITE command code with 2-byte parameter 0xf0 (Start) and 0xff (End) and the following 64-byte data to be written and 2-byte CRC. The BC45B4211 will respond 4-bit ACK or NACK to the reader.

Reader Command

Command Code	Start	End	Data	CRC Check
0xA6	0xf0	0xff	D0, D1, … , D63	CRC

BC45B4211 Response

BC45B4211 Response
ACK (4-bit 0xA) or NAK (4-bit 0x0)

- **Get Version Command**

The GVER command is used to read the BC45B4211 tag version which includes the information about the product version, storage size, ISO/IEC standard following and any other product information required in the BC45B4211. The reader issues the GVER command with 2-byte CRC to the BC45B4211, the BC45B4211 will respond 8-byte corresponding data to reader.

Reader Command

Command Code	CRC Check
0x60	CRC

BC45B4211 Response

BC45B4211 Response
D0 + D1 + D2+ ……+ D7 + CRC0 + CRC1 or NAK (4-bit 0x0) if address is outside read range

Response Data Content

Byte No.	Name	Data	Description
0	Header	0x00	Fixed header data
1	Vender ID	0x7E	IC manufacture code ID
2	Product type	0x04	NFC Tag
3	Product subtype	0x05	50pF capacitance, I²C, Field detection

Byte No.	Name	Data	Description
4	Major product version	0x01	Version 1.x
5	Minor product version	0x00	Version x.0
6	Storage size	0x13	Note
7	Product type	0x03	ISO/IEC 14443A-3 compliant

Note: Storage size = 0x13, the most significant 7 bit value 0001_001b is interpreted as the unsigned integer value 09d. If the least significant bit b0 is 0b, this byte will be indicating the user memory storage size to be 2^9 bytes exactly. If the least significant bit b0 is 1b, this byte will be indicating the user memory storage size to be between 2^9~2^{10} bytes. Because the BC45B4211's user memory bytes is 888 bytes, this byte will be set to 13h.

- **Fast Read Command**

The FREAD command is used to read more pages which are not limited to 16 pages one procedure. The reader issues the FREAD command with 1-byte StartAddr and 1-byte EndAddr followed by 2-byte CRC to the BC45B4211. The BC45B4211 will respond the corresponding page data between StartAddr and EndAddr to the reader. For example, if the StartAddr is 08h, the EndAddr is 11h, a success FREAD command to the BC45B4211, the response page data will be page 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 10h and 11h.

Reader Command

Command Code	Parameter 1	Parameter 2	CRC Check
0x3A	StartAddr	EndAddr	CRC

BC45B4211 Response

BC45B4211 Response
(D0 + D1 + D2+ D3) × n + CRC0 + CRC1 or NAK (4-bit 0x0) if address is outside read range

Note: n is the page number counts from StartAddr to EndAddr.
(n = EndAddr – StartAddr + 1)

- **Sector Select Command**

The SEC_SEL command is used to switch the access region between different sectors. This command is divided to two steps. First, the reader issues the SEC_SEL command code with 1-byte parameter 0xff and 2-byte CRC. The BC45B4211 will respond 4-bit ACK or NACK to the reader. Second, the reader issues the 1-byte SecNo for sector number to be switched and 3-byte 00h for dummy and 2-byte CRC. The BC45B4211 will not respond for more than 1ms as success or respond NAK as fail to the reader.

Step1.

Reader Command

Command Code	Parameter	CRC Check
0xC2	0xFF	CRC

BC45B4211 Response

BC45B4211 Response
AK (4-bit 0xa) or NAK (4-bit 0x0) if error

Step2.

Reader Command

SecNo	Parameter	CRC Check
0x00~0xFE	0x00, 0x00, 0x00	CRC

BC45B4211 Response

BC45B4211 Response
AK (No Response for > 1ms) or NAK (4-bit 0x0) if error

- **Password Authentication Command**

  The PWD_AUTH command is used to access the area which is protected by passwords. As the AUTH0 byte is set, the memory page area which the address is greater than AUTH0 value would be protected. As soon as the pages are protected, users can access these pages only after a successful passwords authenticated flow. The access ability depends on the NFC_PROT bit setting. As the NFC_PROT bit is set to 0, the protected pages are read only before authentication, otherwise the NFC_PROT bit is set to 1, the protected page are read/write inhibit before authentication. To prevent the brute force passwords trying, setting the 3-bit AUTHLIM is necessary. As soon as the AUTHLIM bits are set greater than 000b, the authentication limit is begin. As the wrong passwords authenticating count is greater than $2^{AUTHLIM}$ value, the authentication flow is inhibited anymore. It is recommended to set AUTH0 before PWD pages address (0xE5) to protect passwords page from been changed by an un-authenticated flow.

  The reader issues the PWD_AUTH command with 4-byte PWD followed by 2-byte CRC to the BC45B4211. The BC45B4211 will response 2-byte PACK to the reader to indicate the password authentication is success. The PACK is programmable in Page E6. Any READ or FREAD to Page E5 (PWD) and Page E6 (PACK), the response data would be all 0s.

  Reader Command

Command Code	Passwords	CRC Check
0x1b	PWD0_PWD1_PWD2_PWD3	CRC

  BC45B4211 Response

BC45B4211 Response
PACK0, PACK1, CRC0, CRC1 or NAK (4-bit 0x0) if error

- **Read Signature Command**

  The RSIG command is used to read out the 32-byte ECDSA signature for further ECC verification. The BC45B4211's digital signature is based on standard Elliptic Curve Cryptography algorithm. The curve name is secp128r1. With the ECC verification, users can easily check this BC45B4211 device vender is Holtek indeed. Each BC45B4211 UID is signed with Holtek's private key and generate 32-byte ECDSA. Users can verify this signature with the public key provided by Holtek.

  The Reader issues the RSIG command with 1-byte fixed value address 0x00 followed by 2-byte CRC to the BC45B4211. The BC45B4211 will response the 32-byte signature to reader.

  Reader Command

Command Code	Address	CRC Check
0x3c	0x00	CRC

  BC45B4211 Response

BC45B4211 Response
SIG00, SIG01, … , SIG31, CRC0, CRC1 or NAK (4-bit 0x0) if error

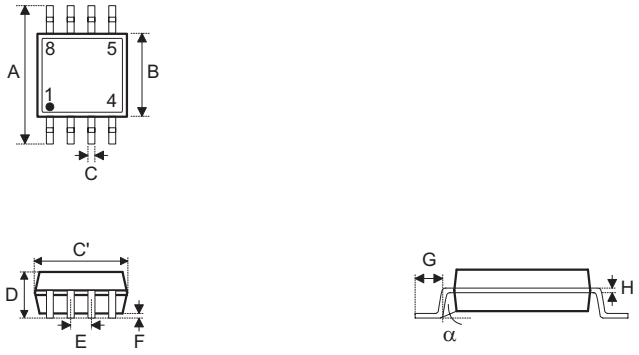
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

8-pin SOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.236 BSC	
B		0.154 BSC	
C	0.012	—	0.020
C′		0.193 BSC	
D	—	—	0.069
E		0.050 BSC	
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		6.00 BSC	
B		3.90 BSC	
C	0.31	—	0.51
C′		4.90 BSC	
D	—	—	1.75
E		1.27 BSC	
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°