Features

- Fully qualified Bluetooth v2.1 + EDR specification system
- Best-in-class Bluetooth radio with 5.5dBm transmit power and -91dBm receive sensitivity
- 64MIPS Kalimba DSP coprocessor
- 16-bit internal stereo codec: 95dB SNR for DAC
- Low-power 1.5V operation, 1.8V to 3.6V I/O
- Integrated 1.5V and 1.8V linear regulators
- Integrated switch-mode regulator
- Integrated battery charger
- USB, I²C and UART with dual-port bypass mode to 4Mbits/s
- 16Mb internal flash memory
- Multi-configurable I²S, PCM or SPDIF interface
- Enhanced audibility and noise cancellation
- 7 x 7 x 1.3mm, 0.5mm pitch 120-ball LFBGA
- Support for IEEE 802.11 coexistence
- Green (RoHS compliant and no antimony or halogenated flame retardants)

BlueCore®5-Multimedia Flash (16Mb)

Fully Qualified Single-chip Bluetooth® v2.1 + EDR System

Production Information

BC57G687C

Issue 3

BlueCore5-Multimedia Flash (16Mb) Data Sheet

General Description

BlueCore®5-Multimedia Flash (16Mb) is a product from CSR's Connectivity Centre. It is a single-chip radio and baseband IC for Bluetooth v2.1 + EDR specification systems.

BlueCore5-Multimedia Flash (16Mb) contains 16Mb internal flash memory, which makes it one of the most powerful and flexible Bluetooth audio solutions with the smallest PCB footprint on the market today. When used with CSR's Bluetooth stack, it provides a fully compliant Bluetooth v2.1 + EDR specification for data and voice.

BlueCore5-Multimedia Flash (16Mb) contains the Kalimba DSP coprocessor with double the MIPS and double the memory of BlueCore3-Multimedia, supporting enhanced audio applications.

BlueCore5-Multimedia Flash (16Mb) is designed to reduce the number of external components required which ensures production costs are minimised.

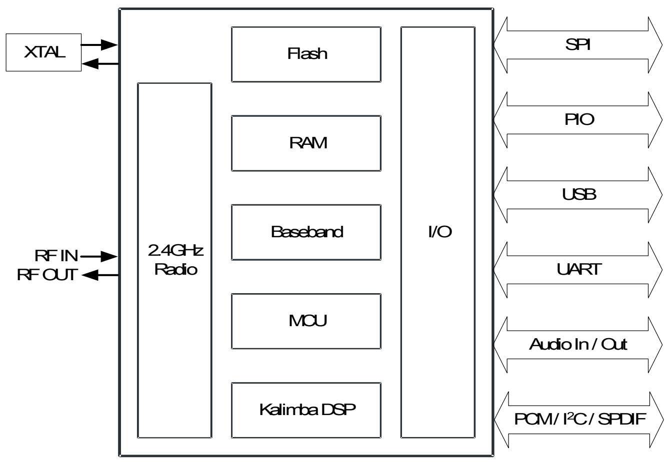
Applications

- Bluetooth-enabled automotive wireless gateways
- High-quality stereo wireless headsets
- High-quality mono headsets
- Hands-free car kits
- Wireless speakers
- VoIP handsets
- Analogue and USB multimedia dongles

Contains auto-calibration and BIST routines to simplify development, type approval and production test.

To improve the performance of both Bluetooth and IEEE 802.11b/g co-located systems a wide range of coexistence features are available including a variety of hardware signalling: basic activity signalling, Intel WCS activity and channel signalling.

For further device performance and additional information refer to the *BlueCore5-Multimedia Flash (16Mb) Performance Specification*.



Document History

Revision	Date	Change Reason
1	01 DEC 09	Original publication of document.
2	17 DEC 09	Updates to improve clarity of ESD Precautions and Power Consumption.
3	21 DEC 09	ESD updates. If you have any comments about this document, email comments@csr.com giving the number, title and section with your feedback.

Status Information

The status of this Data Sheet is **Production Information**.

CSR Product Data Sheets progress according to the following format:

Advance Information

Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.

Pre-production Information

Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.

All electrical specifications may be changed by CSR without notice.

Production Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Production Data Sheets supersede all previous document versions.

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BlueCore5-Multimedia Flash (16Mb) devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

BlueCore5-Multimedia Flash (16Mb) devices are also free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

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1 Device Details

Radio

- Common TX/RX terminal simplifies external matching; eliminates external antenna switch
- BIST minimises production test time
- Bluetooth v2.1 + EDR specification compliant

Transmitter

- 5.5dBm RF transmit power with level control from on-chip 6-bit DAC over a dynamic range >30dB
- Class 2 and Class 3 support without the need for an external power amplifier or TX/RX switch

Receiver

- Receiver sensitivity of -91dBm
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available on HCI interface
- Fast AGC for enhanced dynamic range

Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 16MHz to 26MHz or an external clock 12MHz to 52MHz
- Accepts 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz TCXO frequencies for GSM and CDMA devices with sinusoidal or logic level signals

Baseband and Software

- 16Mb internal flash
- 48KB internal RAM, allows full-speed data transfer, mixed voice/data and full piconet support
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Transcoders for A-law, µ-law and linear voice from host and A-law, µ-law and CVSD voice over air

Physical Interfaces

- SPI with clock speeds up to 64MHz in master mode, requires firmware support, and 32MHz in slave mode
- I²C master compatible interface
- UART interface with programmable data rate up to 3Mbits/s with an optional bypass mode
- USB v2.0 interface
- Bidirectional serial programmable audio interface supporting PCM, I²S and SPDIF formats
- 2 LED drivers with faders

Kalimba DSP

- Very low power Kalimba DSP coprocessor, 64MIPS, 24-bit fixed point core
- SBC decode takes approximately 4mW power consumption while streaming music
- Single-cycle MAC; 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 6K x 32-bit program RAM, 16K x 24-bit + 12K x 24-bit data RAM
- 64-word x 32-bit program memory cache when executing from internal flash

Stereo Audio Codec

- 16-bit internal stereo codec
- Dual ADC and DAC for stereo audio
- Integrated amplifiers for driving 16Ω speakers; no need for external components
- Support for single-ended speaker termination and line output
- Integrated low-noise microphone bias
- ADC sample rates are 8, 11.025, 16, 22.05, 32 and 44.1kHz
- DAC sample rates are 8, 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48kHz

Auxiliary Features

- User space on processor for customer applications
- Crystal oscillator with built-in digital trimming
- Power management includes digital shutdown and wake-up commands with an integrated low-power oscillator for ultra-low power Park/Sniff/Hold mode
- Clock request output to control external clock
- On-chip regulators: 1.5V output from 1.8V to 2.7V input and 1.8V output from 2.7V to 4.5V input
- On-chip high-efficiency switch-mode regulator; 1.8V output from 2.7V to 4.4V input
- Power-on-reset cell detects low supply voltage
- 10-bit ADC and 8-bit DAC available to applications
- On-chip charger for lithium ion/polymer batteries

Bluetooth Stack

CSR's Bluetooth Protocol Stack runs on the on-chip MCU in a variety of configurations:

- Standard HCI, UART or USB
- Audio codec and echo-noise suppression or customer-specific algorithms running on the DSP

Package Option

- LFBGA 120-ball, 7 x 7 x 1.3mm, 0.5mm pitch

2 Functional Block Diagram

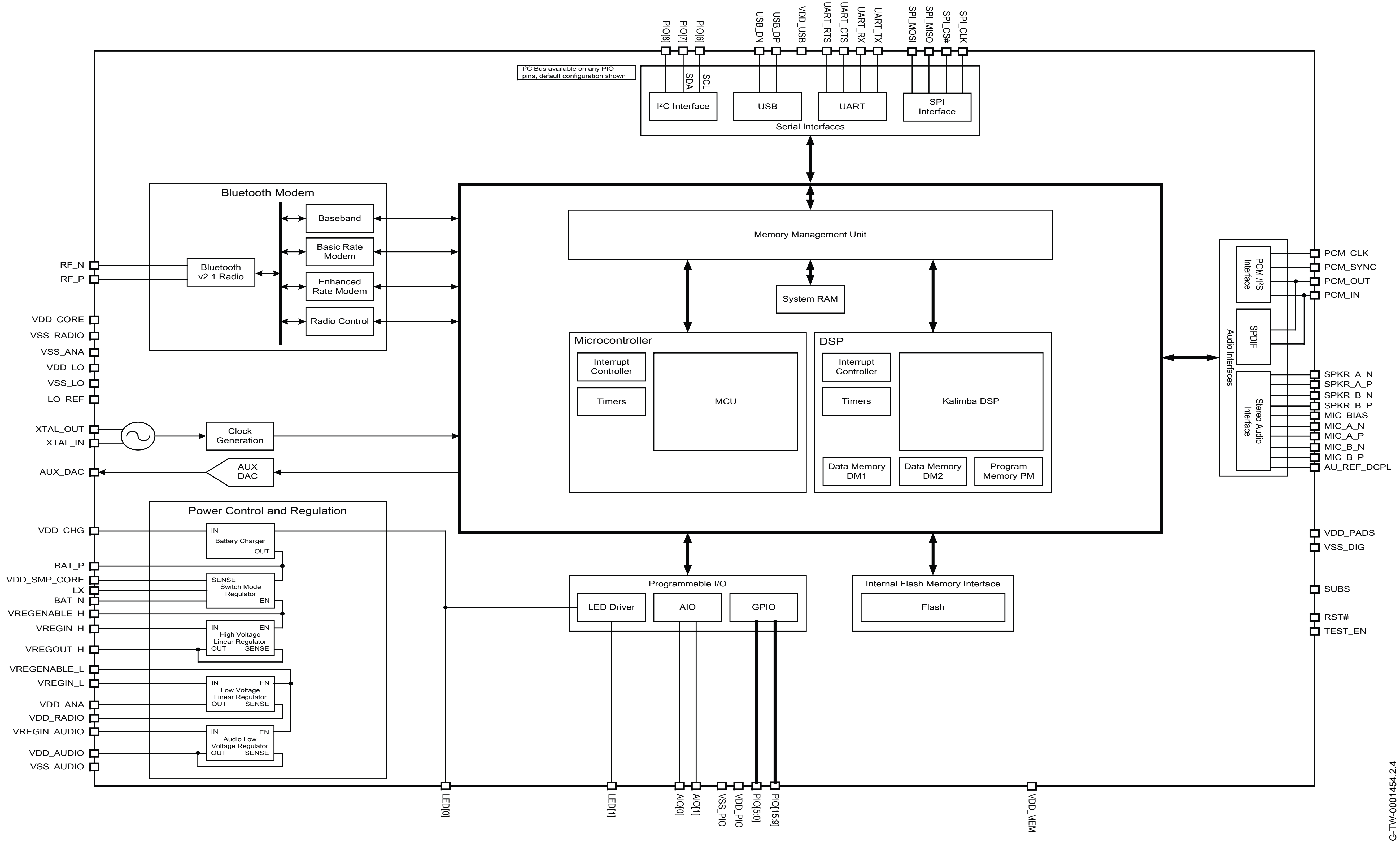


Figure 2.1: Functional Block Diagram

3 Package Information

3.1 Pinout Diagram

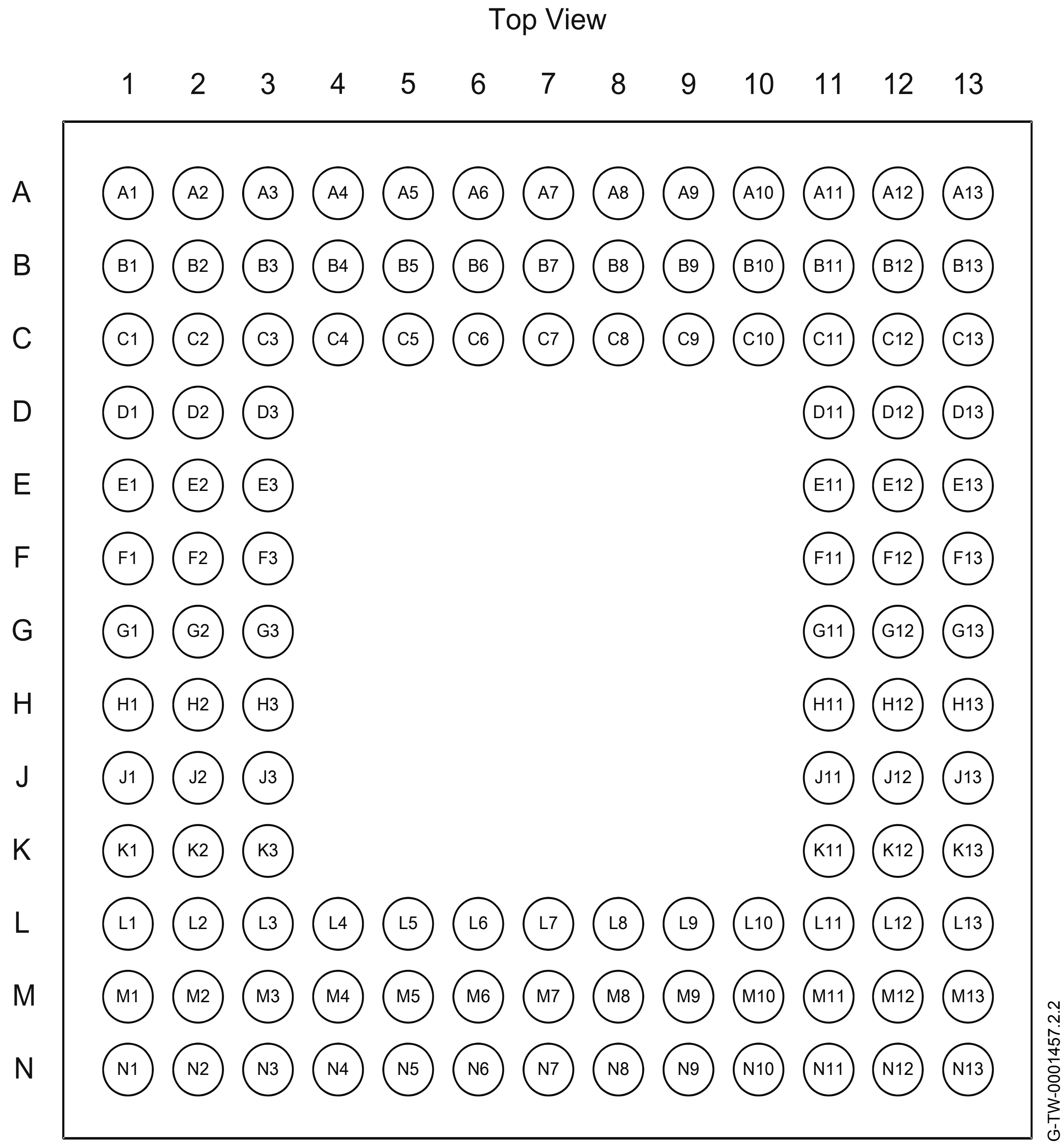


Figure 3.1: Device Pinout

3.2 Device Terminal Functions

Radio	Ball	Pad Type	Supply Domain	Description
RF_P	H1	RF	VDD_RADIO	Transmitter output/switched receiver input
RF_N	J1			Complement of RF_P
AUX_DAC	H3	Analogue	VDD_PIO	Voltage DAC

Synthesiser and Oscillator	Ball	Pad Type	Supply Domain	Description
XTAL_IN	N1	Analogue	VDD_ANA	For crystal or external clock input
XTAL_OUT	N2			Drive for crystal
LO_REF	N5			Reference voltage to decouple the synthesiser

UART	Ball	Pad Type	Supply Domain	Description
UART_TX	L13	Bidirectional CMOS output, tristate, with weak internal pull-up	VDD_USB	UART data output
UART_RX	M12	CMOS input with weak internal pull-down		UART data input
UART_RTS	M11	Bidirectional CMOS output, tristate, with weak internal pull-up		UART request to send, active low
UART_CTS	M13	CMOS input with weak internal pull-down		UART clear to send, active low

USB	Ball	Pad Type	Supply Domain	Description
USB_DP	N13	Bidirectional	VDD_USB	USB data plus with selectable internal 1.5kΩ pull-up resistor
USB_DN	N12			USB data minus

PCM Interface	Ball	Pad Type	Supply Domain	Description
PCM_OUT	F11	CMOS output, tristate, with weak internal pull-down	VDD_PADS	Synchronous data output
PCM_IN	F13	CMOS input, with weak internal pull-down		Synchronous data input
PCM_SYNC	G11	Bidirectional with weak internal pull-down		Synchronous data sync
PCM_CLK	H11	Bidirectional with weak internal pull-down		Synchronous data clock

SPI Interface	Ball	Pad Type	Supply Domain	Description
SPI_MISO	E12	CMOS output, tristate, with weak internal pull-down	VDD_PADS	SPI data output
SPI_MOSI	F12	CMOS input, with weak internal pull-down		SPI data input
SPI_CS#	E13	Input with weak internal pull-up		Chip select for SPI, active low
SPI_CLK	E11	Input with weak internal pull-down		SPI clock

PIO Port	Ball	Pad Type	Supply Domain	Description
PIO[0]/RXEN	E3	Bidirectional with programmable strength internal pull-up/down	VDD_PIO	Programmable input/output line (external RXEN)
PIO[1]/TXEN	F3			Programmable input/output line (external TXEN)
PIO[2]	E2			Programmable input/output line
PIO[3]	D3			Programmable input/output line

PIO Port	Ball	Pad Type	Supply Domain	Description
PIO[4]	H12	Bidirectional with programmable strength internal pull-up/down	VDD_PADS	Programmable input/output line
PIO[5]	J11			
PIO[6]	M8			
PIO[7]	H13			
PIO[8]	J12			
PIO[9]	L12			
PIO[10]	L10			
PIO[11]	M10			
PIO[12]	K12			
PIO[13]	M9			
PIO[14]	L9			
PIO[15]	N9			
AIO[0]	N6	Bidirectional	VDD_ANA	Analogue programmable input/ output line
AIO[1]	M5			

Test and Debug	Ball	Pad Type	Supply Domain	Description
RST#	G13	CMOS input with weak internal pull-up	VDD_PADS	Reset if low. Input debounced so must be low for >5ms to cause a reset
TEST_EN	G12	CMOS input with strong internal pull-down	VDD_PADS	For test purposes only (leave unconnected)

Codec	Ball	Pad Type	Supply Domain	Description
MIC_A_P	B2	Analogue	VDD_AUDIO	Microphone input positive, left
MIC_A_N	B1			Microphone input negative, left
MIC_B_P	A2	Analogue	VDD_AUDIO	Microphone input positve, right
MIC_B_N	A1			Microphone input negative, right

Codec	Ball	Pad Type	Supply Domain	Description
SPKR_A_P	D1	Analogue	VDD_AUDIO	Speaker output positive, left
SPKR_A_N	D2			Speaker output negative, left
SPKR_B_P	A3	Analogue	VDD_AUDIO	Speaker output positive, right
SPKR_B_N	B3			Speaker output negative, right
MIC_BIAS	A5	Analogue	VDD_AUDIO	Microphone bias
AU_REF_DCPL	C1	Analogue	VDD_AUDIO	Decoupling of audio reference (for high-quality audio)

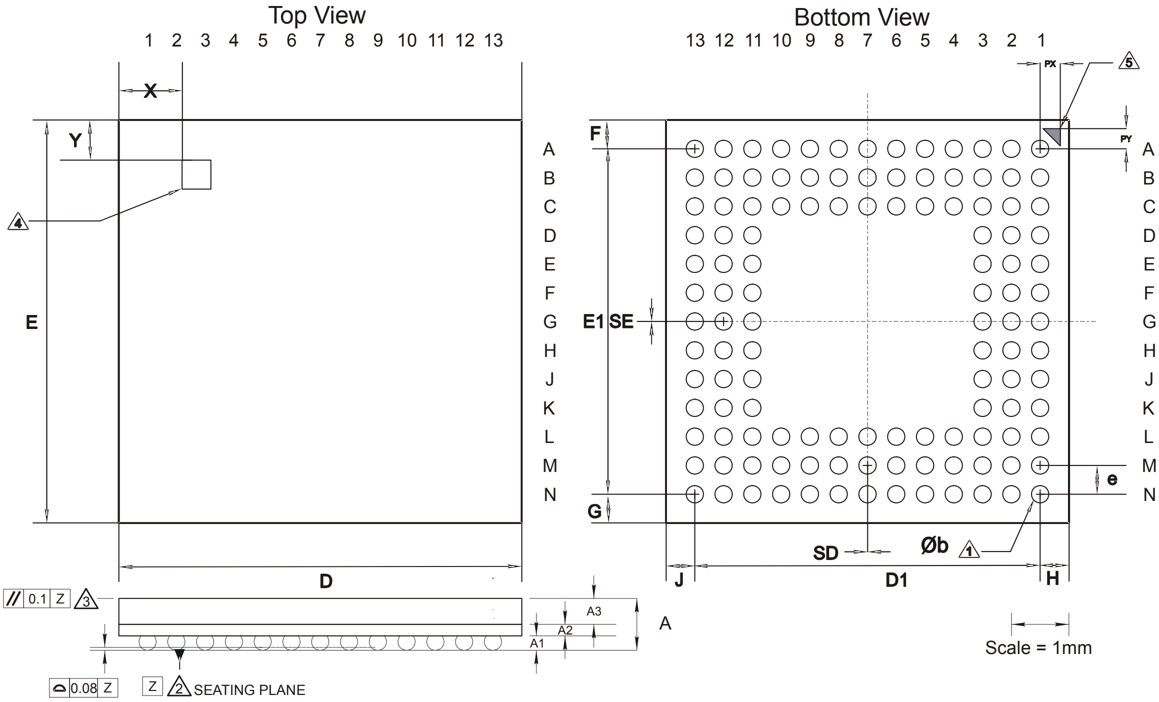
LED Drivers	Ball	Pad Type	Supply Domain	Description
LED[1]	C8	Open drain output	See Section 11.9	LED driver
LED[0]	D11			LED driver

Power Supplies and Control	Ball	Pad Type	Description
VREGENABLE_L	M3	Analogue	Take high to enable both low-voltage regulator and audio low-voltage regulator
VREGENABLE_H	C7	Analogue	Take high to enable high-voltage linear regulator and switch-mode regulator
VREGIN_L	M2	Regulator input	Low-voltage linear regulator input for non-audio core circuitry
VREGIN_AUDIO	A4	Regulator input	Audio low-voltage linear regulator input
VREGIN_H	B12, C12	Regulator input	High-voltage linear regulator input
VREGOUT_H	D12, D13	Supply	High-voltage linear regulator output
LX	A11, B11	Switch-mode power regulator output	Switch-mode power regulator output
VDD_USB	N10	VDD	Positive supply for UART and USB ports
VDD_PIO	E1	VDD	Positive supply for PIO and AUX DAC
VDD_PADS	K13	VDD	Positive supply for all other digital input/output ports
VDD_CORE	C13, J13	VDD	Positive supply for internal digital circuitry, 1.5V

Power Supplies and Control	Ball	Pad Type	Description
VDD_RADIO	K1	VDD/Low-voltage regulator sense	Positive supply for RF circuitry, 1.5V
VDD_LO	L1	VDD	Positive supply for local oscillator circuitry, 1.5V
VDD_ANA	M1	VDD/Low-voltage regulator output	Positive supply output for analogue circuitry and 1.5V regulated output (from low-voltage regulator)
VDD_AUDIO	B4	VDD	Positive supply for audio, 1.5V
BAT_P	A12, A13	Battery terminal +ve	Lithium ion/polymer battery positive terminal. Battery charger output and input to switch-mode regulator.
VDD_CHG	B8, B9, C9	Charger input	Lithium ion/polymer battery charger input
VDD_SMP_CORE	B13	VDD	Positive supply for switch mode control circuitry
VDD_MEM	A8, N11	VDD	Positive supply for internal Flash memory
VSS_DIG	G3, C6, N7, A9, A10, C11, K11, L11	VSS	Ground connection for internal digital circuitry
VSS_RADIO	F2, G2, H2, J2	VSS	Ground connections for RF circuitry
VSS_LO	L2, L3	VSS	Ground connections for local oscillator
VSS_ANA	N3, N4	VSS	Ground connections for analogue circuitry
VSS_AUDIO	C2, C3, C4	VSS	Ground connection for audio
BAT_N	B10, C10	Battery terminal -ve	Lithium ion/polymer battery negative terminal. Ground connection for switch-mode regulator.
SUBS	K2, J3, K3, L4, M4, B5, C5, L5, A6, B6, L6, M6, A7, B7, L7, M7, L8, N8	VSS	Connection to internal die substrate. Connect to lowest possible potential.

Unconnected Terminals	Ball	Description
NC	F1, G1	Leave unconnected

3.3 Package Dimensions



Description	120-Ball Low-Profile Fine-Pitch Ball Grid Array (LFBGA)			
Size	7 x 7 x 1.3mm			
Pitch	0.5mm			
Package Ball Land	Solder mask defined. Solder mask aperture 275µm Ø			
Dimension	**Minimum**	**Typical**	**Maximum**	**Notes**
A	-	-	1.30	1: Dimension b is measured at the maximum solder ball diameter parallel to datum plane Z
A1	0.16	-	0.26	
A2	-	0.21	-	
A3	-	0.80	-	2: Datum Z is defined by the spherical crowns of the solder balls
b	0.27	-	0.37	
D	-	7	-	
E	-	7	-	3: Parallelism measurement shall exclude any effect of mark on top surface of package
e	-	0.50	-	
D1	-	6.00	-	4: Top-side polarity mark. The dimensions of the square polarity mark are 0.5 x 0.5mm.
E1	-	6.00	-	
F	0.450	0.500	0.550	5: Bottom-side polarity mark. The dimensions of the triangular polarity mark are 0.30 x 0.30 x 0.42mm.
G	0.450	0.500	0.550	
H	0.450	0.500	0.550	
J	0.450	0.500	0.550	
PX	-	0.350	-	
PY	-	0.350	-	
SD	-	0	-	
SE	-	0	-	
X	-	1.10	-	
Y	-	0.70	-	
JEDEC	MO-225			
Unit	mm			

Figure 3.2: 120-ball LFBGA Package Dimensions

3.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 7 x 7 x 1.3mm LFBGA 120-ball package:

- NSMD lands, i.e. lands smaller than the solder mask aperture, are preferred because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- Ideally, via-in-pad technology should be used to achieve truly NSMD lands. Where this is not possible, a maximum of one trace connected to each land is preferred and this trace should be as thin as possible – taking into consideration its current carrying and the RF requirements.
- 35µm thick (1oz) copper lands are recommended rather than 17µm thick (0.5oz). This results in a greater standoff which has been proven to provide greater reliability during thermal cycling.
- Land diameter should be the same as that on the package to achieve optimum reliability.
- Solder paste is preferred to flux during the assembly process because this adds to the final volume of solder in the joint, increasing its reliability.
- Where a nickel gold plating finish is used, the gold thickness should be kept below 0.5µm to prevent brittle gold/tin intermetallics forming in the solder.

3.5 Typical Solder Reflow Profile

See *Typical Solder Reflow Profile for Lead-free Devices* for information.

4 Bluetooth Modem

4.1 RF Ports

4.1.1 RF_N and RF_P

RF_N and RF_P form a complementary balanced pair and are available for both transmit and receive. On transmit their outputs are combined using an external balun into the single-ended output required for the antenna. Similarly, on receive their input signals are combined internally.

Both terminals present similar complex impedances that may require matching networks between them and the balun. Viewed from the chip, the outputs can each be modelled as an ideal current source in parallel with a lossy capacitor. An equivalent series inductance can represent the package parasitics.

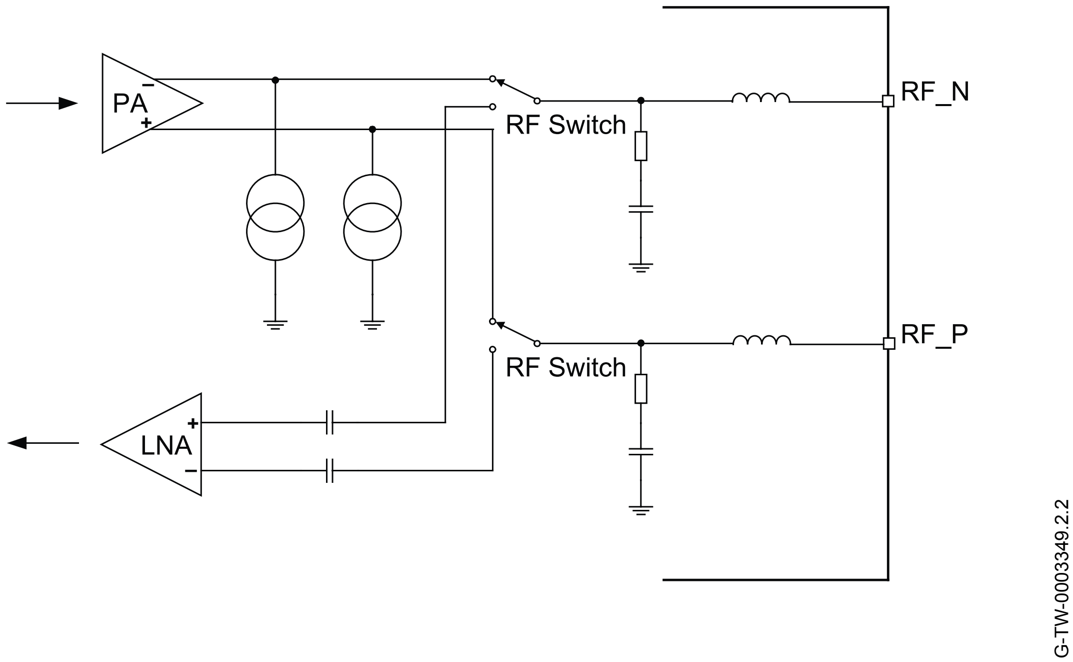


Figure 4.1: Simplified Circuit RF_N and RF_P

RF_N and RF_P require an external DC bias. The DC level must be set at VDD_RADIO.

4.2 RF Receiver

The receiver features a near-zero IF architecture that allows the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input allows the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. The use of a digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise allows BlueCore5-Multimedia Flash (16Mb) to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

For EDR, the demodulator contains an ADC which digitises the IF received signal. This information is then passed to the EDR modem.

4.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the shared RF port.

4.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference limited environments.

4.3 RF Transmitter

4.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

4.3.2 Power Amplifier

The internal PA has a maximum output power that allows BlueCore5-Multimedia Flash (16Mb) to be used in Class 2 and Class 3 radios without an external RF PA.

4.3.3 Transmit RF Power Control for Class 1 Applications (TX_PWR)

An 8-bit voltage DAC, AUX_DAC, controls the amplification level of the external PA for Class 1 operation. The DAC output is derived from the on-chip band gap and is virtually independent of temperature and supply voltage. Equation 4.1 and Equation 4.2 show the the output voltage:

$$V_{DAC} = \text{MIN}\left(\left(3.7V \times \frac{\text{EXT\_PA\_GAIN}}{255} - 0.008 \times I\right), \text{PIOSupply} - 0.008 \times I\right)$$

Equation 4.1: Output Voltage with Load Current I

or

$$V_{DAC} = \text{MIN}\left(\left(3.7V \times \frac{\text{EXT\_PA\_GAIN}}{255}\right), \text{PIOSupply}\right)$$

Equation 4.2: Output Voltage with No Load Current

Note:

PIOSupply = VDD_PIO

BlueCore5-Multimedia Flash (16Mb) enables the external PA only when transmitting. Before transmitting, the chip normally ramps up the power to the internal PA, then it ramps it down again afterwards. However, if a suitable external PA is used, it may be possible to ramp the power externally by driving the TX_PWR pin on the PA from AUX_DAC.

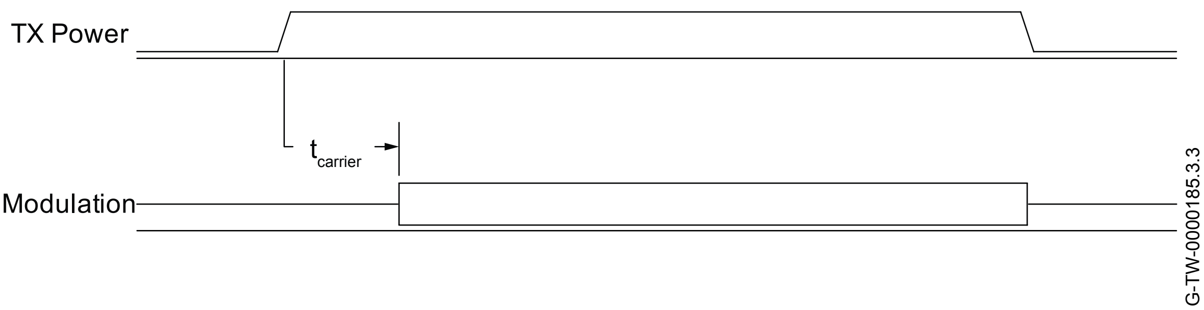


Figure 4.2: Internal Power Ramping

The PS Key PSKEY_TX_GAINRAMP, is used to control the delay, in units of µs, between the end of the transmit power ramp and the start of modulation.

PS Key TXRX_PIO_CONTROL controls external RF components such as a switch, an external PA or an external LNA. PIO[0], PIO[1] and the AUX_DAC can be used for this purpose, as Table 4.1 shows.

TXRX_PIO_CONTROL Value	PIO and AUX_DAC Use
0	PIO[0], PIO[1] and AUX_DAC not used to control RF. Power ramping is internal.
1	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC not used. Power ramping is internal.
2	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
3	PIO[0] is low during RX, PIO[1] is low during TX. AUX_DAC used to set gain of external PA. Power ramping is external.
4	PIO[0] is high during RX, PIO[1] is high during TX. AUX_DAC used to set gain of external PA. Power ramping is internal.

Table 4.1: TXRX_PIO_CONTROL Values

4.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v2.1 + EDR specification.

4.5 Baseband

4.5.1 Burst Mode Controller

During transmission the BMC constructs a packet from header information previously loaded into memory-mapped registers by the software and payload data/voice taken from the appropriate ring buffer in the RAM. During reception, the BMC stores the packet header in memory-mapped registers and the payload data in the appropriate ring buffer in RAM. This architecture minimises the intervention required by the processor during transmission and reception.

4.5.2 Physical Layer Hardware Engine

Dedicated logic performs the following:

- Forward error correction
- Header error control
- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation
- Audio transcoding

Firmware performs the following voice data translations and operations:

- A-law/µ-law/linear voice data (from host)
- A-law/µ-law/CVSD (over the air)
- Voice interpolation for lost packets
- Rate mismatch correction

The hardware supports all optional and mandatory features of Bluetooth v2.1 + EDR specification including AFH and eSCO.

4.6 Basic Rate Modem

The basic rate modem satisfies the basic data rate requirements of the Bluetooth v2.1 + EDR specification. The basic rate was the standard data rate available on the Bluetooth v1.2 specification and below, it is based on GFSK modulation scheme.

Including the basic rate modem allows BlueCore5-Multimedia Flash (16Mb) compatibility with earlier Bluetooth products.

The basic rate modem uses the RF ports, receiver, transmitter and synthesiser, alongside the baseband components described in Section 4.5.

4.7 Enhanced Data Rate Modem

The EDR modem satisfies the requirements of the Bluetooth v2.1 + EDR specification. EDR has been introduced to provide 2x and 3x data rates with minimal disruption to higher layers of the Bluetooth stack. BlueCore5-Multimedia Flash (16Mb) supports both the basic and enhanced data rates and is compliant with the Bluetooth v2.1 + EDR specification.

At the baseband level, EDR uses the same 1.6kHz slot rate and the 1MHz symbol rate defined for the basic data rate. EDR differs in that each symbol in the payload portion of a packet represents 2 or 3 bits. This is achieved using 2 new distinct modulation schemes. Table 4.2 and Figure 4.3 summarise these. Link Establishment and Management are unchanged and still use GFSK for both the header and payload portions of these packets.

The enhanced data rate modem uses the RF ports, receiver, transmitter and synthesiser, with the baseband components described in Section 4.5.

Data Rate Scheme	Bits Per Symbol	Modulation
Basic Rate	1	GFSK
EDR	2	π/4 DQPSK
EDR	3	8DPSK (optional)

Table 4.2: Data Rate Schemes

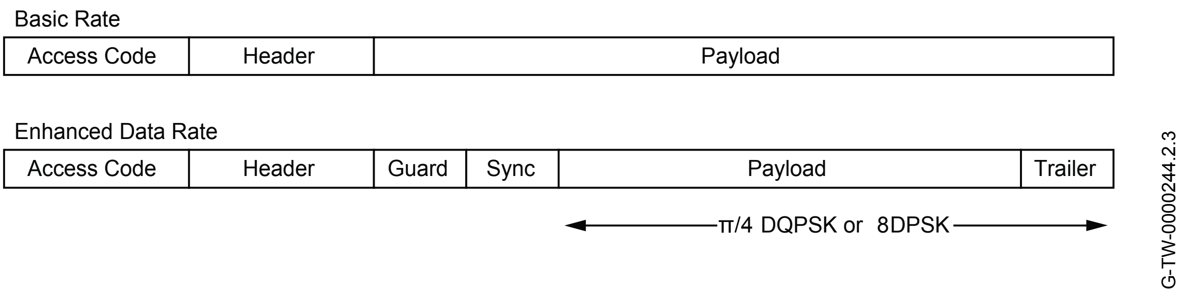


Figure 4.3: BDR and EDR Packet Structure

5 Clock Generation

BlueCore5-Multimedia Flash (16Mb) requires a Bluetooth reference clock frequency of 12MHz to 52MHz from either an externally connected crystal or from an external TCXO source.

All BlueCore5-Multimedia Flash (16Mb) internal digital clocks are generated using a phase locked loop, which is locked to the frequency of either the external 12MHz to 52MHz reference clock source or an internally generated watchdog clock frequency of 1kHz.

The Bluetooth operation determines the use of the watchdog clock in low-power modes.

5.1 Clock Architecture

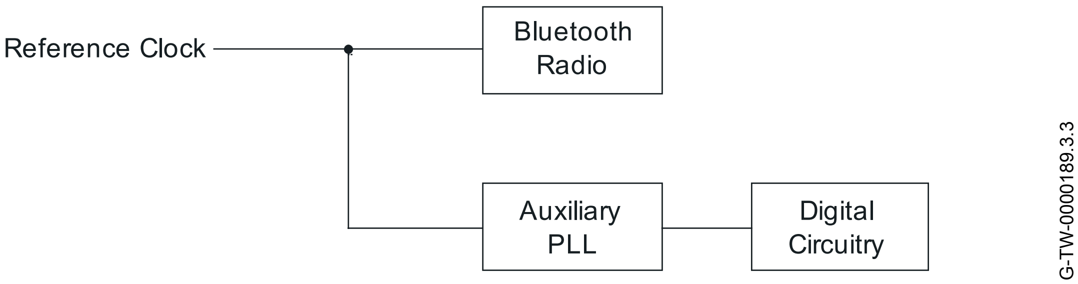


Figure 5.1: Clock Architecture

5.2 Input Frequencies and PS Key Settings

BlueCore5-Multimedia Flash (16Mb) should be configured to operate with the chosen reference frequency. Do this by setting the PS Key PSKEY_ANA_FREQ for all frequencies with an integer multiple of 250kHz. The input frequency default setting in BlueCore5-Multimedia Flash (16Mb) is 26MHz depending on the software build. Full details are in the software release note for the specific build from www.csrsupport.com.

The following CDMA/3G phone TCXO frequencies are also catered for: 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz. The value of the PS Key is a multiple of 1kHz, so 38.4MHz is selected by using a PS Key value of 38400.

Reference Crystal Frequency (MHz)	PSKEY_ANA_FREQ (kHz)
14.40	14400
15.36	15360
16.20	16200
16.80	16800
19.20	19200
19.44	19440
19.68	19680
19.80	19800
38.40	38400
n x 0.25	n x 250
26.00 (default)	26000

Table 5.1: PS Key Values for CDMA/3G Phone TCXO

5.3 External Reference Clock

5.3.1 Input: XTAL_IN

The external reference clock is applied to the BlueCore5-Multimedia Flash (16Mb) XTAL_IN input. BlueCore5-Multimedia Flash (16Mb) is configured to accept the external reference clock at XTAL_IN by connecting XTAL_OUT to ground.

The external clock can be either a digital level square wave or sinusoidal, and this may be directly coupled to XTAL_IN without the need for additional components. A digital level reference clock gives superior noise immunity, as the high slew rate clock edges have lower voltage to phase conversion. If peaks of the reference clock are either below VSS_ANA or above VDD_ANA, it must be driven through a DC blocking capacitor (approximately 33pF) connected to XTAL_IN.

The external reference clock signal should meet the specifications in Table 5.2.

			Min	Typ	Max	Unit
Frequency[a]			12	26	52	MHz
Duty cycle			20:80	50:50	80:20	-
Edge jitter (at zero crossing)			-	-	15	ps rms
Signal level	AC coupled sinusoid		0.4	-	VDD_ANA[b]	V pk-pk
	DC coupled digital	V_{IL}	-	VSS_ANA[c]	-	V
		V_{IH}	-	VDD_ANA[b][c]	-	V

Table 5.2: External Clock Specifications

[a] The frequency should be an integer multiple of 250kHz except for the CDMA/3G frequencies

[b] VDD_ANA is 1.50V nominal

[c] If driven via a DC blocking capacitor max amplitude is reduced to 750mV pk-pk for non 50:50 duty cycle

5.3.2 XTAL_IN Impedance in External Mode

The impedance of XTAL_IN does not change significantly between operating modes, typically 10fF. When transitioning from deep sleep to an active state a spike of up to 1pC may be measured. For this reason CSR recommends that a buffered clock input is used.

5.3.3 Clock Start-up Delay

BlueCore5-Multimedia Flash (16Mb) hardware incorporates an automatic 5ms delay after the assertion of the system clock request signal before running firmware, see Figure 5.2. This is suitable for most applications using an external clock source. However, there may be scenarios where the clock cannot be guaranteed to either exist or be stable after this period. Under these conditions, BlueCore5-Multimedia Flash (16Mb) firmware provides a software function that extends the system clock request signal by a period stored in PSKEY_CLOCK_STARTUP_DELAY. This value is set in milliseconds from 1ms to 31ms. Zero is the default entry for 5ms delay.

This PS Key allows the designer to optimise a system where clock latencies may be longer than 5ms while still keeping the current consumption of BlueCore5-Multimedia Flash (16Mb) as low as possible. BlueCore5-Multimedia Flash (16Mb) consumes about 2mA of current for the duration of PSKEY_CLOCK_STARTUP_DELAY before activating the firmware.

5.3.4 Clock Timing Accuracy

As Figure 5.2 shows, the 250ppm timing accuracy on the external clock is required 2ms after the firmware begins to run. This is to guarantee that the firmware can maintain timing accuracy in accordance with the Bluetooth v2.1 + EDR specification. Radio activity may occur after 6ms after the firmware starts. Therefore, at this point the timing accuracy of the external clock source must be within ±20ppm.

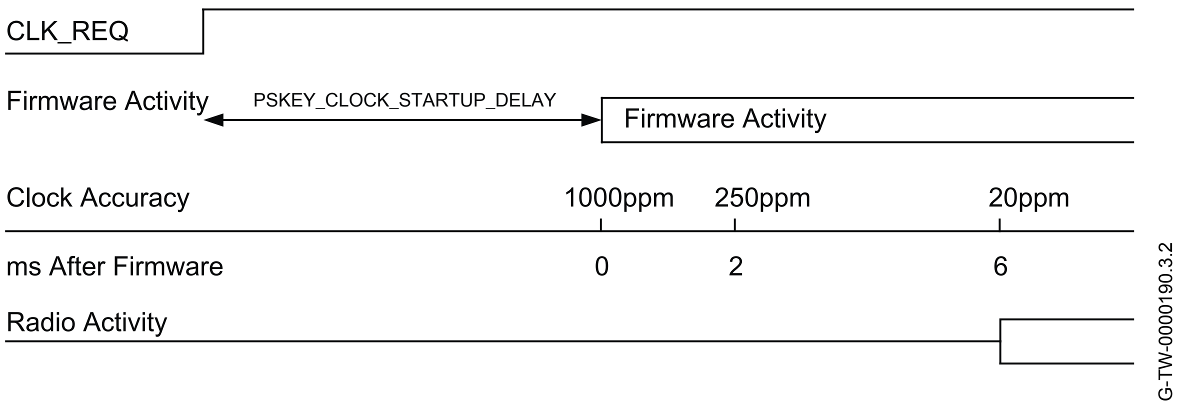


Figure 5.2: TCXO Clock Accuracy

5.4 Crystal Oscillator: XTAL_IN and XTAL_OUT

BlueCore5-Multimedia Flash (16Mb) contains a crystal driver circuit. This operates with an external crystal and capacitors to form a Pierce oscillator. Figure 5.3 shows the external crystal is connected to pins XTAL_IN, XTAL_OUT.

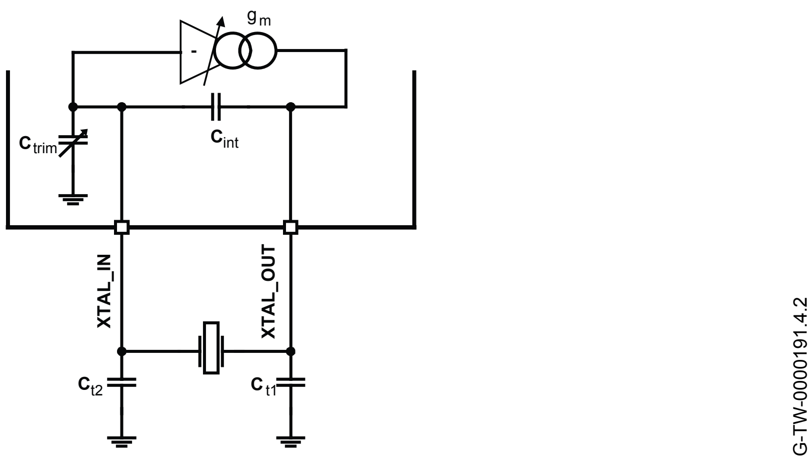


Figure 5.3: Crystal Driver Circuit

Figure 5.4 shows an electrical equivalent circuit for a crystal. The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors.

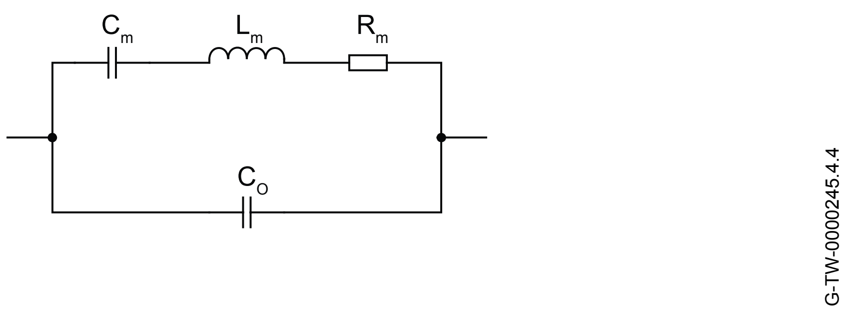


Figure 5.4: Crystal Equivalent Circuit

The resonant frequency may be trimmed with the crystal load capacitance. BlueCore5-Multimedia Flash (16Mb) contains variable internal capacitors to provide a fine trim.

Parameter	Min	Typ	Max	Unit
Frequency	16	26	26	MHz
Initial Tolerance	-	±25	-	ppm
Pullability	-	±20	-	ppm/pF

Table 5.3: Crystal Specification

The BlueCore5-Multimedia Flash (16Mb) driver circuit is a transconductance amplifier. A voltage at XTAL_IN generates a current at XTAL_OUT. The value of transconductance is variable and may be set for optimum performance.

5.4.1 Load Capacitance

For resonance at the correct frequency the crystal should be loaded with its specified load capacitance, which is defined for the crystal. This is the total capacitance across the crystal viewed from its terminals. BlueCore5-Multimedia Flash (16Mb) provides some of this load with the capacitors C_{trim} and C_{int}. The remainder should be from the external capacitors labelled C_{t1} and C_{t2}. C_{t1} should be three times the value of C_{t2} for best noise performance. This maximises the signal swing and slew rate at XTAL_IN (to which all on-chip clocks are referred).

Crystal load capacitance, C_l is calculated using Equation 5.1:

$$C_l = C_{int} + \frac{(C_{t2} + C_{trim})\, C_{t1}}{C_{t2} + C_{trim} + C_{t1}}$$

Equation 5.1: Load Capacitance

Note:

C_{trim} = 3.4pF nominal (mid-range setting)

C_{int} = 1.5pF

C_{int} does not include the crystal internal self capacitance; it is the driver self capacitance.

5.4.2 Frequency Trim

BlueCore5-Multimedia Flash (16Mb) enables frequency adjustments to be made. This feature is typically used to remove initial tolerance frequency errors associated with the crystal. Frequency trim is achieved by adjusting the crystal load capacitance with an on-chip trim capacitor, C_{trim}. The value of C_{trim} is set by a 6-bit word in PSKEY_ANA_FTRIM. Its value is calculated as follows:

$$C_{trim} = 125\text{fF} \times \text{PSKEY\_ANA\_FTRIM}$$

Equation 5.2: Trim Capacitance

The C_{trim} capacitor is connected between XTAL_IN and ground. When viewed from the crystal terminals, the combination of the tank capacitors and the trim capacitor presents a load across the terminals of the crystal which varies in steps of typically 125fF for each least significant bit increment of PSKEY_ANA_FTRIM.

Equation 5.3 describes the frequency trim.

$$\frac{\Delta(F_x)}{F_x} = \text{pullability} \times 0.110 \times \left(\frac{C_{t1}}{C_{t1} + C_{t2} + C_{trim}}\right)(\text{ppm/LSB})$$

Equation 5.3: Frequency Trim

Note:

F_x = crystal frequency

Pullability is a crystal parameter with units of ppm/pF

Total trim range is 0 to 63

If not specified, the pullability of a crystal may be calculated from its motional capacitance with Equation 5.4.

$$\frac{\partial(F_X)}{\partial(C_l)} = F_X \bullet \frac{C_m}{2(C_l + C_0)^2}$$

Equation 5.4: Pullability

Note:

C_0 = Crystal self capacitance (shunt capacitance)

C_m = Crystal motional capacitance (series branch capacitance in crystal model), see Figure 5.4

It is a Bluetooth requirement that the frequency is always within ±20ppm. The trim range should be sufficient to pull the crystal within ±5ppm of the exact frequency. This leaves a margin of ±15ppm for frequency drift with ageing and temperature. A crystal with an ageing and temperature drift specification of better than ±15ppm is required.

5.4.3 Transconductance Driver Model

The crystal and its load capacitors should be viewed as a transimpedance element, whereby a current applied to one terminal generates a voltage at the other. The transconductance amplifier in BlueCore5-Multimedia Flash (16Mb) uses the voltage at its input, XTAL_IN, to generate a current at its output, XTAL_OUT. Therefore, the circuit oscillates if the transconductance, transimpedance product is greater than unity. For sufficient oscillation amplitude, the product should be greater than three. The transconductance required for oscillation is defined by the relationship shown in Equation 5.5.

$$g_m > 3\,\frac{(2\pi F_x)^2\,R_m\,((C_0 + C_{int})(C_{t1} + C_{t2} + C_{trim}) + C_{t1}\,(C_{t2} + C_{trim}))}{C_{t1}\,(C_{t2} + C_{trim})}$$

Equation 5.5: Transconductance Required for Oscillation

BlueCore5-Multimedia Flash (16Mb) guarantees a transconductance value of at least 2mA/V at maximum drive level.

Note:

More drive strength is required for higher frequency crystals, higher loss crystals (larger R_m) or higher capacitance loading

Optimum drive level is attained when the level at XTAL_IN is approximately 1V pk-pk. The drive level is determined by the crystal driver transconductance.

5.4.4 Negative Resistance Model

An alternative representation of the crystal and its load capacitors is a frequency dependent resistive element. The driver amplifier may be considered as a circuit that provides negative resistance. For oscillation, the value of the negative resistance must be greater than that of the crystal circuit equivalent resistance. Although the BlueCore5-Multimedia Flash (16Mb) crystal driver circuit is based on a transimpedance amplifier, it is possible to calculate an equivalent negative resistance for it using the formula in Equation 5.6.

$$R_{neg} > \frac{C_{t1}(C_{t2} + C_{trim})}{g_m(2\pi F_x)^2(C_0 + C_{int})((C_{t1} + C_{t2} + C_{trim}) + C_{t1}(C_{t2} + C_{trim}))^2}$$

Equation 5.6: Equivalent Negative Resistance

Equation 5.6 shows the negative resistance of the BlueCore5-Multimedia Flash (16Mb) driver as a function of its drive strength.

The value of the driver negative resistance may be easily measured by placing an additional resistance in series with the crystal. The maximum value of this resistor (oscillation occurs) is the equivalent negative resistance of the oscillator.

5.4.5 Crystal PS Key Settings

The BlueCore5-Multimedia Flash (16Mb) firmware automatically controls the drive level on the crystal circuit to achieve optimum input swing. PSKEY_XTAL_TARGET_AMPLITUDE is used by the firmware to servo the required amplitude of crystal oscillation. Refer to the software build release note for a detailed description.

Configure the BlueCore5-Multimedia Flash (16Mb) to operate with the chosen reference frequency.

6 Bluetooth Stack Microcontroller

A 16-bit RISC MCU is used for low power consumption and efficient use of memory.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

6.1 TCXO Enable OR Function

An OR function exists for clock enable signals from a host controller and BlueCore5-Multimedia Flash (16Mb) where either device can turn on the clock without having to wake up the other device, see Figure 6.1. PIO[3] can be used as the host clock enable input and PIO[2] can be used as the OR output with the TCXO enable signal from BlueCore5-Multimedia Flash (16Mb).

Note:

To turn on the clock, the clock enable signal on PIO[3] must be high.

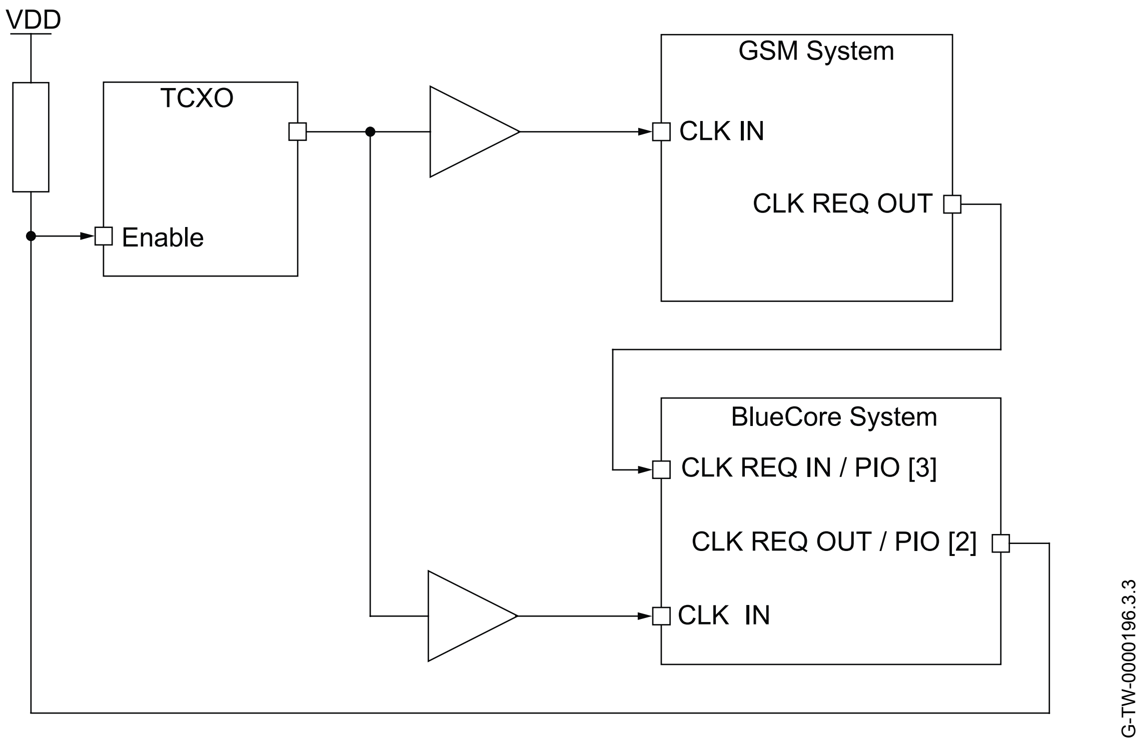


Figure 6.1: Example TCXO Enable OR Function

On reset and up to the time the PIO has been configured, PIO[2] is tristate. Therefore, the developer must ensure that the circuitry connected to this pin is pulled via a 470kΩ resistor to the appropriate power rail. This ensures that the TCXO is oscillating at start up.

6.2 Programmable I/O Ports, PIO and AIO

18 lines of programmable bidirectional I/O are provided.

Note:

PIO[15:4] are powered from VDD_PADS and PIO[3:0] are powered from VDD_PIO. AIO[1:0] are powered from VDD_ANA.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes. PIO[6] or PIO[2] can be configured as a request line for an external clock source. Using PSKEY_CLOCK_REQUEST_ENABLE, this terminal can be configured to be low when BlueCore5-Multimedia Flash (16Mb) is in deep sleep and high when a clock is required.

Note:

CSR cannot guarantee that the PIO assignments remain as described. Refer to the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

BlueCore5-Multimedia Flash (16Mb) has 2 general-purpose analogue interface pins, AIO[1:0], used to access internal circuitry and control signals. Auxiliary functions available on the analogue interface include a 10-bit ADC and a 8-bit DAC. Signals selectable on this interface include the band gap reference voltage and a variety of clock signals: 64, 48, 32, 24, 16, 12, 8, 6 and 2MHz (outputted from AIO[0] only) and the XTAL and XTAL/2 clock frequency (outputted from AIO[0] and AIO[1]). When used with analogue signals the voltage range is constrained by the analogue supply voltage. When configured to drive out digital level signals (clocks) generated from within the analogue part of the device, the output voltage level is determined by VDD_ANA.

6.3 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of WLAN coexistence schemes. Channel skipping AFH, priority signalling, channel signalling and host passing of channel instructions are all supported. The features are configured in firmware.

For more information see *Bluetooth and IEEE 802.11 b/g Co-existence Solutions Overview*.

7 Kalimba DSP

The Kalimba DSP is an open platform Kalimba DSP allowing signal processing functions to be performed on over-air data or codec data in order to enhance audio applications. Figure 7.1 shows the Kalimba DSP interfaces to other functional blocks within BlueCore5-Multimedia Flash (16Mb).

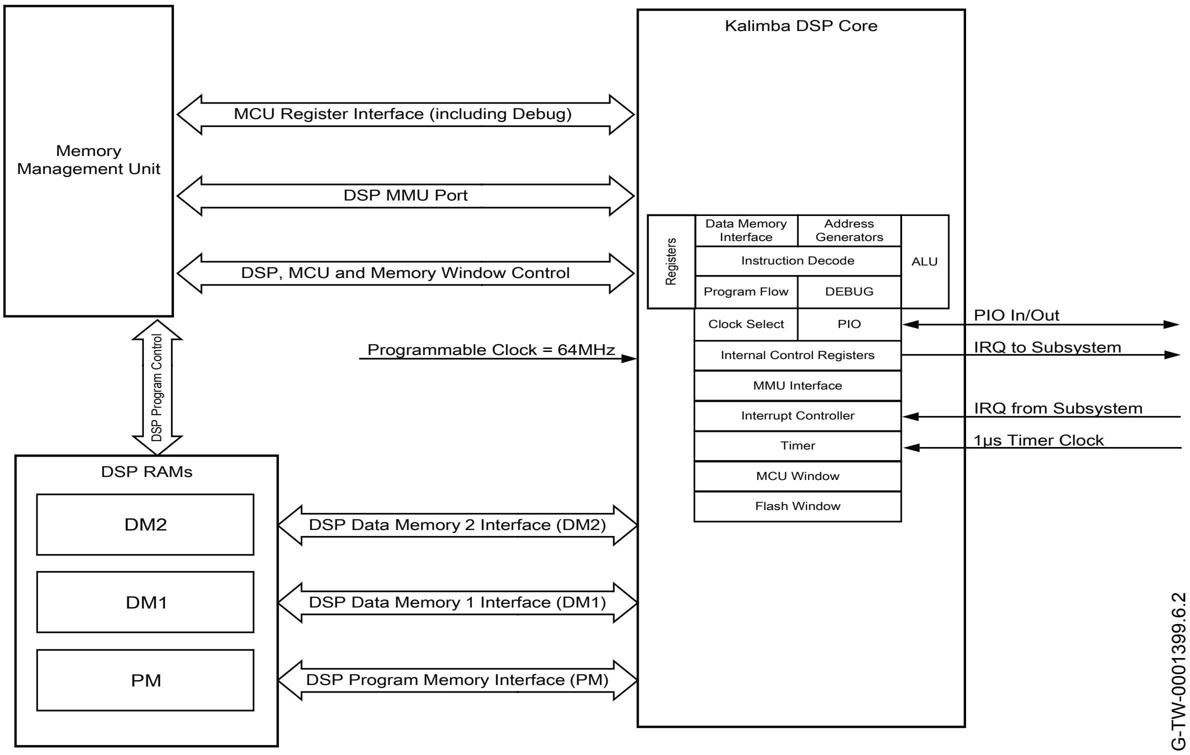


Figure 7.1: Kalimba DSP Interface to Internal Functions

The key features of the DSP include:

- 64MIPS performance, 24-bit fixed point DSP core
- Single cycle MAC of 24 x 24-bit multiply and 56-bit accumulate
- 32-bit instruction word
- Separate program memory and dual data memory, allowing an ALU operation and up to two memory accesses in a single cycle
- Zero overhead looping
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 24-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

8 Memory Interface and Management

8.1 Memory Management Unit

The MMU provides a number of dynamically allocated ring buffers that hold the data that is in transit between the host, the air or the Kalimba DSP. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by a hardware MMU to minimise the overheads on the processor during data/voice transfers.

8.2 System RAM

48KB of on-chip RAM supports the RISC MCU and is shared between the ring buffers used to hold voice/data for each active connection and the general-purpose memory required by the Bluetooth stack.

8.3 Kalimba DSP RAM

Additional on-chip RAM is provided to support the Kalimba DSP:

- 16K x 24-bit for data memory 1 (DM1)
- 12K x 24-bit for data memory 2 (DM2)
- 6K x 32-bit for program memory (PM)

Note:

The Kalimba DSP can also execute directly from internal flash, using a 64-instruction on-chip cache.

8.4 Internal Flash Memory (16Mb)

16Mb of internal flash memory is available on the BlueCore5-Multimedia Flash (16Mb). The internal flash memory is provided for system firmware and the Kalimba DSP coprocessor code implementation.

The internal flash memory provides 16Mb of internal code and data storage. This storage is used to store BlueCore5-Multimedia Flash (16Mb) settings and program code, and Kalimba DSP coprocessor code and data.

8.4.1 Flash Specification

The flash device used with BlueCore5-Multimedia Flash (16Mb) meets the following criteria:

Parameter	Value
Data width	16-bit
Capacity	16Mb
Access time	70ns

Table 8.1: Internal Flash Device Specifications

9 Serial Interfaces

9.1 UART Interface

BlueCore5-Multimedia Flash (16Mb) has a standard UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

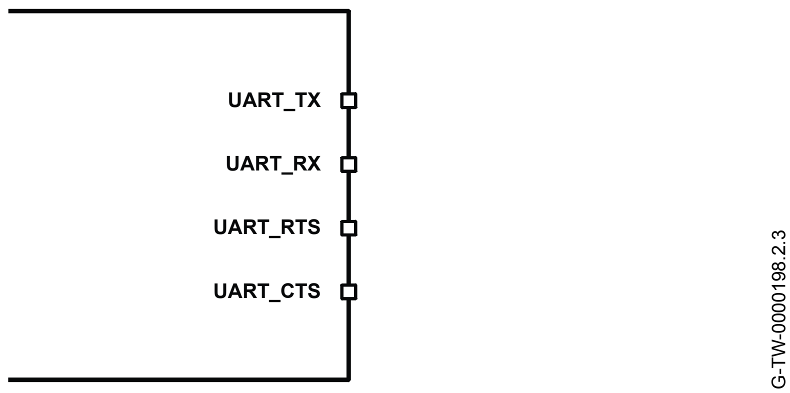


Figure 9.1: Universal Asynchronous Receiver

Figure 9.1 shows the 4 signals that implement the UART function. When BlueCore5-Multimedia Flash (16Mb) is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, can implement RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using BlueCore5-Multimedia Flash (16Mb) firmware.

Note:

> To communicate with the UART at its maximum data rate using a standard PC, an accelerated serial port adapter card is required for the PC.

Parameter		Possible Values
Baud rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4Mbaud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 9.1: Possible UART Settings

The UART interface can reset BlueCore5-Multimedia Flash (16Mb) on reception of a break signal. A break is identified by a continuous logic low (0V) on the UART_RX terminal, as Figure 9.2 shows. If t_{BRK} is longer than the value, defined by PSKEY_HOSTIO_UART_RESET_TIMEOUT, a reset occurs. This feature allows a host to initialise the system to a known state. Also, BlueCore5-Multimedia Flash (16Mb) can emit a break character that may be used to wake the host.

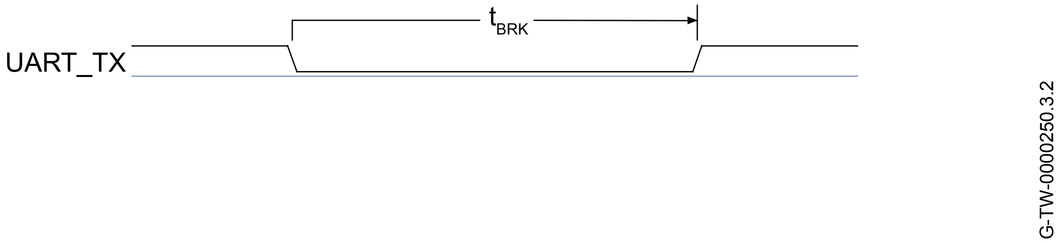


Figure 9.2: Break Signal

Note:

The DFU boot loader must be loaded into the flash device before the UART or USB interfaces can be used. This initial flash programming can be done via the SPI.

Table 9.2 shows a list of commonly used baud rates and their associated values for the PSKEY_UART_BAUDRATE. There is no requirement to use these standard values. Any baud rate within the supported range can be set in the PS Key according to the formula in Equation 9.1.

$$\text{Baud Rate} = \frac{\text{PSKEY\_UART\_BAUDRATE}}{0.004096}$$

Equation 9.1: Baud Rate

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
1200	0x0005	5	1.73%
2400	0x000a	10	1.73%
4800	0x0014	20	1.73%
9600	0x0027	39	-0.82%
19200	0x004f	79	0.45%
38400	0x009d	157	-0.18%
57600	0x00ec	236	0.03%
76800	0x013b	315	0.14%
115200	0x01d8	472	0.03%
230400	0x03b0	944	0.03%

Baud Rate	Persistent Store Value		Error
	Hex	Dec	
460800	0x075f	1887	-0.02%
921600	0x0ebf	3775	0.00%
1382400	0x161e	5662	-0.01%
1843200	0x1d7e	7550	0.00%
2764800	0x2c3d	11325	0.00%
3686400	0x3afb	15099	0.00%

Table 9.2: Standard Baud Rates

9.1.1 UART Configuration While Reset is Active

The UART interface is tristate while BlueCore5-Multimedia Flash (16Mb) is being held in reset. This allows the user to daisy chain devices onto the physical UART bus. The constraint on this method is that any devices connected to this bus must tristate when BlueCore5-Multimedia Flash (16Mb) reset is de-asserted and the firmware begins to run.

9.1.2 UART Bypass Mode

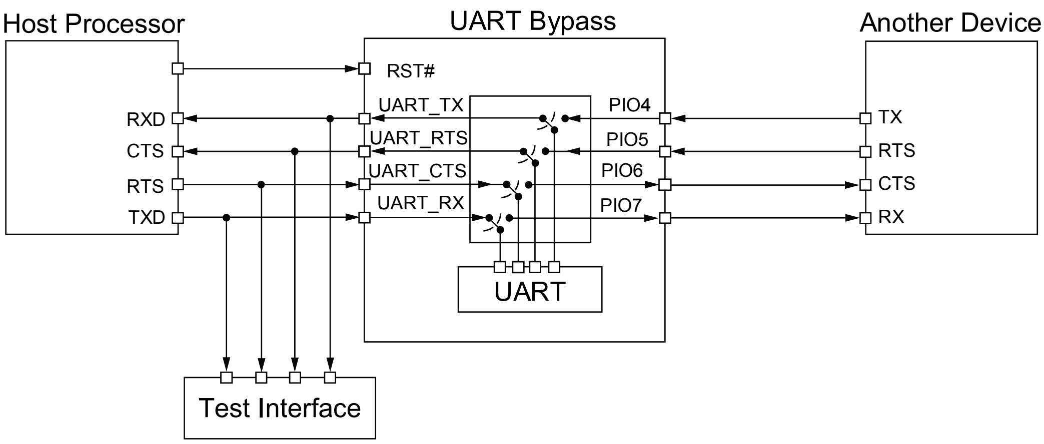


Figure 9.3: UART Bypass Architecture

Alternatively, for devices that do not tristate the UART bus, the UART bypass mode on BlueCore5-Multimedia Flash (16Mb) can be used. The default state of BlueCore5-Multimedia Flash (16Mb) after reset is de-asserted; this is for the host UART bus to be connected to the BlueCore5-Multimedia Flash (16Mb) UART, thereby allowing communication to BlueCore5-Multimedia Flash (16Mb) via the UART. All UART bypass mode connections are implemented using CMOS technology and have signalling levels of 0V and VDD_PADS.

To apply the UART bypass mode, a BCCMD command is issued to BlueCore5-Multimedia Flash (16Mb). Upon this issue, it switches the bypass to PIO[7:4] as Figure 9.3 shows. When the bypass mode has been invoked, BlueCore5-Multimedia Flash (16Mb) enters the deep sleep state indefinitely.

To re-establish communication with BlueCore5-Multimedia Flash (16Mb), the chip must be reset so that the default configuration takes effect.

It is important for the host to ensure a clean Bluetooth disconnection of any active links before the bypass mode is invoked. Therefore, it is not possible to have active Bluetooth links while operating the bypass mode.

Note:

When in bypass mode, the UART signal levels on the PIO are at VDD_PADS level and when not bypassed, i.e. when using the normal UART pins, the levels are at VDD_USB levels.

9.1.3 Current Consumption in UART Bypass Mode

The current consumption for a device in UART bypass mode is equal to the values quoted for a device in standby mode.

9.2 USB Interface

BlueCore5-Multimedia Flash (16Mb) has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on the BlueCore5-Multimedia Flash (16Mb) acts as a USB peripheral, responding to requests from a master host controller.

BlueCore5-Multimedia Flash (16Mb) supports the *Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification)*, available from http://www.usb.org. For more information on how to integrate the USB interface on BlueCore5-Multimedia Flash (16Mb) see the *Bluetooth and USB Design Considerations Application Note*.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw
  - PIO status in suspend mode
  - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

9.3 Programming and Debug Interface

Important Note:

> The SPI is used to program and configure (PS Keys), and debug the BlueCore5-Multimedia Flash (16Mb). It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header.
>
> CSR provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from CSR.

BlueCore5-Multimedia Flash (16Mb) uses a 16-bit data and 16-bit address programming and debug interface. Transactions can occur when the internal processor is running or is stopped.

Data may be written or read one word at a time, or the auto-increment feature is available for block access.

9.3.1 Instruction Cycle

The BlueCore5-Multimedia Flash (16Mb) is the slave and receives commands on SPI_MOSI and outputs data on SPI_MISO. Table 9.3 shows the instruction cycle for a SPI transaction.

1	Reset the SPI interface	Hold SPI_CS# high for two SPI_CLK cycles
2	Write the command word	Take SPI_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take SPI_CS# high

Table 9.3: Instruction Cycle for a SPI Transaction

With the exception of reset, SPI_CS# must be held low during the transaction. Data on SPI_MOSI is clocked into the BlueCore5-Multimedia Flash (16Mb) on the rising edge of the clock line SPI_CLK. When reading, BlueCore5-Multimedia Flash (16Mb) replies to the master on SPI_MISO with the data changing on the falling edge of the SPI_CLK. The master provides the clock on SPI_CLK. The transaction is terminated by taking SPI_CS# high.

Sending a command word and the address of a register for every time it is to be read or written is a significant overhead, especially when large amounts of data are to be transferred. To overcome this BlueCore5-Multimedia Flash (16Mb) offers increased data transfer efficiency via an auto increment operation. To invoke auto increment, SPI_CS# is kept low, which auto increments the address, while providing an extra 16 clock cycles for each extra word to be written or read.

9.3.2 Multi-slave Operation

BlueCore5-Multimedia Flash (16Mb) should not be connected in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BlueCore5-Multimedia Flash (16Mb) is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, BlueCore5-Multimedia Flash (16Mb) outputs `0` if the processor is running or `1` if it is stopped.

9.4 I²C Interface

9.4.1 Software I²C Interface

PIO[8:6] can be used to form a master I²C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix LCD, keyboard scanner or EEPROM.

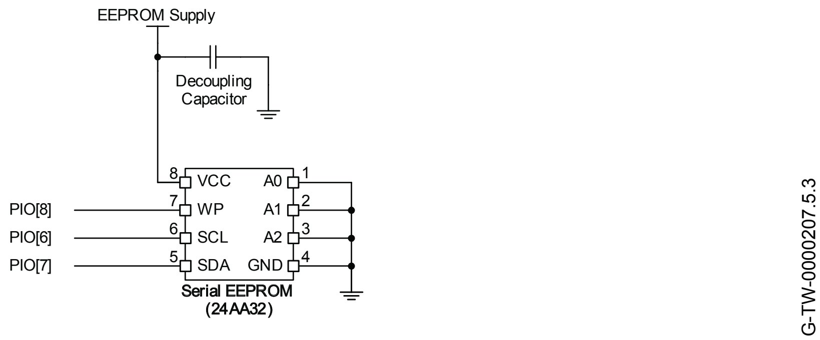


Figure 9.4: Example EEPROM Connection

9.4.2 Bit-serialiser Interface

In addition to the software I²C interface outlined in Section 9.4.1, the BlueCore5-Multimedia Flash (16Mb) includes a configurable hardware bit-serialiser interface. Any 3 PIOs can be used as a serial master interface by configuring the hardware bit-serialiser. In the I²C master mode, the hardware bit-serialiser supports address, direction and ACK handling, but does not support multi-master I²C bus systems. I²C slave mode is also not supported.

Note:

The I²C interface can be directly controlled by the MCU or the Kalimba DSP.

Suitable firmware is required to support the hardware bit-serialiser interface.

I²C and SPI are supported.

10 Audio Interface

The audio interface circuit consists of:

- Stereo audio codec
- Dual audio inputs and outputs
- A configurable PCM, I²S or SPDIF interface

Figure 10.1 shows the functional blocks of the interface. The codec supports stereo playback and recording of audio signals at multiple sample rates with a resolution of 16-bit. The ADC and the DAC of the codec each contain 2 independent channels. Any ADC or DAC channel can be run at its own independent sample rate.

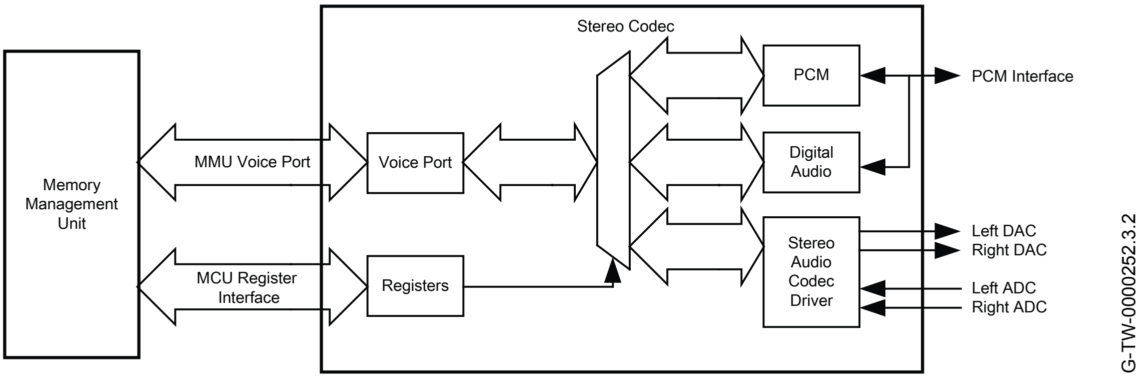


Figure 10.1: Audio Interface

The interface for the digital audio bus shares the same pins as the PCM codec interface described in Section 10.3 which means each of the audio buses are mutually exclusive in their usage. Table 10.1 lists these alternative functions.

PCM Interface	SPDIF Interface	I²S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC	-	WS
PCM_CLK	-	SCK

Table 10.1: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

10.1 Audio Input and Output

The audio input circuitry consists:

- 2 independent channels programmed for either microphone or line input
- Each channel is independently configurable to be either single-ended or fully differential
- Each channel has an analogue and digital programmable gain stage for optimisation of different microphones

The audio output circuitry consists of a dual differential class A-B output stage.

10.2 Stereo Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I²S
- Support for IEC-60958 standard stereo digital audio bus standards, e.g. SPDIF and AES3/EBU
- Support for PCM interfaces including PCM master codecs that require an external system clock

Important Note:

To avoid any confusion regarding stereo operation this data sheet explicitly states which is the left and right channel for audio input and output. With respect to software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel for both input and output.

10.2.1 Stereo Audio Codec Block Diagram

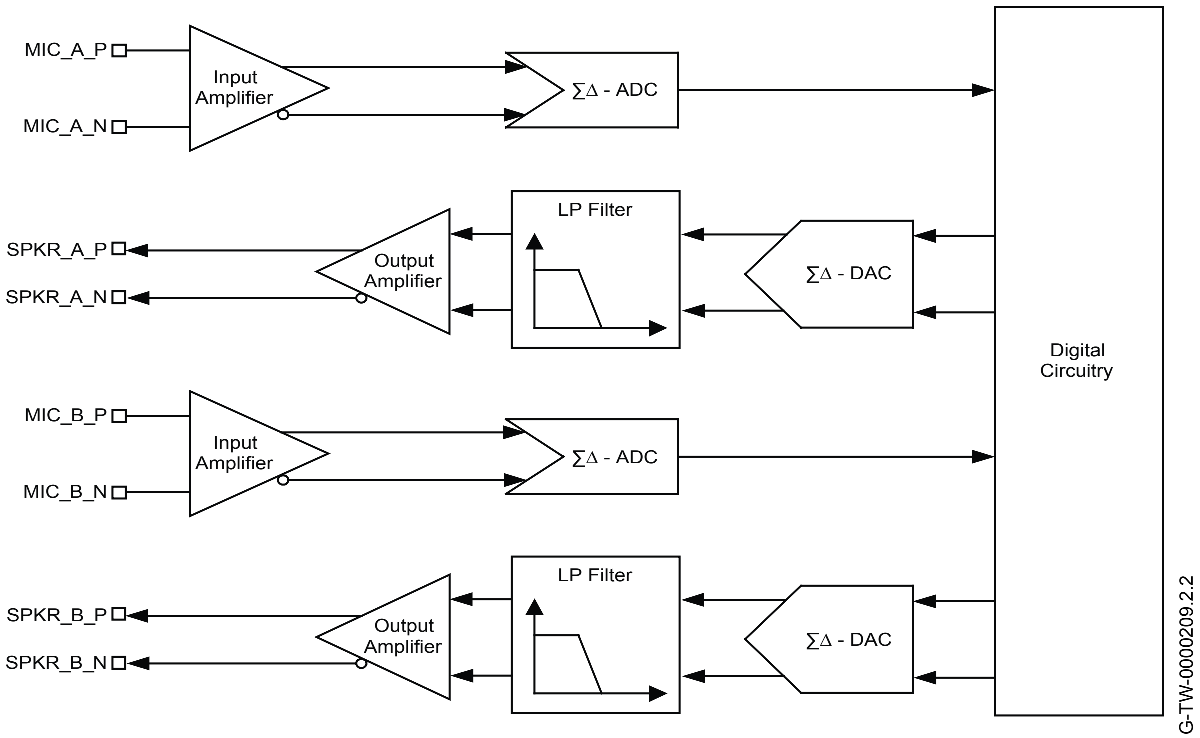


Figure 10.2: Stereo Codec Audio Input and Output Stages

The stereo audio codec uses a fully differential architecture in the analogue signal path, which results in low noise-sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a single power-supply of 1.5V and uses a minimum of external components.

10.2.2 Stereo Codec Set-up

The configuration and control of the ADC is through VM functions described in appropriate SDK documentation. This section is an overview of the parameters that can be set up using the VM functions.

The Kalimba DSP can communicate its codec requirements to the MCU, and therefore also to the VM, by exchange of messages. The messages used between the Kalimba DSP and the embedded MCU are based on interrupts:

- 1 interrupt between the MCU and Kalimba DSP
- 1 interrupt between the Kalimba DSP and the MCU

Message content is transmitted using shared memory. There are VM and DSP library functions to send and receive messages; refer to appropriate SDK documentation for further details.

10.2.3 ADC

The ADC consists of:

- 2 second-order Sigma-Delta converters allowing 2 separate channels that are identical in functionality, as Figure 10.2 shows.
- 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage.

10.2.4 ADC Sample Rate Selection

Each ADC supports the following sample rates:

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 24kHz
- 32kHz
- 44.1kHz

10.2.5 ADC Digital Gain

The digital gain stage has a programmable selection value in the range of 0 to 15 with the associated ADC gain settings summarised in Table 10.2. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32dB steps. Contact CSR for more information.

Gain Selection Value	ADC Digital Gain Setting (dB)	Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 10.2: ADC Digital Gain Rate Selection

10.2.6 ADC Analogue Gain

Figure 10.3 shows the equivalent block diagram for the ADC analogue amplifier. It is a two-stage amplifier:

- The first stage amplifier has a 24dB gain for the microphone.
- The second stage has a programmable gain with 7 individual 3dB steps. By combining the 24dB gain selection of the microphone input with the 7 individual 3dB gain steps, the overall range of the analogue amplifier is approximately -3dB to 42dB in 3dB steps. The VM function controls all the gain control of the ADC.

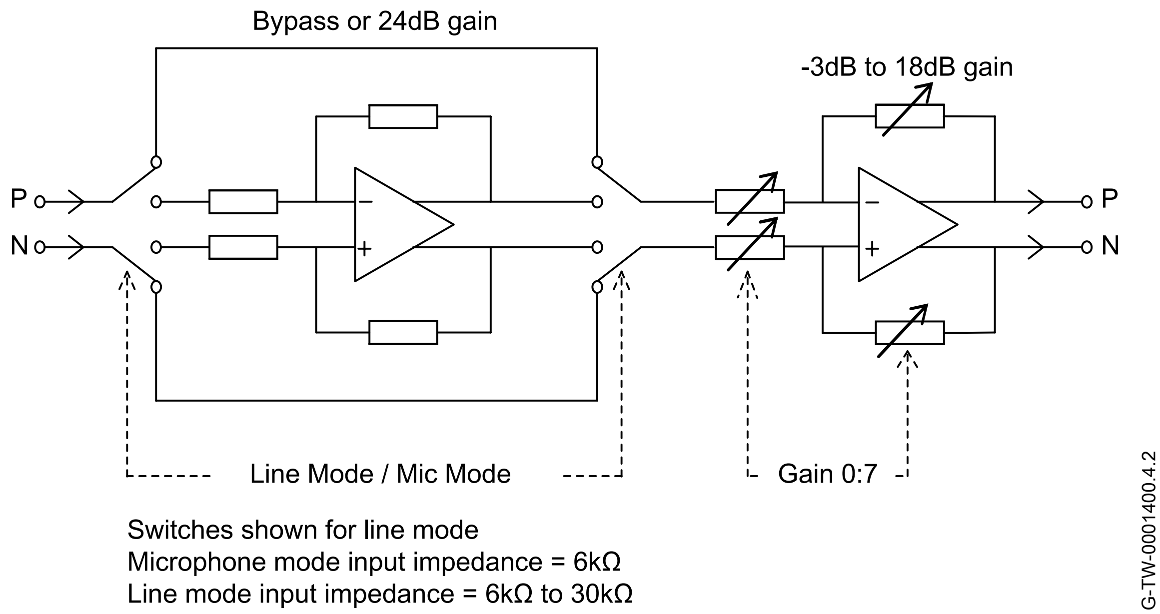


Figure 10.3: ADC Analogue Amplifier Block Diagram

10.2.7 DAC

The DAC consists of:

- 2 second-order Sigma-Delta converters allowing 2 separate channels that are identical in functionality, as Figure 10.2 shows.
- 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage.

10.2.8 DAC Sample Rate Selection

Each DAC supports the following samples rates:

- 8kHz
- 11.025kHz
- 12kHz
- 16kHz
- 22.050kHz
- 24kHz
- 32kHz
- 44.1kHz
- 48kHz

10.2.9 DAC Digital Gain

The digital gain stage has a programmable selection value in the range of 0 to 15 with associated DAC gain settings, summarised in Table 10.3. There is also a high resolution digital gain mode that allows the gain to be changed in 1/32dB steps. Contact CSR for more information.

The overall gain control of the DAC is controlled by VM function. Its setting is a combined function of the digital and analogue amplifier settings.

Digital Gain Selection Value	DAC Digital Gain Setting (dB)	Digital Gain Selection Value	DAC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 10.3: DAC Digital Gain Rate Selection

10.2.10 DAC Analogue Gain

As Table 10.4 shows the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dB steps.

The VM function controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)
7	3	3	-9
6	0	2	-12
5	-3	1	-15
4	-6	0	-18

Table 10.4: DAC Analogue Gain Rate Selection

10.2.11 Microphone Input

Figure 10.4 shows recommended biasing for each microphone. The microphone bias, MIC_BIAS, derives its power from the BAT_P and requires a 1µF capacitor on its output.

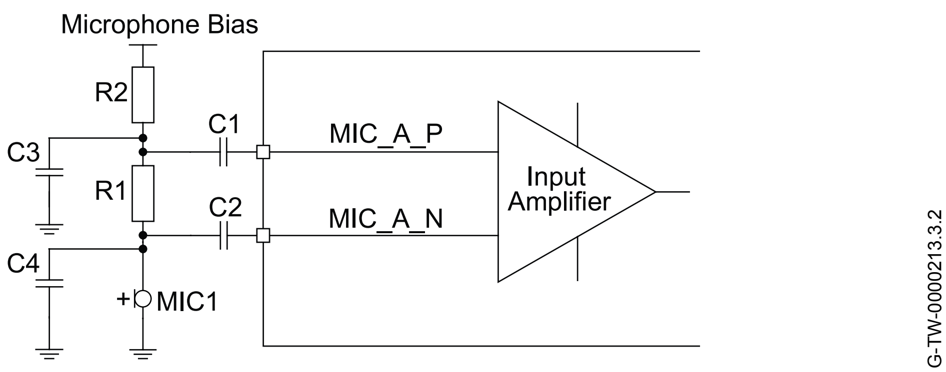


Figure 10.4: Microphone Biasing

Note:

Figure 10.4 shows a single channel only.

The MIC_BIAS is like any voltage regulator and requires a minimum load to maintain regulation. The MIC_BIAS maintains regulation within the limits 0.200mA to 1.230mA. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.

The audio input is intended for use in the range from 1µA at 94dB SPL to about 10µA at 94dB SPL. With biasing resistors R1 and R2 equal to 1kΩ, this requires microphones with sensitivity between about –40dBV and –60dBV.

The input impedance at MIC_A_N, MIC_A_P, MIC_B_N and MIC_B_P is typically 6.0kΩ.

C1 and C2 should be 150nF if bass roll-off is required to limit wind noise on the microphone.

R1 sets the microphone load impedance and is normally in the range of 1kΩ to 2kΩ.

R2, C3 and C4 improve the supply rejection by decoupling supply noise from the microphone. Values should be selected as required. R2 may be connected to a convenient supply, in which case the bias network is permanently enabled, or to the MIC_BIAS output (which is ground referenced and provides good rejection of the supply), which may be configured to provide bias only when the microphone is required.

Table 10.5 shows the 4-bit programmable output voltage that the microphone bias provides, and Table 10.6 shows the 4-bit programmable output current.

The characteristics of the microphone bias include:

- Power supply:
  - BlueCore5-Multimedia Flash (16Mb) microphone supply is BAT_P
  - Minimum input voltage = Output voltage + drop-out voltage
  - Maximum input voltage is 4.4V
  - Typically the microphone bias is between 2V and 2.5V, or as specified by the microphone vendor
- Drop-out voltage:
  - 300mV minimum
  - Guaranteed for configuration of voltage or current output shown in Table 10.5 and Table 10.6
- Output voltage:
  - 4-bit programmable from 1.7V to 3.6V
  - Tolerance 90% to 110%
- Output current:
  - 4-bit programmable from 200µA to 1.230mA
  - Maximum current guaranteed to be >1mA
- Load capacitance:
  - Unconditionally stable for 1µF ± 20% and 2.2µF ± 20% pure C

Output Step	VOL_SET[3:0]	Min	Typ	Max	Units
0	0000	-	1.71	-	V
1	0001	-	1.76	-	V
2	0010	-	1.82	-	V
3	0011	-	1.87	-	V
4	0100	-	1.95	-	V
5	0101	-	2.02	-	V
6	0110	-	2.10	-	V
7	0111	-	2.18	-	V
8	1000	-	2.32	-	V
9	1001	-	2.43	-	V
10	1010	-	2.56	-	V
11	1011	-	2.69	-	V
12	1100	-	2.90	-	V
13	1101	-	3.08	-	V
14	1110	-	3.33	-	V
15	1111	-	3.57	-	V

Table 10.5: Voltage Output Steps

Output Step	CUR_SET[3:0]	Typ	Units
0	0000	0.200	mA
1	0001	0.280	mA
2	0010	0.340	mA
3	0011	0.420	mA
4	0100	0.480	mA
5	0101	0.530	mA
6	0110	0.610	mA
7	0111	0.670	mA
8	1000	0.750	mA
9	1001	0.810	mA
10	1010	0.860	mA
11	1011	0.950	mA
12	1100	1.000	mA
13	1101	1.090	mA
14	1110	1.140	mA
15	1111	1.230	mA

Table 10.6: Current Output Steps

Note:

For BAT_P, the PSRR at 100Hz to 22kHz, with >300mV supply headroom, decoupling capacitor of 1.1µF, is typically 58.9dB and worst case 53.4dB.

For VDD_AUDIO, the PSRR at 100Hz to 22kHz, decoupling capacitor of 1.1µF, is typically 88dB and worst case 60dB.

10.2.12 Line Input

If the input analogue gain is set to less than 24dB, BlueCore5-Multimedia Flash (16Mb) automatically selects line input mode. In line input mode the first stage of the amplifier is automatically disabled, providing additional power saving. In line input mode the input impedance varies from 6kΩ to 30kΩ, depending on the volume setting. Figure 10.5 and Figure 10.6 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

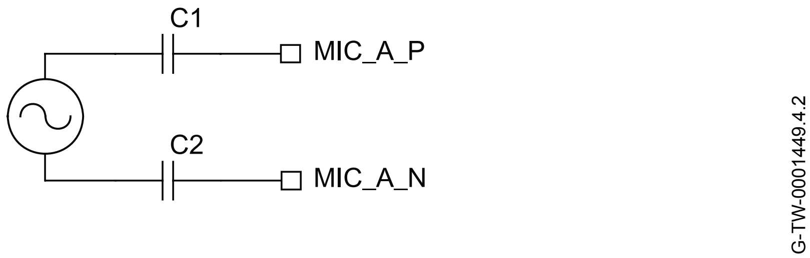


Figure 10.5: Differential Input

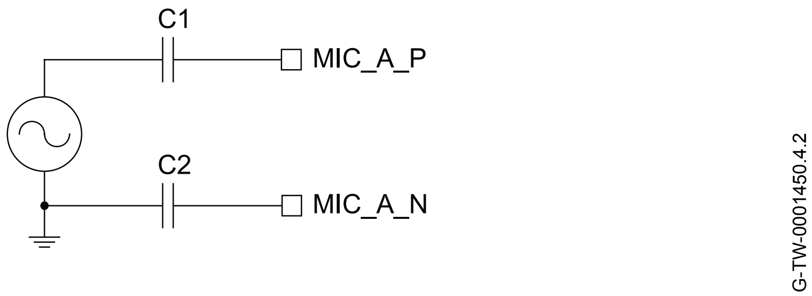


Figure 10.6: Single-ended Input

Note:

In Figure 10.5 and Figure 10.6 show only single channels.

10.2.13 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The output stage circuit comprises a DAC with gain setting and class AB output stage amplifier. The output is available as a differential signal between SPKR_A_N and SPKR_A_P for the left channel, as Figure 10.7 shows, and between SPKR_B_N and SPKR_B_P for the right channel.

The output stage is capable of driving a speaker directly when its impedance is at least 8Ω and an external regulator is used, but this will be at a reduced output swing.

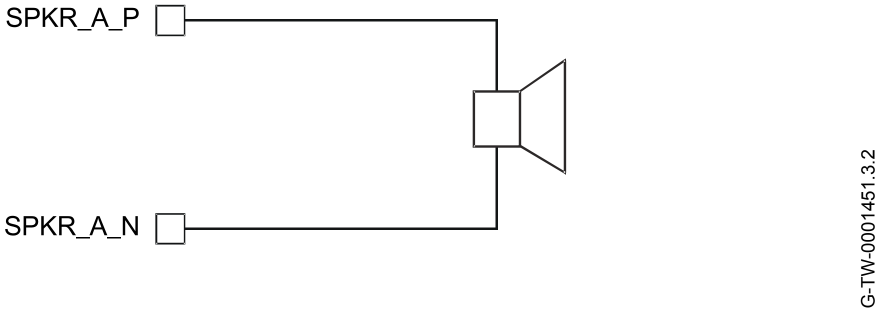


Figure 10.7: Speaker Output

Note:

Figure 10.7 shows a single channel only.

A 3-bit programmable resistive divider controls the analogue gain of the output stage, which sets the gain in steps of approximately 3dB.

BlueCore5-Multimedia Flash (16Mb) Data Sheet

10.2.14 Mono Operation

Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation the right channel is the auxiliary mono channel that may be used in dual mono channel operation.

In single channel mono operation, disable the other channel to reduce power consumption.

Important Note:

For mono operation this data sheet uses the left channel for standard mono operation for audio input and output and with respect to software and any registers, channel 0 or channel A represents the standard mono channel for audio input and output. In mono operation the second channel which is the right channel, channel 1 or channel B can be used as a second mono channel if required and this channel is referred to as the auxiliary mono channel for audio input and output.

10.2.15 Side Tone

In some applications it is necessary to implement side tone. This involves feeding an attenuated version of the microphone signal to the earpiece. The BlueCore5-Multimedia Flash (16Mb) codec contains side tone circuitry to do this. The side tone hardware is configured through the following PS Keys:

- PSKEY_SIDE_TONE_ENABLE
- PSKEY_SIDE_TONE_GAIN
- PSKEY_SIDE_TONE_AFTER_ADC
- PSKEY_SIDE_TONE_AFTER_DAC

10.2.16 Integrated Digital Filter

BlueCore5-Multimedia Flash (16Mb) has a programmable digital filter integrated into the ADC channel of the codec. The filter is a 2 stage, second order IIR and is used for functions such as custom wind noise rejection. The filter also has optional DC blocking.

The filter has 10 configuration words used as follows:

- 1 for gain value
- 8 for coefficient values
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit 2's complement signed integer with the format `XX.XXXXXXXXXX`

Note:

The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

For example:

`01.1111111111` = most positive number, close to `2`

`01.0000000000` = `1`

`00.0000000000` = `0`

`11.0000000000` = `-1`

`10.0000000000` = `-2`, most negative number

Equation 10.1 shows the equation for the IIR filter. Equation 10.2 shows the equation for when the DC blocking is enabled.

The filter can be configured, enabled and disabled from the VM via the `CodecSetIIRFilterA` and `CodecSetIIRFilterB` traps. This requires firmware support. The configuration function takes 10 variables in the order shown below:

0 : Gain

1 : b_{01}

2 : b_{02}

3 : a_{01}

4 : a_{02}

5 : b_{11}

6 : b_{12}

7 : a_{11}

8 : a_{12}

9 : DC Block (1 = enable, 0 = disable)

$$\text{Filter, } H(z) = \text{Gain} \times \frac{(1 + b_{01} z^{-1} + b_{02} z^{-2})}{(1 + a_{01} z^{-1} + a_{02} z^{-2})} \times \frac{(1 + b_{11} z^{-1} + b_{12} z^{-2})}{(1 + a_{11} z^{-1} + a_{12} z^{-2})}$$

Equation 10.1: IIR Filter Transfer Function, H(z)

$$\text{Filter with DC Blocking, } H_{DC}(z) = H(z) \times (1 - z^{-1})$$

Equation 10.2: IIR Filter plus DC Blocking Transfer Function, $H_{DC}(z)$

10.3 PCM Interface

The audio PCM interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

PCM is a standard method used to digitise audio, particularly voice, for transmission over digital communication channels. Through its PCM interface, BlueCore5-Multimedia Flash (16Mb) has hardware support for continual transmission and reception of PCM data, so reducing processor overhead. BlueCore5-Multimedia Flash (16Mb) offers a bidirectional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on BlueCore5-Multimedia Flash (16Mb) allows the data to be sent to and received from a SCO connection.

Up to 3 SCO connections can be supported by the PCM interface at any one time.

BlueCore5-Multimedia Flash (16Mb) can operate as the PCM interface master generating PCM_SYNC and PCM_CLK or as a PCM interface slave accepting externally generated PCM_SYNC and PCM_CLK. BlueCore5-Multimedia Flash (16Mb) is compatible with various clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit µ-law or A-law companded sample formats, and can receive and transmit on any selection of 3 of the first 4 slots following PCM_SYNC. The PCM configuration options are enabled by setting the PS Key PSKEY_PCM_CONFIG32.

10.3.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, BlueCore5-Multimedia Flash (16Mb) generates PCM_CLK and PCM_SYNC.

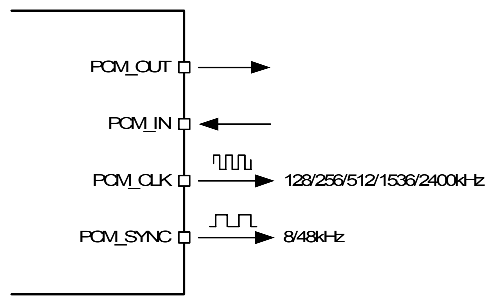


Figure 10.8: PCM Interface Master

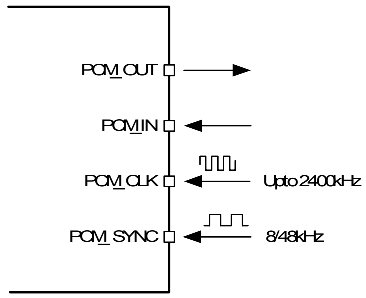


Figure 10.9: PCM Interface Slave

10.3.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When BlueCore5-Multimedia Flash (16Mb) is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When BlueCore5-Multimedia Flash (16Mb) is configured as PCM Slave, PCM_SYNC may be from one cycle PCM_CLK to half the PCM_SYNC rate.

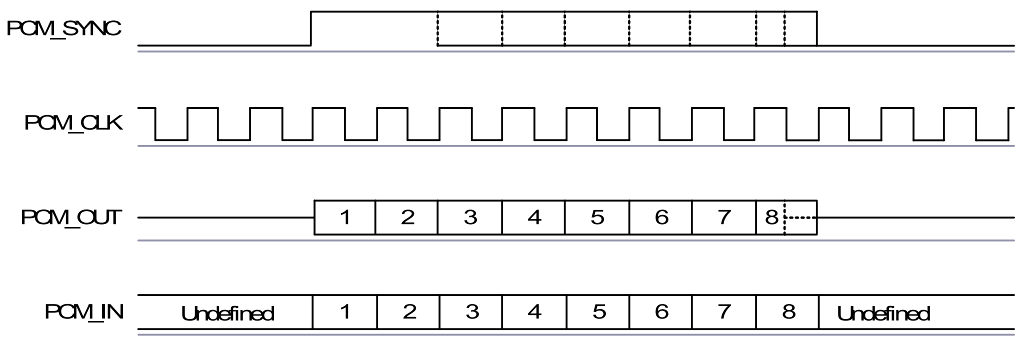


Figure 10.10: Long Frame Sync (Shown with 8-bit Companded Sample)

BlueCore5-Multimedia Flash (16Mb) samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.3.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

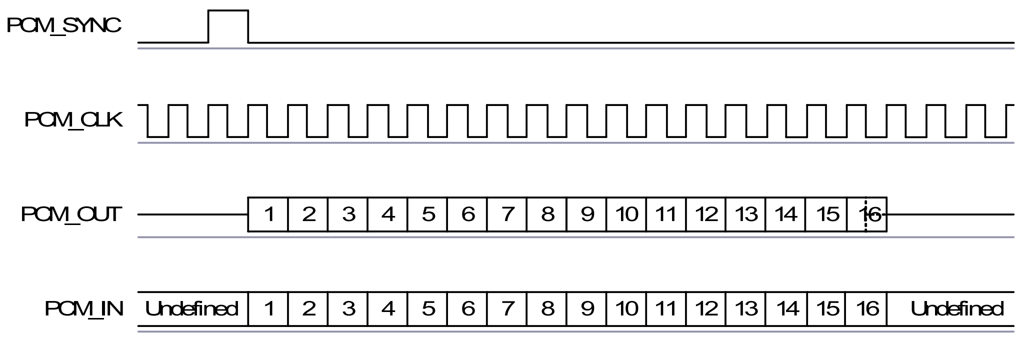


Figure 10.11: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, BlueCore5-Multimedia Flash (16Mb) samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

10.3.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

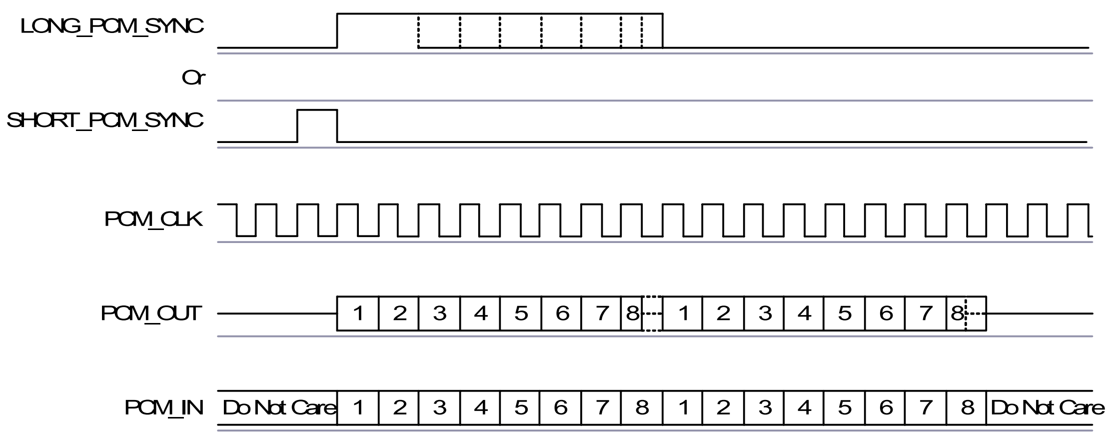


Figure 10.12: Multi-slot Operation with Two Slots and 8-bit Companded Samples

10.3.5 GCI Interface

BlueCore5-Multimedia Flash (16Mb) is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The 2 64kbps B channels can be accessed when this mode is configured.

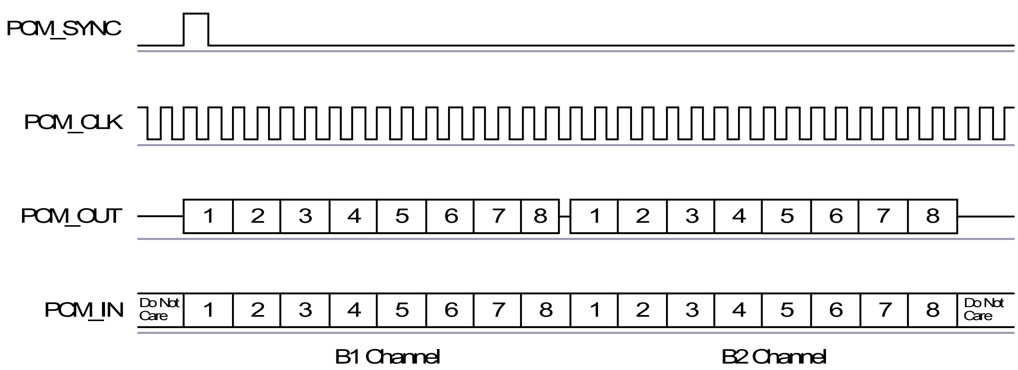


Figure 10.13: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz.

BlueCore5-Multimedia Flash (16Mb) Data Sheet

10.3.6 Slots and Sample Formats

BlueCore5-Multimedia Flash (16Mb) can receive and transmit on any selection of the first 4 slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats.

BlueCore5-Multimedia Flash (16Mb) supports 13-bit linear, 16-bit linear and 8-bit µ-law or A-law sample formats. The sample rate is 8ksamples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola codecs.

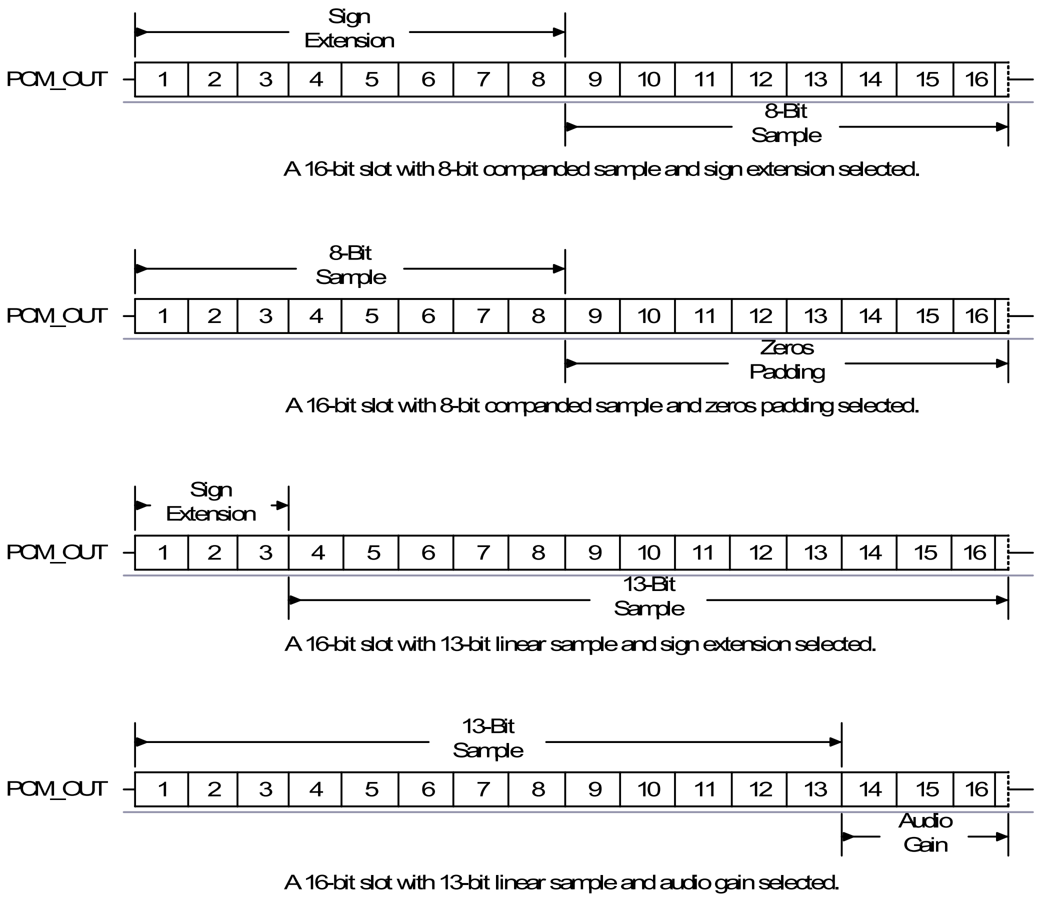


Figure 10.14: 16-Bit Slot Length and Sample Formats

10.3.7 Additional Features

BlueCore5-Multimedia Flash (16Mb) has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some codecs use to control power down.

10.3.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f_{mclk}	PCM_CLK frequency	4MHz DDS generation. Selection of frequency is programmable. See Table 10.10.	-	128	-	kHz
				256		
				512		
		48MHz DDS generation. Selection of frequency is programmable. See Table 10.9 and Section 10.3.9.	2.9	-	-	kHz
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t_{mclkh} [(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} [(a)]	PCM_CLK low	4MHz DDS generation	730	-	-	ns
-	PCM_CLK jitter	48MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 10.7: PCM Master Timing

[(a)] Assumes normal system clock operation. Figures will vary during low-power modes, when system clock speeds are reduced.

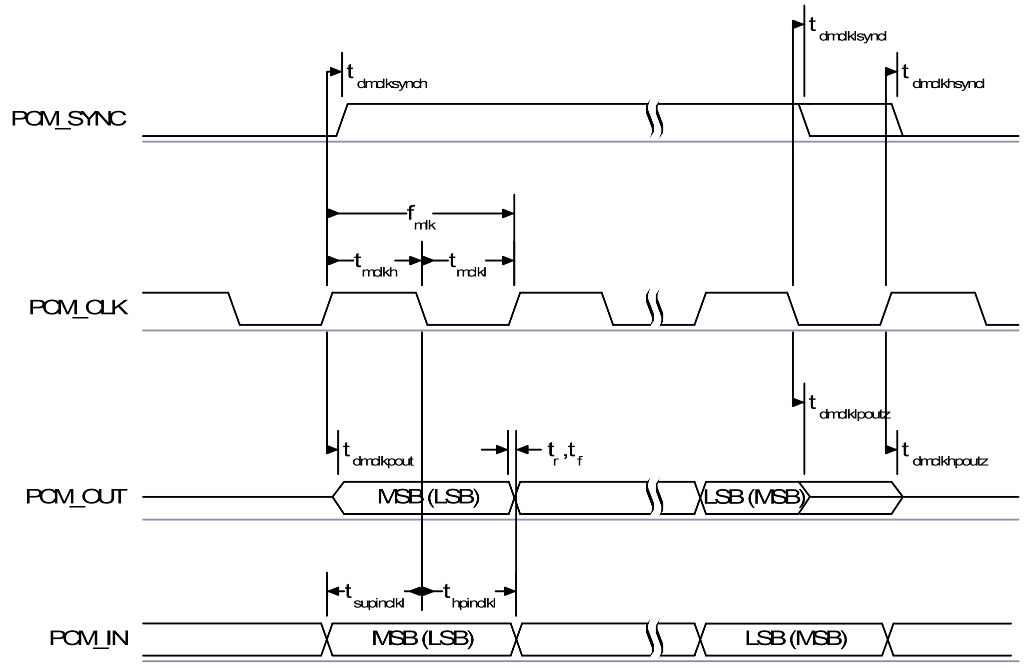


Figure 10.15: PCM Master Timing Long Frame Sync

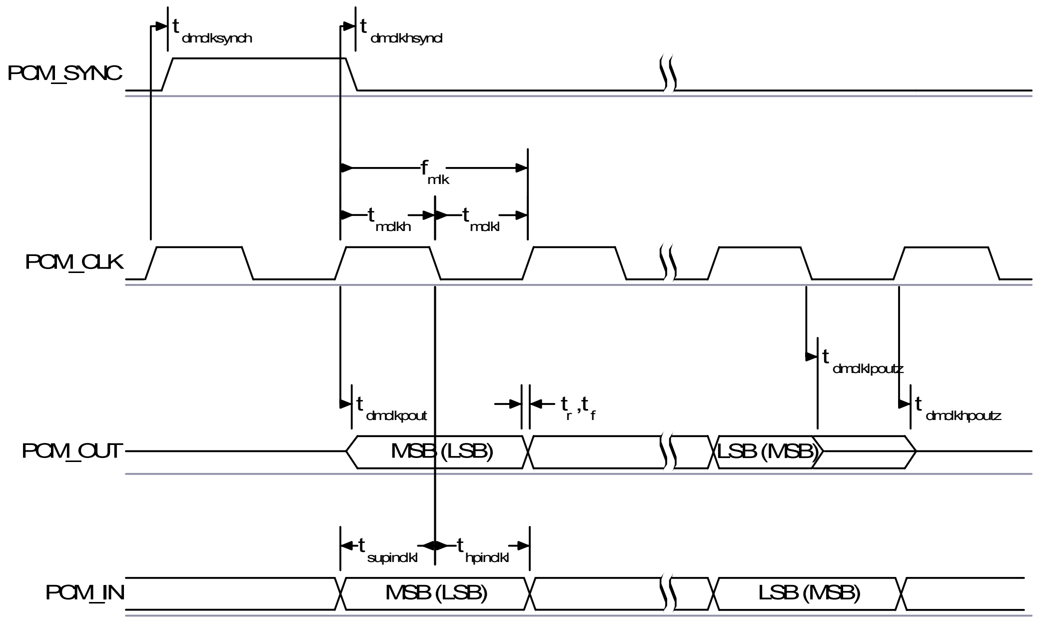


Figure 10.16: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	[a]	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	[b]	kHz
t_{sclkl}	PCM_CLK low time	80	-	-	ns
t_{sclkh}	PCM_CLK high time	80	-	-	ns
$t_{hsclksynch}$	Hold time from PCM_CLK low to PCM_SYNC high	20	-	-	ns
$t_{susclksynch}$	Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{dsclkhpout}$	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for PCM_IN valid to CLK low	20	-	-	ns
$t_{hpinsclkl}$	Hold time for PCM_CLK low to PCM_IN invalid	20	-	-	ns

Table 10.8: PCM Slave Timing

[a] Max frequency is the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

[b] Max frequency is twice the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

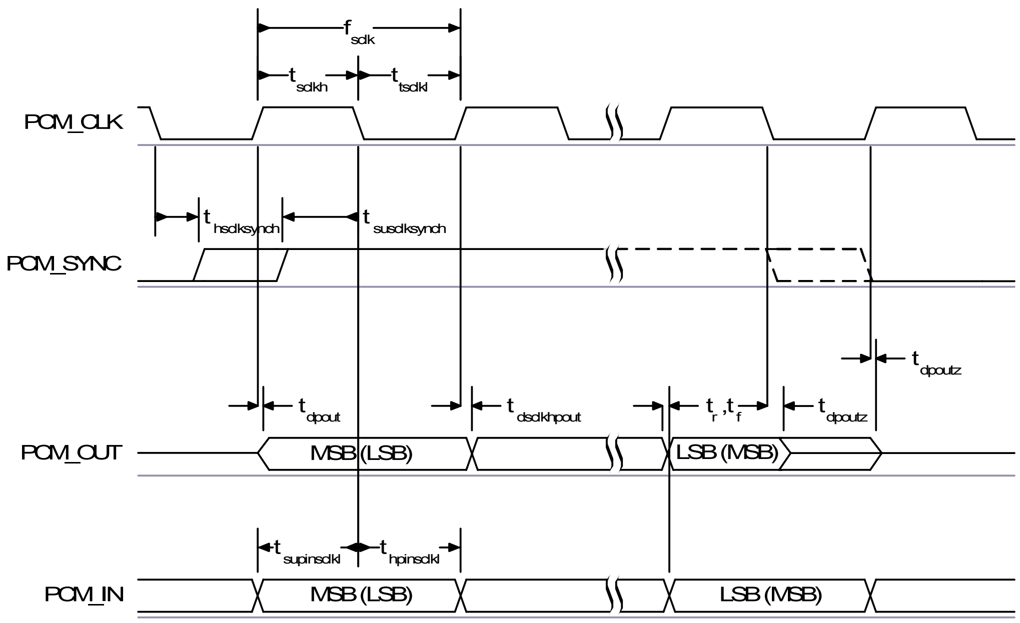


Figure 10.17: PCM Slave Timing Long Frame Sync

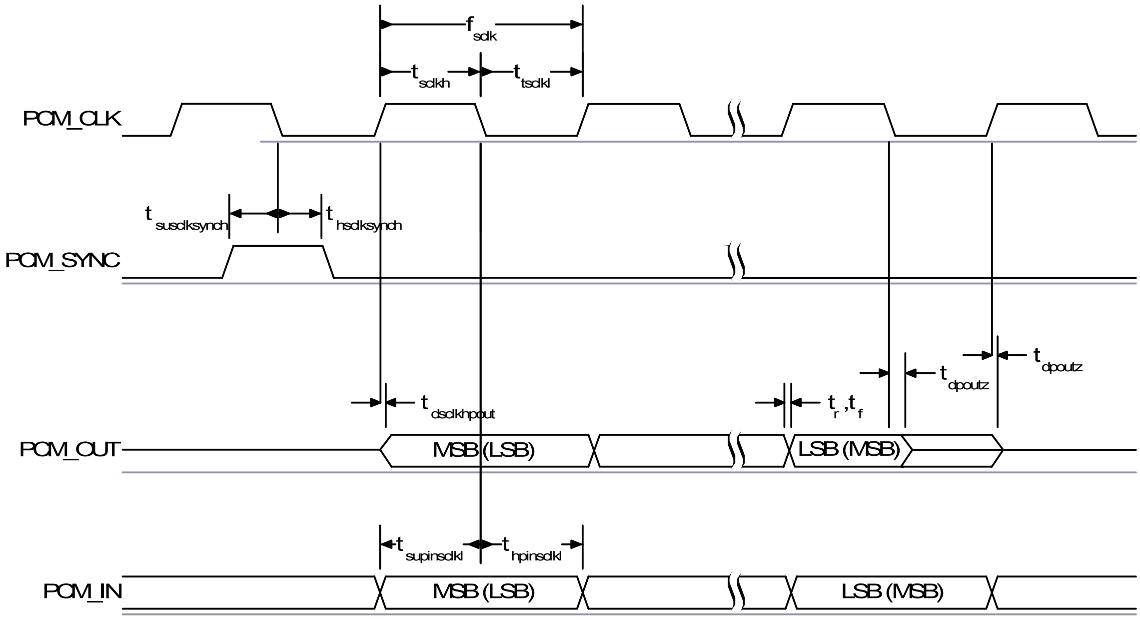


Figure 10.18: PCM Slave Timing Short Frame Sync

10.3.9 PCM_CLK and PCM_SYNC Generation

BlueCore5-Multimedia Flash (16Mb) has 2 methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from BlueCore5-Multimedia Flash (16Mb) internal 4MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512kHz and PCM_SYNC to 8kHz.
- Generating these signals by DDS from an internal 48MHz clock (which allows a greater range of frequencies to be generated with low jitter but consumes more power). To select this second method set bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC can be either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

Equation 10.3 describes PCM_CLK frequency when being generated using the internal 48MHz clock:

$$f = \frac{\mathrm{CNT\_RATE}}{\mathrm{CNT\_LIMIT}} \times 24\mathrm{MHz}$$

Equation 10.3: PCM_CLK Frequency When Being Generated Using the Internal 48MHz Clock

Set the frequency of PCM_SYNC relative to PCM_CLK using Equation 10.4:

$$f = \frac{\mathrm{PCM\_CLK}}{\mathrm{SYNC\_LIMIT} \times 8}$$

Equation 10.4: PCM_SYNC Frequency Relative to PCM_CLK

CNT_RATE, CNT_LIMIT and SYNC_LIMIT are set using PSKEY_PCM_LOW_JITTER_CONFIG. As an example, to generate PCM_CLK at 512kHz with PCM_SYNC at 8kHz, set PSKEY_PCM_LOW_JITTER_CONFIG to 0x08080177.

10.3.10 PCM Configuration

The PCM configuration is set using the PS Keys, PSKEY_PCM_CONFIG32 described in Table 10.10 and PSKEY_PCM_LOW_JITTER_CONFIG in Table 10.9. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256kHz PCM_CLK from 4MHz internal clock with no tristate of PCM_OUT.

Name	Bit Position	Description
CNT_LIMIT	[12:0]	Sets PCM_CLK counter limit
CNT_RATE	[23:16]	Sets PCM_CLK count rate
SYNC_LIMIT	[31:24]	Sets PCM_SYNC division relative to PCM_CLK

Table 10.9: PSKEY_PCM_LOW_JITTER_CONFIG Description

Name	Bit Position	Description
-	0	Set to 0.
SLAVE_MODE_EN	1	0 = master mode with internal generation of PCM_CLK and PCM_SYNC. 1 = slave mode requiring externally generated PCM_CLK and PCM_SYNC.
SHORT_SYNC_EN	2	0 = long frame sync (rising edge indicates start of frame). 1 = short frame sync (falling edge indicates start of frame).
-	3	Set to 0.
SIGN_EXTEND_EN	4	0 = padding of 8 or 13-bit voice sample into a 16-bit slot by inserting extra LSBs. When padding is selected with 13-bit voice sample, the 3 padding bits are the audio gain setting; with 8-bit sample the 8 padding bits are zeroes. 1 = sign-extension.
LSB_FIRST_EN	5	0 = MSB first of transmit and receive voice samples. 1 = LSB first of transmit and receive voice samples.
TX_TRISTATE_EN	6	0 = drive PCM_OUT continuously. 1 = tristate PCM_OUT immediately after falling edge of PCM_CLK in the last bit of an active slot, assuming the next slot is not active.
TX_TRISTATE_RISING_EDGE_EN	7	0 = tristate PCM_OUT immediately after falling edge of PCM_CLK in last bit of an active slot, assuming the next slot is also not active. 1 = tristate PCM_OUT after rising edge of PCM_CLK.
SYNC_SUPPRESS_EN	8	0 = enable PCM_SYNC output when master. 1 = suppress PCM_SYNC while keeping PCM_CLK running. Some codecs use this to enter a low power state.
GCI_MODE_EN	9	1 = enable GCI mode.
MUTE_EN	10	1 = force PCM_OUT to 0.

Name	Bit Position	Description
48M_PCM_CLK_GEN_EN	11	0 = set PCM_CLK and PCM_SYNC generation via DDS from internal 4MHz clock. 1 = set PCM_CLK and PCM_SYNC generation via DDS from internal 48MHz clock.
LONG_LENGTH_SYNC_EN	12	0 = set PCM_SYNC length to 8 PCM_CLK cycles. 1 = set length to 16 PCM_CLK cycles. Only applies for long frame sync and with 48M_PCM_CLK_GEN_EN set to 1.
-	[20:16]	Set to `0b00000`.
MASTER_CLK_RATE	[22:21]	Selects 128 (`0b01`), 256 (`0b00`), 512 (`0b10`) kHz PCM_CLK frequency when master and 48M_PCM_CLK_GEN_EN (bit 11) is low.
ACTIVE_SLOT	[26:23]	Default is 0001. Ignored by firmware.
SAMPLE_FORMAT	[28:27]	Selects between 13 (`0b00`), 16 (`0b01`), 8 (`0b10`) bit sample with 16-cycle slot duration or 8 (`0b11`) bit sample with 8-cycle slot duration.

Table 10.10: PSKEY_PCM_CONFIG32 Description

10.4 Digital Audio Interface (I²S)

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage. Table 10.11 lists these alternative functions. Figure 10.19 shows the timing diagram.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 10.11: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Table 10.12 describes the values for the PS Key PSKEY_DIGITAL_AUDIO_CONFIG that is used to set-up the digital audio interface. For example, to configure an I²S interface with 16-bit SD data set PSKEY_DIGITAL_AUDIO_CONFIG to 0x0406.

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0: left justified 1: right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: ■ 0: is MSB of SD data occurs in the first SCLK period following WS transition ■ 1: is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	0: SD data is left channel when WS is high. 1: SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	0: 17-bit SD data is rounded down to 16bits. 1: the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00f0	CONFIG_AUDIO_ATTEN	Attenuation in 6dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN: ■ 00: 16-bit ■ 01: 20-bit ■ 10: 24-bit ■ 11: reserved This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	0: 17-bit SD_IN data is rounded down to 16bits. 1: only the most significant 16bits of data are received.

Table 10.12: PSKEY_DIGITAL_AUDIO_CONFIG

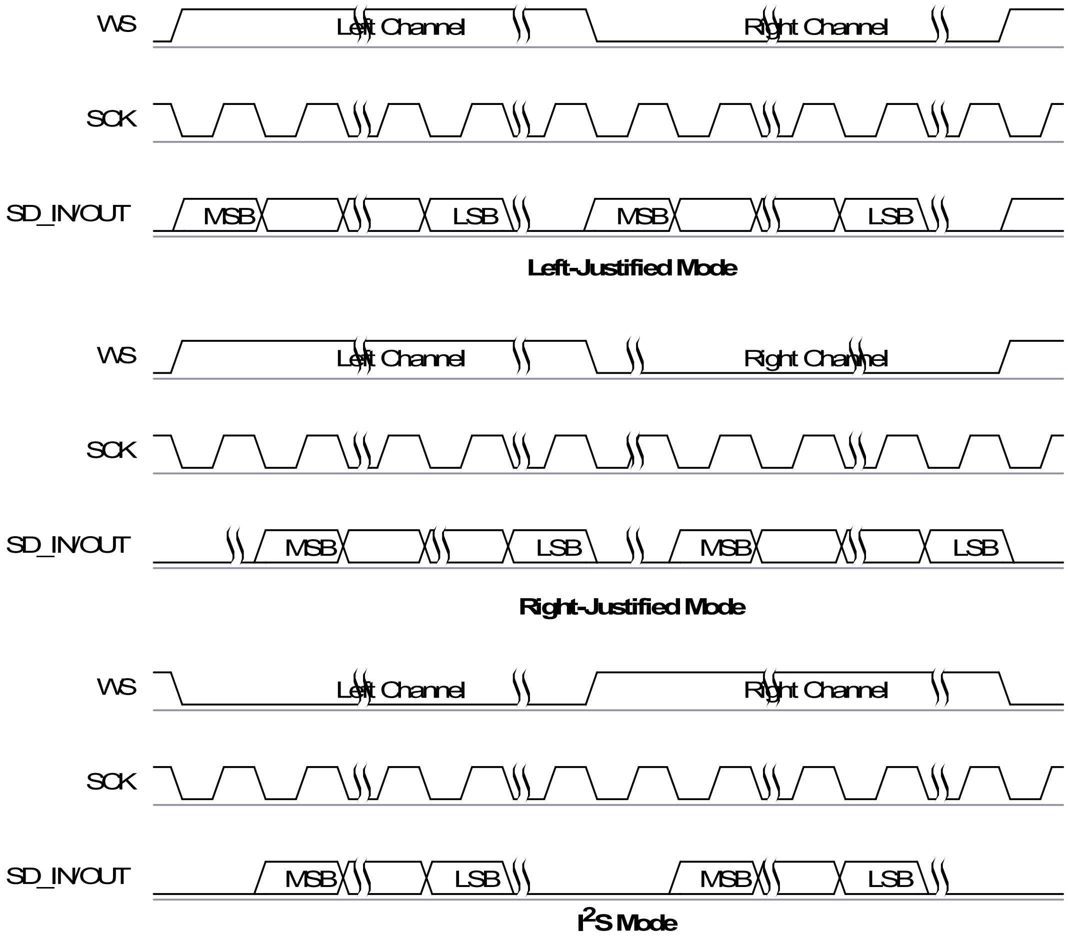


Figure 10.19: Digital Audio Interface Modes

The internal representation of audio samples within BlueCore5-Multimedia Flash (16Mb) is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK set-up time	20	-	-	ns
t_{sh}	WS to SCK hold time	20	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	20	-	-	ns

Table 10.13: Digital Audio Interface Slave Timing

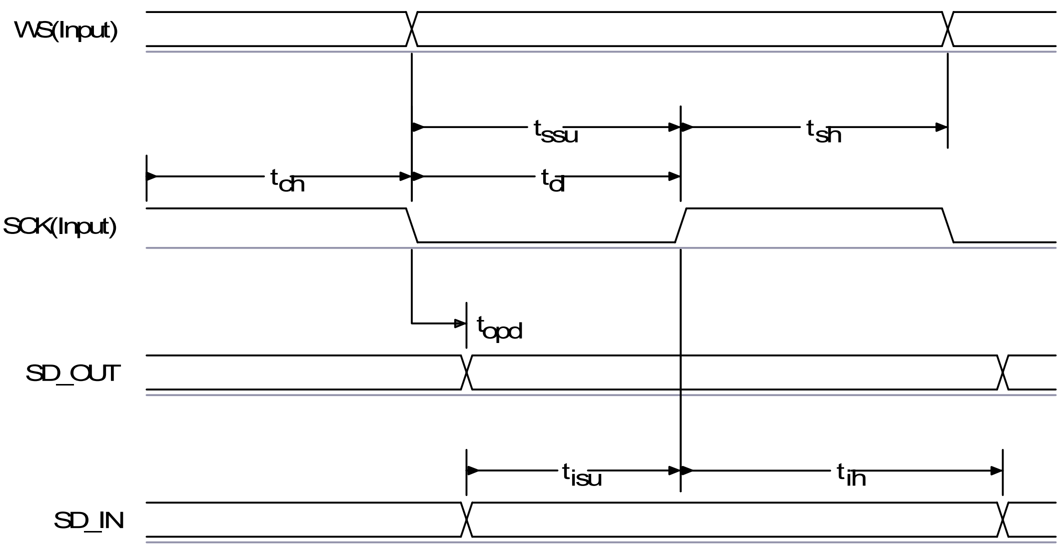


Figure 10.20: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{spd}	SCK to WS delay	-	-	20	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	10	-	-	ns

Table 10.14: Digital Audio Interface Master Timing

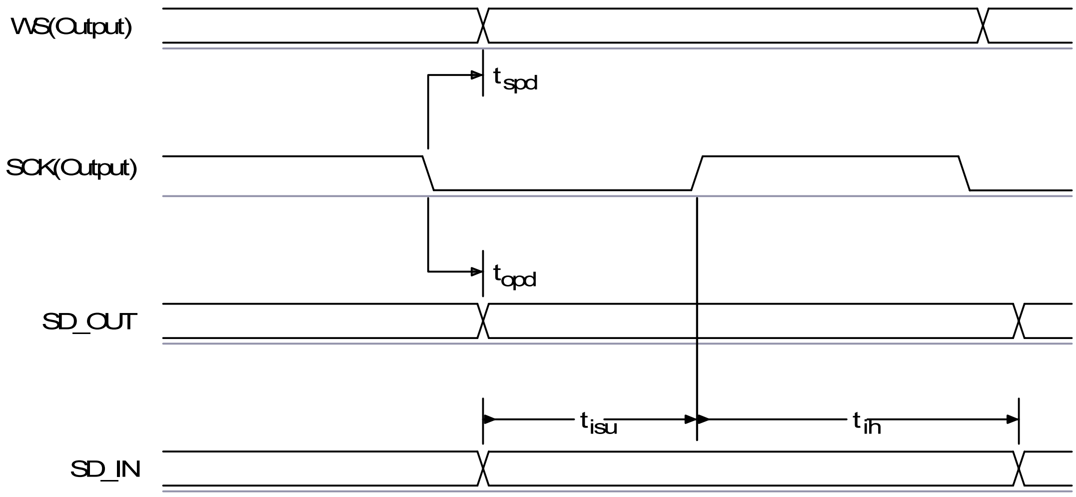


Figure 10.21: Digital Audio Interface Master Timing

11 Power Control and Regulation

BlueCore5-Multimedia Flash (16Mb) contains 4 regulators:

- A switch-mode regulator for generating the 1.8V supply rail.
- 2 low-voltage regulators, running in parallel to supply the 1.5V core supplies from a 1.8V supply rail.

Various configurations for power control and regulation with the BlueCore5-Multimedia Flash (16Mb) are available:

- A high-voltage rail running the switch-mode regulator and the low-voltage regulators in series, as Figure 11.1 shows
- BlueCore5-Multimedia Flash (16Mb) powered directly from an external 1.8V supply rail, by-passing the switch-mode regulator
- An external 1.5V rail omitting all regulators
- A 1.8V linear voltage regulator

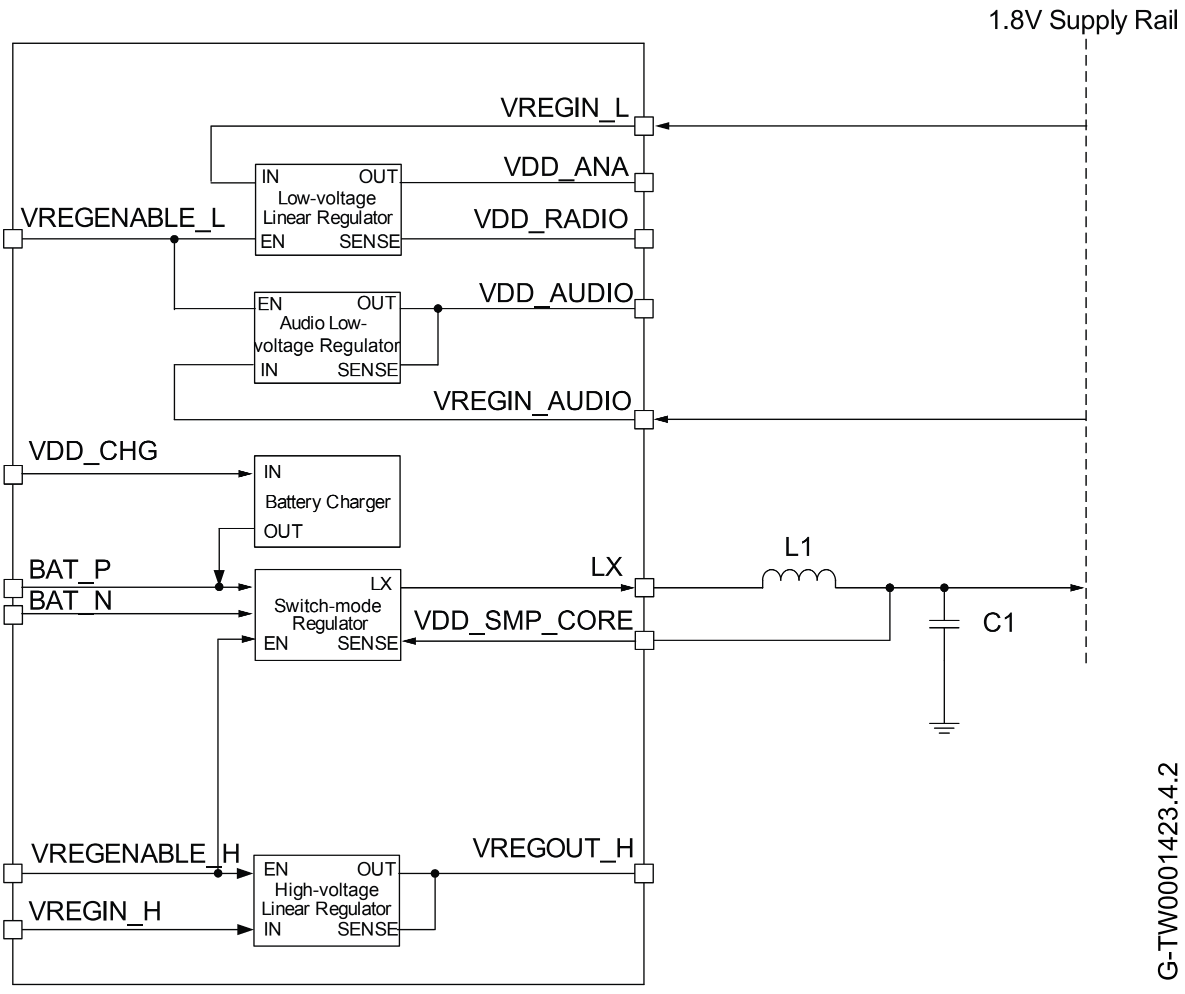


Figure 11.1: Voltage Regulator Configuration

11.1 Power Sequencing

The 1.50V supply rails are VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO. CSR recommends that these supply rails are all powered at the same time.

The digital I/O supply rails are VDD_PADS, VDD_PIO and VDD_USB.

The sequence of powering the 1.50V supply rails relative to the digital I/O supply rails is not important. If the digital I/O supply rails are powered before the 1.50V supply rails, all digital I/Os will have a weak pull-down irrespective of the reset state.

VDD_ANA, VDD_AUDIO, VDD_LO and VDD_RADIO can connect directly to a 1.50V supply.

A simple RC filter is recommended for VDD_CORE to reduce transients fed back onto the power supply rails.

The digital I/O supply rails are connected either together or independently to an appropriate voltage rail. Decoupling of the digital I/O supply rails is recommended.

11.2 External Voltage Source

If any of the supply rails for BlueCore5-Multimedia Flash (16Mb) are supplied from an external voltage source, rather than one of the internal voltage regulators, CSR recommends that VDD_AUDIO, VDD_LO and VDD_RADIO should have less than 10mV rms noise levels between 0 and 10MHz. Also avoid single tone frequencies.

The transient response of any external regulator used should match or be better than the internal regulator available on BlueCore5-Multimedia Flash (16Mb). For more information, refer to regulator characteristics in Section 13. It is essential that the power rail recovers quickly at the start of a packet, where the power consumption jumps to high levels.

11.3 Switch-mode Regulator

CSR recommends the on-chip switch-mode regulator to power the 1.8V supply rail.

An external LC filter circuit of a low-resistance series inductor, L1 (22µH), followed by a low ESR shunt capacitor, C1 (4.7µF), is required between the LX terminal and the 1.8V supply rail. A connection between the 1.8V supply rail and the VDD_SMP_CORE pin is required.

A 2.2µF decoupling capacitor is required between BAT_P and BAT_N.

To maintain high-efficiency power conversion and low supply ripple, it is essential that the series resistance of tracks between the BAT_P and BAT_N terminals, the filter and decoupling components, and the external voltage source are minimised.

The switch-mode regulator is enabled by either:

- VREGENABLE_H pin
- BlueCore5-Multimedia Flash (16Mb) device firmware
- BlueCore5-Multimedia Flash (16Mb) battery charger

The switch-mode regulator switches into a low-power pulse skipping mode when the device is sent into deep sleep mode, or in reset.

When the switch-mode regulator is not required the terminals BAT_P and LX must be grounded or left unconnected.

11.4 High-voltage Linear Regulator

A high-voltage linear regulator with a 1.8V output is available. This regulator should not be used to power external circuitry, prior to using this regulator contact CSR.

A smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground, should be connected to the output of the high-voltage linear regulator, VREGOUT_H. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The high-voltage linear regulator is enabled by either:

- VREGENABLE_H pin
- BlueCore5-Multimedia Flash (16Mb) device firmware
- BlueCore5-Multimedia Flash (16Mb) battery charger

The regulator is switched into a low-power mode when the device is in deep sleep mode, or in reset.

When the high-voltage linear regulator is not used the terminals VREGIN_H and VREGOUT_H must be left unconnected, or tied to ground.

11.5 Low-voltage Linear Regulator

The low-voltage linear regulator is available to power a 1.5V supply rail. Its output is connected internally to VDD_ANA, and can be connected externally to the other 1.5V power inputs.

If the low-voltage linear regulator is used, connect a smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground to the output of the low-voltage linear regulator, VDD_ANA. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The low-voltage linear regulator is enabled by either:

- VREGENABLE_L pin
- BlueCore5-Multimedia Flash (16Mb) device firmware
- BlueCore5-Multimedia Flash (16Mb) battery charger

The low-voltage linear regulator switches into a low power mode when the device is in deep sleep mode, or in reset.

When the low-voltage linear regulator is not used, either leave the terminal VREGIN_L unconnected, or tie it to VDD_ANA.

11.6 Low-voltage Audio Linear Regulator

The low-voltage audio linear regulator is available to power a 1.5V audio supply rail. Its output is connected internally to VDD_AUDIO, and can be connected externally to the other 1.5V audio power inputs.

If the low-voltage audio linear regulator is used, connect a smoothing circuit using a low ESR 2.2µF capacitor and a 2.2Ω resistor to ground to the output of the low-voltage audio linear regulator, VDD_AUDIO. Alternatively use a 2.2µF capacitor with an ESR of at least 2Ω.

The low-voltage audio linear regulator is enabled by either:

- VREGENABLE_L pin
- BlueCore5-Multimedia Flash (16Mb) device firmware

The low-voltage audio linear regulator switches into a low-power mode when no audio cells are enabled, or when the chip is in reset.

When this regulator is not used, either leave the terminal VREGIN_AUDIO unconnected or tie it to VDD_AUDIO.

11.7 Voltage Regulator Enable Pins

The voltage regulator enable pins, VREGENABLE_H and VREGENABLE_L, are used to enable the BlueCore5-Multimedia Flash (16Mb) device if the on-chip regulators are being used. Table 11.1 shows the enable pin responsible for each voltage regulator.

Enable Pin	Regulator
VREGENABLE_H	High-voltage Linear Regulator and Switch-mode Regulator
VREGENABLE_L	Low-voltage Linear Regulator and Low-voltage Audio Linear Regulator

Table 11.1: BlueCore5-Multimedia Flash (16Mb) Voltage Regulator Enable Pins

The voltage regulator enable pins are active high, with weak pull-downs.

BlueCore5-Multimedia Flash (16Mb) boots-up when the voltage regulator enable pins are pulled high, enabling the appropriate regulators. The firmware then latches the regulators on and the voltage regulator enable pins may then be released.

The status of the VREGENABLE_H pin is available to firmware through an internal connection. VREGENABLE_H also works as an input line.

11.8 Battery Charger

The battery charger is a constant current / constant voltage charger circuit, and is suitable for lithium ion/polymer batteries only. It shares a connection to the battery terminal, BAT_P, with the switch-mode regulator. However it may be used in conjunction with either of the high-voltage regulators on the device.

The constant current level can be varied to allow charging of different capacity batteries.

The charger enters various states of operation as it charges a battery, as listed below. A full operational description is in *BlueCore5 Charger Description and Calibration Procedure Application Note*:

- Off : entered when charger disconnected.
- Trickle charge: entered when battery is below 2.9V. The battery is charged at a nominal 4.5mA. This mode is for the safe charge of deeply discharged cells.
- Fast charge constant current: entered when battery is above 2.9V. The charger enters the main fast charge mode. This mode charges the battery at the selected constant current, I_{chgset}.
- Fast charge constant voltage: entered when battery has reached a selected voltage, V_{float}. The charger switches mode to maintain the cell voltage at the V_{float} voltage by adjusting the charge current.
- Standby: this is the state when the battery is fully charged and no charging takes place. The battery voltage is continuously monitored and if it drops by more than 150mV below the V_{float} voltage the charger will re-enter the fast charge constant current mode to keep the battery fully charged.

When a voltage is applied to the charger input terminal VDD_CHG, and the battery is not fully charged, the charger operates and an LED connected to the terminal LED[0] illuminates. By default, until the firmware is running, the LED pulses at a low-duty cycle to minimise current consumption.

The battery charger circuitry auto-detects the presence of a power source, allowing the firmware to detect, using an internal status bit, when the charger is powered. Therefore when the charger supply is not connected to VDD_CHG, the terminal must be left open-circuit. When not connected, the VDD_CHG pin must be allowed to float and not pulled to a power rail. When the battery charger is not enabled this pin may float to a low undefined voltage. Any DC connection increases current consumption of the device. Capacitive components may be connected such as diodes, FETs and ESD protection.

The battery charger is designed to operate with a permanently connected battery. If the application enables the charger input to be connected while the battery is disconnected, then the BAT_P pin voltage may become unstable. This in turn may cause damage to the internal switch-mode regulator. Connecting a 470µF capacitor to BAT_P limits these oscillations which prevents damage.

11.9 LED Drivers

BlueCore5-Multimedia Flash (16Mb) includes 2 pads dedicated to driving LED indicators. Both terminals can be controlled by firmware, while LED[0] can also be set by the battery charger.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current limiting resistor.

CSR recommends that the LED pad, LED[0] or LED[1] pins, operate with a pad voltage below 0.5V. In this case, the pad is like a resistor, R_{ON}. The resistance together with the external series resistor sets the current, I_{LED}, in the LED. The current is also dependent on the external voltage, VDD, as Figure 11.2 shows.

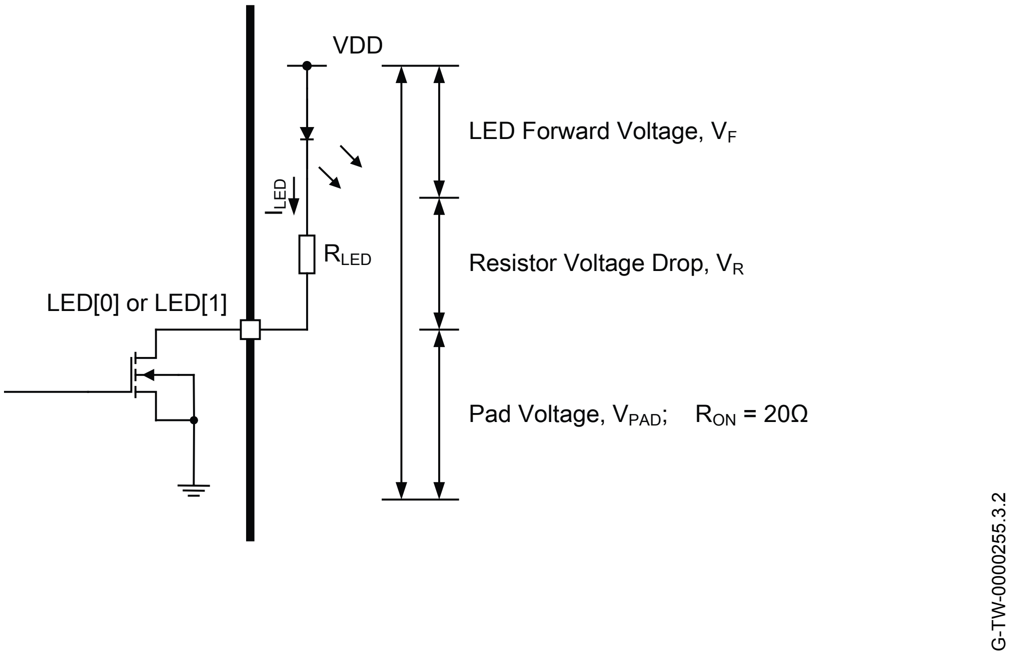


Figure 11.2: LED Equivalent Circuit

From Figure 11.2 it is possible to derive Equation 11.1 to calculate I_{LED}. If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} can be calculated.

$$I_{LED} = \frac{VDD - V_F}{R_{LED} + R_{ON}}$$

Equation 11.1: LED Current

For the LED[0] or LED[1] pad to act as resistance, the external series resistor, R_{LED}, needs to be such that the voltage drop across it, V_R, keeps V_{PAD} below 0.5V. Equation 11.2 also applies.

$$VDD = V_F + V_R + V_{PAD}$$

Equation 11.2: LED PAD Voltage

Note:

The LED current will add to the overall application current, so conservative selection of the LEDs will preserve power consumption.

11.10 Reset, RST#

BlueCore5-Multimedia Flash (16Mb) can be reset from several sources:

- RST# pin
- Power-on reset
- UART break character
- Software configured watchdog timer

The RST# pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5ms and 4.0ms following RST# being active. CSR recommends applying RST# for a period greater than 5ms.

The power-on reset occurs when the VDD_CORE supply falls below typically 1.25V and is released when VDD_CORE rises above typically 1.30V. At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate. Following a reset, BlueCore5-Multimedia Flash (16Mb) assumes the maximum XTAL_IN frequency, which ensures that the internal clocks run at a safe (low) frequency until BlueCore5-Multimedia Flash (16Mb) is configured for the actual XTAL_IN frequency. If no clock is present at XTAL_IN, the oscillator in BlueCore5-Multimedia Flash (16Mb) free runs, again at a safe frequency.

11.10.1 Digital Pin States on Reset

Table 11.2 shows the pin states of BlueCore5-Multimedia Flash (16Mb) on reset. PU and PD default to weak values unless specified otherwise.

Pin Name / Group	I/O Type	No Core Voltage Reset	Full Chip Reset
USB_DP	Digital bidirectional	N/A	N/A
USB_DN	Digital bidirectional	N/A	N/A
UART_RX	Digital input with PD	PD	PD
UART_CTS	Digital input with PD	PD	PD
UART_TX	Digital bidirectional with PU	PU	PU
UART_RTS	Digital bidirectional with PU	PU	PU
SPI_MOSI	Digital input with PD	PD	PD
SPI_CLK	Digital input with PD	PD	PD
SPI_CS#	Digital input with PU	PU	PU
SPI_MISO	Digital tristate output with PD	PD	PD
PCM_IN	Digital input with PD	PD	PD
PCM_CLK	Digital bidirectional with PD	PD	PD
PCM_SYNC	Digital bidirectional with PD	PD	PD
PCM_OUT	Digital tristate output with PD	PD	PD
RST#	Digital input with PU	PU	PU
TEST_EN	Digital input with PD	PD	PD
PIO[15:0]	Digital bidirectional with PU/ PD	PD	PD

Table 11.2: Pin States on Reset

11.10.2 Status after Reset

The status of BlueCore5-Multimedia Flash (16Mb) after a reset is:

- Warm reset: data rate and RAM data remain available
- Cold reset: data rate and RAM data not available

12 Example Application Schematic

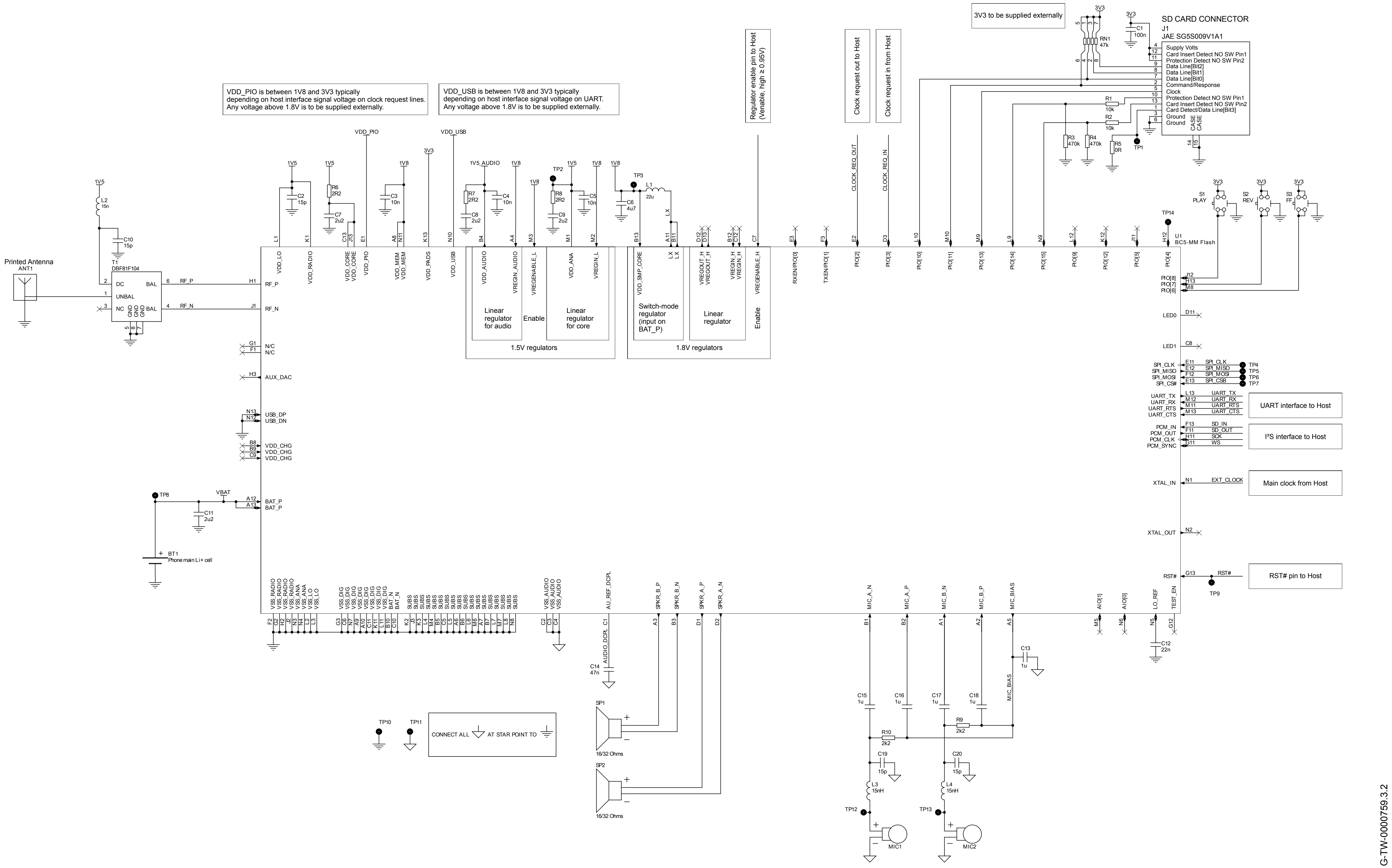


Figure 12.1: Example Application Schematic

13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage Temperature		-40	105	°C
Core Supply Voltage	VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO	-0.4	1.65	V
I/O Voltage	VDD_PADS, VDD_PIO and VDD_USB	-0.4	3.6	V
	VDD_MEM	-0.4	1.95	V
Supply Voltage	VREGIN_L	-0.4	2.7	V
	VREGIN_AUDIO	-0.4	2.7	V
	VREGIN_H, VREGENABLE_H and VREGENABLE_L	-0.4	4.9	V
	BAT_P	-0.4	4.4	V
	LED[1:0]	-0.4	4.4	V
	VDD_CHG	-0.4	6.5	V
Other Terminal Voltages		VSS - 0.4	VDD + 0.4	V

13.2 Recommended Operating Conditions

Operating Condition		Min	Typ	Max	Unit
Operating Temperature Range[(a)]		-40	20	85	°C
Core Supply Voltage	VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO	1.42	1.50	1.57	V
I/O Supply Voltage	VDD_PADS, VDD_PIO and VDD_USB	1.70	3.30	3.60	V
	VDD_MEM	1.70	1.80	1.95	V

[(a)] For radio performance over temperature, see *BlueCore5-Multimedia Flash (16Mb) Performance Specification.*

BlueCore5-Multimedia Flash (16Mb) Data Sheet

13.3 Input/Output Terminal Characteristics

Note:

For all I/O terminal characteristics:

- VDD_ANA, VDD_AUDIO, VDD_CORE, VDD_LO and VDD_RADIO at 1.50V unless shown otherwise.
- VDD_PADS, VDD_PIO and VDD_USB at 3.30V unless shown otherwise.
- Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

13.3.1 High-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	2.7	-	5.5[(a)]	V
Output voltage (I_{load} = 100mA / VREGIN_H = 3.0V)	1.70	1.80	1.95	V
Temperature coefficient	-300	0	300	ppm/°C
Output noise[(b)] [(c)]	-	-	1	mV rms
Load regulation (100µA < I_{load} < 200mA), ΔV_{out}	-	-	5	mV
Settling time[(b)] [(d)]	-	-	50	µs
Output current	-	-	200	mA
Minimum load current	5	-	-	µA
Drop-out voltage (I_{load} = 200mA)	-	-	900	mV
Quiescent current (excluding load, I_{load} < 1mA)	30	50	60	µA
Low-power Mode [(e)]				
Quiescent current (excluding load, I_{load} < 100µA)	11	15	21	µA

(a) Short-term operation up to 5.5V is permissible without damage and without the output voltage rising sufficiently to damage the rest of the device, but output regulation and other specifications are no longer guaranteed at input voltages in excess of 4.9V. 5.5V can only be tolerated for short periods.

(b) Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors.

(c) Frequency range 100Hz to 100kHz.

(d) 10mA to 200mA pulsed load.

(e) The regulator is in low power mode when the chip is in deep sleep mode, or in reset.

13.3.2 Low-voltage Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage (I_{load} = 70mA / VREGIN_L = 1.7V)	1.42	1.50	1.57	V
Temperature coefficient	-300	0	300	ppm/°C
Output noise[a] [b]	-	-	1	mV rms
Load regulation (100µA < I_{load} < 90mA), ΔV_{out}	-	-	5	mV
Load regulation (100µA < I_{load} < 115mA), ΔV_{out}	-	-	25	mV
Settling time[a] [c]	-	-	50	µs
Output current	-	-	115	mA
Minimum load current	5	-	100	µA
Quiescent current (excluding load, I_{load} < 1mA)	50	90	150	µA
Low-power Mode [d]				
Quiescent current (excluding load, I_{load} < 100µA)	5	8	15	µA

[a] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[b] Frequency range 100Hz to 100kHz

[c] 1mA to 115mA pulsed load

[d] The regulator is in low power mode when the chip is in deep sleep mode, or in reset

13.3.3 Low-voltage Linear Audio Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage (I_{load} = 70mA / VREGIN_AUDIO = 1.7V)	1.42	1.50	1.57	V
Temperature coefficient	-300	0	300	ppm/°C
Output noise[(a)] [(b)]	-	-	1	mV rms
Load regulation (100µA < I_{load} < 70mA), ΔV_{out}	-	-	5	mV
Settling time[(a)] [(c)]	-	-	50	µs
Output current	-	-	70	mA
Minimum load current	5	-	100	µA
Quiescent current (excluding load, I_{load} < 1mA)	25	30	50	µA
Low-power Mode [(d)]				
Quiescent current (excluding load, I_{load} < 100µA)	5	8	15	µA

[(a)] Regulator output connected to 47nF pure and 4.7µF 2.2Ω ESR capacitors

[(b)] Frequency range 100Hz to 100kHz

[(c)] 1mA to 70mA pulsed load

[(d)] The regulator is in low power mode when the chip is in deep sleep mode, or in reset

13.3.4 Reset

Power-on Reset	Min	Typ	Max	Unit
VDD_CORE falling threshold	1.13	1.25	1.30	V
VDD_CORE rising threshold	1.20	1.30	1.35	V
Hysteresis	0.05	0.10	0.15	V

13.3.5 Regulator Enable

Switching Threshold	Min	Typ	Max	Unit
VREGENABLE_H				
Rising threshold	0.50	-	0.95	V
Falling threshold	0.35	-	0.80	V
Hysteresis	0.14	-	0.28	V
VREGENABLE_L				
Rising threshold	0.50	-	0.95	V
Falling threshold	0.35	-	0.80	V
Hysteresis	0.14	-	0.28	V

13.3.6 Switch-mode Regulator

Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.5	-	4.4	V
Output voltage (I_{load} = 70mA)	1.70	1.80	1.90	V
Temperature coefficient	-250	-	250	ppm/°C
Normal Operation				
Output ripple	-	-	10	mV rms
Transient settling time[a]	-	-	50	µs
Maximum load current	200	-	-	mA
Conversion efficiency (I_{load} = 70mA)	-	90	-	%
Switching frequency[b]	-	1.333	-	MHz
Start-up current limit[c]	30	50	80	mA
Low-power Mode [d]				
Output ripple	-	-	1	mV rms
Transient settling time[e]	-	-	700	µs
Maximum load current	5	-	-	mA
Minimum load current	1	-	-	µA
Conversion efficiency (I_{load} = 1mA)	-	80	-	%
Switching frequency[f]	50	-	150	kHz

[a] For step changes in load of 30 to 80mA and 80 to 30mA

[b] Locked to crystal frequency

[c] Current is limited on start-up to prevent excessive stored energy in the filter inductor

[d] The regulator is in low power mode when the chip is in deep sleep mode, or in reset

[e] 100µA to 1mA pulsed load

[f] Defines minimum period between pulses. Pulses are skipped at low current loads

Note:

The external inductor used with the switch-mode regulator must have an ESR in the range 0.3Ω to 0.7Ω:

- Low ESR < 0.3Ω causes instability.
- High ESR > 0.7Ω derates the maximum current.

13.3.7 Battery Charger

Battery Charger		Min	Typ	Max	Unit
Input voltage		4.5	-	6.5	V

Charging Mode (BAT_P rising to 4.2V)		Min	Typ	Max	Unit
Supply current[a]		-	4.5	6	mA
Battery trickle charge current[b]		-	4	-	mA
Maximum battery fast charge current (I-CTRL = 15)[c] [d]	Headroom[e] > 0.7V	-	140	-	mA
	Headroom = 0.3V	-	120	-	mA
Minimum battery fast charge current (I-CTRL = 0)[c] [d]	Headroom > 0.7V	-	40	-	mA
	Headroom = 0.3V	-	35	-	mA
Fast charge step size (I-CTRL = 0 to 15)	Spread ±17%	-	6.3	-	mA
Trickle charge voltage threshold		-	2.9	-	V
Float voltage (with correct trim value set), V_{FLOAT} [f]		4.17	4.2	4.23	V
Float voltage trim step size[f]		-	50	-	mV
Battery charge termination current, % of fast charge current		5	10	20	%

[a] Current into VDD_CHG does not include current delivered to battery (I_{VDD_CHG} - I_{BAT_P})

[b] BAT_P < trickle charge voltage threshold

[c] Charge current can be set in 16 equally spaced steps

[d] Trickle charge threshold < BAT_P < Float voltage

[e] Where headroom = VDD_CHG - BAT_P

[f] Float voltage can be adjusted in 15 steps. Trim setting is determined in production test and must be loaded into the battery charger by firmware during boot-up sequence

Standby Mode (BAT_P falling from 4.2V)	Min	Typ	Max	Unit
Supply current[a]	-	1.5	2	mA
Battery current	-	-5	-	µA
Battery recharge hysteresis[b]	100	-	200	mV

[a] Current into VDD_CHG; does not include current delivered to battery (I_{VDD_CHG} - I_{BAT_P})

[b] Hysteresis of (V_{FLOAT} - BAT_P) for charging to restart

Shutdown Mode (VDD_CHG too low or disabled by firmware)		Min	Typ	Max	Unit
Supply current		-	1.5	2	mA
Battery current		-1	-	0	μA
VDD_CHG under-voltage threshold	VDD_CHG rising	-	3.90	-	V
	VDD_CHG falling	-	3.70	-	V
VDD_CHG - BAT_P lockout threshold	VDD_CHG rising	-	0.22	-	V
	VDD_CHG falling	-	0.17	-	V

13.3.8 Digital Terminals

Supply Voltage Levels		Min	Typ	Max	Unit
VDD_{PRE}	Pre-driver supply voltage	1.4	1.5	1.6	V
VDD I/O supply voltage (post-driver)	Full spec.	3.0	3.3	3.6	V
	Reduced spec.	1.7	-	3.0	V

Input Voltage Levels	Min	Typ	Max	Unit
V_{IL} input logic level low	-0.3	-	0.25 x VDD	V
V_{IH} input logic level high	0.625 x VDD	-	VDD + 0.3	V
$V_{SCHMITT}$ Schmitt voltage	0.25 x VDD	-	0.625 x VDD	V

Output Voltage Levels	Min	Typ	Max	Unit
V_{OL} output logic level low, I_{OL} = 4.0mA	0	-	0.125	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 x VDD	-	VDD	V

Input and Tristate Currents	Min	Typ	Max	Unit
I_i input leakage current at V_{in} = VDD or 0V	-100	0	100	nA
I_{oz} tristate output leakage current at V_o = VDD or 0V	-100	0	100	nA
With strong pull-up	-100	-40	-10	μA
With strong pull-down	10	40	100	μA
With weak pull-up	-5	-1.0	-0.2	μA
With weak pull-down	-0.2	1.0	5.0	μA
C_I input capacitance	1.0	-	5.0	pF

Resistive Strength	Min	Typ	Max	Unit
R_{puw} weak pull-up strength at VDD - 0.2V	0.5	-	2	MΩ
R_{pdw} weak pull-down strength at 0.2V	0.5	-	2	MΩ
R_{pus} strong pull-up strength at VDD - 0.2V	10	-	50	kΩ
R_{pds} strong pull-down strength at 0.2V	10	-	50	kΩ

13.3.9 LED Driver Pads

LED Driver Pads		Min	Typ	Max	Unit
Off current		-	1	2	µA
On resistance	V_{PAD} < 0.5V	-	20	33	Ω
On resistance, pad enabled by battery charger	V_{PAD} < 0.5V	-	20	50	Ω

13.3.10 USB

	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1	-	3.6	V
Input Threshold				
V_{IL} input logic level low	-	-	0.3 x VDD_USB	V
V_{IH} input logic level high	0.7 x VDD_USB	-	-	V
Input Leakage Current				
VSS_DIG < V_{IN} < VDD_USB[a]	-1	1	5	µA
C_I input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

[a] Internal USB pull-up disabled

13.3.11 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range[a]		0	-	VDD_ANA	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		-	2.5	-	µs
Sample rate[b]		-	-	700	Samples/ s

[a] LSB size = VDD_ANA/1023

[b] The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

13.3.12 Auxiliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	8	Bits
Average output step size[a]	12.5	14.5	17.0	mV
Output Voltage		monotonic[a]		
Voltage range (I_O = 0mA)	VSS_DIG	-	VDD_PIO	V
Current range	-10.0	-	0.1	mA
Minimum output voltage (I_O=100µA)	0.0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO - 0.3	-	VDD_PIO	V
High impedance leakage current	-1	-	1	µA
Offset	-220	-	120	mV
Integral non-linearity[a]	-2	-	2	LSB
Settling time (50pF load)	-	-	10	µs

[a] Specified for an output voltage between 0.2V and VDD_PIO - 0.2V. Output is high impedance when chip is in deep sleep mode.

13.3.13 Clocks

Crystal Oscillator	Min	Typ	Max	Unit
Crystal frequency[a]	16	26	26	MHz
Digital trim range[b]	5.0	6.2	8.0	pF
Trim step size[b]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance[c]	870	1500	2400	Ω
External Clock	**Min**	**Typ**	**Max**	**Unit**
Input frequency[d]	12	26	52	MHz
Clock input level[e]	0.4	-	VDD_ANA	V pk-pk
Edge jitter (allowable jitter), at zero crossing	-	-	15	ps rms
XTAL_IN input impedance	-	≥10	-	kΩ
XTAL_IN input capacitance	-	≤4	-	pF

[a] Integer multiple of 250kHz

[b] Difference between the internal capacitance at minimum and maximum settings of the internal digital trim

[c] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF.

[d] Clock input can be any frequency from 12MHz to 52MHz in steps of 250kHz plus CDMA/3G TCXO frequencies of 14.40, 15.36, 16.2, 16.8, 19.2, 19.44, 19.68, 19.8 and 38.4MHz.

[e] Clock input can be either sinusoidal or square wave. If the peaks of the signal are below VSS_ANA or above VDD_ANA. A DC blocking capacitor is required between the signal and XTAL_IN.

13.3.14 Stereo Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	Conditions		Min	Typ	Max	Unit
Resolution	-		-	-	16	Bits
Input Sample Rate, F_{sample}	-		8	-	44.1	kHz
Signal to Noise Ratio, SNR[(a)]	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 1% $150mV_{pk\text{-}pk}$ input	F_{sample}				
		8kHz	-	79	-	dB
		11.025kHz	-	77	-	dB
		16kHz	-	76	-	dB
		22.050kHz	-	76	-	dB
		32kHz	-	75	-	dB
		44.1kHz	-	75	-	dB
Digital Gain	Digital Gain Resolution = 1/32dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		-	-	42	dB
Input full scale at maximum gain (differential)			-	4	-	mV rms
Input full scale at minimum gain (differential)			-	800	-	mV rms
3dB Bandwidth			-	20	-	kHz
Microphone mode input impedance			-	6.0	-	kΩ
THD+N (microphone input) @ 30mV rms input			-	0.04	-	%

(a) Improved SNR performance can be achieved at the expense of current consumption. See Optimising BlueCore5-Multimedia ADC Performance Application Note for details.

13.3.15 Stereo Codec: Digital to Analogue Converter

Digital to Analogue Converter						
Parameter	Conditions		Min	Typ	Max	Unit
Resolution	-		-	-	16	Bits
Output Sample Rate, F_{sample}	-		8	-	48	kHz
Signal to Noise Ratio, SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 0.01% 0dBFS signal Load = 100kΩ	F_{sample}				
		8kHz	-	95	-	dB
		11.025kHz	-	95	-	dB
		16kHz	-	95	-	dB
		22.050kHz	-	95	-	dB
		32kHz	-	95	-	dB
		44.1kHz	-	95	-	dB
		48kHz	-	95	-	dB
Digital Gain	Digital Gain Resolution = 1/32dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		0	-	-21	dB
Output voltage full-scale swing (differential)[(a)]			-	750	-	mV rms
Allowed Load		Resistive	16(8)	-	O.C.	Ω
		Capacitive	-	-	500	pF
THD+N 100kΩ load			-	-	0.01	%
THD+N 16Ω load			-	-	0.1	%
SNR (Load = 16Ω, 0dBFS input relative to digital silence)			-	95	-	dB

[(a)] Any combination of gain (digital and / or analogue) and input signal which results in the output signal level exceeding the minimum or maximum signal level (analogue or digital) could result in distortion.

13.4 ESD Precautions

BlueCore5-Multimedia Flash (16Mb) is classified as a:

- JESD22-A114 class 1A (I/O) and class 2 (RF, Supplies, Audio I/O and USB I/O) product:
  - USB I/O includes the USB_DP and USB_DN pins.
  - Audio I/O includes the MIC_B_P, MIC_B_N, MIC_A_P, MIC_A_N, SPKR_B_N, SPKR_B_P, AU_REF_DCPL, SPKR_A_N and SPKR_A_P pins.
- JESD22-A115 class A product

Important Note:

Apply ESD static handling precautions during manufacturing.

14 Power Consumption

Role	Connection	Audio Packet Type	Description	Current				Unit
				VREGIN_L = 1.8V		VDD_CHG = 3.6V		
				16MHz	32MHz	16MHz	32MHz	
	Stand-by	-	Host connection	0.07	0.08	0.06	0.07	mA
	Page Scan	-	Interval = 1280ms	0.46	0.47	0.31	0.32	mA
	Inquiry and Page Scan	-	Inquiry scan = 1280ms Page scan = 1280ms	0.92	0.88	0.51	0.54	mA
Master	ACL	-	No traffic	4.2	4.2	2.6	2.7	mA
Master	ACL	-	File transfer TX	8.9	9.1	5.1	5.2	mA
Master	ACL	-	Sniff = 40ms	1.8	1.8	1.1	1.1	mA
Master	ACL	-	Sniff = 1280ms	0.21	0.20	0.15	0.14	mA
Master	eSCO	EV3	-	21	22	12	12	mA
Master	eSCO	EV3	Setting S1	23	23	13	13	mA
Master	eSCO	2 EV3	Setting S2	22	22	12	12	mA
Master	eSCO	2 EV3	Setting S3	16	17	9.0	9.1	mA
Master	eSCO	EV5	-	16	16	8.8	8.9	mA
Master	SCO	HV1	-	39	41	22	23	mA
Master	SCO	HV3	-	21	22	12	12	mA

Role	Connection	Audio Packet Type	Description	Current				Unit
				VREGIN_L = 1.8V		VDD_CHG = 3.6V		
				16MHz	32MHz	16MHz	32MHz	
Master	SCO	HV3	Sniff = 30ms	21	22	12	12	mA
Slave	ACL	-	No Traffic	15	15	8.2	8.2	mA
Slave	ACL	-	File transfer RX	20	18	10	9.44	mA
Slave	ACL	-	Sniff = 40ms	1.5	1.6	0.96	1.0	mA
Slave	ACL	-	Sniff = 1280ms	0.27	0.27	0.18	0.18	mA
Slave	eSCO	EV3	-	25	25	13	14	mA
Slave	eSCO	EV3	Setting S1	27	28	14	15	mA
Slave	eSCO	2 EV3	Setting S2	26	26	14	15	mA
Slave	eSCO	2 EV3	Setting S3	23	24	13	13	mA
Slave	eSCO	EV5	-	21	22	12	12	mA
Slave	SCO	HV1	-	39	41	22	23	mA
Slave	SCO	HV3	-	27	28	14	15	mA
Slave	SCO	HV3	Sniff = 30ms	21	21	11	12	mA

14.1 Kalimba DSP and Codec Typical Average Current Consumption

DSP		Average	Unit
DSP core (including PM memory access)	Minimum (NOP)	0.11	mA/MIPS
	Maximum (MAC)	0.32	mA/MIPS
DSP memory access (DM1 or DM2)		0.08	mA/MIPS

14.2 Typical Peak Current at 20°C

Device Activity / State	Typ	Unit
Peak current during cold boot	45	mA
Master TX peak current	45	mA
Master RX peak current	45	mA
Slave TX peak current	45	mA
Slave RX peak current	45	mA

14.3 Conditions

- Power consumption measurements based on BlueCore5-Multimedia Flash (8Mb).
- Host interface = UART
- Baud rate = 115200
- Supply = 1.8V in to VREGIN_L and VREGIN_AUDIO
- AFH switched OFF
- No audio load
- RF Output power = 0dBm
- VM OFF
- eSCO settings:
  - EV3 and EV5 = no retry
  - Setting S1 = optimised for power consumption
- Firmware build ID = 4508

15 CSR Green Semiconductor Products and RoHS Compliance

15.1 RoHS Statement

BlueCore5-Multimedia Flash (16Mb) where explicitly stated in this Data Sheet meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the *Restriction of Hazardous Substance* (RoHS).

15.1.1 List of Restricted Materials

BlueCore5-Multimedia Flash (16Mb) is compliant with RoHS in relation to the following substances:

- Cadmium
- Lead
- Mercury
- Hexavalent chromium
- Polybrominated Biphenyl
- Polybrominated Diphenyl Ether

In addition, the following substances are not intentionally added to BlueCore5-Multimedia Flash (16Mb) devices:

- Halogenated flame retardant
- Antimony (Sb) and Compounds, including Antimony Trioxide flame retardant
- Polybrominated Diphenyl and Biphenyl Oxides
- Tetrabromobisphenol-A bis (2,3-dibromopropylether)
- Asbestos or Asbestos compounds
- Azo compounds
- Organic tin compounds
- Mirex
- Polychlorinated napthelenes
- Polychlorinated terphenyls
- Polychlorinated biphenyls
- Polychlorinated/Short chain chlorinated paraffins
- Polyvinyl Chloride (PVC) and PVC blends
- Formaldehyde
- Arsenic and compounds (except as a semiconductor dopant)
- Beryllium and its compounds
- Ethylene Glycol Monomethyl Ether or its acetate
- Ethylene Glycol Monoethyl Ether or its acetate
- Halogenated dioxins and furans
- Persistent Organic Pollutants (POP), including Perfluorooctane sulphonates
- Red phosphorous
- Ozone Depleting Chemicals (Class I and II): Chlorofluorocarbons (CFC) and Halons
- Radioactive substances

For further information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products.*

16 CSR Synergy and Bluetooth Software Stack

BlueCore5-Multimedia Flash (16Mb) is supplied with Bluetooth v2.1 + EDR specification compliant stack firmware, which runs on the internal RISC MCU. The stack firmware is compatible with CSR's **Synergy**™ wireless Host Software Platform, for more information see http://www.csr.com/synergy.

The BlueCore5-Multimedia Flash (16Mb) software architecture allows Bluetooth processing and the application program to be shared in different ways between the internal RISC MCU and an external host processor. The upper layers of the Bluetooth stack, above the HCI, can be run either on-chip or on the host processor.

16.1 BlueCore HCI Stack

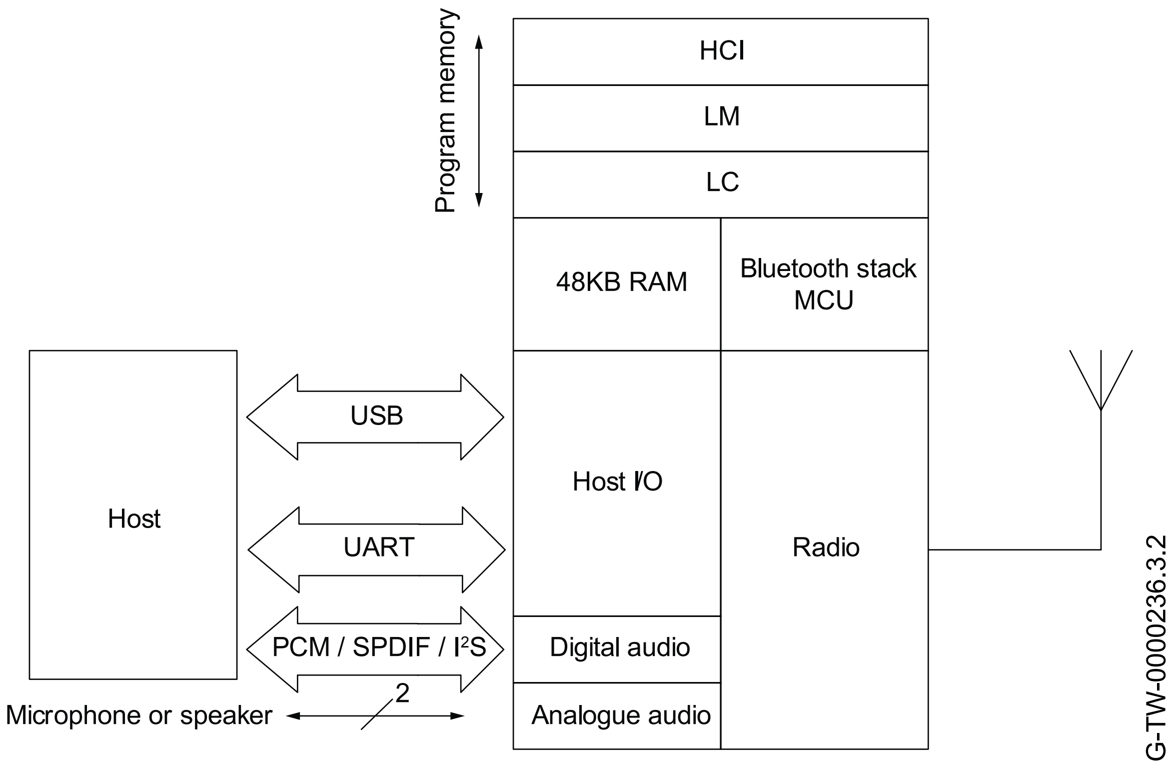


Figure 16.1: BlueCore HCI Stack

Note:

Program Memory in Figure 16.1 is internal flash.

In the implementation shown in Figure 16.1 the internal MCU runs the Bluetooth stack up to the HCI. The Host processor must provide all upper layers including the application.

16.1.1 Key Features of the HCI Stack: Standard Bluetooth Functionality

CSR supports the following Bluetooth v2.1 + EDR specification functionality:

- Secure simple pairing
- Sniff subrating
- Encryption pause resume
- Packet boundary flags
- Encryption
- Extended inquiry response

As well as the following mandatory functions of Bluetooth v2.0 + EDR specification:

- AFH, including classifier
- Faster connection: enhanced inquiry scan (immediate FHS response)
- LMP improvements
- Parameter ranges

And optional Bluetooth v2.0 + EDR specification functionality:

- AFH as master and automatic channel classification
- Fast connect: interlaced inquiry and page scan plus RSSI during inquiry
- eSCO, eV3 + CRC, eV4, eV5
- SCO handle
- Synchronisation

The firmware was written against the Bluetooth v2.1 + EDR specification:

- Bluetooth components:
  - Baseband including LC
  - LM
  - HCI
- Standard UART HCI Transport Layers
- All standard Bluetooth radio packet types
- Full Bluetooth data rate, enhanced data rates of 2 and 3Mbps
- Operation with up to 7 active slaves (this is the maximum Bluetooth v2.1 + EDR specification allows)
- Scatternet v2.5 operation
- Maximum number of simultaneous active ACL connections: 7
- Maximum number of simultaneous active SCO connections: 3 (BlueCore5-Multimedia Flash (16Mb) supports all combinations of active ACL and SCO channels for both master and slave operation, as specified by the Bluetooth v2.1 + EDR specification)
- Operation with up to 3 SCO links, routed to one or more slaves
- All standard SCO voice coding, plus transparent SCO
- Standard operating modes: Page, Inquiry, Page-Scan and Inquiry-Scan
- All standard pairing, authentication, link key and encryption operations
- Standard Bluetooth power saving mechanisms: Hold, Sniff and Park modes, including Forced Hold
- Dynamic control of peers' transmit power via LMP
- Master/slave switch
- Broadcast
- Channel quality driven data rate
- All standard Bluetooth test modes

16.1.2 Key Features of the HCI Stack: Extra Functionality

The firmware extends the standard Bluetooth functionality with the following features:

- Supports BCSP, a proprietary, reliable alternative to the standard Bluetooth UART Host Transport
- Supports H4DS, a proprietary alternative to the standard Bluetooth UART Host Transport, supporting deep sleep for low-power applications
- Provides a set of approximately 50 manufacturer-specific HCI extension commands. This command set, called BCCMD, provides:
  - Access to BlueCore5-Multimedia Flash (16Mb) general-purpose PIO port
  - The negotiated effective encryption key length on established Bluetooth links
  - Access to the firmware random number generator
  - Controls to set the default and maximum transmit powers; these can help minimise interference between overlapping, fixed-location piconets
  - Dynamic UART configuration
  - Bluetooth radio transmitter enable/disable. A simple command connects to a dedicated hardware switch that determines whether the radio can transmit.
- The firmware can read the voltage on a pair of BlueCore5-Multimedia Flash (16Mb) external pins. This is normally used to build a battery monitor.
- A block of BCCMD commands provides access to the BlueCore5-Multimedia Flash (16Mb) persistent store configuration database. The database sets the BlueCore5-Multimedia Flash (16Mb) Bluetooth address, Class of Device, Bluetooth radio (transmit class) configuration, SCO routing, LM, etc.
- A UART break condition can be used in three ways:
  - Presenting a UART break condition to the chip can force the chip to perform a hardware reboot
  - Presenting a break condition at boot time can hold the IC in a low power state, preventing normal initialisation while the condition exists
  - With BCSP, the firmware can be configured to send a break to the host before sending data. (This is normally used to wake the host from a deep sleep state.)
- A block of Bluetooth radio test or BIST commands allows direct control of the BlueCore5-Multimedia Flash (16Mb) radio. This aids the development of modules' radio designs, and can be used to support Bluetooth qualification.
- Hardware low power modes: shallow sleep and deep sleep. The chip drops into modes that significantly reduce power consumption when the software goes idle.
- SCO channels are normally routed via HCI (over BCSP). However, up to three SCO channels can be routed over the PCM interface (at the same time as routing any remaining SCO channels over HCI).

Note:

Always refer to the Firmware Release Note for the specific functionality of a particular build.

16.2 Stand-alone BlueCore5-Multimedia Flash (16Mb) and Kalimba DSP Applications

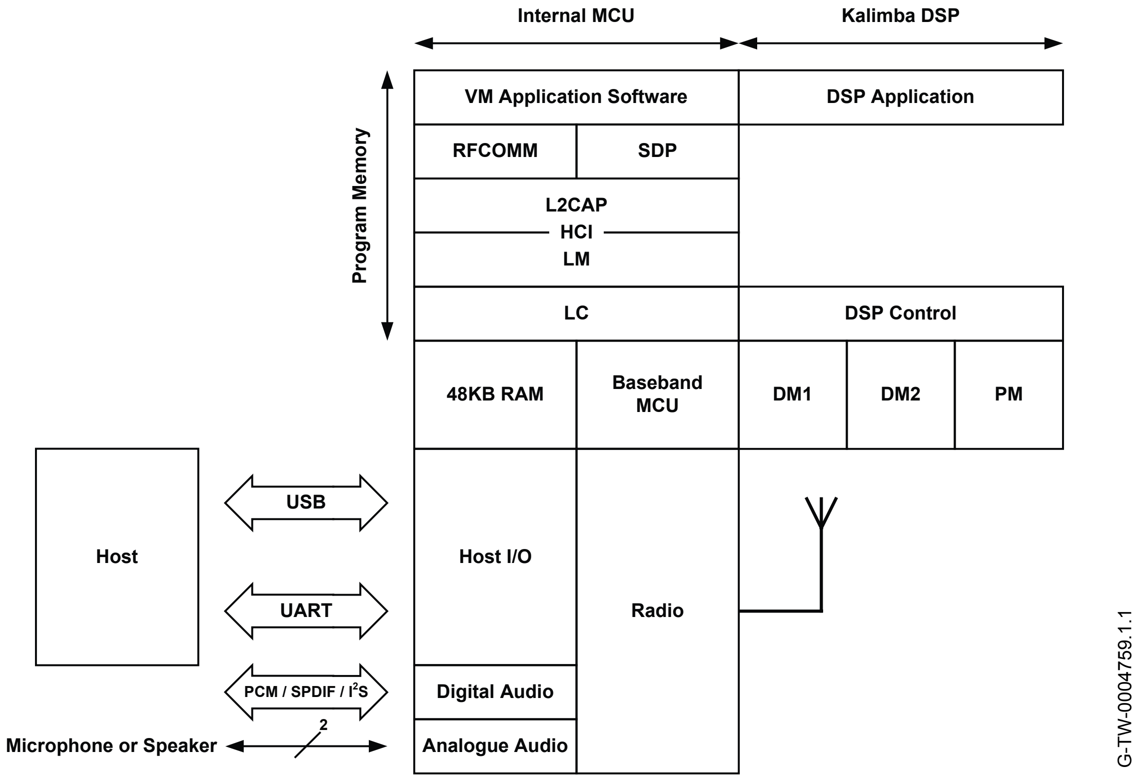


Figure 16.2: Stand-alone BlueCore5-Multimedia Flash (16Mb) and Kalimba DSP Applications

Note:

Program memory in Figure 16.2 is internal flash.

In Figure 16.2, this version of the stack firmware requires no host processor (but can use a host processor for debugging etc. as Figure 16.2 shows). The software layers for the application software run on the internal MCU in a protected user software execution environment known as a VM and the DSP application code runs from the DSP program memory RAM.

CSR provides a number of SDKs focused on end product use cases. These include Mono Headsets, Stereo Headsets, Audio Adaptors, Car Kits. The SDKs include firmware components, applications and appropriate profile support. For more information see www.csrsupport.com.

16.3 Host-Side Software

BlueCore5-Multimedia Flash (16Mb) can be ordered with companion host-side software:

- BlueCore5-PC includes software for a full Windows 98/ME, Windows 2000 or Windows XP Bluetooth host-side stack together with IC hardware described in this document.
- BlueCore5-Mobile includes software for a full host-side stack designed for modern ARM chip-based mobile handsets together with IC hardware described in this document.

16.4 eXtension

A wide range of software options is available from 3rd parties through the CSR eXtension partner program, see http://www.csr.com/eXtension.

17 Ordering Information

Interface Version	Package			Order Number
	Type	Size	Shipment Method	
UART and USB	LFBGA 120-ball (Pb free)	7 x 7 x 1.3mm, 0.5mm pitch	Tape and reel	BC57G687C-GITM-E4

Note:

Minimum order quantity is 2kpcs taped and reeled.

Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

To contact a CSR representative, email sales@csr.com or go to www.csr.com/contacts

18 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

18.1 Tape Orientation

Figure 18.1 shows the BlueCore5-Multimedia Flash (16Mb) packing tape orientation.

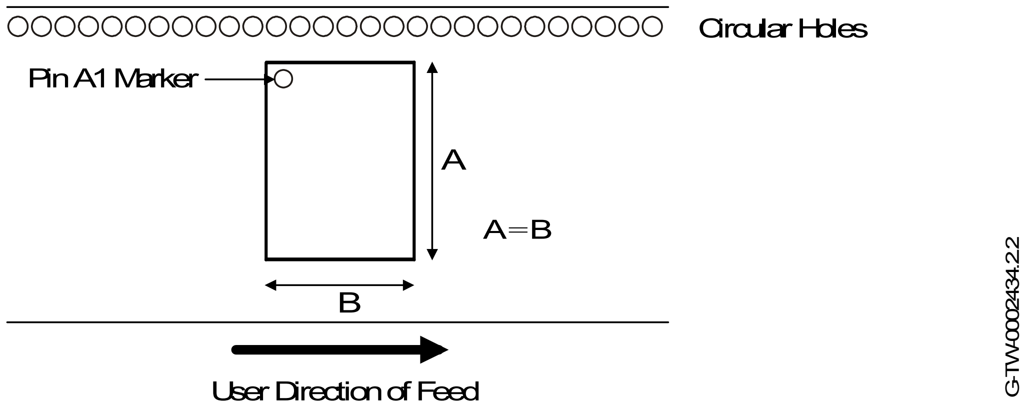


Figure 18.1: BlueCore5-Multimedia Flash (16Mb) Tape Orientation

18.2 Tape Dimensions

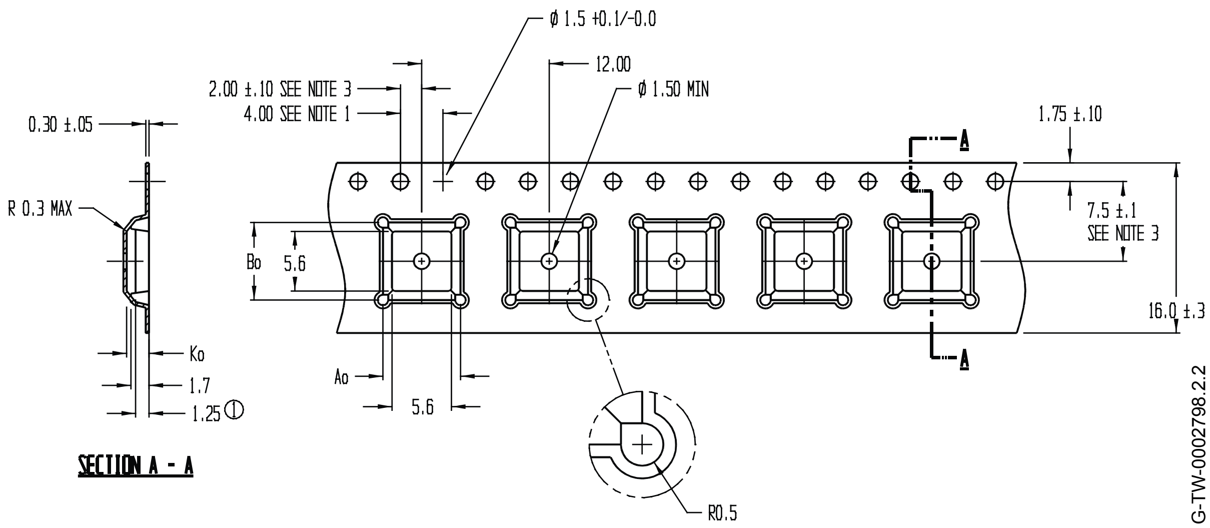


Figure 18.2: Tape Dimensions

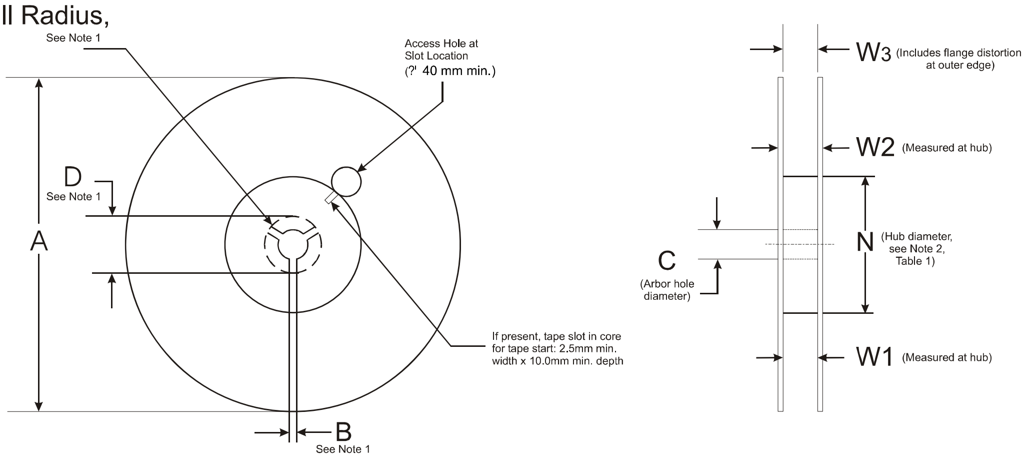
A_0	B_0	K_0	Unit	Notes
7.30	7.30	2.10	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2 2. Camber in compliance with EIA 481 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

BlueCore5-Multimedia Flash (16Mb) Data Sheet

18.3 Reel Information

Reel dimensions

(All dimensions in millimeters)



Notes:
1. Drive spokes optional; if used , dimensions B and D shall apply.
2. Maximum weight of reel and contents 13.6kg.

G-TW-0000386.3.2

Figure 18.3: Reel Dimensions

Package Type	Tape Width	A Max	B	C	D Min	N Min	W1	W2 Max	W3		Units
									Min	Max	
7 x 7 x 1.3mm LFBGA	16	332	1.5	13.0 (0.5/-0.2)	20.2	50	16.4 (3.0/-0.2)	19.1	16.4	19.1	mm

18.4 Moisture Sensitivity Level

BlueCore5-Multimedia Flash (16Mb) is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

19 Document References

Document	Reference, Date
BlueCore5 Charger Description and Calibration Procedure Application Note	CS-113282-ANP
BlueCore5-Multimedia Flash (16Mb) Performance Specification	CS-129296-SPP
Bluetooth and IEEE 802.11 b/g Co-existence Solutions Overview	bcore-an-066P
Bluetooth and USB Design Considerations	CS-101412-AN
Core Specification of the Bluetooth System	v2.1 + EDR, 26 July 2007
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	JESD22-A114
IC Packing and Labelling Specification	CS-112584-SPP
Moisture / Reflow Sensitivity Classification for Nonhermitic Solid State Surface Mount Devices	IPC / JEDEC J-STD-020
Optimising BlueCore5-Multimedia ADC Performance Application Note	CS-120059-AN
Selection of I^2C EEPROMS for Use with BlueCore	bcore-an-008P
Test Suite Structure (TSS) and Test Purposes (TP) System Specification 1.2/2.0/2.0 + EDR/ 2.1/2.1 + EDR	RF.TS/2.1.E.0, 27 December 2006
Typical Solder Reflow Profile for Lead-free Device	CS-116434-ANP
Universal Serial Bus Specification	v2.0, 27 April 2000

Terms and Definitions

Term	Definition
3G	3rd Generation of mobile communications technology
802.11™	WLAN specification defined by a working group within the IEEE
8DPSK	8-phase Differential Phase Shift Keying
π/4 DQPSK	π/4 rotated Differential Quaternary Phase Shift Keying
µ-law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
AC	Alternating Current
ACK	ACKnowledge
ACL	Asynchronous Connection-oriented
ADC	Analogue to Digital Converter
AFC	Automatic Frequency Control
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
ALU	Arithmetic logic unit
b	Bit
B	Byte
BCCMD	BlueCore Command
BCSP	BlueCore Serial Protocol
BGA	Ball Grid Array
BIST	Built-In Self-Test
BlueCore®	Group term for CSR's range of Bluetooth wireless technology ICs
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
BMC	Burst Mode Controller
CDMA	Code Division Multiple Access
CFC	Chlorofluorocarbon
CMOS	Complementary Metal Oxide Semiconductor
codec	Coder decoder
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CTS	Clear to Send
CVSD	Continuous Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
dBm	Decibels relative to 1mW
DC	Direct Current
DDS	Direct Digital Synthesis
DFU	Device Firmware Upgrade
DNL	Differential Non Linearity (ADC accuracy parameter)
DSP	Digital Signal Processor
e.g.	*exempli gratia*, for example
EDR	Enhanced Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory

Term	Definition
eSCO	Extended SCO
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
etc	*et cetera*, and the rest, and so forth
FET	Field Effect Transistor
FHS	Frequency Hop Synchronisation
FSK	Frequency Shift Keying
GCI	General Circuit Interface
GFSK	Gaussian Frequency Shift Keying
GSM	Global System for Mobile communications
H4DS	H4 Deep Sleep
HBM	Human Body Model
HCI	Host Controller Interface
I^2C	Inter-Integrated Circuit Interface
I^2S	Inter-Integrated Circuit Sound
i.e.	*Id est*, that is
I/O	Input/Output
IC	Integrated Circuit
IEEE	Institute of Electronic and Electrical Engineers
IF	Intermediate Frequency
IIR	Infinite Impulse Response (filter)
INL	Integral Non Linearity (ADC accuracy parameter)
IQ	In-Phase and Quadrature
ISDN	Integrated Services Digital Network
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
Kalimba	An open platform DSP co-processor, enabling support of enhanced audio applications, such as echo and noise suppression, and file compression / decompression
LC	An inductor (L) and capacitor (C) network
LC	Link Controller
LCD	Liquid-Crystal Display
LED	Light-Emitting Diode
LM	Link Manager
LMP	Link Manager Protocol
LNA	Low Noise Amplifier
LSB	Least-Significant Bit (or Byte)
MAC	Multiplier and ACcumulator
Mbps	Megabits per second
MCU	MicroController Unit
MIPS	Million Instructions Per Second
MISO	Master In Slave Out
MMU	Memory Management Unit
MSB	Most Significant Bit (or Byte)
N/A	Not Applicable

Term	Definition
NSMD	Non Solder Mask Defined
O.C.	Open Circuit
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Pull-down
PIO	Programmable Input/Output
plc	Public Limited Company
POP	Persistent Organic Pollutants
ppm	parts per million
PS Key	Persistent Store Key
PSRR	Power Supply Rejection Ratio
PU	Pull-up
PVC	Poly Vinyl Chloride
RAM	Random Access Memory
RC	Resistor Capacitor
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
RSSI	Received Signal Strength Indication
RTS	Request To Send
RX	Receive or Receiver
SBC	Sub-band Coding
SCO	Synchronous Connection-Oriented
SDK	Software Development Kit
SIG	(Bluetooth) Special Interest Group
SNR	Signal-to-Noise Ratio
S/PDIF	Sony/Philips Digital InterFace (also IEC 958 type II, part of IEC-60958). An interface designed to transfer stereo digital audio signals between various devices and stereo components with minimal loss.
SPI	Serial Peripheral Interface
SPL	Sound Pressure Level
TCXO	Temperature Compensated crystal Oscillator
THD+N	Total Harmonic Distortion and Noise
TP	Test Purposes
TSS	Test Suite Structure
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

Term	Definition
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
VoIP	Voice over Internet Protocol
W-CDMA	Wideband Code Division Multiple Access
WCS	Wireless Coexistence System
WLAN	Wireless Local Area Network