

# BCT3253

## 3ch Current Sink RGB LED driver for illumination

### Introduction

The BCT3253 is a 3 channel current sink RGB LED driver. Each channel can be independent programmed by I2C interface and can be configured up to 256 constant current level. By synchronous clock function, combined operation of three channels is possible. It can be used to make amazing lighting effects of over 67million colors for portable devices. With the build-in internal RAMs, the RGB lighting effects can be running independently, which can save the system (CPU/MCU/AP) resources. Less than 2 uA shut down current effective extend battery usage time. BCT3253 is a lead-free environmental protection product, and the temperature range is -40 °C to + 85 °C. It offers in tiny 12Pin 1.6 x 1.2 WCSP package, with the thickness of 0.65 mm.

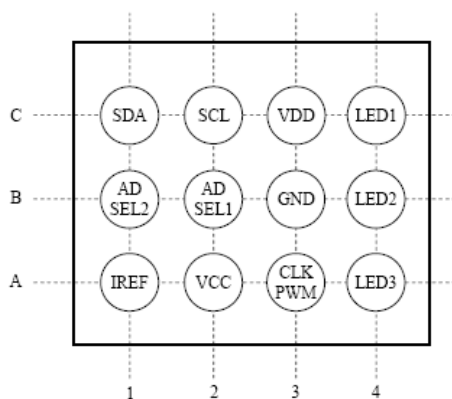
### Features

- High speed I2C Interface with 400khz (Slave address is switchable.)
- Build-in 3ch LED Driver Circuit ( Max Current Selectable of 63.75 / 31.875 / 25.50 / 12.75mA )
- Each channel has 256 current levels, programmed by I2C interface.
- Built-in POR (Power On reset) function
- Co-Anode LED connection
- 2.4MHz OSC
- 12Pin 1.6 x 1.2 WCSP package

### Application

- Mobile phone
- MP3/MP4 /CD/Media Players
- RGB LED drivers
- LED Status Indicators

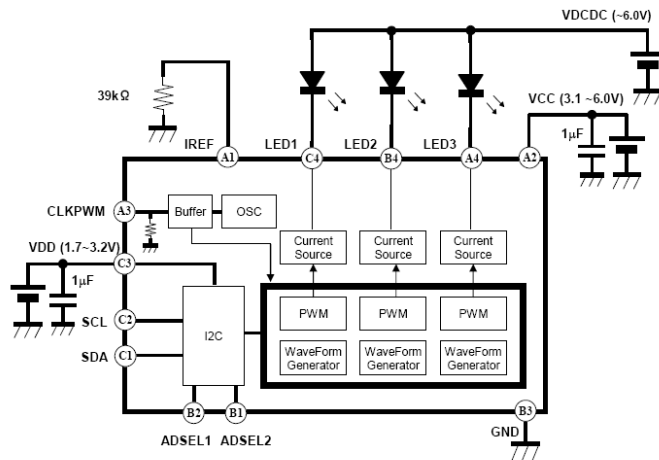
Pin Descriptions (Bottom view)



### Ordering Information

Order Number	Package Type	Temperature Range	Marking	QTY/Reel
BCT3253EGG-TR	WCSP-12(1.56x1.26)	-40°C to +85°C	LBZ	3000

## Typical application



### Notes

1. When LED output pins and CLKPWM pin are not used, it is recommended to leave them floating.

### I2C Slave address

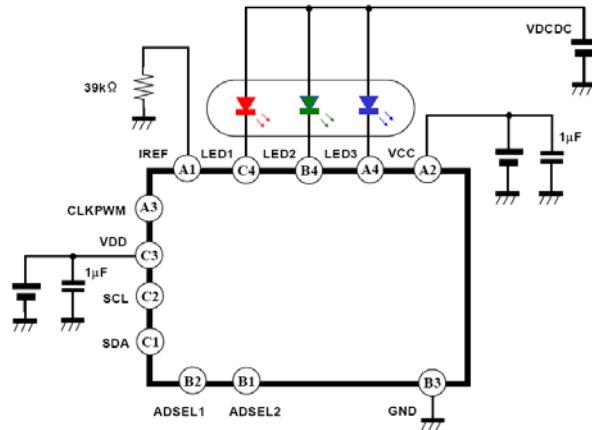
ADSEL1	ADSEL2	Address
L	L	30 h
L	H	31 h
H	L	32 h
H	H	33 h

### Pin Description

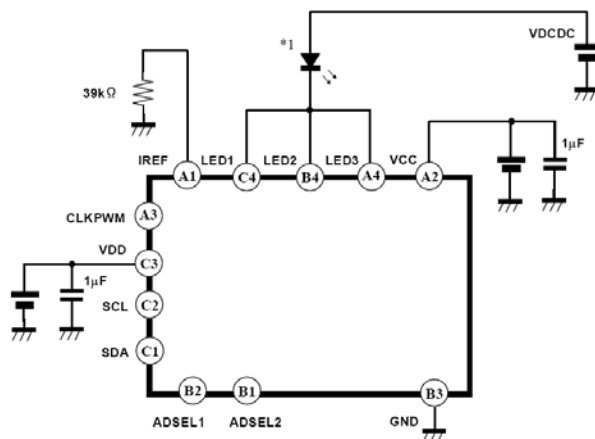
Pin No.	Pin Name	Type	Description
A2	VCC	Power Supply	Power supply connection pin for LED Circuit
C3	VDD	Power Supply	Power Supply connection pin for interface
B3	GND	Ground	GND Pin
C4	LED1	Output	LED1 output pin
B4	LED2	Output	LED2 output pin
A4	LED3	Output	LED3 output pin
A1	IREF	Input	Resistor connection pin for constant current value setting
C2	SCL	Input	I2C Interface clock input pin
C1	SDA	Input/Output	I2C Interface data I/O pin
A3	CLKPWM	Input/Output	Reference clock input output /PWM input pin
B2	ADSEL1	Input	I2C Interface slave address switch pin 1
B1	ADSEL2	Input	I2C Interface slave address switch pin 2

## More Application Circuit Examples

### 1. Basic RGB Application

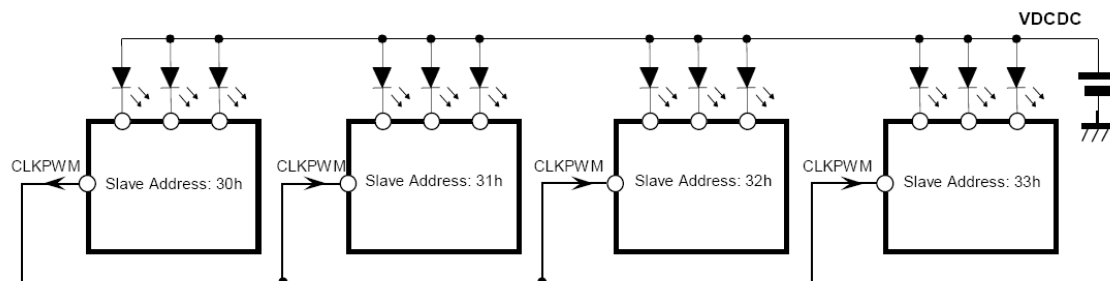


### 2. Typical Torch Application



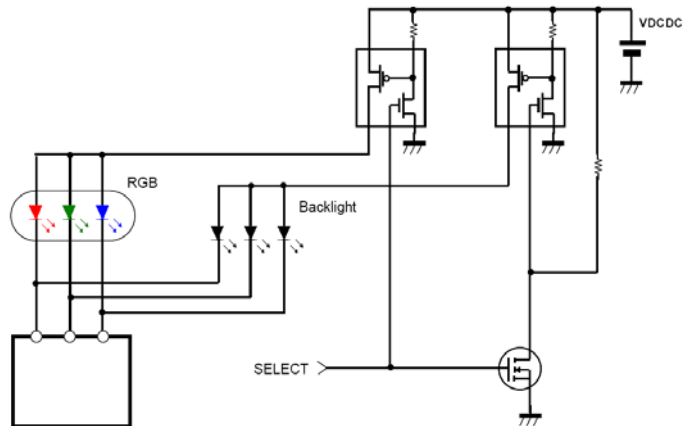
Note) \*1 : The maximum current supported is 191.25mA (63.75mA x 3).

### 3. Connected Application



The IC can be connected and controlled individually by using different slave addresses. It is possible to connect up to 4 of the ICs by using synchronous clock.

#### 4. Multiplex RGB and Backlight Application



#### Absolute Maximum Ratings

Supply voltage, $V_{CCMAX}$ .....	+7.0V
Supply voltage, $V_{DDMAX}$ .....	+4.6V
Supply current, $I_{CC}$ .....	A
Power dissipation, $P_d$ .....	46.8 mW
Working temperature, $T_{opr}$ .....	-30 °C to +85°C
Storage temperature, $T_{stg}$ .....	-55 °C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### Allowable voltage range

Supply voltage, VCC .....	-0.2 V ~ +7.0V
Supply voltage, VDD .....	-0.2 V ~ +4.6V
Voltage at output pin LED1,LED2,LED3.....	0 V ~ +7.0V
Voltage at input pin IREF .....	0V ~ VCC+0.3V
Voltage at Other input pins .....	0V ~ VDD+0.3V

## Electrical Characteristic (part 1)

Note) Ta=25°C, VCC=3.6 V, VDD=1.8V unless otherwise specified.

B No.	Parameter	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
Current consumption									
1	Current consumption 1 OFF mode	ICC1	1	VDD=0V	—	0	2	μA	—
2	Current consumption 2 OFF mode	ICC2	1	VDD=1.8V	—	1	5	μA	—
3	Current consumption 3 LED lighting mode	ICC3	1	I <sub>LED</sub> =25.50 mA setting All LED = ON	—	0.6	1	mA	—
LED Driver									
4	Off time leak current	I <sub>leak</sub>	1	Off setting LED*=6.0V	—	—	1.0	μA	—
5	Minimum setting current value 1	I <sub>min1</sub>	1	IMAX[1:0]=01, LED*=1.0V	0.05	0.10	0.15	mA	—
6	Minimum setting current value 2	I <sub>min2</sub>	1	IMAX[1:0]=01, LED*=1.0V	0.736	0.80	0.864	mA	—
7	Maximum setting current value	I <sub>max</sub>	1	IMAX[1:0]=01, LED*=1.0V	23.46	25.50	27.54	mA	—
8	Current step	I <sub>step</sub>	1	IMAX[1:0]=01, LED*=1.0V	0.00	0.10	0.18	mA	—
9	Minimum voltage for retainable constant current value	V <sub>sat</sub>	1	IMAX[1:0]=01, Terminal minimum voltage of LED* becoming 95% of the LED current value in 1V.	—	0.2	0.4	V	—
10	Error between channels	I <sub>match</sub>	1	12.80mA setting, LED*=1.0V	-5	—	5	%	—
Internal oscillator									
11	Oscillation frequency	f <sub>osc</sub>	1	—	1.92	2.40	2.88	MHz	—

## Electrical Characteristic (part 2)

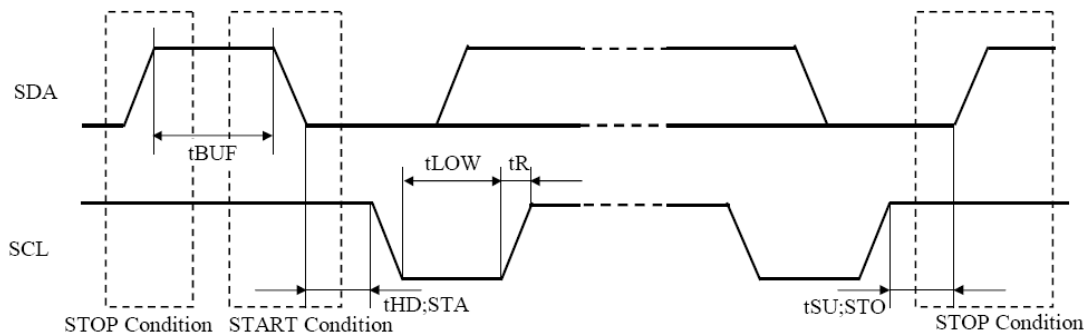
Note) Ta=25°C, VCC=3.6 V, VDD=1.8V unless otherwise specified.

B NO	Parameter	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					Min	Typ	Max		
SCL, SDA									
12	High-level input voltage range	VIH1	1	—	VDD×0.7	—	VDD+0.2	V	—
13	Low-level input voltage range	VIL1	1	—	-0.2	—	VDD×0.3	V	—
14	High-level input current	I <sub>IH1</sub>	1	V <sub>in</sub> = 1.8 V	—	0	1	uA	—
15	Low-level input current	I <sub>IL1</sub>	1	V <sub>in</sub> = 0 V	—	0	1	uA	—
16	Low-level output voltage (SDA)	VOL1H	1	I <sub>in</sub> = 3mA, VDD > 2 V	0	—	0.4	V	—
17	Low-level output voltage (SDA)	VOL1L	1	I <sub>in</sub> = 3mA, VDD < 2 V	0	—	VDD×0.2	V	—
CLKPWM									
18	High-level input voltage range	VIH2	1	—	VDD×0.7	—	VDD+0.2	V	—
19	Low-level input voltage range	VIL2	1	—	-0.2	—	VDD×0.3	V	—
20	Pin pull down resistance value	RPD2	1	—	0.5	1	2	MΩ	—
21	High-level output voltage	VOH2	1	I <sub>out</sub> = -2 mA	VDD×0.8	—	VDD+0.2	V	—
22	Low-level output voltage	VOL2	1	I <sub>out</sub> = 2 mA	-0.2	—	VDD×0.2	V	—
ADSEL1, ADSEL2									
23	High-level input voltage range	VIH3	1	—	VDD×0.7	—	VDD+0.2	V	—
24	Low-level input voltage range	VIL3	1	—	-0.2	—	VDD×0.3	V	—
25	High-level input current	I <sub>IH3</sub>	1	V <sub>in</sub> = 1.8 V	—	0	1	uA	—
26	Low-level input current	I <sub>IL3</sub>	1	V <sub>in</sub> = 0 V	—	0	1	uA	—

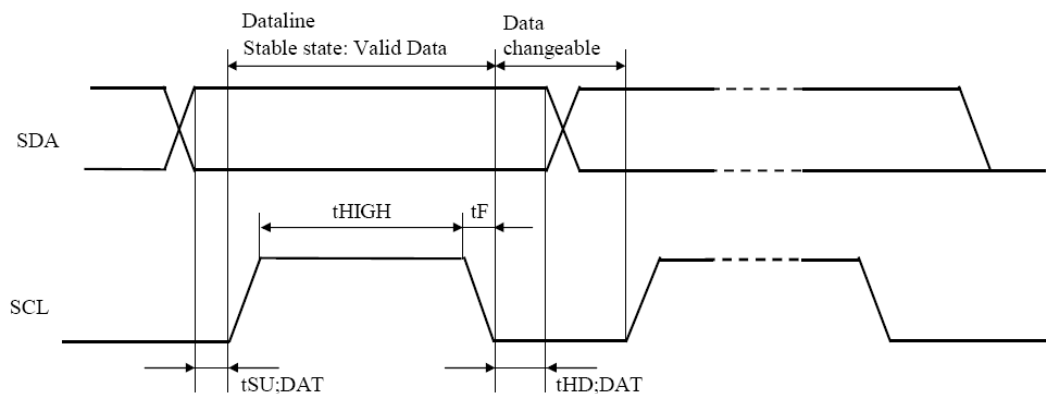
## Electrical Characteristic (Reference values for design) (part 1)

Note)  $T_a=25^{\circ}\text{C}$ ,  $V_{CC}=3.6\text{ V}$ ,  $V_{DD}=1.8\text{ V}$  unless otherwise specified.

B No.	Parameter	Symbol	Test Circuit	Conditions	Reference Values			Unit	Note
					Min	Typ	Max		
CLKPWM									
27	External PWM operation mode Data-enabled high pulse width	Wpwm	1	—	2	—	—	$\mu\text{s}$	—
I2C signal timing									
28	Input voltage hysteresis (1)	Vhys1	1	SCL, SDA hysteresis voltage $V_{DD} > 2\text{ V}$	$0.05 \times V_{DD}$	—	—	V	—
29	Input voltage hysteresis (2)	Vhys2	1	SCL, SDA hysteresis voltage, $V_{DD} > 2\text{ V}$	$0.1 \times V_{DD}$	—	—	V	—
30	Spike pulse width kept down by input filter	Tsp	1	—	0	—	50	ns	—
31	I/O pin capacitance	Ci	1	—	—	—	10	pF	—



### Data recognition condition

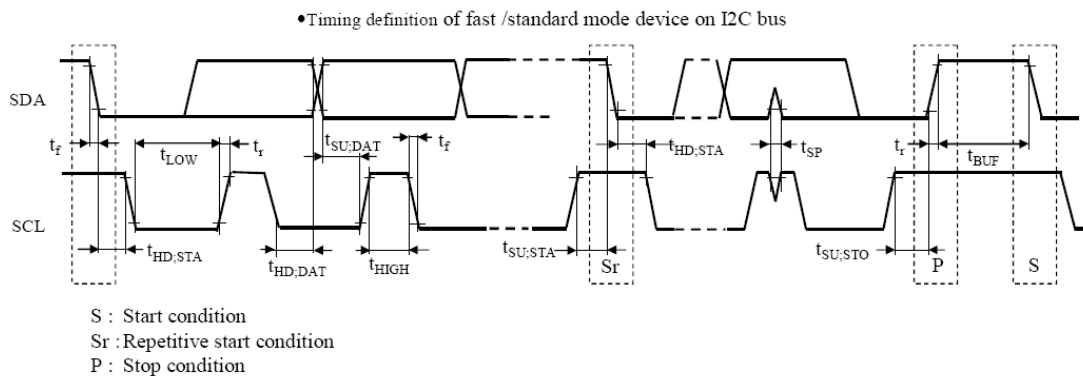


## Electrical Characteristic (Reference values for design) (part 2)

Note) Ta=25°C, VCC=3.6 V, VDD=1.8V unless otherwise specified.

B No.	Parameter	Symbol	Test Circuit	Conditions	Reference Values			Unit	Note
					Min	Typ	Max		
I2C signal timing									
32	Hold duration (recursive)	t <sub>HD:STA</sub>	1	After t <sub>HD:STA</sub> , the first clock pulse is generated.	0.6	—	—	μs	—
33	SCL clock "L" duration	t <sub>LOW</sub>	1	—	1.3	—	—	μs	—
34	SCL clock "H" duration	t <sub>HIGH</sub>	1	—	0.6	—	—	μs	—
35	Recursive 「START」 condition setting time	t <sub>SU:STA</sub>	1	—	0.6	—	—	μs	—
36	Data hold time	t <sub>HD:DAT</sub>	1	—	0	—	0.9	μs	—
37	Data setup time	t <sub>SU:DAT</sub>	1	—	100	—	—	ns	—
38	SDA, SCL signal rise up time	t <sub>r</sub>	1	—	20+0.1 C <sub>b</sub>	—	300	ns	—
39	SDA, SCL signal fall time	t <sub>f</sub>	1	—	20+0.1 C <sub>b</sub>	—	300	ns	—
40	Setup time under 「STOP」 condition	t <sub>SU:STO</sub>	1	—	0.6	—	—	μs	—
41	Bus free time between under 「STOP」 condition and 「START」 condition	t <sub>BUF</sub>	1	—	1.3	—	—	μs	—
42	Noise margin of each connection device at "L" level	V <sub>aL</sub>	1	—	0.1×VDD	—	—	V	—
43	Noise margin of each connection device at "H" level	V <sub>aH</sub>	1	—	0.2×VDD	—	—	V	—

Timing definition of fast /standard mode device on I2C bus.

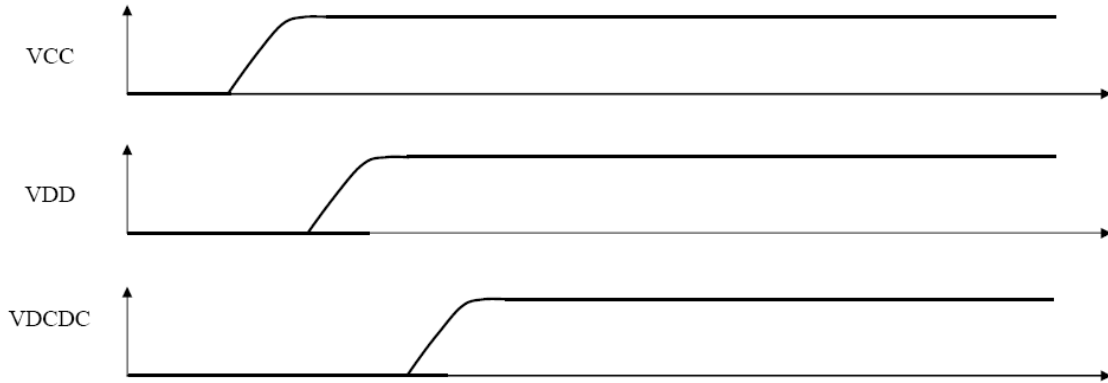




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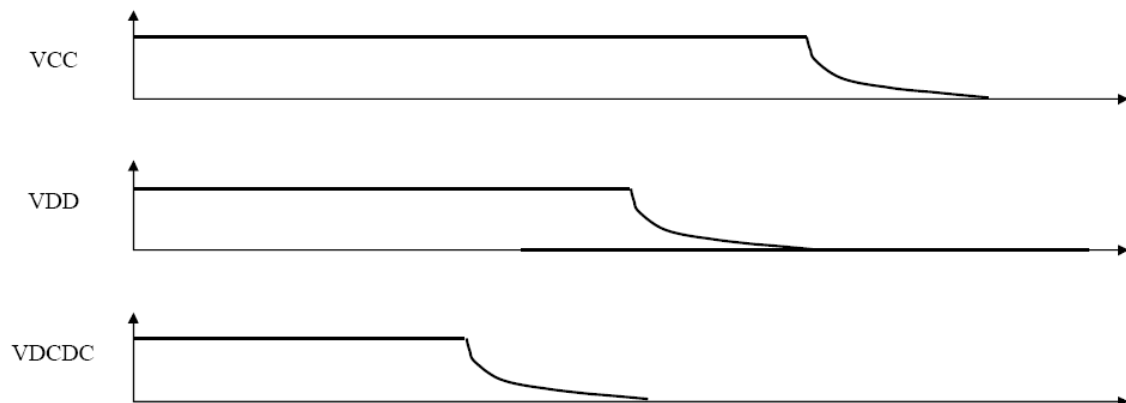
## Power-on / Power-off Sequence

### 6.1 Power-on



Note) \* : There is no problem if VCC and VDCDC rise at the same time.

### 6.2 Power-off



Note) \* : There is no problem if VCC and VDCDC fall at the same time.

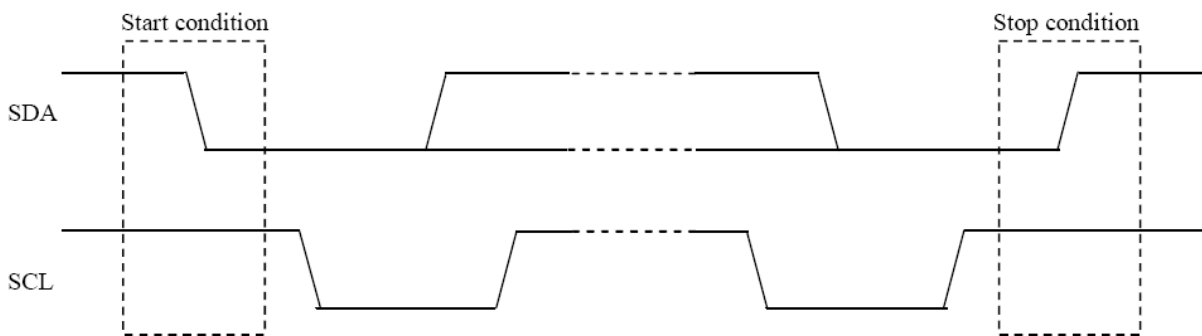
## I2C-bus Interface

### 10.1 Basic standards

- I2C bus of this product is designed to be compatible with the standard mode ( 100kbps ) and fast mode of specification, version 2.1 by Philips, but not with HS mode ( ~ 3.4 Mbps ).
- This product operates as a slave device in I2C bus system.
- An operation check has not been conducted in multimaster bus system and mixed speed bus system for this product. Connection confirmation with CBUS server has not been conducted. Please contact us if you use in this modes.
- By purchasing I2C bus enabled product of Semiconductor Company, Broadchip subject to be used in conformity with I2C bus standard specification authorized by Philips under the I2C patent right owned by Philips, the right to use these two products will be granted.

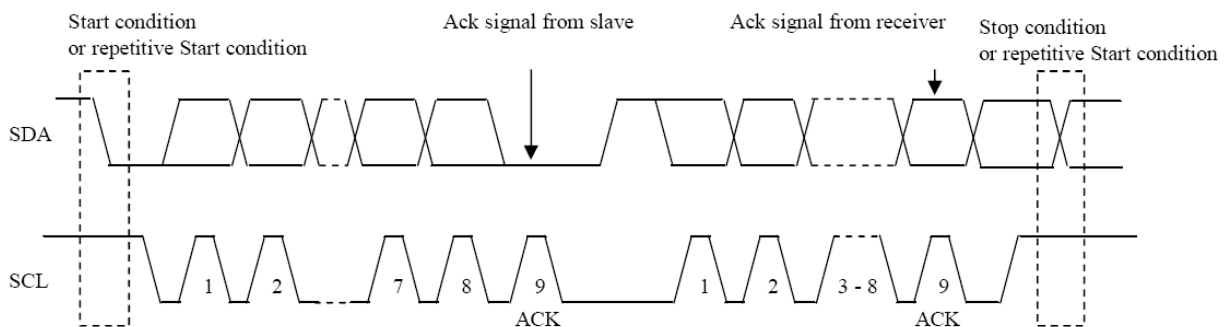
### 10.2 Start condition and Stop condition

- When SCL is “H”, if SDA line is changed from “H” to “L”, it is Start condition. When SCL is “H”, if SDA line is changed from “L” to “H”, it is Stop condition.
- Start condition is always generated by master. After Start condition is initiated, bus becomes busy state. After Stop condition is initiated, bus return to free state.



### 10.3 Data transfer

- Each length of byte output in SDA line is 8 bit.
- There is no limit for the number of byte in a single transfer.
- Each bit must be followed by Ack (acknowledge byte).
- Data is sequentially sent from the most significant byte ( MSB ).
- In case the receiver is unable to receive all the bytes which constitute data until it finished executing, for example, internal interruption service, transmitter can be set to standby state by keeping the clock line SCL in the state of “L”. Data transfer will be resumed after the receiver becomes able to receive data byte and clock line SCL is released .



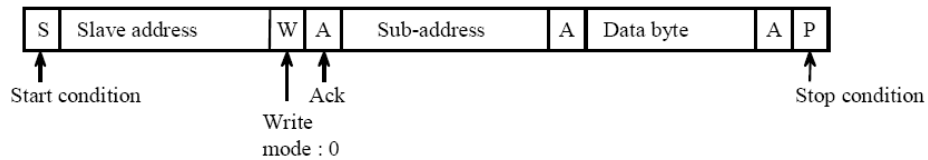
## I2C-bus Interface (continued)

### 10.4 DATA format

Four different slave addresses can be selected by configuring the ADSEL1, ADSEL2 pin connections. The chart below shows the possible slave addresses of this product.

ADSEL2	ADSEL1	Slave address
L (Ground)	L (Ground)	30 h
L (Ground)	H (VDD)	31 h
H (VDD)	L (Ground)	32 h
H (VDD)	H (VDD)	33 h

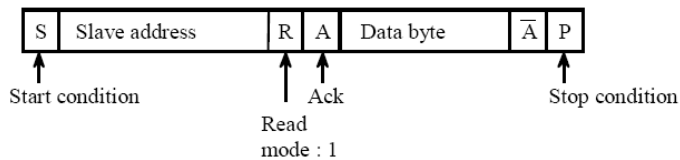
#### \* Write mode



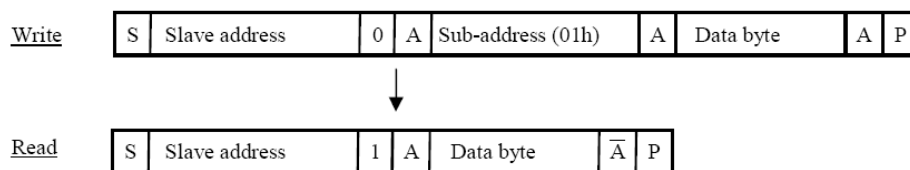
#### \* Read mode

A) When sub-address is not assigned.

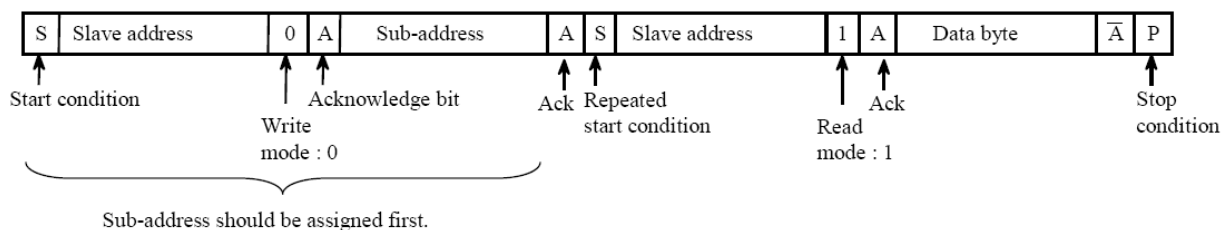
When data is read without assigning sub-address, it is possible to read the value of sub-address specified in Write mode immediately before.



Ex) When writing data into address and reading data from "01 h"



B) When specifying sub-address

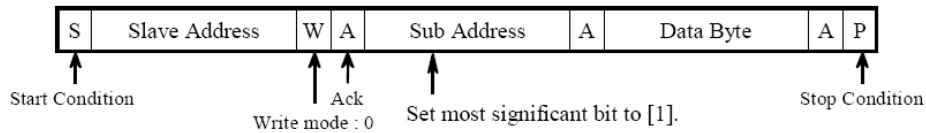


## I2C-bus Interface (continued)

### 10.4 DATA format

#### \* Continuous Write mode

When using the continuous Write mode, the most significant bit of Sub address should be set to [1].

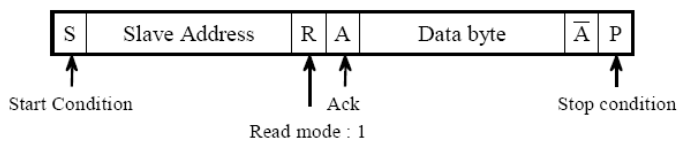


Ex) 05h → 85h, 11h → 91h

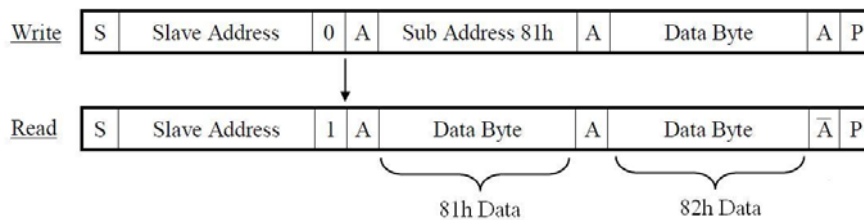
#### \* Continuous Read mode

##### A) When Sub address is not specified

When the most significant bit specified in the last Write mode is [1], it is possible to perform the continuous Read mode operation directly after it.

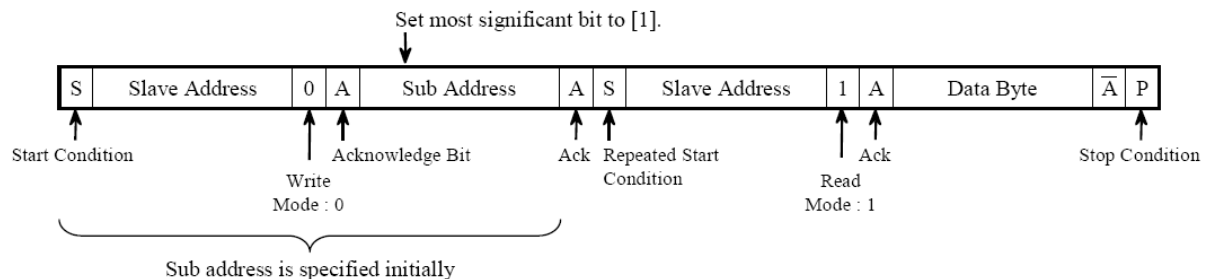


Ex) Case where data is read from Address 01h after data is written to Address 01h



Sub address will be added 1, When using the continuous read mode,

##### B) When Sub address is specified



## LED Driver Control

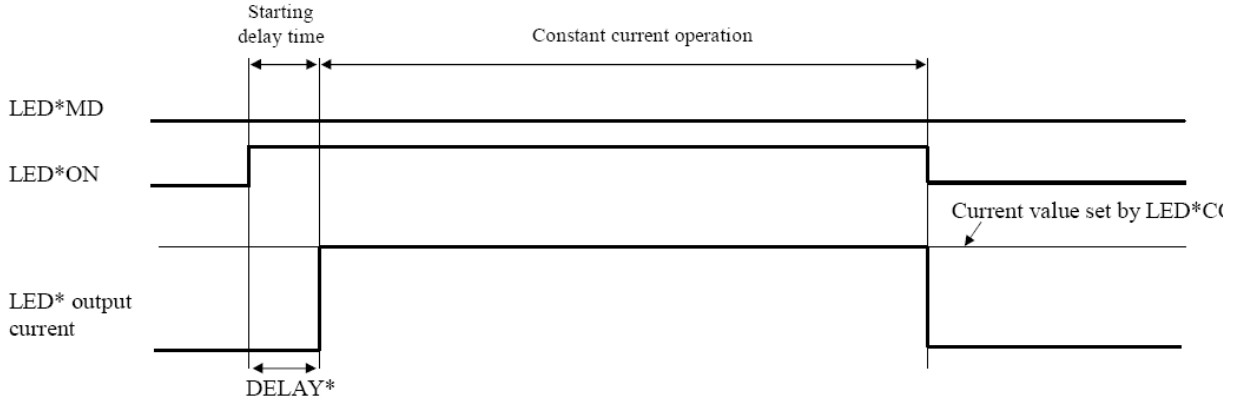
### 11.1 Function table about each LED driver

Functions / LED driver	LED1,2,3 (IMAX[1:0]=00h)	LED1,2,3 (IMAX[1:0]=01h)	LED1,2,3 (IMAX[1:0]=10h)	LED1,2,3 (IMAX[1:0]=11h)
Current value setting *1	12.75 mA max. (8-bit, 0.05 mA step)	25.50 mA max. (8-bit, 0.10 mA step)	31.875 mA max. (8-bit, 0.125 mA step)	63.75 mA max. (8-bit, 0.25 mA step)
PWM duty setting (slope lighting mode)	128 steps *2	128 steps *2	128 steps *2	128 steps *2
Slope control	○	○	○	○

Notes) \*1 : With use the register IMAX[1:0], Current value setting will be set.  
 \*2 : When in constant current mode, it is impossible to fix PWM duty at any time.

### 11.2 Constant Current Lighting Mode

- It is possible to control the lighting mode of each LED driver.
- Choose 'Constant current lighting mode' and 'Slope lighting mode' by setting Register LED\*MD.  
 To operate at 'Constant current mode', please set LED\*MD at "0". ( "\*" can be 1, 2, or 3.)

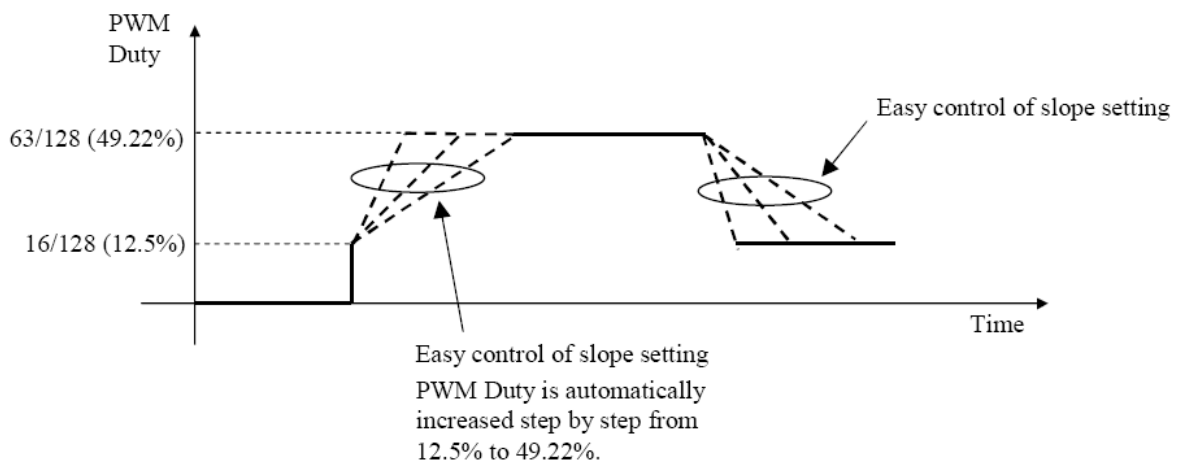


- Upon setting LED\*On to "1", constant current operation will start after the previously set starting delay time, DELAY\*.
- As described later, it is possible to turn on and off at High/Low of CLKPWM pin by making the external PWM operating mode for CLKPWM pin setting valid.

## LED Driver Control (continued)

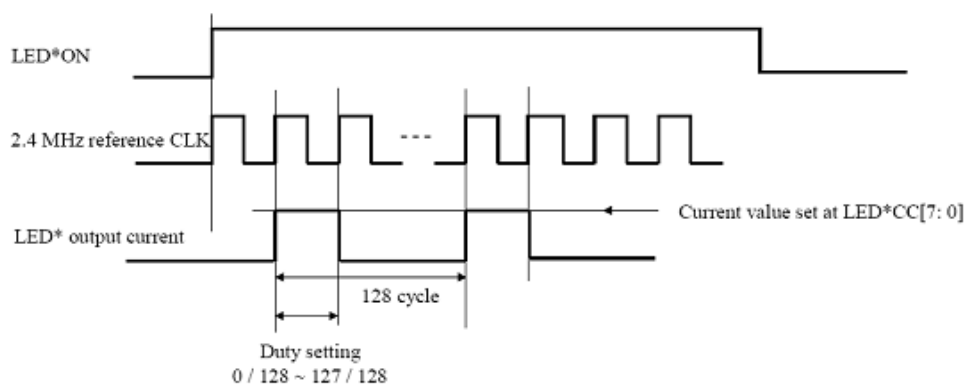
### Slope Lighting Mode

- This mode allows easy control of gradual increase or decrease in brightness of each LED by PWM duty setting.
- Only minimum, middle, and maximum PWM duty ratios have to be specified. After that, the PWM duty is changed automatically.
- The slope operation is repeated over and over again, as long as the lighting mode is not changed and LED is always ON.



< Slope Explanation >

- The minimum resolution of SLOPE sequence control is 2.40 MHz reference clock cycle as below.

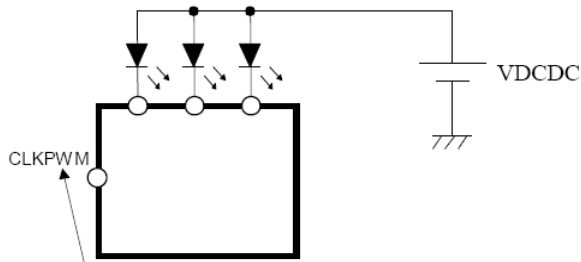


## 11. LED Driver Control (continued)

### 11.5 External Clock Input Mode and Internal Clock Output Mode of CLKPWM Pin

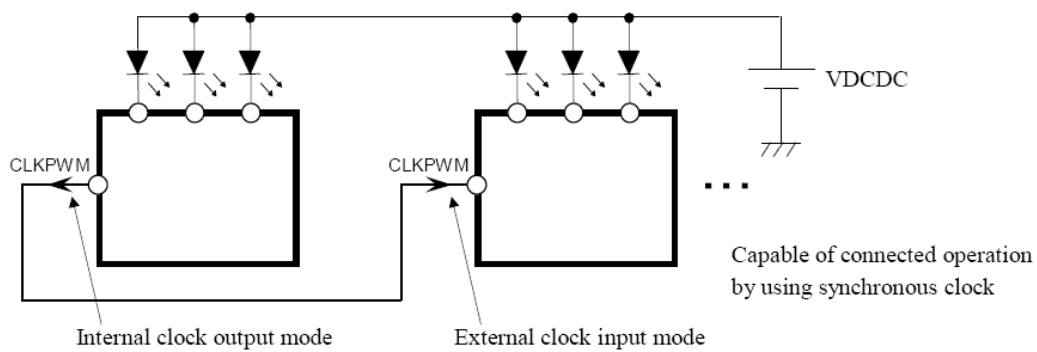
The following configuration can be made up by choosing 'External clock input mode', 'Internal clock output mode' in register setting.

< Single application >



Unused state (CLKPWM operation OFF mode)

< Connected application >

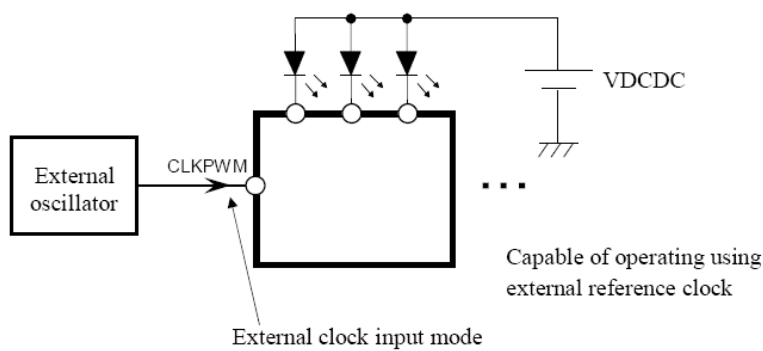


Internal clock output mode

External clock input mode

...  
Capable of connected operation by using synchronous clock

< External reference clock application >



...  
Capable of operating using external reference clock

External clock input mode

## 12. Package information

Unit: mm

