# BCT4257
## Low-Voltage, 2.8Ω SPDT Analog Switch

### General Description

The BCT4257 is a high-bandwidth, fast single pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, 1.65V to 5.5V, the BCT4257 has a maximum ON resistance of 5.1-ohms at 1.65V, 3.9-ohms at 2.3V & 2.85-ohms at 4.5V.

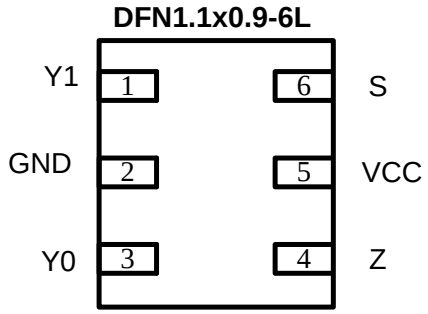
Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

The control input, S, tolerates input drive signals up to 5.5V, independent of supply voltage.

### Applications

Cell Phones
PDAs
Portable Instrumentation
Battery Powered Communications
Computer Peripherals

### Connection Diagram(Top View)




### Features

♦CMOS Technology for Bus and Analog Applications
♦ Low ON Resistance: 3-ohms @ 2.7V
♦ Wide VCC Range: 1.65V to 5.5V
♦ Rail-to-Rail Signal Range
♦ Control Input Overvoltage Tolerance: 5.5V min.
♦ High Off Isolation: 57dB at 10MHz
♦ 54dB (10MHz) Crosstalk Rejection Reduces Signal Distortion
♦ Break-Before-Make Switching
♦ High Bandwidth: 300 MHz
♦ Extended Industrial Temperature Range: –40°C to 85°C
♦ Packaging: DFN1.1x0.9-6L (Pb-free & Green available)

### Pin Description

| Name | Description |
|---|---|
| Y1 | Independent input or output |
| GND | Ground |
| Y0 | Independent input or output |
| Z | Common output or input |
| VCC | Supply voltage |
| S | Select input |

### Logic Function Table

| Logic Input (S) | Function |
|---|---|
| 0 | Y0 Connected to Z |
| 1 | Y1 Connected to Z |

### ORDERING INFORMATION

| Ordering Code | Package Description | Temp Range | Top Marking |
|---|---|---|---|
| BCT4257ELT-TR | DFN1.1x0.9-6L | –40°C to +85°C | AAB |

## ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage $V_{CC}$.....–0.5V to +7V
DC Switch Voltage ($V_S$) (2).....–0.5V to $V_{CC}$ +0.5V
DC Input Voltage ($V_{IN}$) (2).....–0.5V to +7.0V
DC $V_{CC}$ or Ground Current ($I_{CC}/I_{GND}$).....±100mA
DC Output Current ($V_{OUT}$) .....128mA
Storage Temperature Range ($T_{STG}$) ..... –65°C to +150°C
Junction Temperature under Bias ($T_J$) ..... 150°C
Junction Lead Temperature ($T_L$)
(Soldering, 10 seconds) ..... 260°C
Power Dissipation ($P_D$) @ +85°C .....180mW

## RECOMMENDED OPERATING CONDITIONS(3)

Supply Voltage Operating ($V_{CC}$).....1.65V to 5.5V
Control Input Voltage ($V_{IN}$).....0V to $V_{CC}$
Switch Inp ut Voltage ($V_{IN}$).....0V to $V_{CC}$
Output Voltage ($V_{OUT}$).....0V to $V_{CC}$
Operating Temperature ($T_A$).....–40°C to +85°C
Thermal Resistance (θJA).....350°C/W

Note 1:Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.
Note 2:The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.
Note 3:Control input must be held HIGH or LOW; it must not float.

## DC ELECTRICAL CHARACTERISTICS (TA = - 40°C to +85°C)

| Parameter | Description | Test Conditions | Supply Voltage | Temp (ºC) | Min. | Typ | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IAR}$ | Analog Input Signal Range | | $V_{CC}$ | $T_A$ = 25°C & –40°C to 85°C | 0 | | Vcc | V |
| $R_{ON}$ | ON Resistance(4) | $I_{out}$ = 100mA, Y0 or Y1=1.5V | 2.7V | $T_A$ = 25°C | | 3 | 6 | Ω |
| $R_{ON}$ | ON Resistance(4) | $I_{out}$ = 100mA, Y0 or Y1=3.5V | 4.5V | $T_A$ = 25°C | | | 3 | Ω |
| $\Delta R_{ON}$ | ON Resistance Match Between Channels(4,5,6) | $I_{out}$ = 100mA, Y0=Y1=1.5V | 2.7V | $T_A$ = 25°C | | | 0.75 | Ω |
| | | | 4.5V | | | | 0.25 | |
| $R_{ONF}$ | ON Resistance(4,5,7) Flatness | I(Z) = -100mA; Y0 or Y1= 0.75V, 2V | 2.7V | $T_A$ = 25°C | | | 0.5 | Ω |
| $R_{ONF}$ | ON Resistance(4,5,7) Flatness | I(Z) = -100mA; Y0 or Y1=1.5V, 3.0V, | 4.5V | $T_A$ = 25°C | | | 0.1 | Ω |
| $V_{IH}$ | Input High Voltage | Logic High Level | $V_{CC}$ = 1.65V to 1.95V | $T_A$ = 25°C & –40°C to 85°C | 1.5 | | | V |
| | | | $V_{CC}$ = 2.3V to 5.5V | | 1.7 | | | |
| $V_{IL}$ | Input Low Voltage | Logic Low Level | $V_{CC}$ = 1.65V to 1.95V | | | | 0.5 | V |
| | | | $V_{CC}$ = 2.3V to 5.5V | | | | 0.8 | |

## DC ELECTRICAL CHARACTERISTICS (TA = - 40°C to +85°C)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $I_{IN}$ | Input Leakage Current | 0 ≤$V_{IN}$ ≤5.5V | $V_{CC}$ = 0V to 5.5V | $T_A$ = 25°C | | | ±0.1 | µA |
| | | | | $T_A$ = –40°C to 85°C | | | ±1.0 | |
| $I_{OFF}$ | OFF State Leakage Current | Z=1V,4.5V, Y0 or Y1=4.5V, 1V | $V_{CC}$ = 5.5V | $T_A$ = 25°C | -2.0 | | 2.0 | |
| $I_{CC}$ | Quiescent Supply Current | All channels ON or OFF, $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 | $V_{CC}$ = 5.5V | $T_A$ = 25°C | | | 1 | |
| | | | | $T_A$ = –40°C to 85°C | | | 10 | |

Note 4: Measured by voltage drop between Y0/Y1 and Z pins at the indicated current through the device. ON resistance is determined by the lower of the voltages on two ports (Y0 or Y1)
Note 5: Parameter is characterized but not tested in production.
Note 6: $\Delta R_{ON}$ = $R_{ON}$ max – $R_{ON}$ min. measured at identical $V_{CC}$, temperature and voltage levels.
Note 7: Flatness is defined as difference between maximum and minimum value of ON resistance over the specified range of conditions..
Note 8: Guaranteed by design.

## CAPACITANCE(12)

| Parameter | Description | Test Conditions | Supply Voltage | Temp (ºC) | Min. | Typ | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Control Input | f= 1 MHz(12) | $V_{CC}$ = 5.0V | $T_A$ = 25°C | | 2.3 | | pF |
| $C_{IO-Y1}$ | For Y1 Port,Switch OFF | | | | | 6.5 | | |
| $C_{IOA-ON}$ | For Y0 Port, Switch ON | | | | | 18.5 | | |

## SWITCH AND AC CHARACTERISTICS

| Parameter | Description | Test Conditions | Supply Voltage | Temp (ºC) | Min. | Typ | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay: Z to Yn | See test circuit diagrams 1 and 2. $V_I$ Open (10) | $V_{CC}$= 2.3V to 2.7V | $T_A$ = 25°C & –40 to 85°C | | 1.2 | | ns |
| | | | $V_{CC}$ = 3.0V to 3.6V | | | 0.8 | | |
| | | | $V_{CC}$= 4.5V to 5.5V | | | 0.3 | | |
| $t_{PZL}$ $t_{PZH}$ | Output Enable Turn ON Time: Z to Yn | diagrams 1 & 2. See test circuit $V_I$ = 2$V_{CC}$ for $T_{PZL}$, $V_I$ = 0V for $t_{PZH}$ | $V_{CC}$= 1.65V to 1.95V | $T_A$ = 25°C | 7 | | 23 | |
| | | | $V_{CC}$= 2.3V to 2.7V | | 3.5 | | 13 | |
| | | | $V_{CC}$= 3.0V to 3.6V | | 2.5 | | 6.9 | |
| | | | $V_{CC}$= 4.5V to 5.5V | | 1.7 | | 5.2 | |
| $t_{PZL}$ $t_{PZH}$ | Output Enable Turn ON TIME: Z TO Yn | See test circuit diagrams 1 and 2. $V_I$ = 2$V_{CC}$ for $T_{PZL}$, $V_I$ = 0V for $t_{PZH}$ | $V_{CC}$ = 2.5V | $T_A$ = 25°C & –40 to 85°C | | | 24 | |
| | | | $V_{CC}$ = 3.3V | | | | 14 | |
| | | | $V_{CC}$ = 3.0V to 3.6V | | | | 7.6 | |
| | | | $V_{CC}$ = 4.5V to 5.5V | | | | 5.7 | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $t_{PLZ}$ $t_{PHZ}$ | Output Disable Turn OFF Time: Z to Yn | See test circuit diagrams 1 and 2. $V_I = 2V_{CC}$ for $T_{PZL}$, $V_I = 0V$ for $t_{PZH}$ | $V_{CC}$ = 1.65V to 1.95V | $T_A$ = 25°C | 3 | | 12.5 | ns |
| | | | $V_{CC}$ = 2.3V to 2.7V | | 2 | | 7 | |
| | | | $V_{CC}$ = 3.0V to 3.6V | | 1.5 | | 5 | |
| | | | $V_{CC}$ = 4.5V to 5.5V | | 0.8 | | 3.5 | |
| $t_{PLZ}$ $t_{PHZ}$ | Output Disable Turn OFF Time: Z to Yn | See test circuit diagrams 1 and 2. $V_I = 2V_{CC}$ for $T_{PZL}$, $V_I = 0V$ for $t_{PZH}$ | $V_{CC}$ = 2.5V | $T_A$ = –40 to 85°C | | | 13 | |
| | | | $V_{CC}$ = 3.3V | | | | 7.5 | |
| | | | $V_{CC}$ = 3.0V to 3.6V | | | | 5.3 | |
| | | | $V_{CC}$ = 4.5V to 5.5V | | | | 3.8 | |
| $t_{BM}$ | Break Before Make Time | See test circuit diagram 9.(9) | $V_{CC}$ = 2.5V | $T_A$ = 25°C & –40 to 85°C | 0.5 | | | |
| | | | $V_{CC}$ = 3.3V | | 0.5 | | | |
| | | | $V_{CC}$ = 3.0V to 3.6V | | 0.5 | | | |
| | | | VCC = 4.5V to 5.5V | | 0.5 | | | |
| Q | Charge Injection | $C_L$ = 0.1nF, $V_{GEN}$ = 0V, $R_{GEN}$ = 0Ω. See test circuit 4. | $V_{CC}$ = 5.0V | $T_A$ = 25°C | | 7 | | pC |
| | | | VCC = 3.3V | | | 3 | | |
| OIRR | Off Isolation | $R_L$ = 50Ω, $V_{GEN}$ = 0V, $R_{GEN}$ = 0Ω. See test circuit 5. (11) | $V_{CC}$ = 1.65V to 5.5V | $T_A$ = 25°C | | –57 | | dB |
| $X_{TALK}$ | Crosstalk Isolation | See test circuit 6. | $V_{CC}$ = 1.65V to 5.5V | $T_A$ = 25°C | | –54 | | |
| $f_{3dB}$ | –3dB Bandwidth | See test circuit 9 | $V_{CC}$ = 1.65V to 5.5V | $T_A$ = 25°C | | 300 | | MHz |

Note 9: Guaranteed by design
Note 10: Guaranteed by design but not production tested. The device contributes no other propagation delay other than the RC delay of the switch ON resistance and the 50pF load capacitance, when driven by an ideal voltage source with zero output impedance.
Note 11: Off Isolation = 20 Log10 [ $V_Z$ / $V_{Yn}$ ] and is measured in dB.
Note 12: TA = 25°C, f = 1MHz. Capacitance is characterized but not tested in production.

## TEST CIRCUITS AND TIMING DIAGRAMS

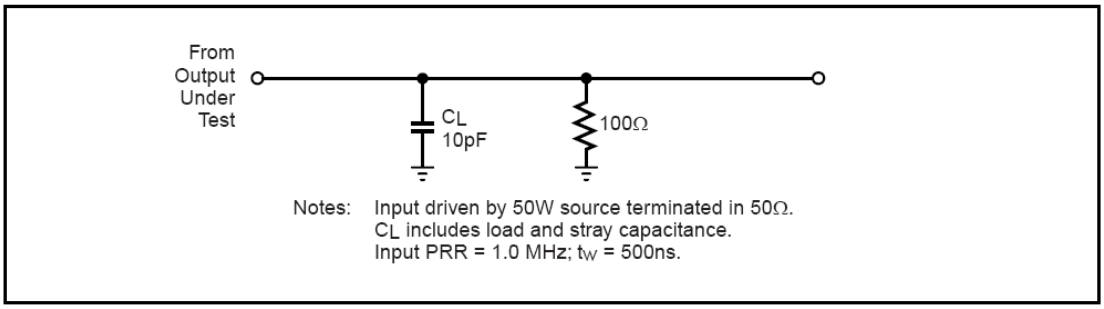



Figure 1. AC Test Circuit

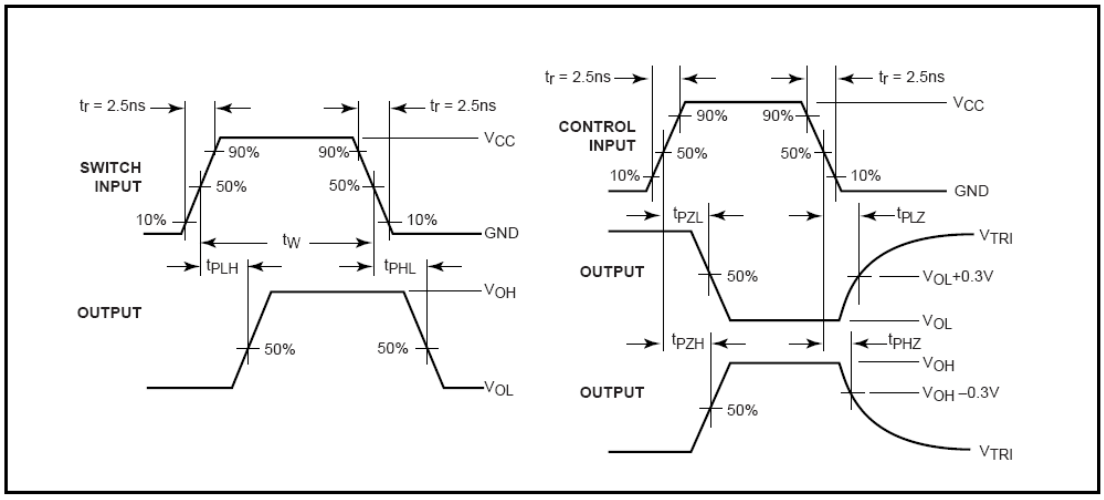



Figure 2. AC Waveforms

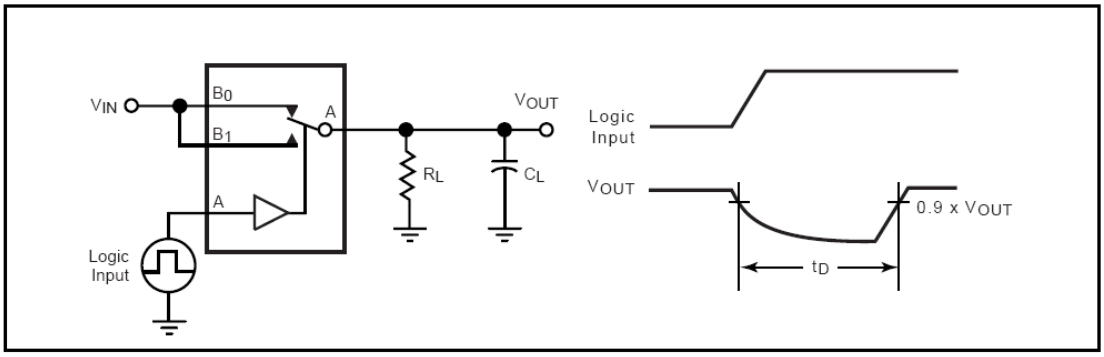



Figure 3. Break Before Make Interval Timing

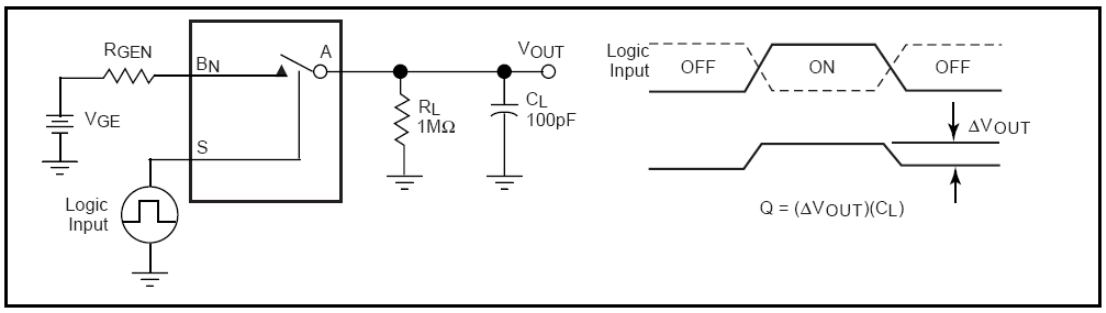



Figure 4. Charge Injection Test

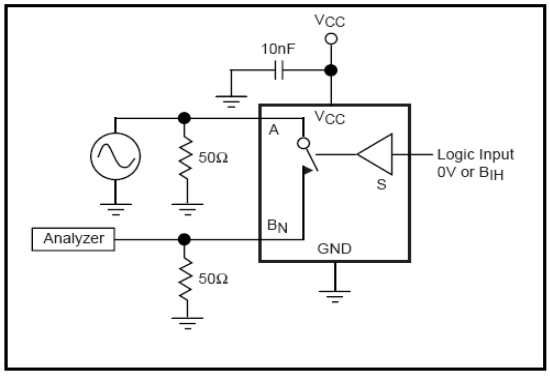



Figure 5. Off Isolation

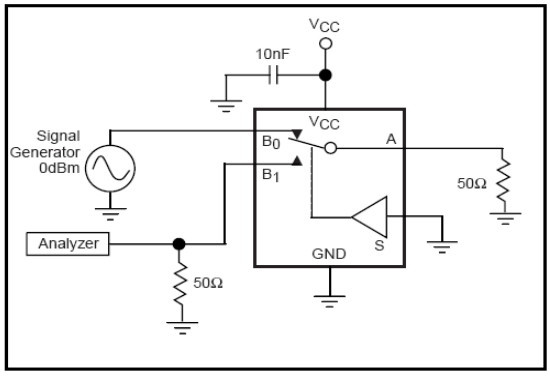



Figure 6. Crosstalk

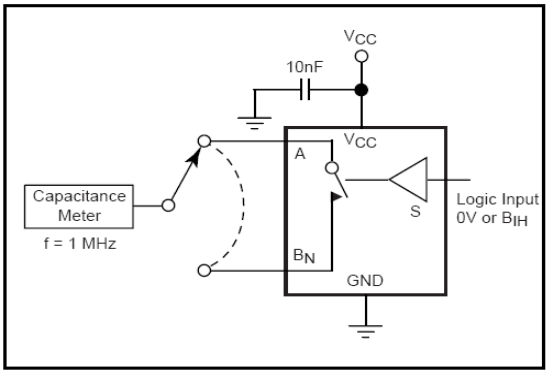



Figure 7. Channel Off Capacitance

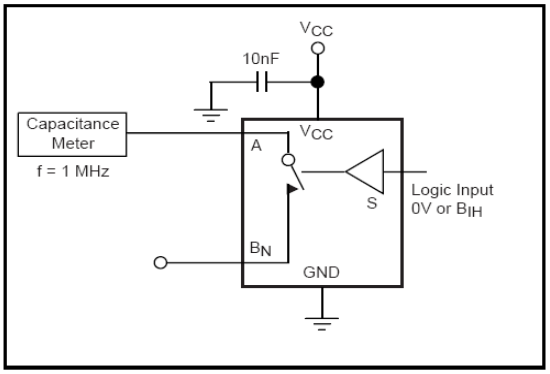



Figure 8. Channel On Capacitance

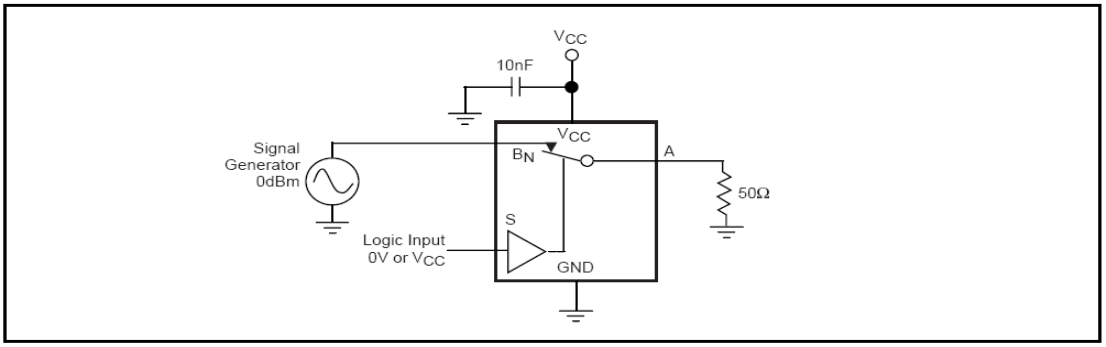
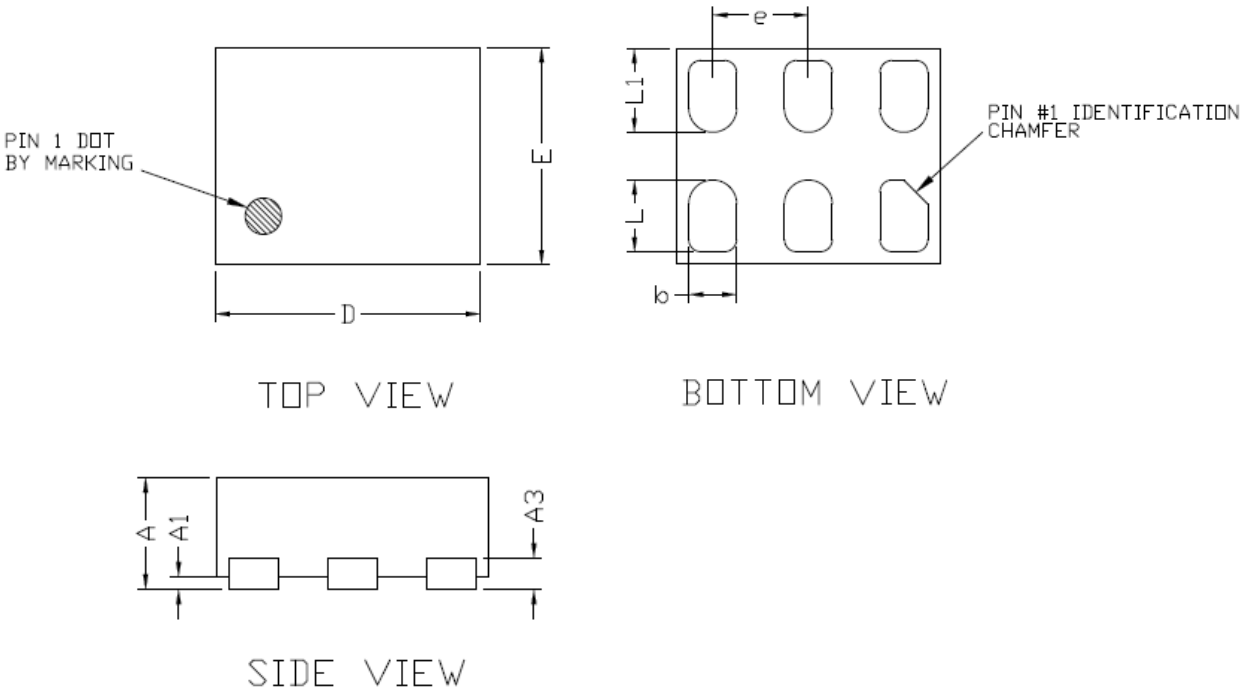


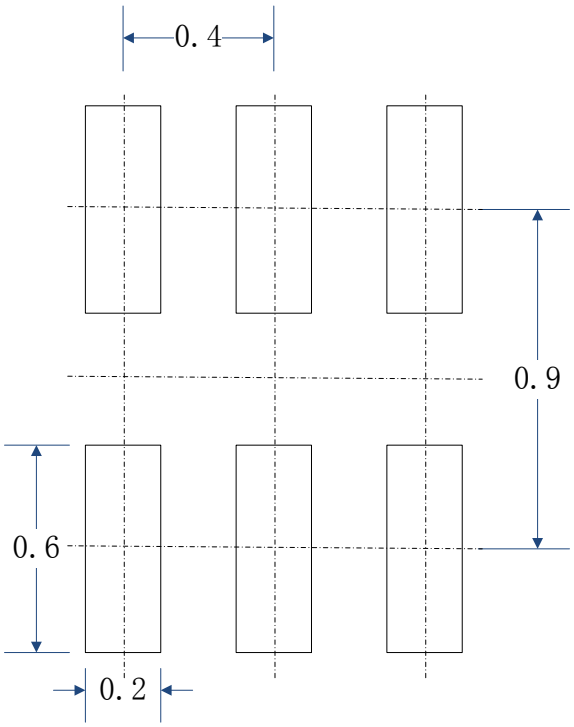

Figure 9. Bandwidth

## DFN1.1x0.9-6L PACKAGE OUTLINE DIMENSIONS




| Symbol | Dimensions In Millimeters(mm) | | |
|---|---|---|---|
| | Min | NOM | Max |
| A | 0.4 | | 0.5 |
| A1 | 0 | | 0.05 |
| A3 | 0.125 REF | | |
| D | 1.05 | 1.10 | 1.15 |
| E | 0.85 | 0.90 | 0.95 |
| b | 0.15 | 0.20 | 0.25 |
| L | 0.25 | 0.30 | 0.35 |
| L1 | 0.30 | 0.35 | 0.40 |
| e | 0.40 BSC | | |

**PCB Layout Pattern: DFN1.1x0.9-6L**




**RECOMMENDED PCB LAYOUT PATTERN** (Unit: mm)