General Description

The BCT72328S is a LED Display Driver and Key Scan with 8-steps digital dimming control. Ten segment output lines, seven grid output lines, one display memory (14 bytes), control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to BCT72328S via a four-line serial interface (DIN, STB, CLK and DOUT).

Differences with respect to uPD16312 VFD Driver

- No LED Ports supported
- No GPIO's supported
- Less Segments and Grids output lines
- No negative and 3.3V voltage supply required

Features

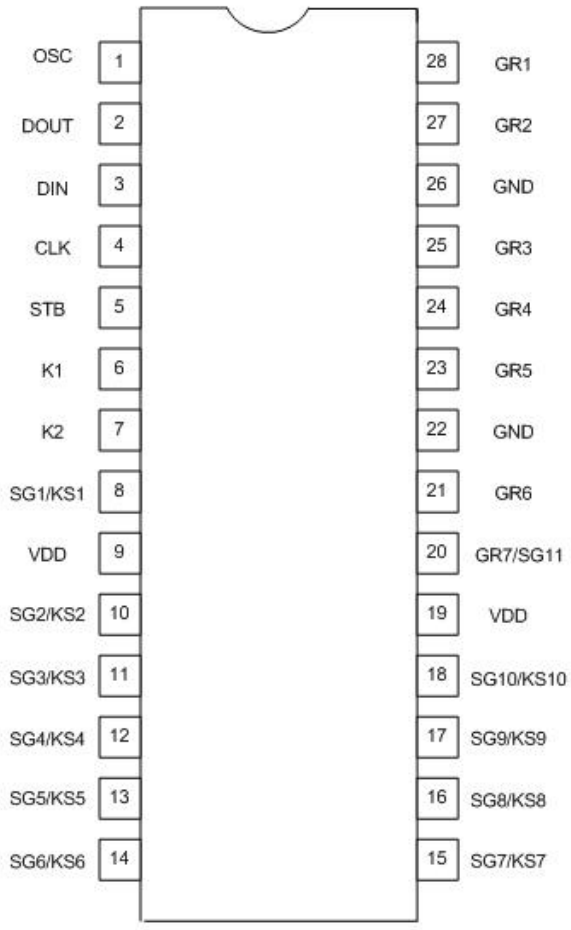
- CMOS Technology
- Low Power Consumption
- Key Scanning (10 x 2 matrix)
- Multiple Display Modes: 11 segments, 6 digits to 10 segments, 7 digits
- 8-Steps Dimming Circuitry
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors Needed for Driver Outputs
- Available in Pb-free SOP28 package or die

Applications

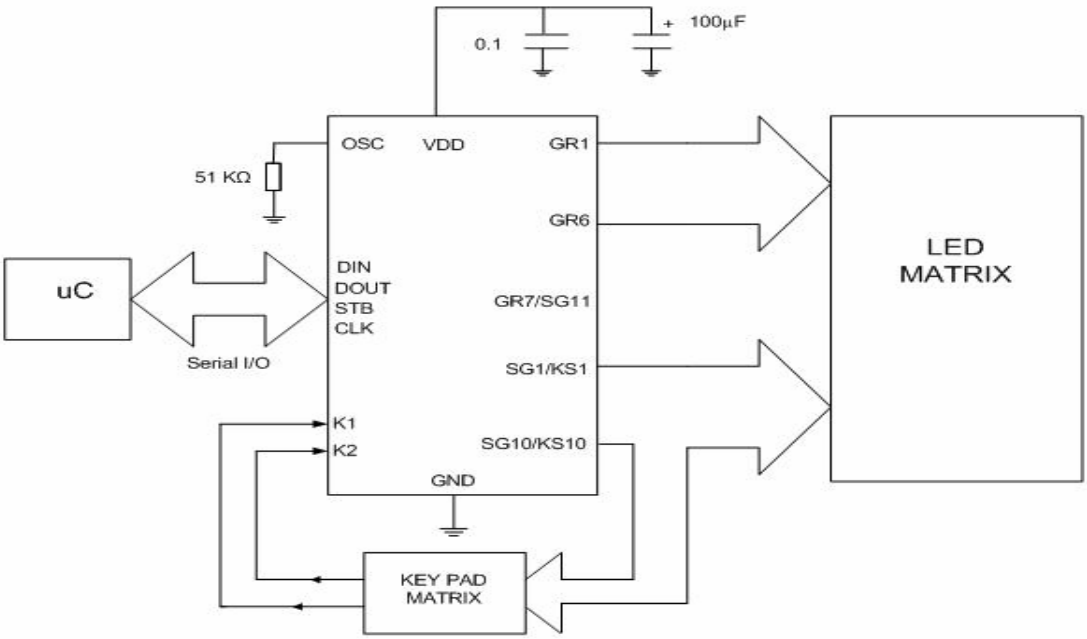
- Front Panel Display for DVD Player and VCD player
- Boom-box system and Electrical Appliance

Package

SOIC 28L Package
(300 mil)



Typical Application Circuit



Block Diagram

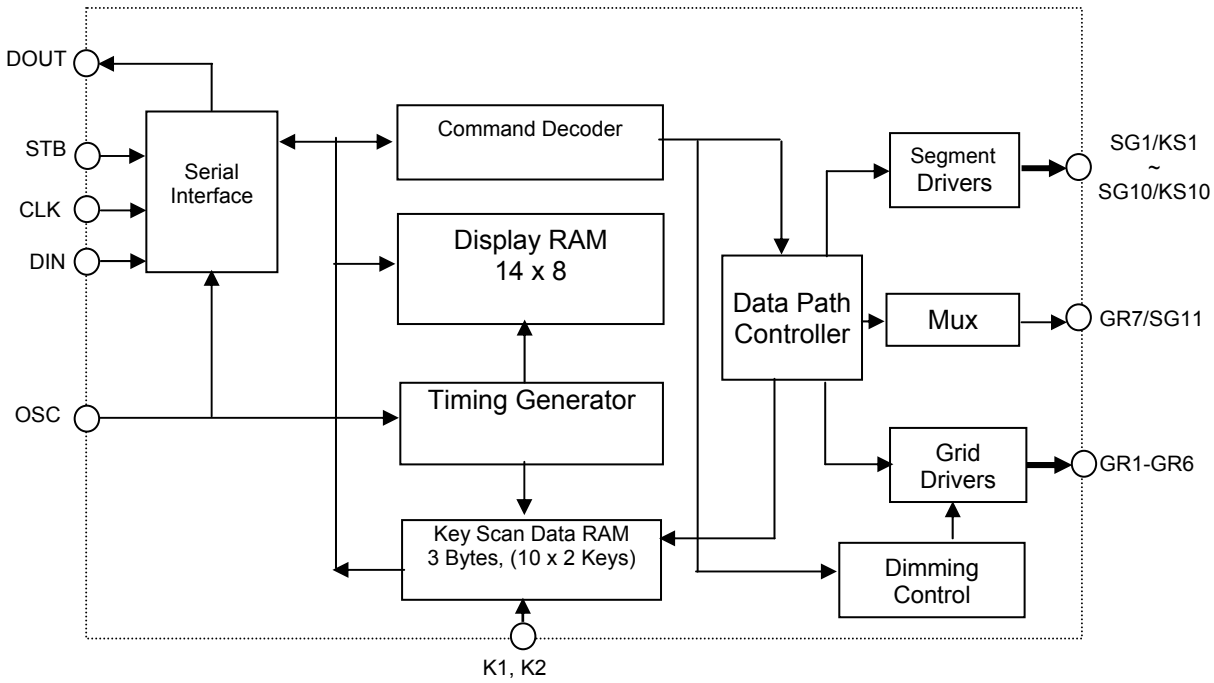


Figure 1: BCT72328S Block Diagram

Pin Descriptions

Pin Number	Pin Name	In/Out	Description
2	DOUT	Output	Output serial data at the falling edge of the shift clock, starting from low order bit. This is an NMOS open-drain output pin.
5	STB	Input	Data input after STB has gone low is processed as a command, while command data is processed, current processing is stopped. When STB is high, CLK is ignored.
4	CLK	Input	Reads serial data at the rising edge and outputs data at the falling edge.
3	DIN	Input	Input serial data at the rising edge of the shift clock, starting from the low order bit.
1	OSC	Input	Connected to an external resistor or an RC oscillator circuit.
28,27,25, 24,23,21	GR1/GR6	Output	Grid Driver Output pins NMOS Open-Drain and Pull Up Outputs.
8,10,11, 12,13,14, 15,16,17,18	SG1/SG10 ~ KS1/KS10	Output	Segment or key source output pins (dual function). PMOS Open-Drain and Pull Down Outputs.
20	GR7/SG11	Output	Segment or Grid Driver Output (Selectable for segment or grid driving based on display setting). NMOS Open-Drain and Pull Up output.
6,7	K1,K2	Input	Keying data input to these pins is latched at the end of the display cycle. Internal pulldown resistor
9,19	VDD	Input	Supply Voltage
22,26	GND	Input	Ground

Functional Description

The static display RAM is organized into 14 x 8 bits and stores the data transmitted from an external device to the BCT72328S through a serial interface. The contents of the RAM are transposed mapping to the matrix of the LED panel. Data in the RAM can be accessed through the data setting, address setting and display control commands. It is assigned addresses in 8-bit unit as follows:

Address	SEG8-SEG1(b7-b0)		SEG11-SEG9 (b2-b0)		Address
	b7-b4	b3-b0	b7-b4 =0000	b3=0,b2-b0	
00	00H	00L	Reserved, set to 0	01L	01
02	02H	02L		03L	03
04	04H	04L		05L	05
06	06H	06L		07L	07
08	08H	08L		09L	09
0A	0AH	0AL		0BL	0B
0C	0CH	0BL		0DL	0D

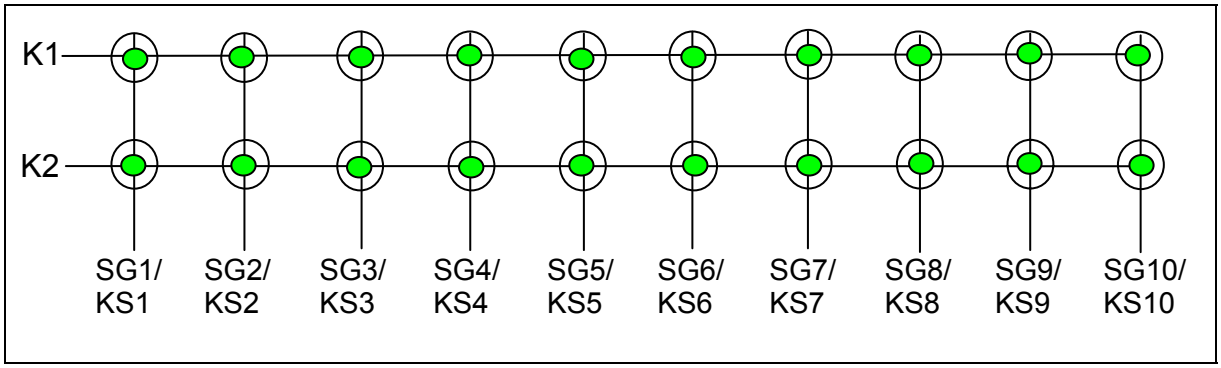
Note: Only the lower 3 bits of the addresses assigned to SEG9-11 are valid, and the higher 5 bits are ignored.

Dimming control

BCT72328S provides 8-step dimmer function on display by controlling the 3-bit binary command code. The full pulse width of grid signal is divides into 16 uniform sections by PWM (Pulse Width Modulation) technology. The 16 uniform sections available form 8 steps dimmer via 3-bit binary code. The 8-step dimmer includes 1/16, 2/16, 4/16, 10/16, 11/16, 12/16, 13/16 and 14/16. The 1/16 pulse width indicates minimum brightness. The 14/16 pulse width represents maximum brightness (Refer to the display control command).

Key matrix and key scan data RAM

The key matrix scans the series key states at each level of the key strobe signal (SG1/KS1~SG10/KS10) output of the BCT72328S. The key strobe signal outputs are time-multiplexed signals from SG1/KS1~SG10/KS10. The states of inputs K1~K2 are sampled by strobe signal and latched SG1/KS1~SG10/KS10 into the registers.



The data of each key is stored in key scan data RAM as illustrated below, and is read with the read command, starting from the least significant bit. This chip does not have any built-in key debounce function; the key debounce operation is performed by user software. The key scan data RAM is re-new at the end of two successive frames as shown in Figure 5.

Reading Sequence

K1 - K2	K1 - K2	K1 - K2	K1 - K2
SG1/KS1	SG2/KS2	SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6	SG7/KS7	SG8/KS8
SG9/KS9	SG10/KS10	00	00
b0 - b1	**b2 - b3**	**b4 - b5**	**b6 - b7**

Commands

Commands set the display mode and status of the LED driver. The first 1 byte input to the BCT72328S through the DIN pin after the STB pin has fallen, is regarded as a command. If STB goes high while commands/data are transmitted, this commands/data being transmitted are not valid and the serial communication link will re-initialized (however, the commands/data previously transmitted remains valid).

1. Display mode setting commands (Command 1)

These commands initialize the BCT72328S and select the number of segments and the number of grids (1/8~1/16 duty, 10 segments to 11 segments). When these commands are executed, the display is forcibly turned off, and key scanning is also stopped. To resume display, the display command “ON” must be executed. If the same mode is selected, nothing happens.

b7	b6	b5	b4	b3	b2	b1	b0
0	0	-	-	-	-	DS1	DS0

DS1	DS0	Display Mode (Segment x Grid)
0	0	8 x 7
0	1	9 x 7 (Default)
1	0	10 x 7
1	1	11 x 6

Default setting: 00xxxx01b = 9 Segments by 7 Grids

2. Data Setting Commands (Command 2)

These commands set the data write and data read modes as shown below

b7	b6	b5	b4	b3	b2	b1	b0
0	1	PANEL	-	NT	ADMODE	WR1	WR0

WR1	WR0	Data Write & Read Mode
0	0	Write to Display RAM
0	1	Reserved
1	0	Read Key Data
1	1	Reserved

ADMODE	Address Increment Mode Settings (Display Memory)
0	Increments address after data has been written
1	Fixes Address

NT	Test Mode Settings
0	Normal Mode
1	Test Mode

PANEL	Display Panel Type
0	Common Anode
1	Common Cathode

Default setting: 0100000b = Write mode, Address increment mode is set, Normal mode operation, Common Anode type LED panel is selected.

3. Address Setting commands (Command 3)

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of “00H” to “0DH”. If the address is set to “0EH” or higher, the data is ignored until a valid address is set.

b7	b6	b5	b4	b3	b2	b1	b0
1	1	-	-	ADR3	ADR2	ADR1	ADR0

Address 00h to 0Dh (used)

Default setting: 11xx0000b = address is set at “00H”

4. Display control commands (Command 4)

This command is used to turn ON or OFF the display panel. It is also used to set the pulse width for dimming function. A total of 8 steps of dimming can be programmed through b2 to b0. The 1/16 pulse width indicates minimum brightness. The 14/16 pulse width represents maximum brightness.

b7	b6	b5	b4	b3	b2	b1	b0
1	0	-	-	DISP_ON_OFF	DIM2	DIM1	DIM0

DIM2	DIM1	DIM0	Set Dimming Quantity
0	0	0	1/16 pulse width
0	0	1	2/16 pulse width
0	1	0	4/16 pulse width
0	1	1	10/16 pulse width
1	0	0	11/16 pulse width
1	0	1	12/16 pulse width
1	1	0	13/16 pulse width
1	1	1	14/16 pulse width

DISP_ON_OFF	Turns Display on/off
0	Display Off (Key Scan continues)
1	Display ON

Default setting: 10xx0000b = 1/16 pulse width is set and the display is turned off, key scanning is stopped.

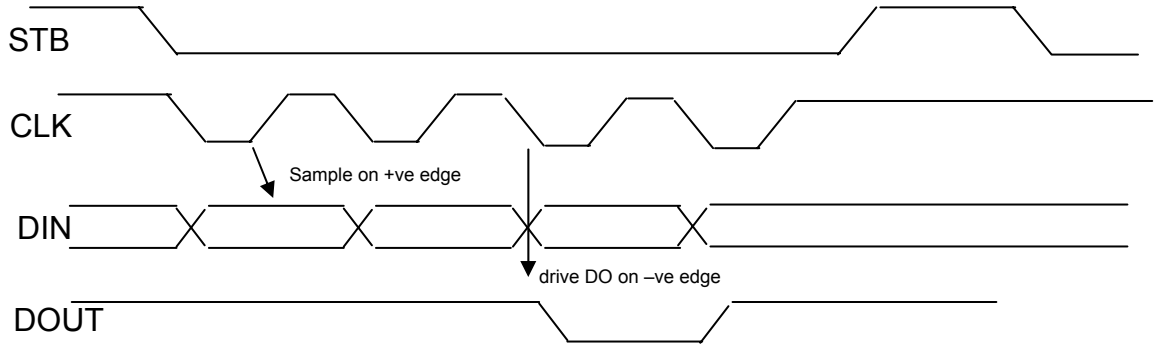
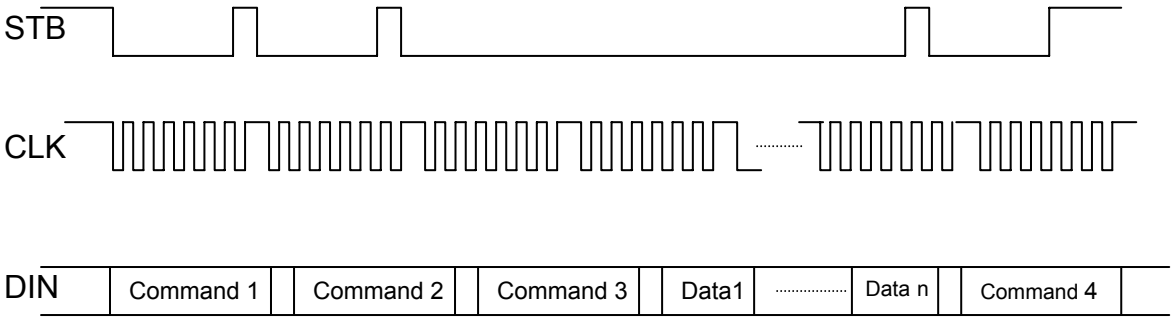
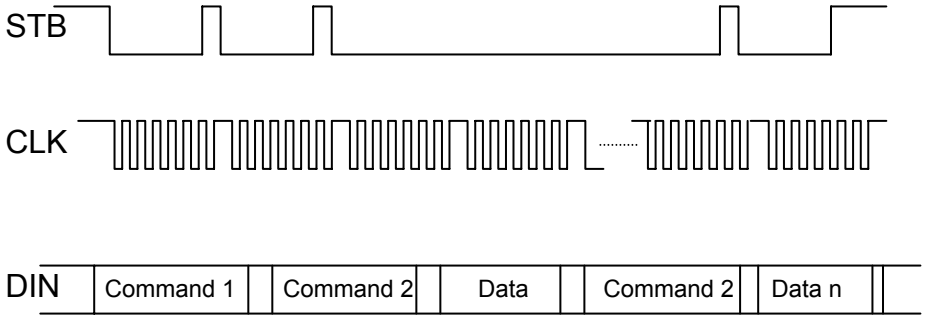


Figure 2. Serial Communication Format



Note: Command 1: sets display mode, Command 2: sets data,
Command 3: sets address
Data1 to n: transfer display data (14 bytes max)
Command 4: controls display

Figure 3. Updating display memory by incrementing address



Note: Command 1: sets data, Command 2: sets address, Data: display data

Figure 4. Updating specific addresses

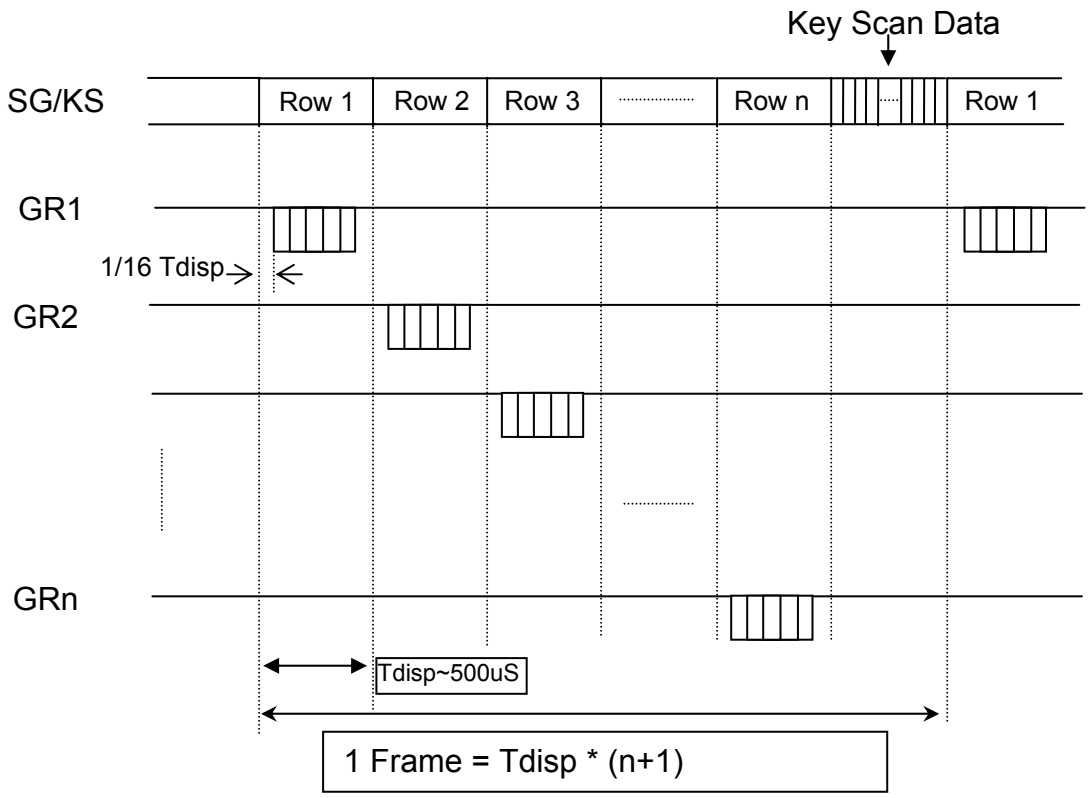


Figure 5. Key Scanning & Display Timing

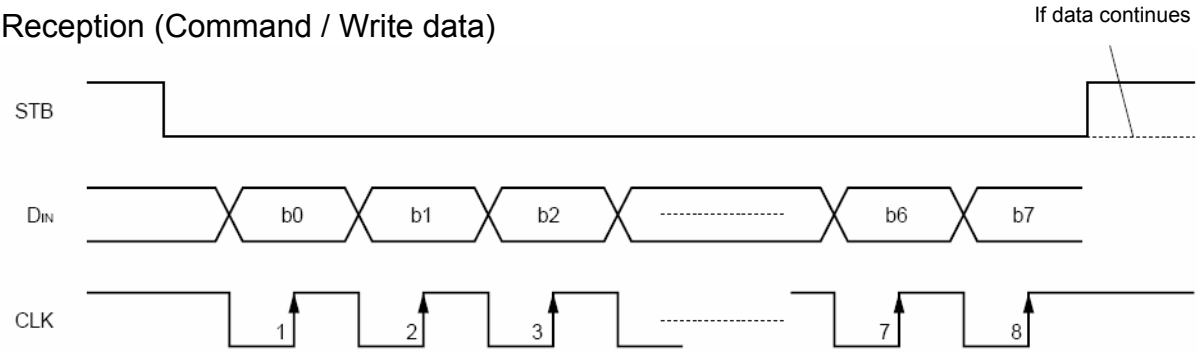
Each Display section is comprised of 16 sub-sections which has duration of 1/16 Tdisp. The Key section is also Tdisp wide (the 6 out of 16 sections are ignored during key scan but the display timing is kept similar to the Display/Grid drive compatibility)

When DISP_ON_OFF is 0, i.e. Display is OFF, the Frame timing is still the same during which time the GR lines are driven high.

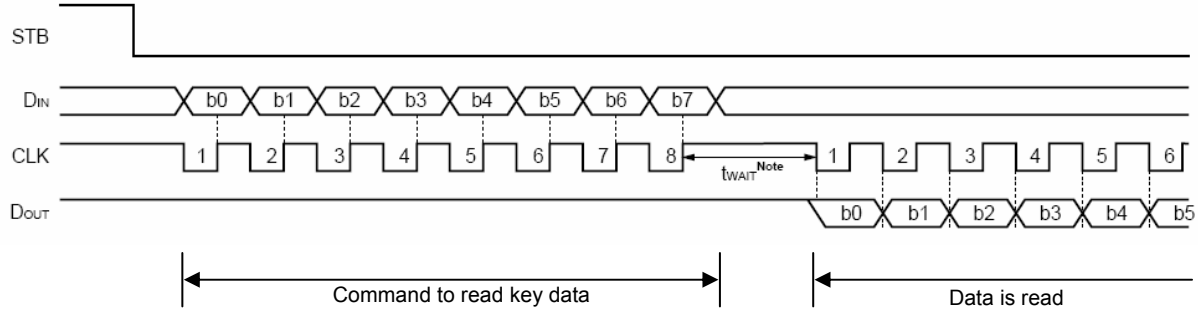
Note: To turn any segment ON, segment is driven high while the grid is pulled low.

Serial Communication

Reception (Command / Write data)



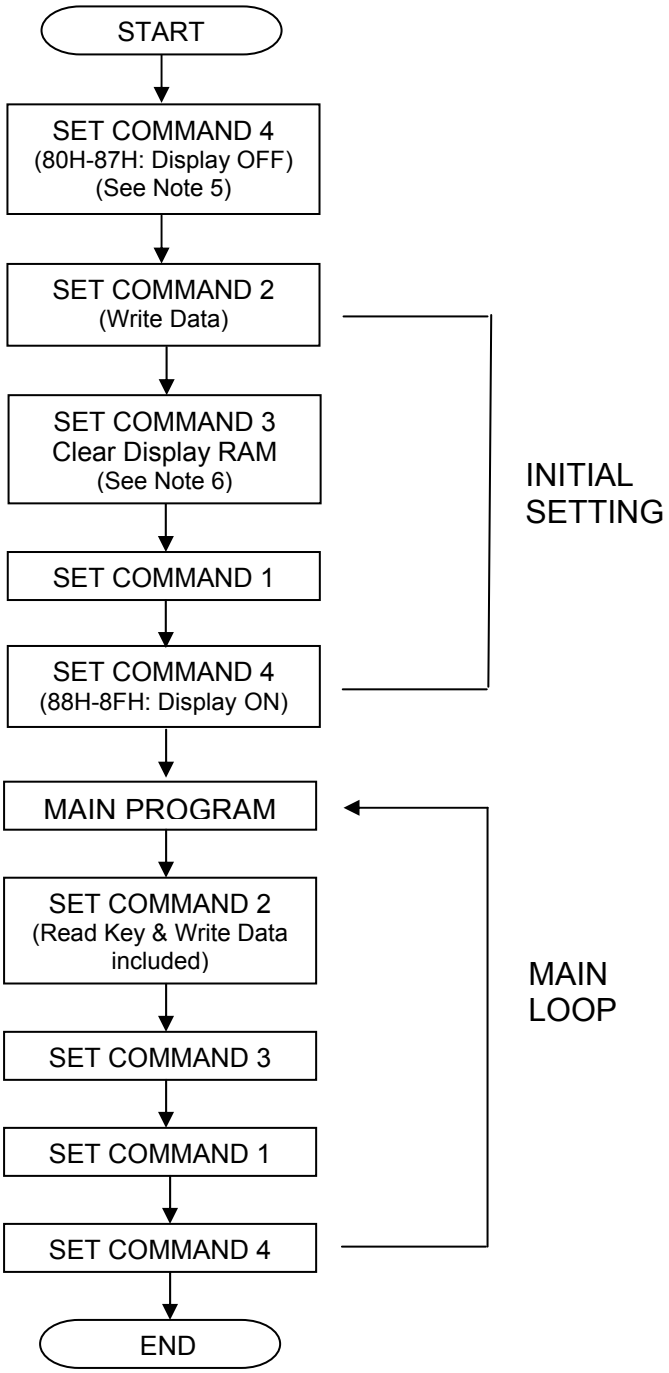
Transmission (Read data)



Because the DOUT pin is an NMOS open-drain output pin, be sure to connect an external pull-up resistor to this pin (1 kΩ to 10 kΩ).

Note: The data should read immediately after the read key data command, while data is read, a wait time tWAIT of 1 μS is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

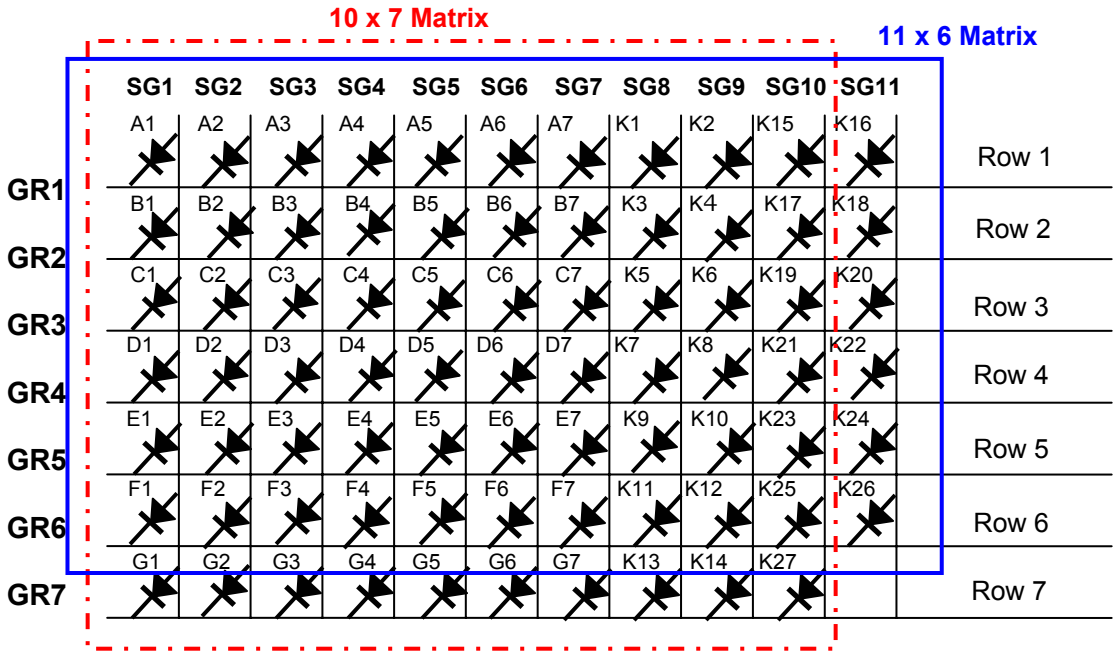
RECOMMENDED SOFTWARE FLOWCHART



NOTE:

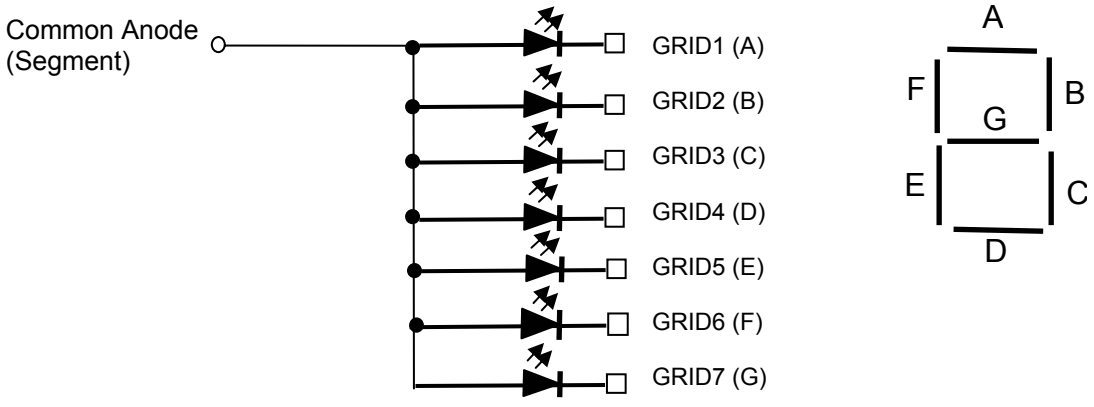
1) Command 1: Display Mode Commands
2) Command 2: Data Setting Commands
3) Command 3: Address Setting Commands
4) Command 4: Display Control Commands
5) When IC power is applied for the first time, the display is turned off; but it is advisable to keep the display OFF when modifying the Display RAM.
6) When IC power is applied for the first time, the contents of the Display RAM are not defined; thus it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

Possible LED Matrix (Common Anode) layout example



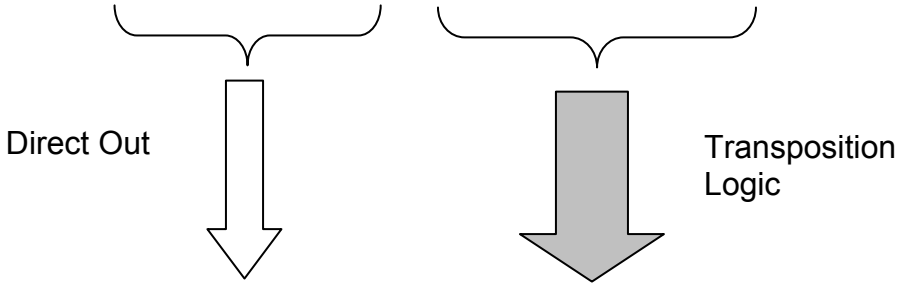
Possible Display Modes:

b1	b0	Display mode Segments x Grids
0	0	8 x 7
0	1	9 x 7 (default mode)
1	0	10 x 7
1	1	11 x 6



Display Memory Mapping (if common anode panel is used)

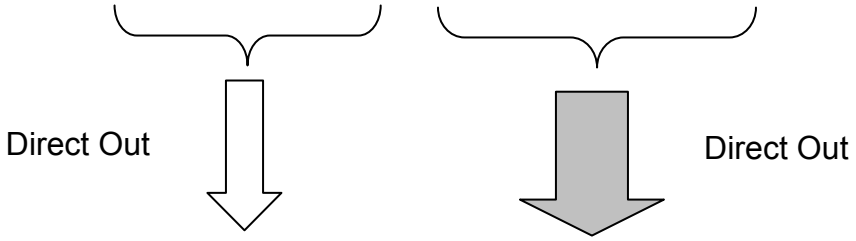
Odd Address	b7…..b3	b2 b1 b0	b7	b6 b5 b4 b3 b2 b1 b0	Even address
01	00000	K16 K15 K2	K1	G1 F1 E1 D1 C1 B1 A1	00
03	00000	K18 K17 K4	K3	G2 F2 E2 D2 C2 B2 A2	02
05	00000	K20 K19 K6	K5	G3 F3 E3 D3 C3 B3 A3	04
07	00000	K22 K21 K8	K7	G4 F4 E4 D4 C4 B4 A4	06
09	00000	K24 K23 K10	K9	G5 F5 E5 D5 C5 B5 A5	08
0B	00000	K26 K25 K12	K11	G6 F6 E6 D6 C6 B6 A6	0A
0D	00000	-- K27 K14	K13	G7 F7 E7 D7 C7 B7 A7	0C



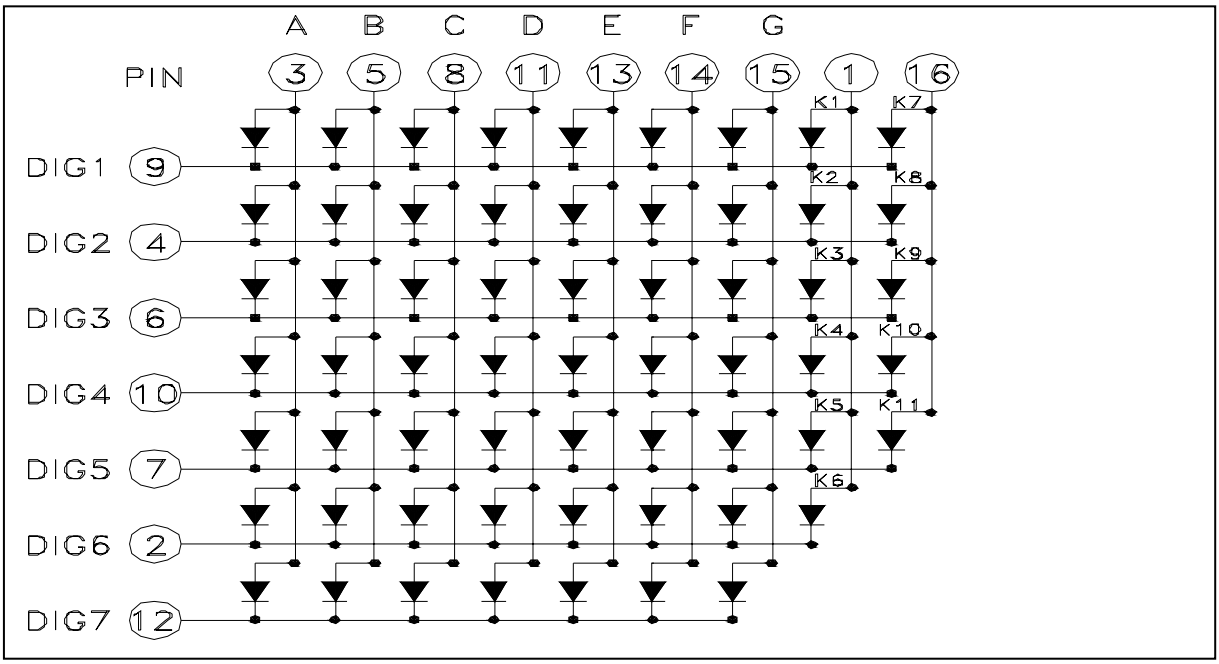
	Segments Out		Output Sequence
Grid Out	SG11 SG10 SG9 SG8	SG7 SG6 SG5 SG4 SG3 SG2 SG1	
GR1	K16 K15 K2 K1	A7 A6 A5 A4 A3 A2 A1	
GR2	K18 K17 K4 K3	B7 B6 B5 B4 B3 B2 B1	
GR3	K20 K19 K6 K5	C7 C6 C5 C4 C3 C2 C1	
GR4	K22 K21 K8 K7	D7 D6 D5 D4 D3 D2 D1	
GR5	K24 K23 K10 K9	E7 E6 E5 E4 E3 E2 E1	
GR6	K26 K25 K12 K11	F7 F6 F5 F4 F3 F2 F1	
GR7	-- K27 K14 K13	G7 G6 G5 G4 G3 G2 G1	

Display Memory Mapping (if common cathode panel is used)

Odd Address	b7.....b3	b2 b1 b0	b7	b6 b5 b4 b3 b2 b1 b0	Even address
01	00000	K16 K15 K2	K1	G1 F1 E1 D1 C1 B1 A1	00
03	00000	K18 K17 K4	K3	G2 F2 E2 D2 C2 B2 A2	02
05	00000	K20 K19 K6	K5	G3 F3 E3 D3 C3 B3 A3	04
07	00000	K22 K21 K8	K7	G4 F4 E4 D4 C4 B4 A4	06
09	00000	K24 K23 K10	K9	G5 F5 E5 D5 C5 B5 A5	08
0B	00000	K26 K25 K12	K11	G6 F6 E6 D6 C6 B6 A6	0A
0D	00000	-- K27 K14	K13	G7 F7 E7 D7 C7 B7 A7	0C

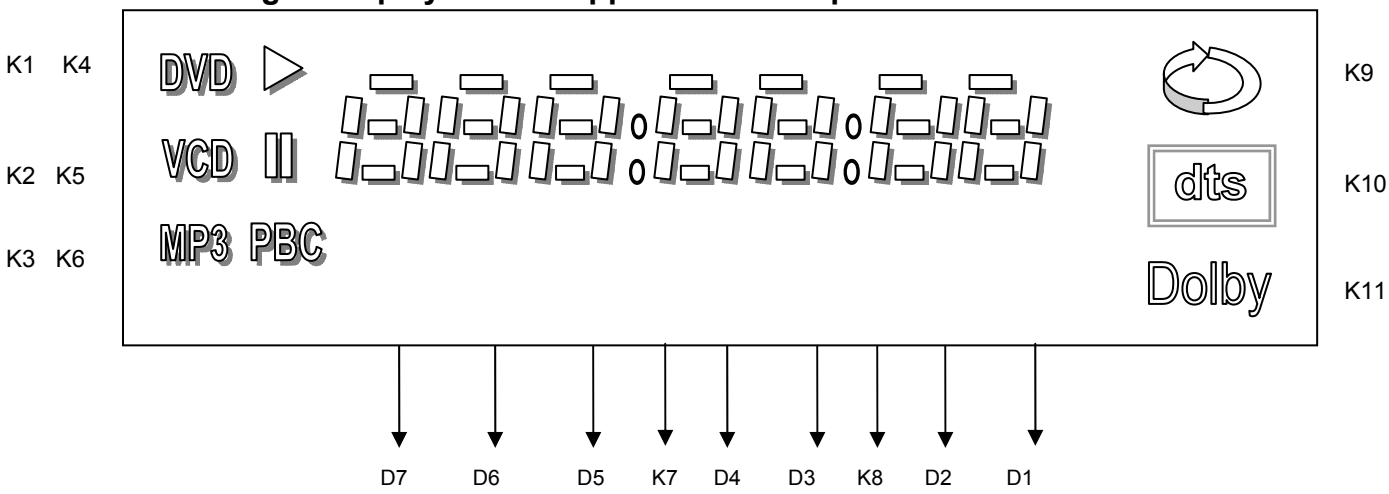


	Segments Out														Output Sequence
Grid Out	SG11		SG10		SG9		SG8		SG7	SG6	SG5	SG4	SG3	SG2	SG1	
GR1	K16		K15		K2		K1		G1	F1	E1	D1	C1	B1	A1	
GR2	K18		K17		K4		K3		G2	F2	E2	D2	C2	B2	A2	
GR3	K20		K19		K6		K5		G3	F3	E3	D3	C3	B3	A3	
GR4	K22		K21		K8		K7		G4	F4	E4	D4	C4	B4	A4	
GR5	K24		K23		K10		K9		G5	F5	E5	D5	C5	B5	A5	
GR6	K26		K25		K12		K11		G6	F6	E6	D6	C6	B6	A6	
GR7	--		K27		K14		K13		G7	F7	E7	D7	C7	B7	A7	



Application Example 1

Seven Digits Display Module application example:



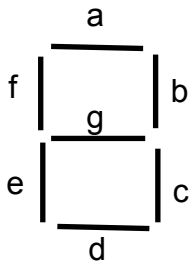
Common Anode Type

Operation Code	Digits Display	Icon Display	Key Press
	D7……D3……D1	Normal - OFF	
Open Door	xxO PE Nx		Open/Close
Close Door	xxC LO SE		Open/Close
Disc IN	xxx di SC		
No Disc	NOx di SC		
DVD Disc	xxd Vd xx	K1	
VCD Disc	xxV cd xx	K2, K6	
CD Disc	xxx cd xx	K3 if MP3 Disc	
Repeat		K9	Repeat Key (A-B)
DTS audio out		K10	
Dolby audio out		K11	
Track/ Time elapsed	### ## ##	K7, K8	TT h : mm : ss
Reading Disc	xxx LO Ad		
Title	xxt it LE		
Root	xxx rO Ot		
Stop	xxx St OP		STOP key
Playing disc	### ## ## (run time)	K4, K7, K8	PLAY key
Pause	### ## ## (frozen)	K5, K7, K8	PAUSE key

Note : xx – no display
- 0~9 digits

Seven segments digit coding table

Segment	a	b	c	d	e	f	g	Hex Byte
Numeric	**b0**	**b1**	**b2**	**b3**	**b4**	**b5**	**b6**	
0	1	1	1	1	1	1	0	3F
1	0	1	1	0	0	0	0	06
2	1	1	0	1	1	0	1	5B
3	1	1	1	1	0	0	1	4F
4	0	1	1	0	0	1	1	66
5	1	0	1	1	0	1	1	6D
6	1	0	1	1	1	1	1	7D
7	1	1	1	0	0	0	0	07
8	1	1	1	1	1	1	1	7F
9	1	1	1	1	0	1	1	6F
Character								
A	1	1	1	0	1	1	1	77
C	1	0	0	1	1	1	0	39
E	1	0	0	1	1	1	1	79
L	0	0	0	1	1	1	0	38
N	1	1	1	0	1	1	0	37
O	1	1	1	1	1	1	0	3F
P	1	1	0	0	1	1	1	73
S	1	0	1	1	0	1	1	6D
V	0	1	1	1	1	1	0	3E
c	0	0	0	1	1	0	1	58
d	0	1	1	1	1	0	1	5E
i	0	0	0	0	1	0	0	10
r	0	0	0	0	1	0	1	50
t	0	0	0	1	1	1	1	78

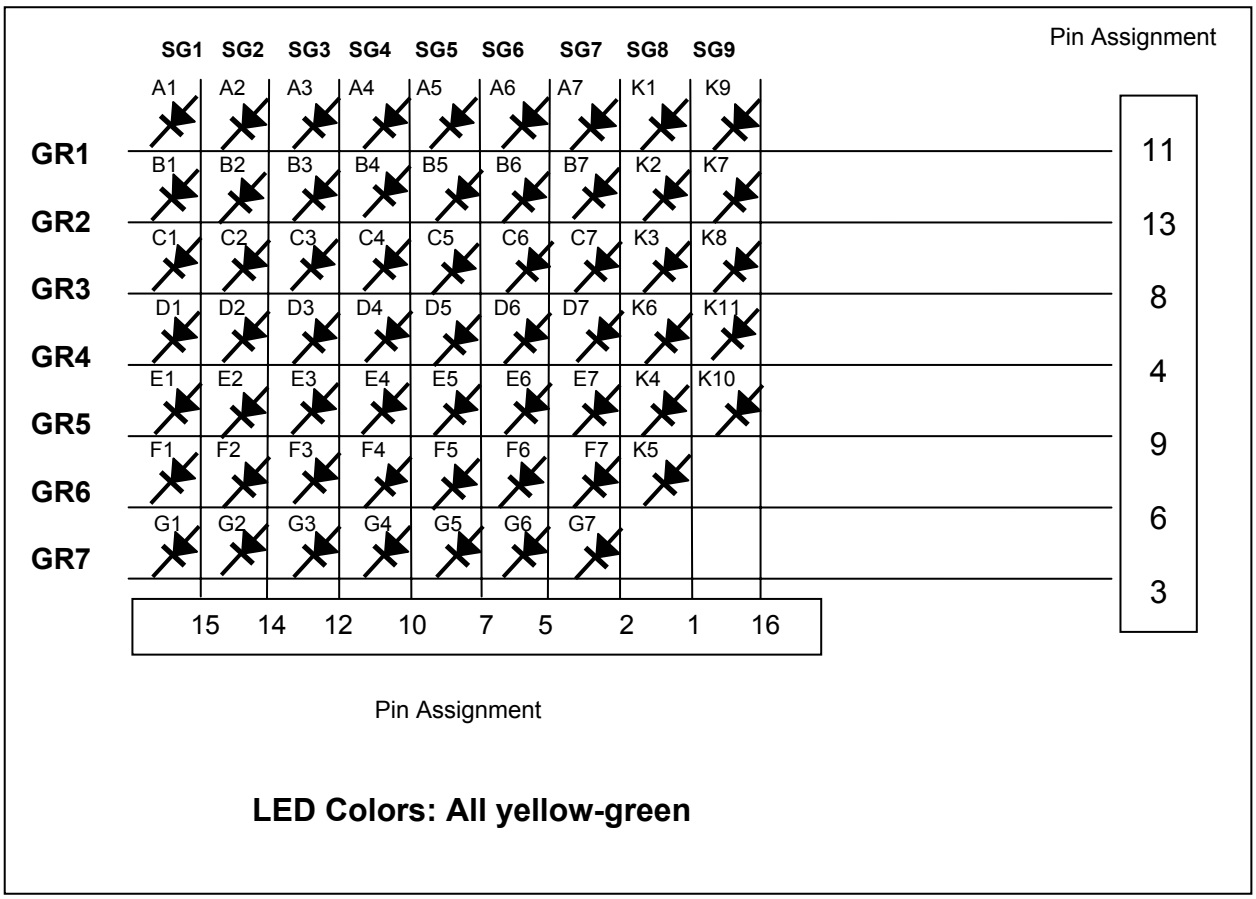


Memory location table (Display mode – 9 x 7 mode)

Odd Address	b7…..b3	b2 b1 b0	b7	b6 b5 b4 b3 b2 b1 b0	Even Address
01	00000	X X K9	K1	G1 F1 E1 D1 C1 B1 A1	00
03	00000	X X K7	K2	G2 F2 E2 D2 C2 B2 A2	02
05	00000	X X K8	K3	G3 F3 E3 D3 C3 B3 A3	04
07	00000	X X K11	K6	G4 F4 E4 D4 C4 B4 A4	06
09	00000	X X K10	K4	G5 F5 E5 D5 C5 B5 A5	08
0B	00000	X X X	K5	G6 F6 E6 D6 C6 B6 A6	0A
0D	00000	-- X X	X	G7 F7 E7 D7 C7 B7 A7	0C

X : Don't care

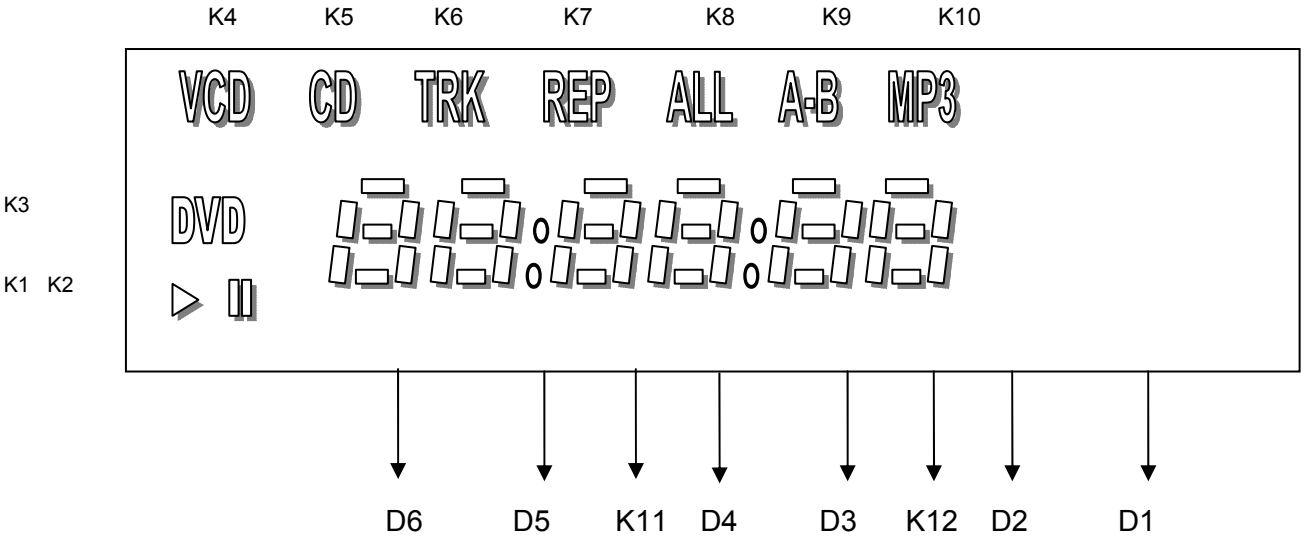
Display Module LED Matrix configuration



LED Colors: All yellow-green

Application Example 2

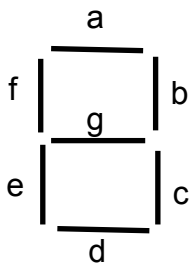
Six Digits Display Module application example



Operation Code	Digits Display	Icon Display	Key Press
	D6……D3……D1	Normal - OFF	
Open Door	xx OP EN		Open/Close
Close Door	xC LO SE		Open/Close
Disc IN	xx di SC		
No Disc	NO di SC		
DVD Disc	xd Vd xx	K3	
VCD Disc	xV cd xx	K4	
CD Disc	xx cd xx	K5, K10 if MP3 Disc	
Repeat		K7	
Track No.	##	K6	
Time Elapsed	## ## ##	K11, K12	hh : mm : ss
Repeat All	## ## ##	K7, K8, K11, K12	hh : mm : ss
Reading Disc	xx LO Ad		
Title	xt it LE		
Root	xx rO Ot		
Stop	xx St OP		STOP key
Playing disc	## ## ## (run time)	K2, K11, K12	PLAY key
Pause	## ## ## (frozen)	K4, K11, K12	PAUSE key

Note : xx – no display
- 0~9 digits

Seven segments digit coding table



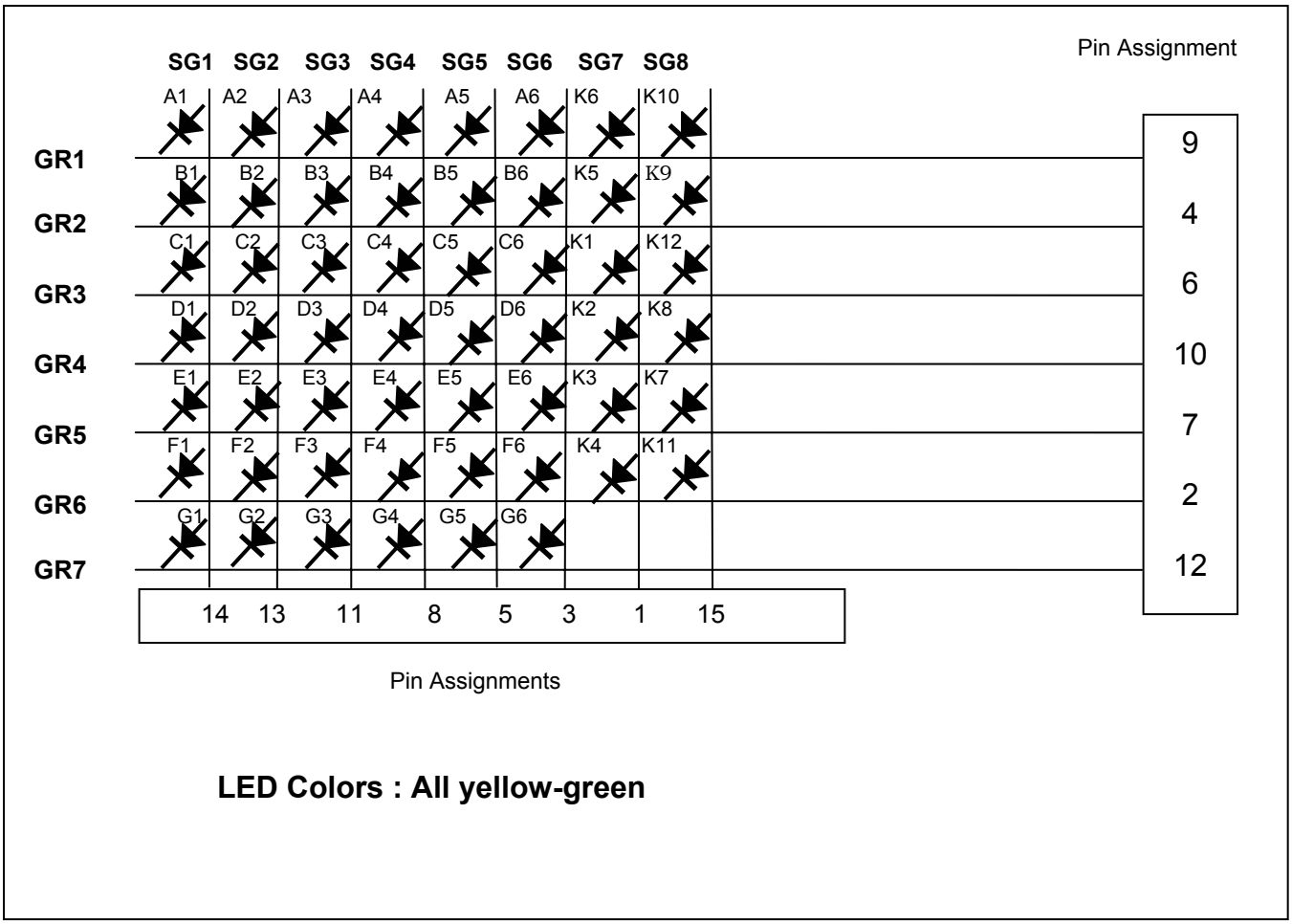
Segment	a	b	c	d	e	f	g	Hex Byte
Numeric	**b0**	**b1**	**b2**	**b3**	**b4**	**b5**	**b6**	
0	1	1	1	1	1	1	0	3F
1	0	1	1	0	0	0	0	06
2	1	1	0	1	1	0	1	5B
3	1	1	1	1	0	0	1	4F
4	0	1	1	0	0	1	1	66
5	1	0	1	1	0	1	1	6D
6	1	0	1	1	1	1	1	7D
7	1	1	1	0	0	0	0	07
8	1	1	1	1	1	1	1	7F
9	1	1	1	1	0	1	1	6F
Character								
A	1	1	1	0	1	1	1	77
C	1	0	0	1	1	1	0	39
E	1	0	0	1	1	1	1	79
L	0	0	0	1	1	1	0	38
N	1	1	1	0	1	1	0	37
O	1	1	1	1	1	1	0	3F
P	1	1	0	0	1	1	1	73
S	1	0	1	1	0	1	1	6D
V	0	1	1	1	1	1	0	3E
c	0	0	0	1	1	0	1	58
d	0	1	1	1	1	0	1	5E
i	0	0	0	0	1	0	0	10
r	0	0	0	0	1	0	1	50
t	0	0	0	1	1	1	1	78

Memory location table (Display mode – 8 x 7 mode)

Odd Address	b7…..b3	b2 b1 b0	b7	b6 b5 b4 b3 b2 b1 b0	Even Address
01	00000	X X K10	K6	G1 F1 E1 D1 C1 B1 A1	00
03	00000	X X K9	K5	G2 F2 E2 D2 C2 B2 A2	02
05	00000	X X K12	K1	G3 F3 E3 D3 C3 B3 A3	04
07	00000	X X K8	K2	G4 F4 E4 D4 C4 B4 A4	06
09	00000	X X K7	K3	G5 F5 E5 D5 C5 B5 A5	08
0B	00000	X X K11	K4	G6 F6 E6 D6 C6 B6 A6	0A

X : Don't care

Display Module LED Matrix configuration



LED Colors : All yellow-green

Absolute Maximum Specifications

Rating	Symbol	Value	Unit
Supply voltage range	V_{DD}	-0.3 to +6.0	Volts
Input voltage range	V_{IN}	-0.3 to Vcc+0.3	Volts
Output voltage range	V_{OUT}	-0.3 to VCC+0.3	Volts
Operating temperature range	T_{OPR}	0 to 70	^{o}C
Storage temperature range	T_{STR}	-20 to 100	^{o}C

Electrical Specifications

All electrical specifications are specified at $T_{AMBIENT}$ from 0 ^{O}C to 70 ^{O}C, V_{CC} from 4.5 volts to 5.5 volts, unless otherwise specified.

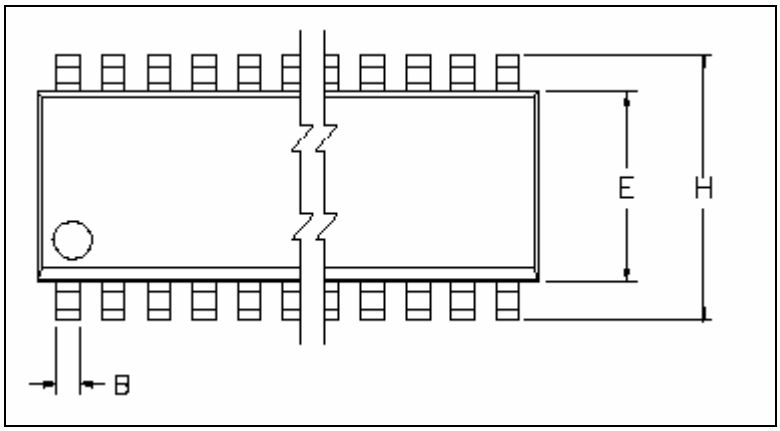
DC Specifications

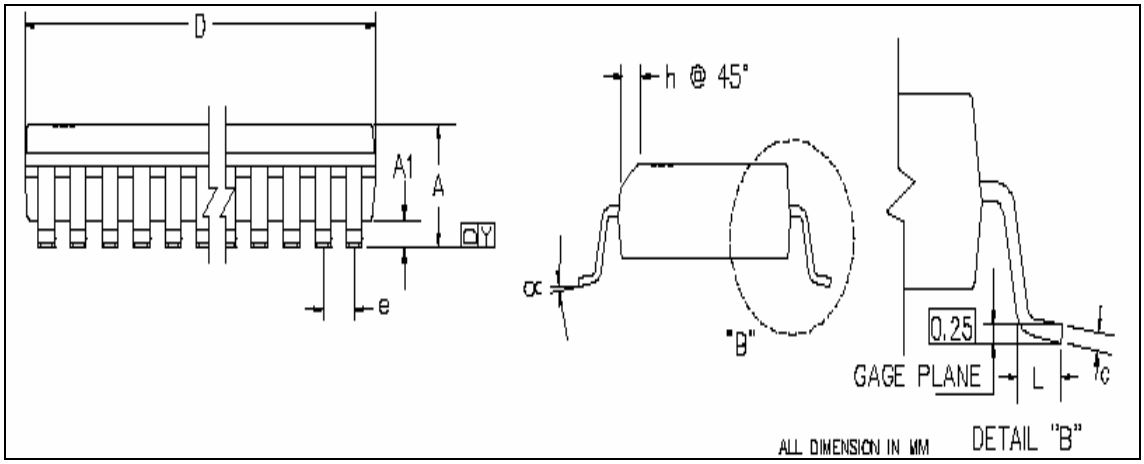
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{DD}	Chip Supply Voltage		4.5	5.0	5.5	Volts
V_{IL}	Input Voltage Low	STB,DIN,DOUT and CLK	0		0.5	Volts
V_{IH}	Input Voltage High 3.3V compatible with MCU interface	STB,DIN,DOUT and CLK	2.8		3.3	Volts
V_{ILK}	Input Voltage Low for Key Scan Input	K1 and K2	0		0.5	Volts
V_{IHK}	Input Voltage High for Key Scan Input	K1 and K2	V_{DD}-1.0		V_{DD}	Volts
V_{HYS}	Hysteresis Voltage for Key Scan Input	K1 and K2	200	350	500	mV
I_{LEAK}	Input Pad Leakage	STB,DIN,DOUT and CLK K1 and K2	-1	0	+1	μA
V_{OLGR}	Grid Output Voltage Low	I_{OL} = 275mA			0.5	Volts
I_{OHSG2V}	Segment Output Current Source	$V_{SG}=V_{DD}$-1V	17	23	27	mA
I_{OLGR}	Grid Output Leakage Current	GRn=OFF		0	10	μA
I_{OLSG}	Segment Output Leakage Current	SGn=OFF	-10	0		μA

AC Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
F_{OSC}	Chip RC Oscillator Frequency	R_{EXT}=51kΩ		500		kHz
T_{WCLK}	Serial Clock Pulse Width		500			ns
T_{WCE}	Serial Enable Pulse Width		1			µs
T_{DSET}	Serial Data Setup Time		20			ns
T_{DHLD}	Serial Data Hold Time		20			ns
T_{CECLK}	Serial Enable To Clock		20			ns
T_{CLKCE}	Serial Clock to Enable		20			ns
T_{WAIT}	Wait Time		1			µs

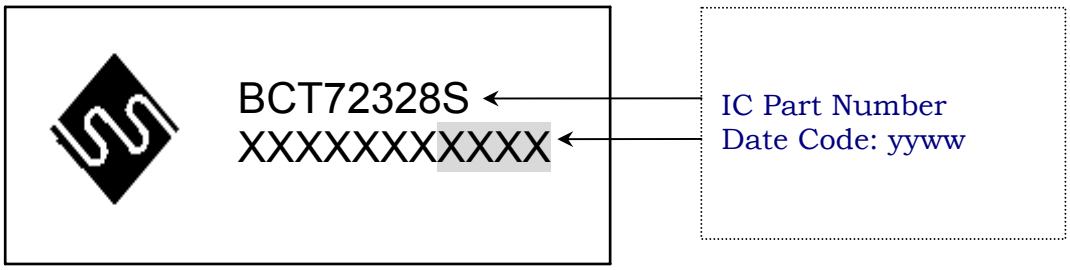
Package Information





CONTROL DIMENSIONS ARE IN MM						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.54	2.65	0.092	0.100	0.104
A1	0.10	0.17	0.30	0.004	0.006	0.012
B	0.33	0.42	0.51	0.013	0.016	0.020
C	0.23	0.25	0.32	0.009	0.010	0.012
D28	17.70	17.90	18.10	0.697	0.705	0.712
E	7.40	7.50	7.60	0.291	0.295	0.299
e					1.27 BSC	
H	10.00	10.30	10.65	0.394	0.406	0.419
h	0.25	0.50	0.75	0.009	0.020	0.029
L	0.40	0.70	1.27	0.015	0.028	0.050
∝	0 °		8 °	0 °		8 °
Y	0		0.10	0		0.004

Marking Notation / Ordering Information



Sales Offices

Malaysia

BCT Technology Bhd (HQ)

Lot G4, Incubator 3
Technology Park Malaysia
Bukit Jqalil, 57000
Kuala Lumpur
Malaysia

Tel : 603 8996 8088
Fax : 603 8996 8087

Singapore

BlueChips Technology Pte Ltd

3 International Business Park
#03-18/19/20
Nordic European Centre
Singapore 609927

Tel : 65 6890 6938
Fax : 65 6896 0928

Hong Kong

BlueChips Technology Pte Ltd

Unit 1101-1103, 11/F,
Yardley Commercial Building,
3 Connaught Road West,
Sheung Wan
Hong Kong

Tel : 852 2776 7968
Fax : 852 2776 8997

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