Motor / Actuator Drivers for DC Brush Motor Series

Automotive 3ch Half Bridge Driver with SPI Control

BD16933EFV-C

General Description

The BD16933EFV-C is 3ch half bridge driver for automotive applications. It can drive compact DC brush motors directly and each output can be controlled in three modes (High, Low and High Impedance).
MCU can control the driver via 16bit Serial Interface (SPI). The part is 60V rated with low ON resistance packaged in compact HTSSOP-20 package, which contributes to realize high reliability, low energy consumption and low cost.

Features

- AEC-Q100 Qualified(Note 1)
- 1.0A DMOS Half Bridge 3 Circuits
- Three Mode Output Control (High, Low & High Impedance)
- Low Standby Current
- Built-in Protection Diode Against Output Reverse Voltage
- Over Current Detection(OCD)
- Under Load Detection(ULD)
- Over Voltage Protection at Output Power Supply Stage(OVP)
- Under Voltage Lock Out at Output Power Supply Stage(UVLO)
- Thermal Shut Down(TSD)

(Note1) Grade 2

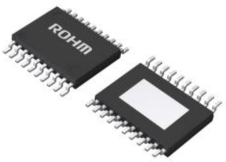
Applications(Note 2)

Automotive Body Electronics, HVAC, Door Mirrors, etc.

Key Specifications

Supply Voltage	7V to 36V
Operating Temperature Range	-40°C to +125°C
Output Current	1.0A (Max)
Output ON Resistance (High Side)	0.96Ω (Typ)
Output ON Resistance (Low Side)	0.85Ω (Typ)

Package	**W(Typ) x D(Typ) x H(Max)**
HTSSOP-B20	6.50mm x 6.40mm x 1.00mm



Typical Application Circuit

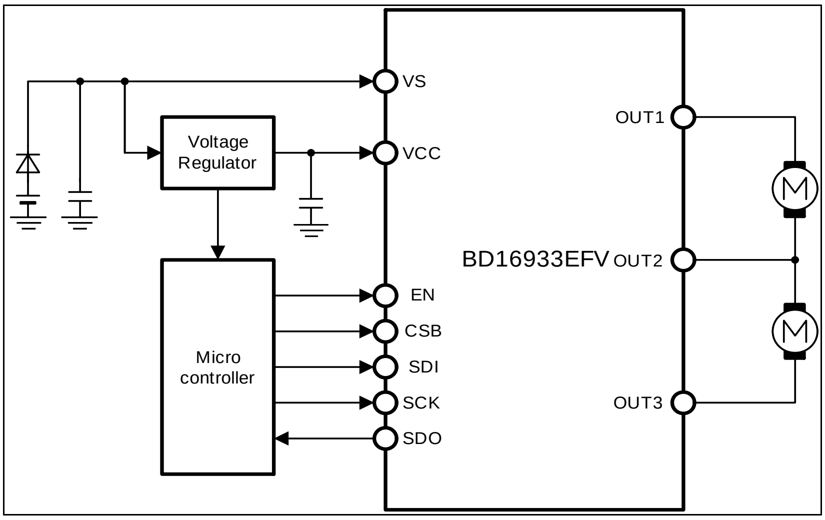


Figure 1. Typical Application Circuit

(Note 2) Please make sure you consult our company sales representative before mass production of this IC, if used other than Door Mirror and HVAC.

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

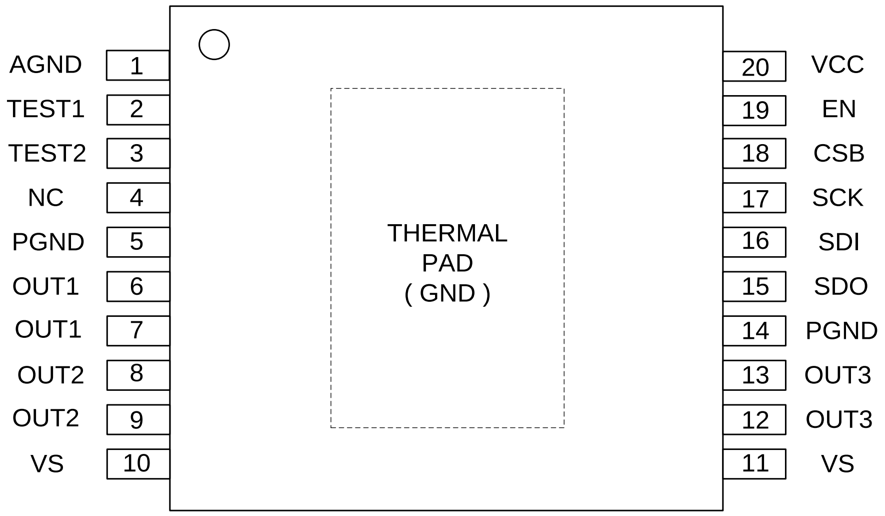

Figure 2. Pin Configuration

Pin Description

PIN No.	Symbol	Function	PIN No.	Symbol	Function
1	AGND	Small signal GND(Note 1)	20	VCC	Power supply
2	TEST1	TEST1 input(Note 2)	19	EN	Enable input
3	TEST2	TEST2 input(Note 2)	18	CSB	SPI chip select input
4	NC	No Connection	17	SCK	SPI clock input
5	PGND	Output GND	16	SDI	SPI data input
6	OUT1	Half bridge output 1	15	SDO	SPI data output
7	OUT1	Half bridge output 1	14	PGND	Output GND
8	OUT2	Half bridge output 2	13	OUT3	Half bridge output 3
9	OUT2	Half bridge output 2	12	OUT3	Half bridge output 3
10	VS	Power supply at output stage	11	VS	Power supply at output stage

(Note 1) Connect to PADGND for power dissipation.
(Note 2) Connect TEST1 and TEST2 to AGND

Block Diagram

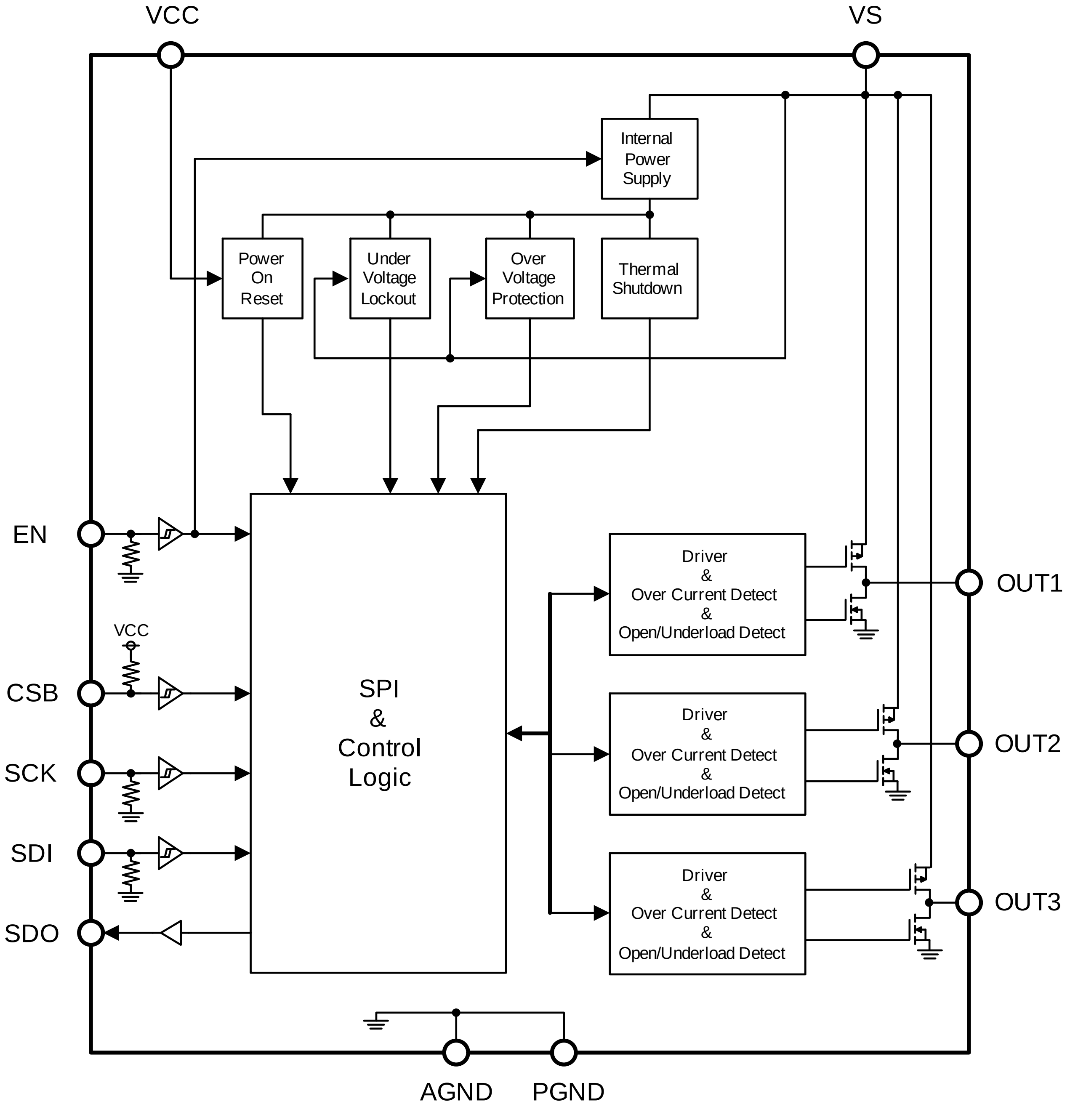

Figure 3. Block Diagram

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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{VS}	-0.3 to +60	V
Driver Supply Voltage	V_{CC}	-0.3 to +7.0	V
Output Voltage	V_{OUT1} to V_{OUT3}	-0.3 to +60	V
Output Current(Note 1)	I_O	1.0	A
Logic Input Voltage	V_{SDI}, V_{SCK}, V_{CSB}, V_{EN}	-0.3 to V_{CC}+0.3	V
Logic Output Voltage	V_{SDO}	-0.3 to V_{CC}+0.3	V
SDO Output Current	I_{SDO}	5.0	mA
Operating Temperature Range	Topr	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature Range	Tj	-40 to +150	°C

(Note 1) ASO should not be exceeded

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance (Note 2)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1 layer (Note 4)	4 layer (Note 5)	
HTSSOP-B20				
Junction to Ambient	θ_{JA}	143.0	26.8	°C/W
Junction to Top Characterization Parameter(Note 3)	Ψ_{JT}	8	4	°C/W

(Note 2) Based on JESD51-2A (Still-Air)

(Note 3) This thermal characterization parameter reports the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

(Note 5)Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 6)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

(Note 6) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions (Ta=-40°C to +125°C)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage(Note 7)	V_{VS}	7	12	36	V
Logic Supply Voltage (Note 7)	V_{CC}	3.0	5	5.5	V
Logic Input Voltage(Note 7)	V_{EN}, V_{CSB}, V_{SCK}, V_{SDI}	-0.3	-	V_{CC}	V

(Note 7) In order to start operation, apply the voltage to VCC (Driver supply voltage) after VS (Power supply voltage) exceeds the minimum operating voltage range (7V). After VCC (Driver supply voltage) exceeds the minimum operating voltage range (3.0V) then apply the voltage to the Logic input pins.

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Electrical Characteristics (Unless otherwise specified, V_{VS} =7V to 36V, V_{CC} = 3.0V to 5.5V, -40°C ≤Tj ≤+150°C)

Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
Circuit Current						
VS Circuit Current1	I_{VS1}	-	0	10	µA	EN = Low
VS Circuit Current 2	I_{VS2}	-	3.5	7	mA	
VCC Circuit Current 1	I_{VCC1}	-	0	10	µA	EN = Low
VCC Circuit Current 2	I_{VCC2}	-	0.1	0.5	mA	
Output						
Output ON Resistance High Side 1	R_{ONH1}	-	0.96	1.5	Ω	I_{Load} = 0.1A to 0.8A, -40°C ≤ Tj < +25°C
Output ON Resistance High Side 2	R_{ONH2}	-	1.5	2.0	Ω	I_{Load} = 0.1A to 0.8A, 25°C ≤ Tj ≤ 150°C
Output ON Resistance Low Side 1	R_{ONL1}	-	0.85	1.35	Ω	I_{Load} = 0.1A to 0.8A, -40°C ≤ Tj <+ 25°C
Output ON Resistance Low Side 2	R_{ONL2}	-	1.35	1.7	Ω	I_{Load} = 0.1A to 0.8A, 25°C ≤ Tj ≤ 150°C
Output Leakage High Side	I_{LH}	-	0	10	µA	OUT1 to OUT3 = 0V
Output Leakage Low Side	I_{LL}	-	0	10	µA	OUT1 to OUT3 = V_{VS}
Output Diode Voltage High Side	V_{FH}	0.2	0.8	1.4	V	I_{Load} = 0.6A
Output Diode Voltage Low Side	V_{FL}	0.2	0.8	1.4	V	I_{Load} = 0.6A
Serial Input						
Input High Voltage	V_{IH}	VCCx0.6	-	-	V	
Input Low Voltage	V_{IL}	-	-	VCCx0.2	V	
Input High Current 1	I_{IH1}	-	50	100	µA	VCC = SDI, SCK, EN = 5V
Input High Current 2	I_{IH2}	-	0	10	µA	VCC = CSB = 5V
Input Low Current 1	I_{IL1}	-	0	10	µA	SDI, SCK, EN = 0V
Input Low Current 2	I_{IL2}	-	50	100	µA	CSB = 0V, VCC = 5V
Serial Output						
Output High Voltage	V_{OH}	VCC-0.6	-	-	V	I_{Load} = -1.0mA
Output Low Voltage	V_{OL}	-	-	0.6	V	I_{Load} = 1.0mA
Protections						
VS Under Voltage Detection (OFF to ON)	V_{UVDH}	6.0	6.5	7.0	V	
VS Under Voltage Detection (OFF to ON)	V_{UVDL}	5.5	6.0	6.5	V	
VS Over Voltage Detection (OFF to ON)	V_{OVPH}	45	50	55	V	
VS Over Voltage Detection (OFF to ON)	V_{OVPL}	40	45	50	V	
VCC Power On Reset (OFF to ON)	V_{PORH}	2.6	2.8	3.0	V	
VCC Power On Reset (OFF to ON)	V_{PORL}	2.4	2.6	2.8	V	
Over Current Detection	I_{OCD}	1.05	1.5	1.95	A	
Over Current Detection Delay Time	T_{DOC}	10	25	50	µs	
Under Load Detection	I_{UD}	5	30	45	mA	
Under Load Detection Delay Time	T_{DUD}	200	370	600	µs	
Thermal Shutdown (Note 1)	T_{TSD}	150	175	200	°C	
Thermal Shutdown Hysteresis (Note 1)	T_{TSDHYS}	-	25	-	°C	

(Note 1) Design guaranteed. Not tested at outgoing.

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Electrical Characteristics (Unless otherwise specified, V_{VS} =7V to 36V, V_{CC} = 3.0V to 5.5V, -40°C ≤Tj ≤+150°C)

Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
Driver Output Timing						
High Side Turn On Time	t_{tonLH}	-	-	33.0	μs	V_{VS} = 12V, No Load
Low Side Turn On Time	t_{tonHL}	-	-	33.0	μs	V_{VS} = 12V, No Load
OUT Rise Time	t_{LHR}	-	1.0	8.0	μs	V_{VS} = 12V, No Load
OUT Fall Time	t_{HLF}	-	1.0	8.0	μs	V_{VS} = 12V, No Load

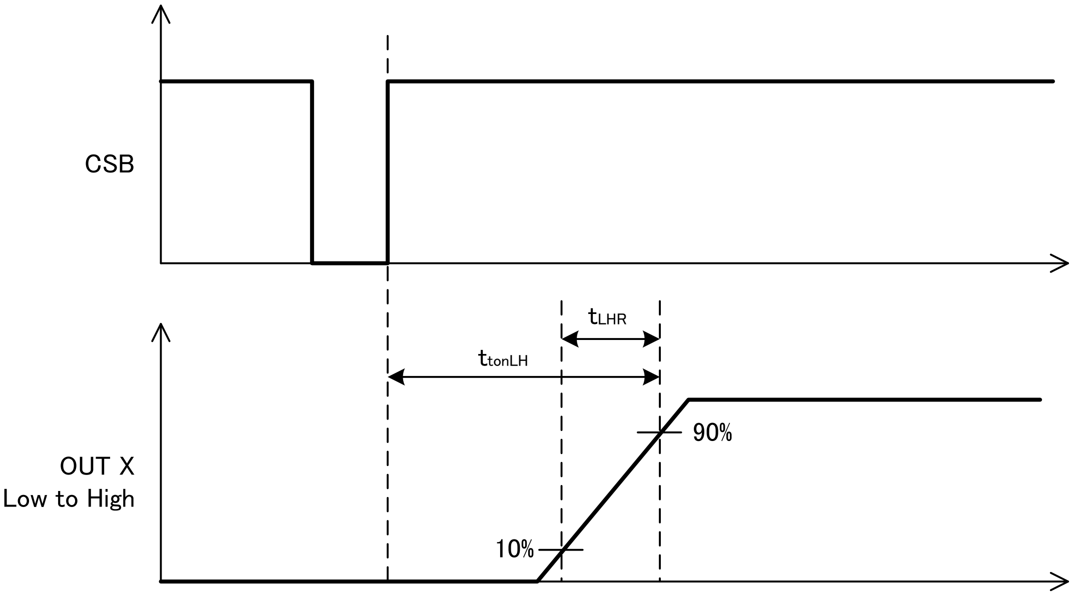

Figure 4. Driver Output Timing (Low to High)

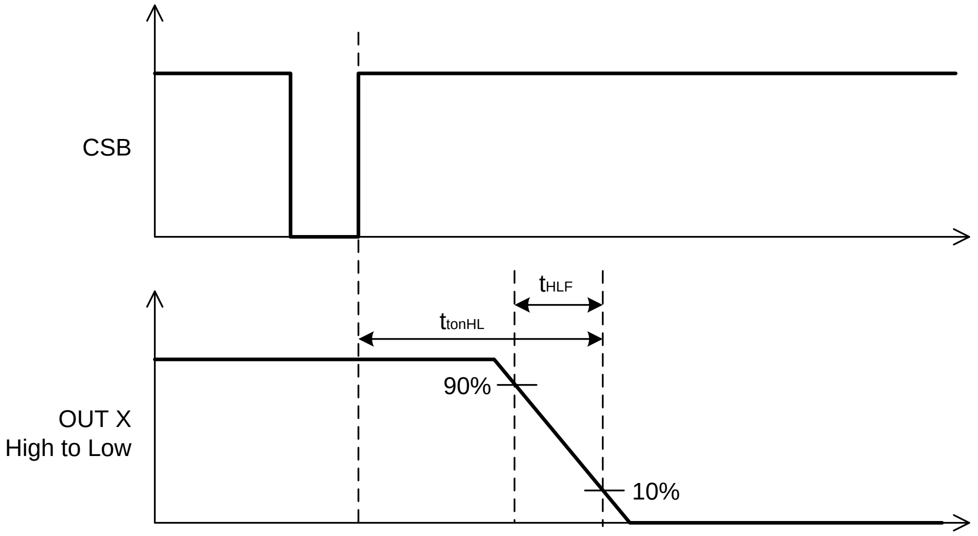

Figure 5. Driver Output Timing (High to Low)

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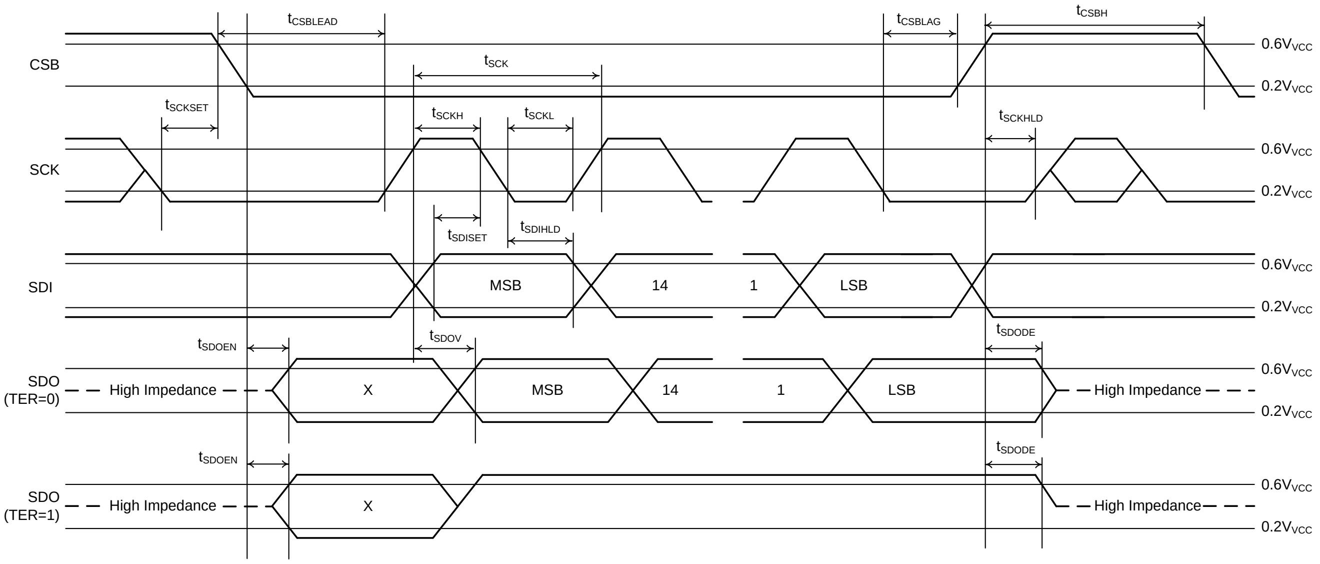
Electrical Characteristics (Unless otherwise specified, V_{VS} =7V to 36V, V_{CC} = 3.0V to 5.5V, -40°C ≤Tj ≤+150°C)

Parameter	Symbol	Specification			Unit	Conditions
		Min	Typ	Max		
Serial Peripheral Interface						
SCK Frequency	f_{SCK}	-	-	4.1	MHz	
SCK Period	t_{SCK}	243	-	-	ns	
SCK High Time	t_{SCKH}	80	-	-	ns	
SCK Low Time	t_{SCKL}	80	-	-	ns	
SCK Setup Time	t_{SCKSET}	125	-	-	ns	
SCK Hold Time	t_{SCKHLD}	125			ns	
CSB Lead Time	$t_{CSBLEAD}$	125	-	-	ns	
CSB Lag Time	t_{CSBLAG}	125	-	-	ns	
CSB High Time	t_{CSBH}	20	-	-	µs	
SDI Setup Time	t_{SDISET}	60	-	-	ns	
SDI Hold Time	t_{SDIHLD}	60	-	-	ns	
SDO Valid Time	t_{SDOV}	-	-	100	ns	No Load
SDO Enable After CSB Falling Edge	t_{SDOEN}	-	-	125	ns	(Note 1)
SDO Disable After CSB Rising Edge	t_{SDODE}	-	-	500	ns	(Note 1)

(Note 1) the timing is prescribed in 0% and 100% of VCC-GND amplitude.



X：Unstable state
TER (Internal signal):” 0” in normal operation /” 1” in detecting erroneous SPI transmission

Figure 6. Serial Interface Timing

Typical Performance Curves

(Unless otherwise specified, V_{VS} =7V to 36V, -40°C ≤Ta ≤+125°C)

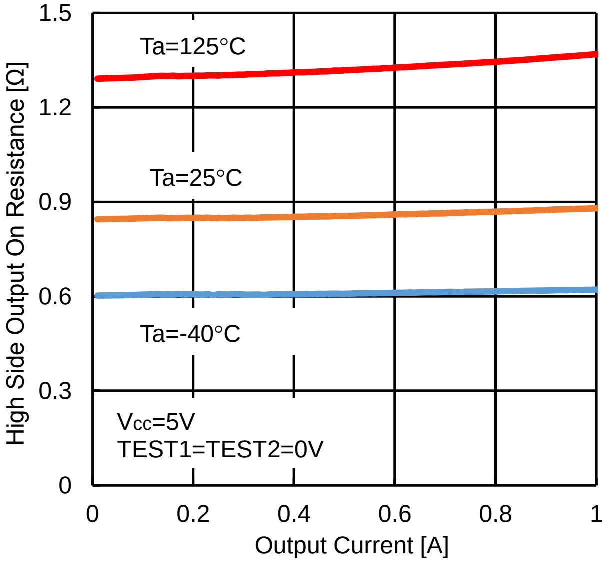


Figure 7. Output On Resistance vs Output Current
(Output ON Resistance High Side, V_{VS} = 12V)

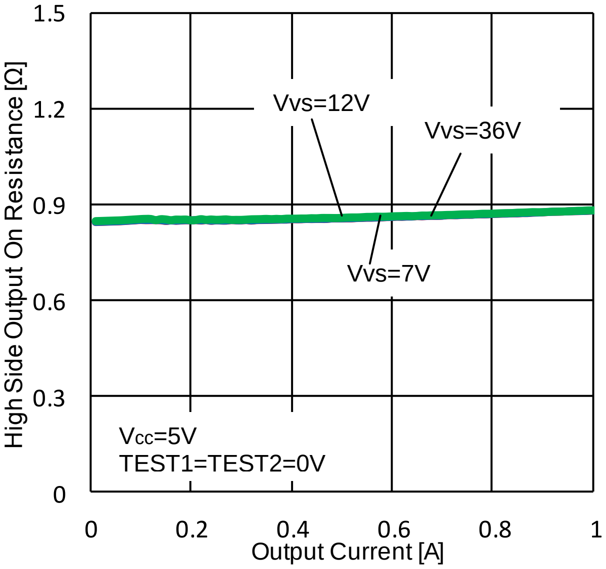


Figure 8. Output On Resistance vs Output Current
(Output ON Resistance High Side, Ta=25°C)

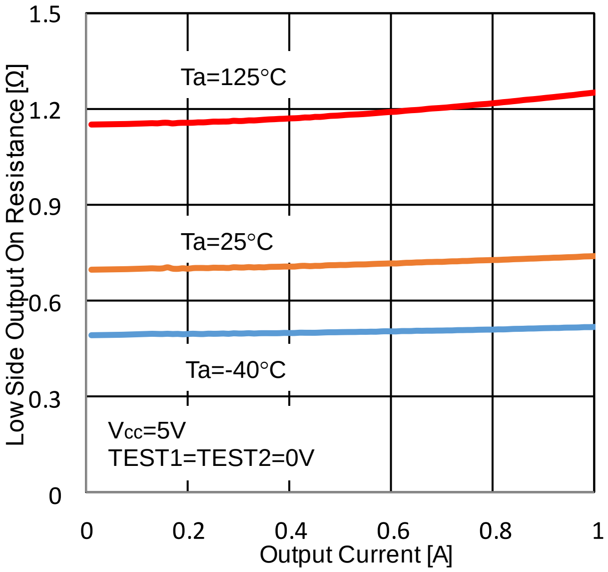


Figure 9. Output On Resistance vs Output Current
(Output ON Resistance Low Side, Vvs = 12V)

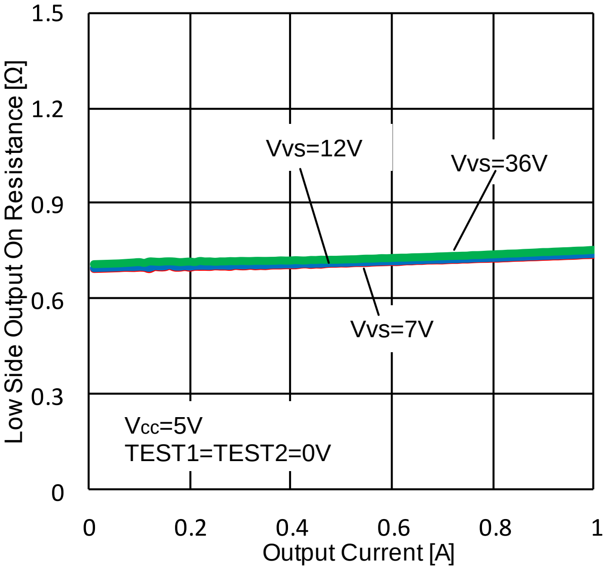


Figure 10. Output On Resistance vs Output Current
(Output ON Resistance Low Side, Ta=25°C)

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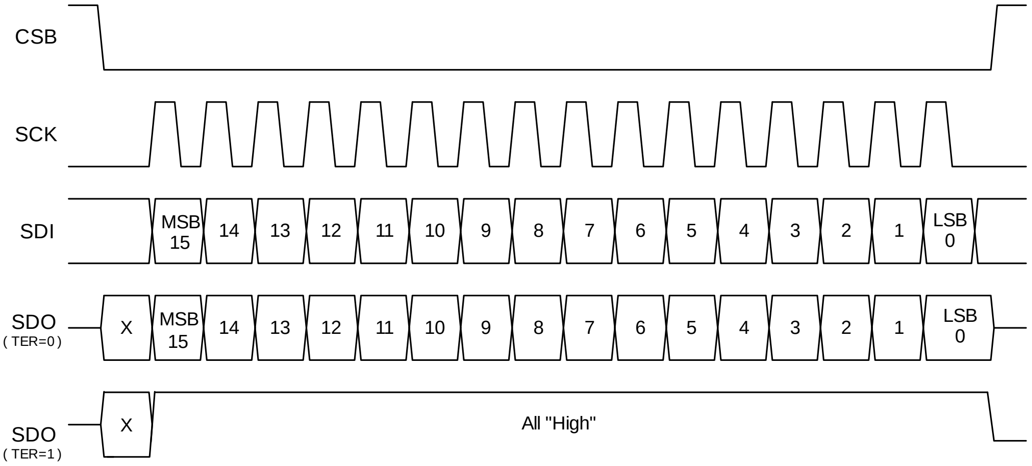
Operation of Each Block

1. Serial Peripheral Interface: SPI



X：Unstable state
TER (Internal signal) : " 0 " in normal operation / " 1 " in detecting erroneous SPI transmission

Figure 11. SPI Communication Format

16bit serial interface is equipped to control ON / OFF of driver and various protections as well as to read out the state of protections. Input / Output register and its functions are described below.

(1) Input Data Register

Bit Number	Name	Description	Bit Status	Initial Value
15	SRR	Status Reset Register (This bit will self clear)	0 : Normal 1 : Reset	0
14	HSC1	Control High side 1	0 : High side Off 1 : High side On	0
13	LSC1	Control Low side 1	0 : Low side Off 1 : Low side On	0
12	HSC2	Control High side 2	0 : High side Off 1 : High side On	0
11	LSC2	Control Low side 2	0 : Low side Off 1 : Low side On	0
10	HSC3	Control High side 3	0 : High side Off 1 : High side On	0
9	LSC3	Control Low side 3	0 : Low side Off 1 : Low side On	0
8	-	Not Used	-	0
7	-	Not Used	-	0
6	-	Not Used	-	0
5	-	Not Used	-	0
4	-	Not Used	-	0
3	UNDER LOAD	Under Loads Register Mode	0 :ON 1 : OFF	0
2	TSDSTH	TSDS Register Mode	0 : Latch 1 : Through	0
1	PSSTH	OVPS / UVLOS Register Mode	0 : Latch 1 : Through	0
0	RESERVE	RESERVE	0 : Normal 1 : Prohibit	0

Input of High Side ON and Low Side ON via SPI control is prohibited. The input of High Side ON and Low Side ON results in High Side OFF and Low Side ON state.

Daisy chain is not recommended due to its reliability concern. Connect Chip Select (CSB) to each device and run by SPI parallel control instead.

(2) Output Data Register

Bit Number	Name	Description	Bit Status	Initial Value$^{(Note\ 1)}$
15	OCDS	Over Current Detection Status	0 : Normal 1 : Fault	1 (Note 1)
14	HSS1	High side 1 Status	0 : High side Off 1 : High side On	0
13	LSS1	Low side 1 Status	0 : Low side Off 1 : Low side On	0
12	HSS2	High side 2 Status	0 : High side Off 1 : High side On	0
11	LSS2	Low side 2 Status	0 : Low side Off 1 : Low side On	0
10	HSS3	High side 3 Status	0 : High side Off 1 : High side On	0
9	LSS3	Low side 3 Status	0 : Low side Off 1 : Low side On	0
8	-	Not Used	-	0
7	-	Not Used	-	0
6	-	Not Used	-	0
5	-	Not Used	-	0
4	-	Not Used	-	0
3	UNDER LOADS	Under Loads Status	0 : Normal 1 : Fault	1 (Note 1)
2	TSDS	Thermal Shutdown Status	0 : Normal 1 : Fault	1 (Note 1)
1	OVPS	Over Voltage Protection Status	0 : Normal 1: Fault	1 (Note 1)
0	UVLOS	UVLO (VS) Status	0 : Normal 1 : Fault	1 (Note 1)

(Note 1) Default is ” 1 (Fault) “. Set SRR register “ 1 “ before use and reset the values.

Settings of Error Output Registers

< PSSTH , TSDSTH >	Under Voltage Lock Out UVLOS	Over Voltage Protection OVPS	Thermal Shut Down TSDS	Over Current Detection OCDS
< 0 , 0 >	Latch	Latch	Latch	Latch
< 0 , 1 >	Latch	Latch	Self Recovery	Latch
< 1 , 0 >	Self Recovery	Self Recovery	Latch	Latch
< 1 , 1 >	Self Recovery	Self Recovery	Self Recovery	Latch

PSSTH, TSDSTH has to be set initially, and it shouldn’t be changed in the middle of operation.
Either Latch or Self Recovery are selectable on UVLOS, OVPS and TSDS error output registers. Only Latch is available on OCDS error output register.
(The registers control only the operation mode of error output registers. It cannot change the operation of OUT 1 to 3 terminals.)
Refer to the explanations of Protection Functions as far as OUT 1 to 3 operations are concerned.

(3) Erroneous SPI Transmission (Transmission Error : TER)

When CSB signal becomes Low to High it will be assumed that SPI has completed the transfer, and the internal registers will be updated. When SCK inputs high pulse of 16, 24, 32, … (8+8xN values) while CSB is low, erroneous SPI transmission is detected. If the error is detected, OUT1 to 3 outputs High Impedance and each error output register (OCDS, TSDS, PSF and ULS) maintains the prior status accordingly. But SDO signal become high in the next transferring of SPI by TER.
At the same time, if the CSB High period (t_{CSBH}) goes below the specified 20μs, an erroneous SPI transmission can be detected. The transmission error status is refreshed every time CSB rises.

TER (Internal signal) : ” 0 ” in normal operation / ” 1 ” in detecting erroneous SPI transmission

2. Over Voltage Protection (OVP)

All outputs run into High impedance when VS terminal voltage goes up to or above 50V (Typ). OVPS register is set “1” in this case.
The outputs come back when VS terminal voltage goes down to or below 45V (Typ) and return to the normal operation.
The state of output data register OVPS can be either Latch or Self Recovery depending on the state of input data register PSSTH.
Input data register PSSTH=0 and output data register OVPS=1 for Latch. Input data register PSSTH=1 and output data register OVPS for Self Recovery when VS terminal voltage goes down to or below 45V (Typ). OVP doesn’t operate when EN terminal is at Low level. Be sure not to exceed the absolute maximum power supply voltage to avoid the IC being destroyed.

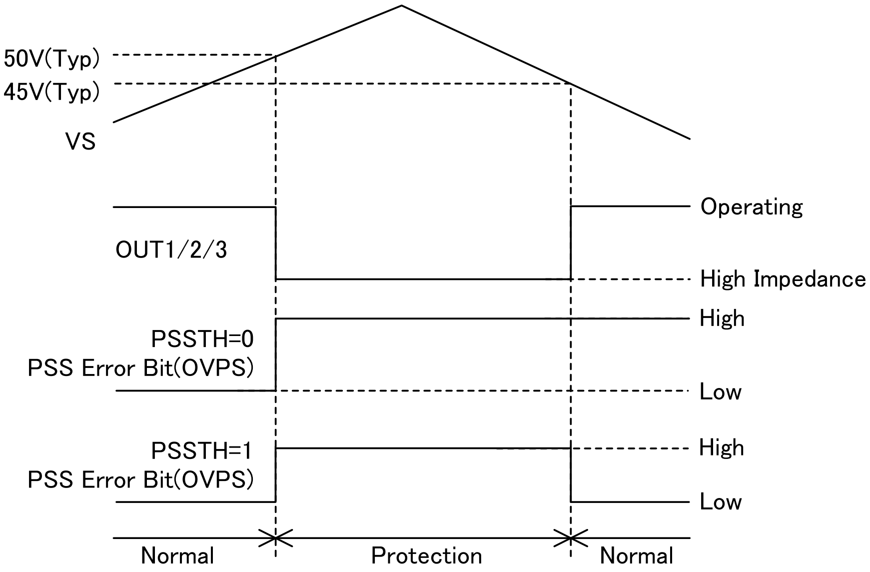


Figure 12. OVP Timing Chart

3. Under Voltage Lock Out (UVLO)

All outputs run into High impedance when VS terminal voltage goes down to or below 6.0V (Typ). UVLOS register is set “1” in this case. Outputs come back when VS terminal voltage goes up to or above 6.5V (Typ) and return to the normal operation mode. Output data register UVLOS in this case can be either Latch or Self Recovery depending on the status of input data register PSSTH. Input data register PSSTH=0 and output data register UVLOS= 1 for Latch. Input data register PSSTH=1 and output data register UVLOS for Self Recovery when VS terminal voltage goes up to or above 6.5V (Typ).

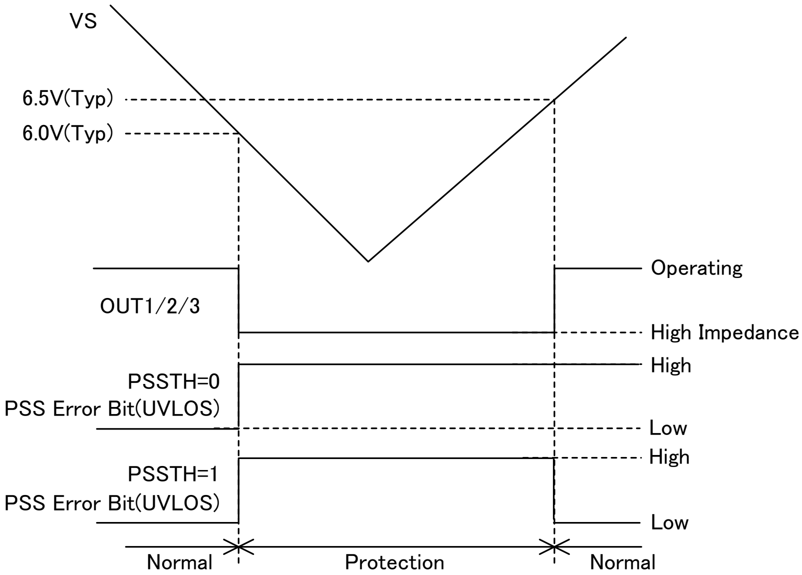


Figure 13. UVLO Timing Chart

4. Over Current Detection (OCD)

When 1.5A (Typ) current flows & 25μs (Typ) delay time into the output terminal, overcurrent is detected and OCDS register is set “1”. Only the Overcurrent Detected output stage is latched at High impedance. In order to release the latch in this case, it has to be reset via SRR register or EN terminal. Also 25μs (Typ) delay time is programmed to avoid the malfunction caused by noise.
OCD is the function to protect the IC from destruction caused by output short. However, the continuous overcurrent condition could lead the IC heating up or degraded and thus an appropriate measure has to be taken such as placing the IC into stand-by mode by application when overcurrent condition continues.

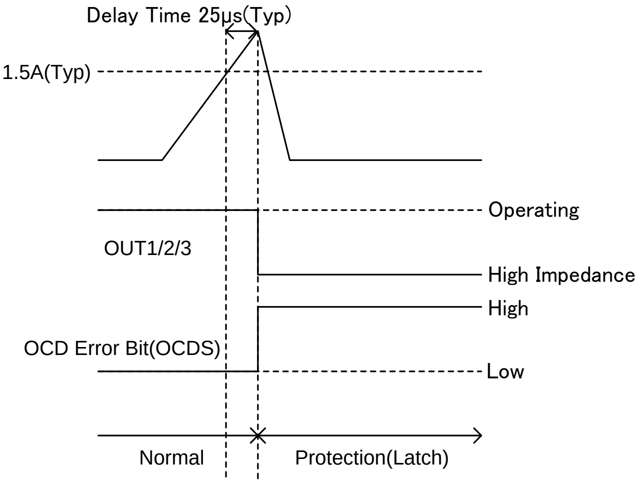


Figure 14. OCD Timing Chart

5. Thermal Shut Down (TSD)

When junction temperature goes up to or above 175°C (Typ), all outputs turn into High impedance.
TSDS register is set “1” in this case.
Self Recovery kicks in when the junction temperature goes down to or below 150°C (Typ) and outputs come back and return to the normal operation. TSDS register in this case is maintained at “1”. Output data register TSDS can be either Latch or Self Recovery depending on the input data register TSDSTH status. Input data register TSDSTH=0 and output data register TSDS=1 for latch. Input data register TSDSTH=1 and output data register TSDS for Self Recovery when the junction temperature goes down to or below 150°C (Typ).

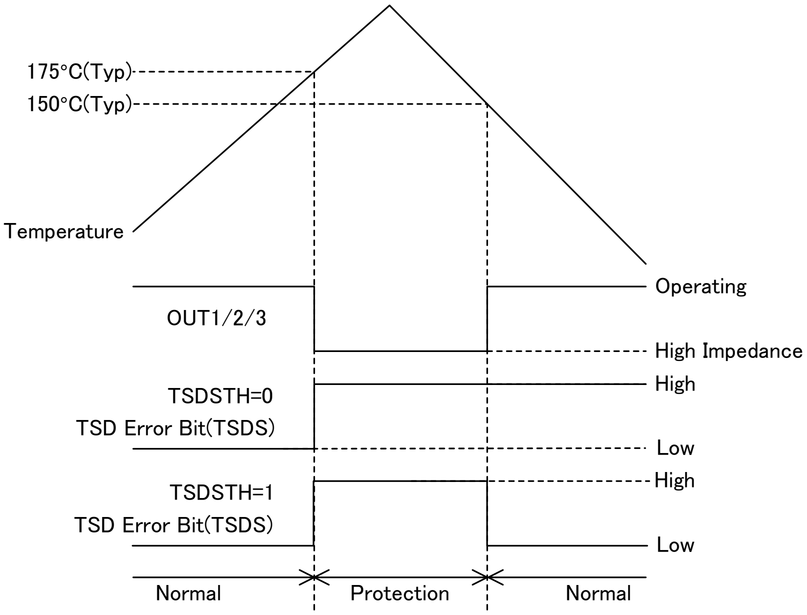


Figure 15. TSD Timing Chart

6. Under Load Detection (ULD)

When 30mA (Typ) current flows & 370µs (Typ) delay time into the output terminal, under load is detected and ULS register is set “1”.The output is not turned OFF if Under Load is detected, but the fault is latched to the ULS register. In order to release the latch in this case, it has to be reset via EN terminal. Also 370µs (Typ) delay time is programmed to avoid the malfunction caused by noise.

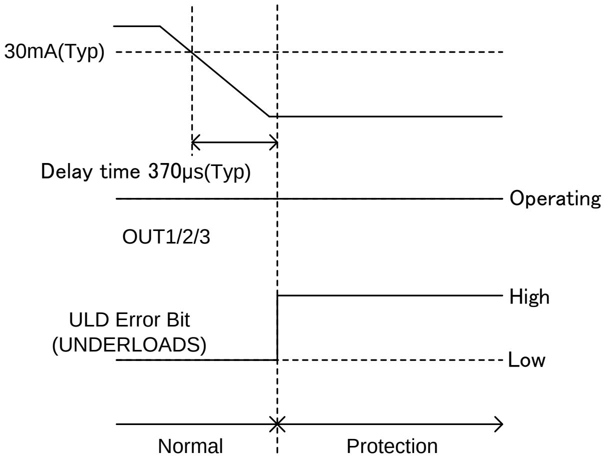


Figure 16. Under load Timing Chart 1

(Note)
When using a load such that the current start up delay exceeds the OPEN detection delay time, please reset the UNDERLOAD bit to ‘0’ (OPEN detection ON) after the load current becomes stable.

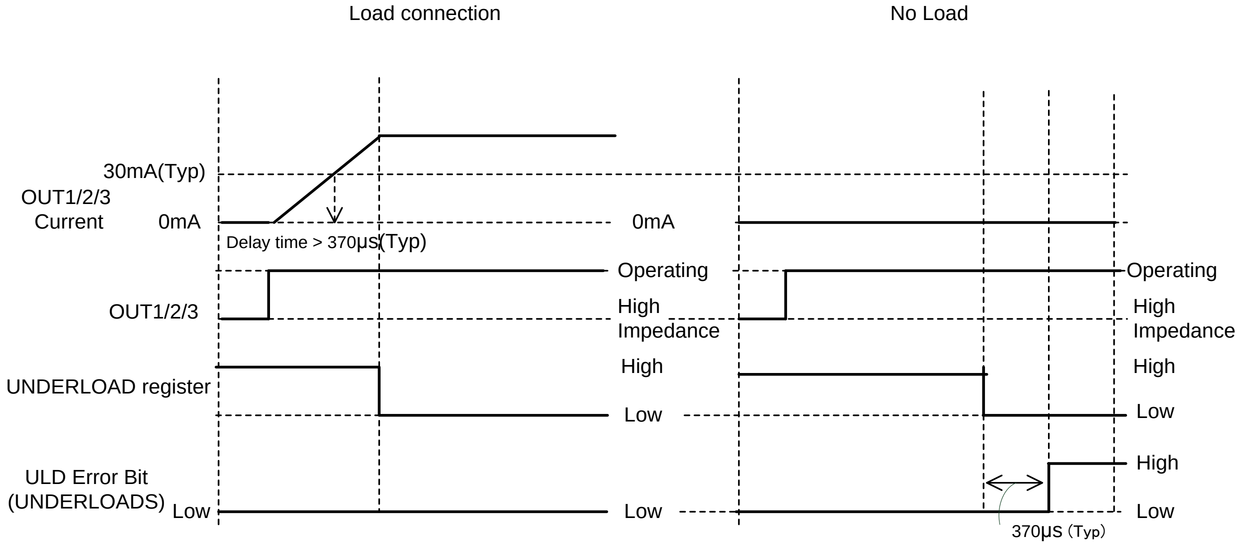
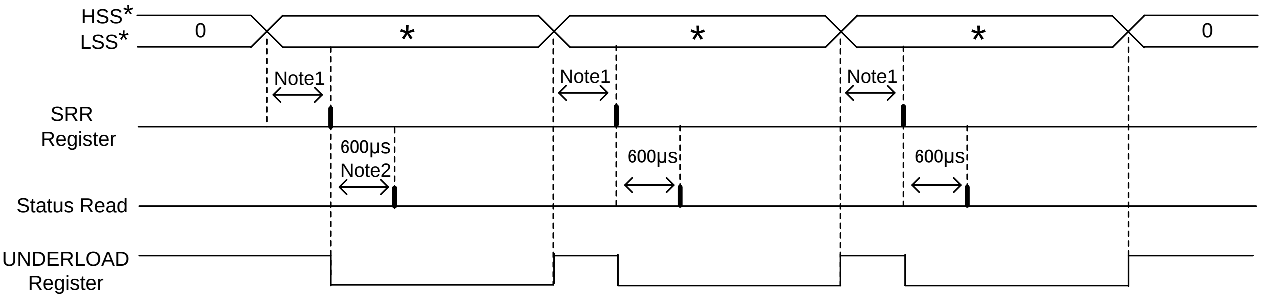


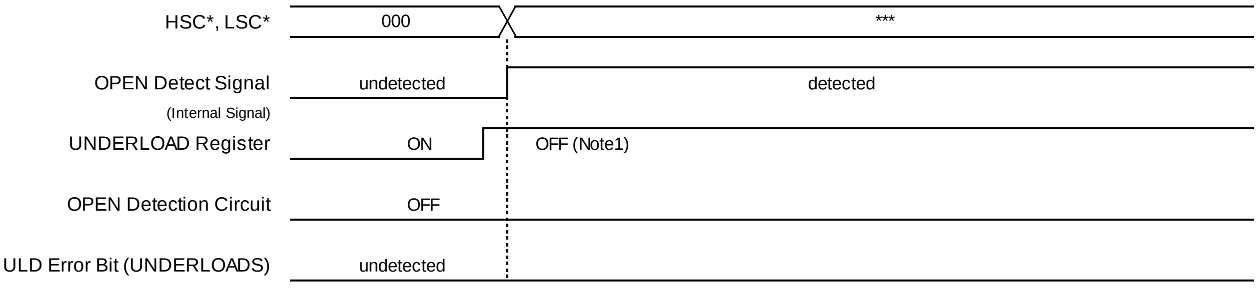
Figure 17. Under load Timing Chart 2



(Note1) Time should be determined based on response of the load connected.
(Note2) OPEN detection time requires minimum 600µs, so please use it by an interval of at least 600µs.

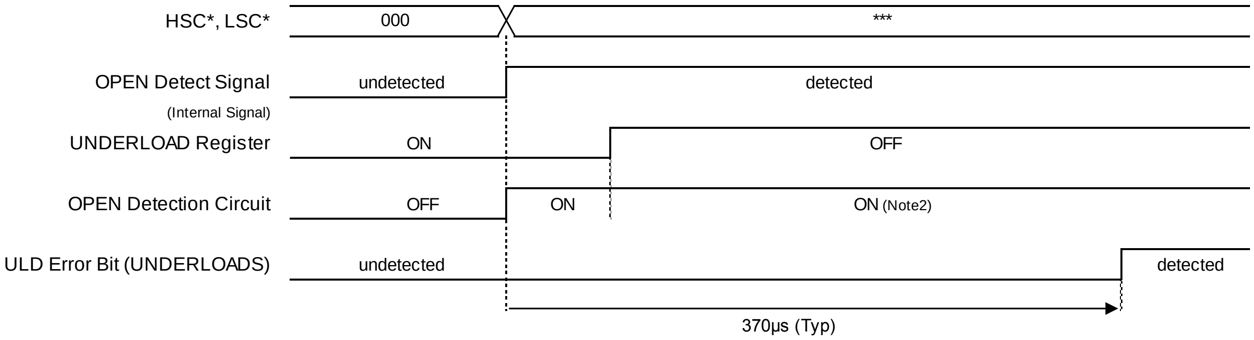
Figure 18. Under load Timing Chart 3

(Precaution)
If Under load detection needs to be masked, please set the UNDERLOAD bit in the write register before turning ON the channels HSC*, LSC* (Figure 19).
Please note that the internal under load detection function will be in operation always, hence if the UNDERLOAD bit is set after turning ON the channels HSC*, LSC* , the under load will still be detected and the UNDERLOADS read register bit will be set (Figure 20). Please use the EN pin to reset it and then set the UNDERLOAD bit in the write register before proceeding further with other commands.



(Note1) Please set UNDERLOAD bit before turning ON HSC*, LSC* to mask Underload detection.

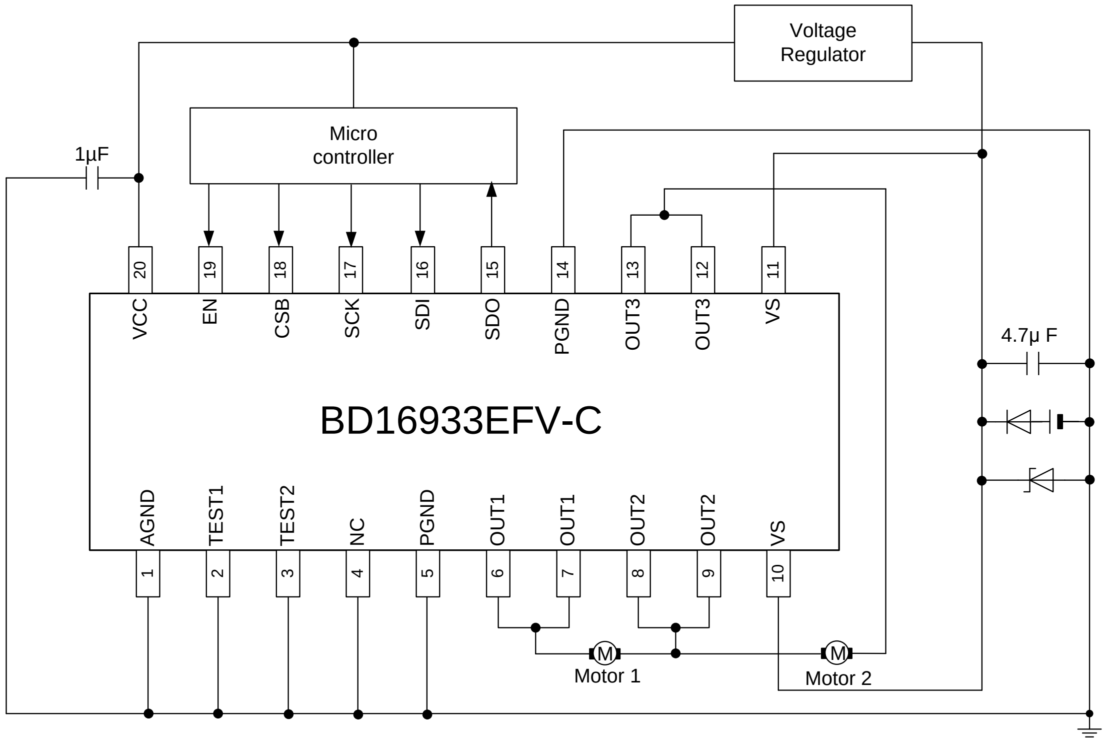
Figure 19. Under load Timing Chart 4



(Note2) Detection will not stop although UNDERLOAD bit is set.
Please reset with EN pin after open is detected.

Figure 20. Under load Timing Chart 5

Recommended Application Example



The external circuit constants shown in the diagram above represent a recommended value, respectively.

Figure 21. Recommended Application Example

Cautions on Designing of Application Circuits

1. Applicable Motors

Be noted that The BD16933EFV-C motor driver can only drive DC motors and cannot drive stepping motors.

2. VS and VCC

Be sure to mount a power supply capacitor in the vicinity of the IC pins between the VS and PGND and between the VCC and GND. Determine the capacitance of the capacitor after fully ensuring that it presents no problems in characteristics. (The recommended value of between VS and PGND is 4.7µF or more. The recommended value of between VCC and GND is 1.0µF or more.)

Furthermore, cause a short circuit between VS (set them to the same potential) before using the IC.

3. Counter-Electromotive Force

The counter-electromotive force may vary with operating conditions and environment, and individual motor characteristics. Fully ensure that the counter-electromotive force presents no problems in the operation or the IC.

4. Fluctuations in Output Pin Voltage

If any output pin makes a significant fluctuation in the voltage to fall below GND potential due to heat generation conditions, power supply, and motor to be used, or other conditions, this may result in malfunctions or other failures. In such cases, take appropriate measures, including the addition of a Schottky diode between the output pin and ground.

5. Rush Current

This IC has no built-in circuit that limits rush currents caused by applying current to the power supply or switching operation mode. To avoid the rush currents, take physical measures such as adding a current-limiting resistor between VS pins and the power supply.

6. Thermal Pad

Since a thermal pad is connected to the sub side of this IC, connect it to the ground potential. Furthermore, do not use the thermal pad as ground interconnect.

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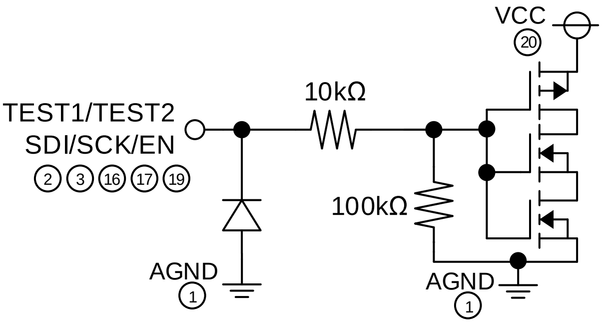
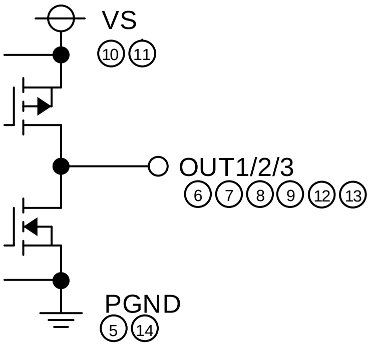
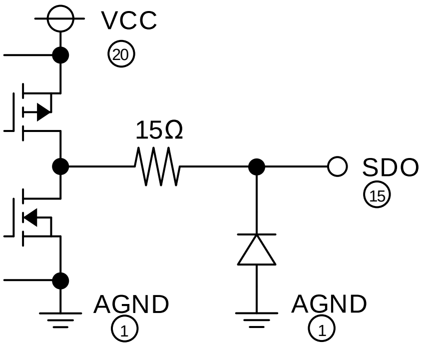
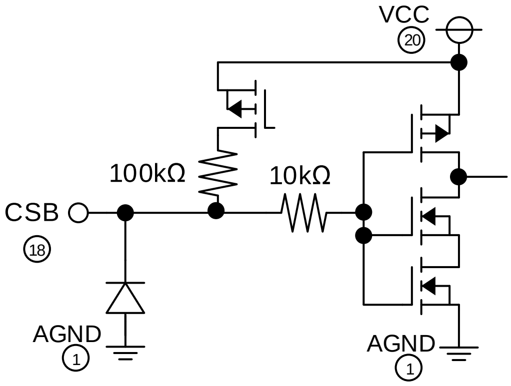
I/O Equivalent Circuits

Pin No.	Pin Name	I/O Equivalence Circuit
2 3 16 17 19	TEST1 TEST2 SDI SCK EN	
6,7 8,9 12,13	OUT1 OUT2 OUT3	
15	SDO	
18	CSB	

The resistance values shown in the above diagram are typical values.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes - continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

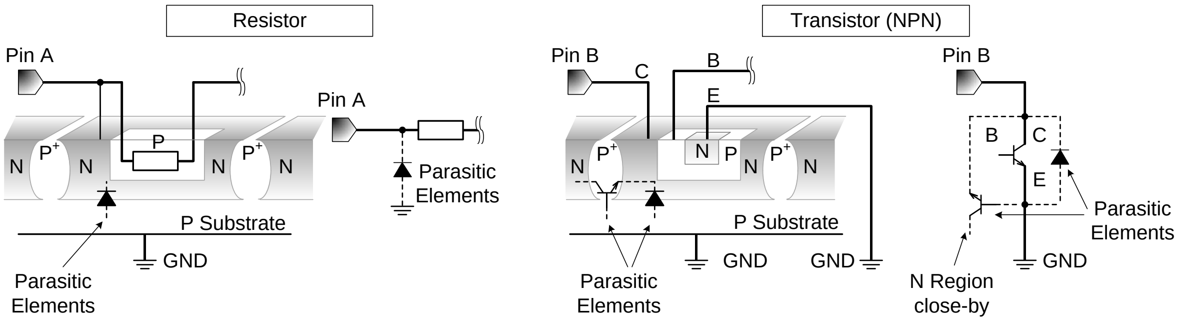


Figure 22. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC’s power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

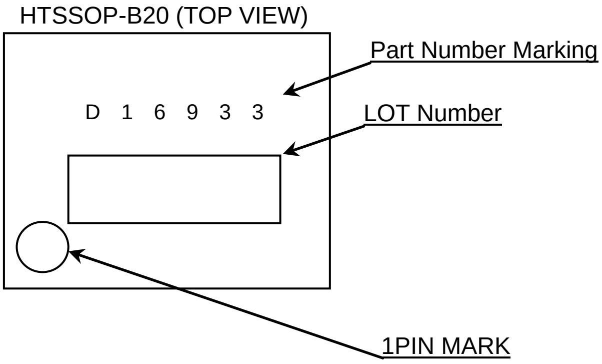
Ordering Information

Part Number

Package
EFV: HTSSOP-B20

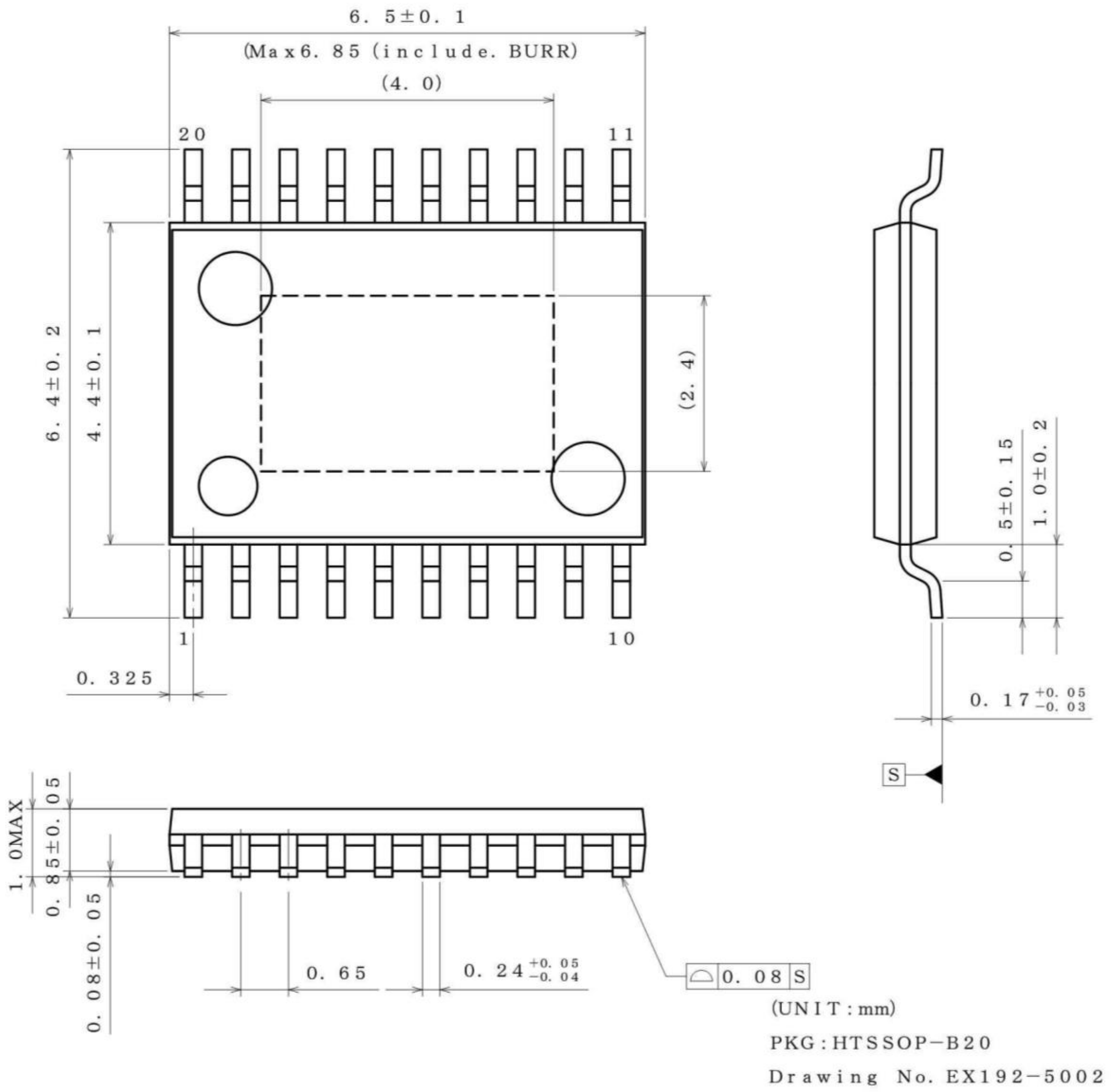
Product Rank
C: for Automotive
Packing and Forming Specification
E2: Embossed Tape and Reel

Marking Diagram



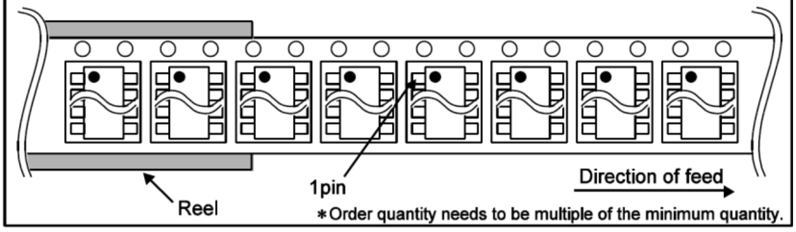
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B20



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
31.Mar.2016	001	New Release
25.Apr.2016	002	P4：2 Internal Layers Copper Pattern 74.2mm^2(Square) ⇒74.2mm x 74.2mm Bottom Copper Pattern 74.2mm^2(Square) ⇒74.2mm x 74.2mm

Notice

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   (Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   - [a] Installation of protection circuits or other protective devices to improve system safety
   - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   - [f] Sealing or coating our Products with resin or other coating materials
   - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   - [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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    - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
    - [b] the temperature or humidity exceeds those recommended by ROHM
    - [c] the Products are exposed to direct sunshine or condensation
    - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BD16933EFV-C - Web Page

Part Number	BD16933EFV-C
Package	HTSSOP-B28
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes