Datasheet

Power Supply Monitor

2ch Reset & Comparator IC

BD3775AF

● General Description

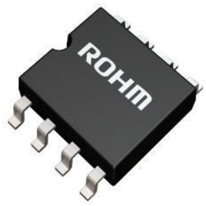
BD3775AF is designed to monitor the voltage level of one or two power supplies (+5V and an arbitrary voltage) in a microprocessor circuit, memory board in large-size computer, for example.
If the circuit's power supply deviates more than a specified amount, then the BD3775AF generates a reset signal to the microprocessor.
Also, the BD3775AF has a comparator for the over voltage protection and the high-precision reference voltage and so on apart from the above features. It is also available for more complex applications so.

● Key Specifications

- Input Voltage: 3.5V to 18V
- Voltage Detection
  - :VSAL 4.20V(Typ.)
  - :VSAH 4.30V(Typ.)
  - :VSB 1.230V(Typ.)
  - :VSC 1.245V(Typ.)
- Operating Temperature: -40℃ to 85℃

● Packages

SOP8 5.00mm x 6.20mm x 1.71mm



SOP8

● Feature

- High precision voltage detection (VSA = 4.20V ± 2.5%).
- Internal reset circuit that user selectable threshold level with hysteresis (VSB = 1.230V ± 1.5%). Internal open collector output comparators to create Over Voltage Detection circuit, reference voltage generator, and more. (VSC,OUTC)
- User selectable delay time of releasing reset signal depending on capacitor of CT node.
- Low power dissipation (Icc = 0.35mA ,VCC = 5V).
- SOP8 package (5.0×6.2mm,1.27mm pitch).

● Applications

- Industrial Equipment.
- Arcade Amusement.

● Typical Application Circuit

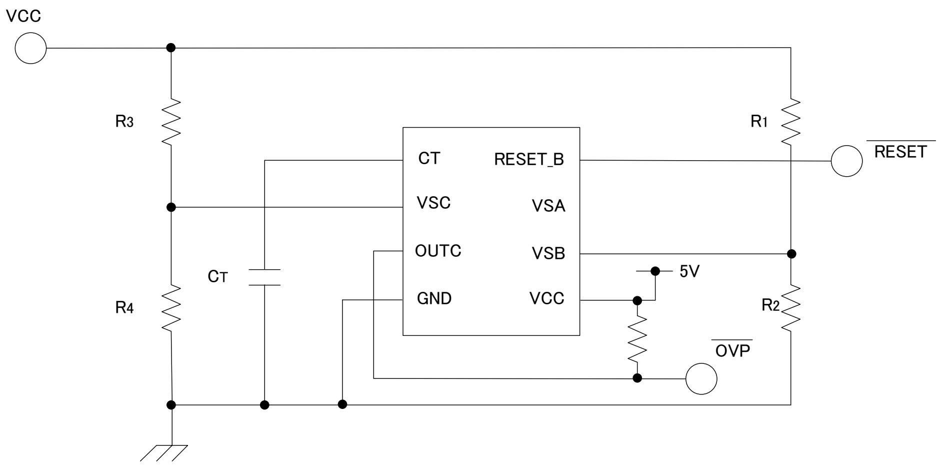


Figure 1. Typical Application Circuit

○Structure:Silicon Monolithic Integrated Circuit ○This product is not designed for normal operation with in a radioactive

●Pin configuration

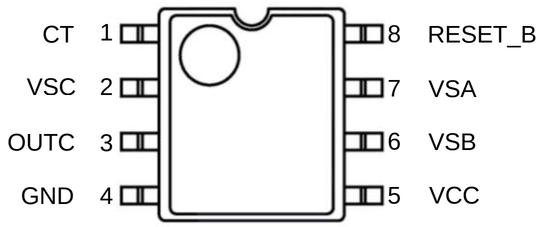


Figure 2. Pin configuration (TOP VIEW)

●Pin Description

Pin No.	Pin Name	Description
1	CT	Connected by capacitor deciding delay time.
2	VSC	Comp.C input voltage.
3	OUTC	Comp.C output detection signal.
4	GND	Ground.
5	VCC	Input supply.
6	VSB	Comp.B input voltage.
7	VSA	Comp input voltage.
8	RESET_B	RESET output signal.

●Block Diagram

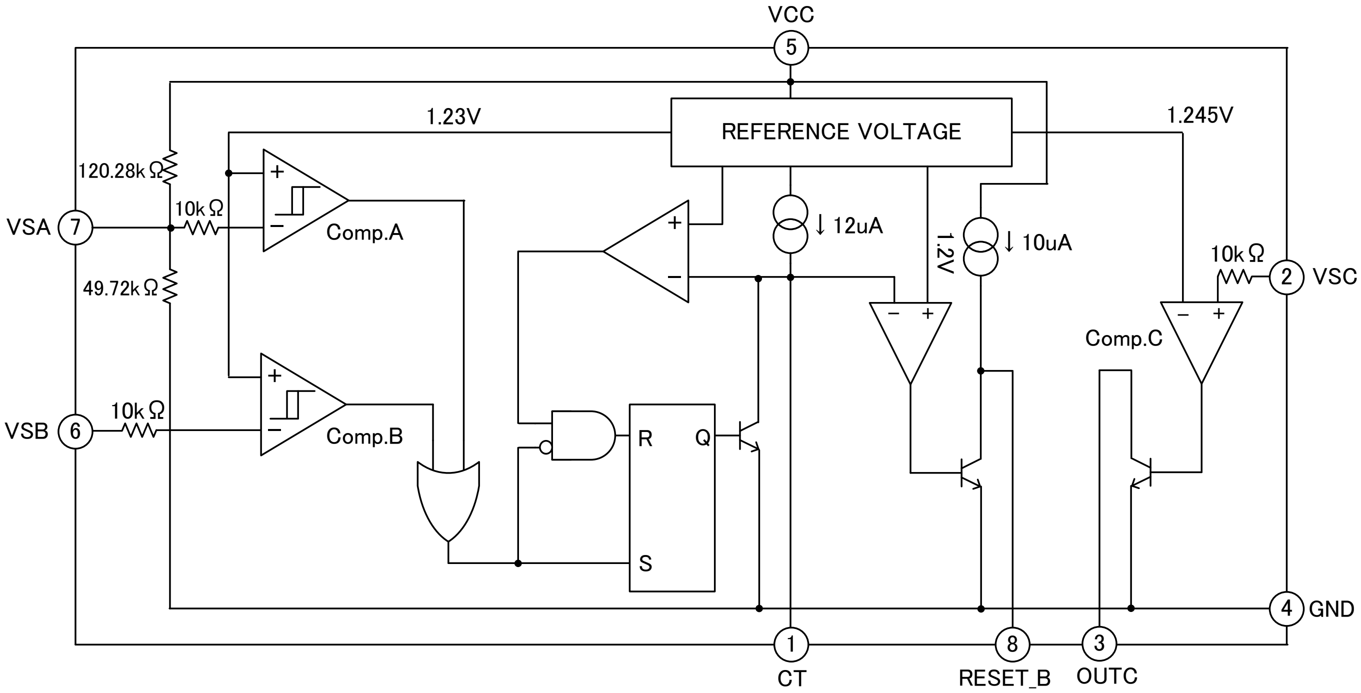


Figure 3. Block Diagram

●Description of Blocks

Comparators Comp.A and Comp.B apply a hysteresis to the detected voltage, so that when the voltage at either the VSA or VSB pin falls below 1.230V the RESET_B output signal goes to "low" level.

Comp. B may be used to detect any given voltage (Sample Application 3), and can also be used as a forced reset pin (with reset hold time) with TTL input (Sample Application 6).
Note that if Comp.B is not used, the VSB pin should be connected to the VCC pin (Sample Application 1).

Instantaneous breaks or drops in the power supply can be detected as abnormal conditions by the BD3775AF within a 2μs interval. A delayed trigger function can be created by connecting capacitors to the VSA or VSB pin (Sample Application 8).

Because the RESET_B output has built-in pull-up resistance, there is no need to connect to external pull-up resistance when connected to a high impedance load such as a CMOS logic IC.

Comparator Comp. C is an open-collector output comparator without hysteresis, in which the polarity of input/output characteristics is reversed. Thus Comp. C is useful for over-voltage detection (Sample Application 11) and positive logic RESET_B signal output (Sample Application 7), as well as for creating a reference voltage (Sample Application 10).

Note that if Comp. C is not used, the VSC pin should be connected to the GND pin (Sample Application 1).

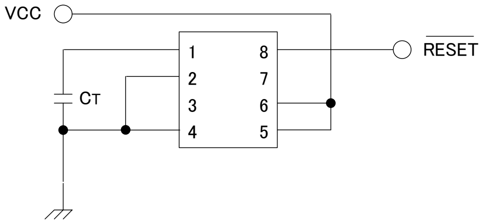


Figure 4. Typical Application Circuit

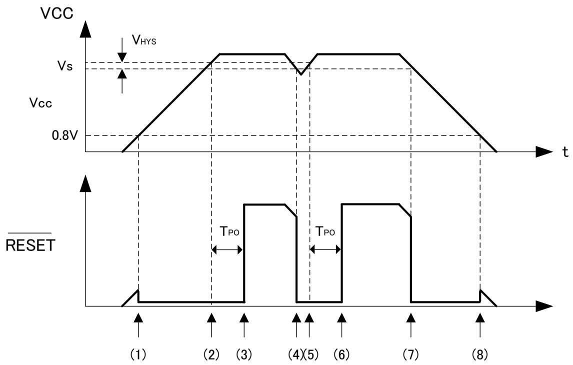


Figure 5. Timing Chart

(1) When Vcc rises to about 0.8V, RESET_B goes low.
(2) When Vcc reaches V_{SAL} +V_{HYS}, C_T then begins charging. RESET_B remains low during this time.
(3) RESET_B goes high when C_T begins charging
$T_{PO} \fallingdotseq C_T \times 10^5$ (Refer to "C_T pin capacitance vs. Reset holds time" in "TYPICAL CARACTERISTICS".)
(4) When Vcc level drops lower then V_{SAL}, then RESET_B goes low and C_T starts discharging.
(5) When Vcc level reaches V_{SAL} + V_{HYS}, then C_T starts charging.
In the case of voltage sagging, if the period from the time Vcc goes lower than or equal to V_S to the time Vcc reaches V_{SaL} +V_{HYS} again, is longer than T_{PL}, (as specified in the AC Characteristics), C_T is discharged and charged successively.
(6) After T_{PO} passes, and Vcc level exceeds V_{SAL} + V_{HYS}, then RESET_B goes high.
(7) Same as Point 4.
(8) RESET_B remains low until Vcc drops below 0.8V.

●Absolute Maximum Ratings(Ta=25℃)

item	Symbol	Rating	Unit
Power Supply Voltage	Vcc	20	V
Power Dissipation	Pd	0.67 (NOTE 1)	W
Input Voltage	V_{SA}	V_{CC}+0.3(＜20)	V
	V_{SB}	20	V
	V_{SC}	20	V
Storage temperature	Tstg	-55 to +125	℃
Junction Temperature	Tjmax	150	℃

(NOTE 1) During mounting of 70×70×1.6mmt 1layer board. Reduce by 186.56℃/W. (Above 25℃)

●Recommended Operating Ratings(Ta=-40℃ to +85℃)

parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	Vcc	3.5	5.0	18	V
Output current	I_{RESET_B}	-	-	20	mA
	I_{OUTC}	-	-	6	mA
Operating Temperature	Topr	-40	-	+85	℃

●Electrical Characteristics **(**Unless otherwise specified Ta=25℃,Vcc=5.0V, CT=0.01uF)

parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Power supply current	I_{CC1}	-	350	500	uA	V_{SB}=5V,V_{SC}=0V
	I_{CC2}	-	400	600	uA	V_{SB}=0V,V_{SC}=0V
Comp.A detection voltage	V_{SAL}	4.10	4.20	4.30	V	V_{CC}=sweep down
		4.05	4.20	4.35	V	V_{CC}=sweep down, Ta=-40℃ to +85℃
	V_{SAH}	4.20	4.30	4.40	V	V_{CC}=sweep up
		4.15	4.30	4.45	V	V_{CC}=sweep up, Ta=-40℃ to +85℃
Comp.A hysteresis width	V_{HYSA}	50	100	150	mV	
Comp.B detection voltage	V_{SB}	1.212	1.230	1.248	V	V_{SB}=sweep down,Ta=25℃
		1.200	1.230	1.260	V	V_{SB}=sweep down, Ta=-40℃ to +85℃
Comp.B deviation of detection voltage	ΔV_{SB}	-	3	10	mV	V_{CC}=4.5V to 18V
Comp.B hysteresis width	V_{HYSA}	14	28	42	mV	
Comp.B input current	I_{IHB}	-	0	250	nA	V_{SB}=5V
	I_{ILB}	-	60	250	nA	V_{SB}=0V

Comp.C detection voltage	V_{SC}	1.225	1.245	1.265	V	
		1.205	1.245	1.285	V	Ta=-40℃ to +85℃
Comp.C deviation of detection voltage	ΔV_{SC}	-	3	10	mV	V_{CC}=3.5V to 18V
Comp.C input current	I_{IHC}	-	0	500	nA	V_{SC}=5V
	I_{ILC}	-	5	500	nA	V_{SC}=0V
RESET_B output voltage	V_{OHR}	4.5	4.9	-	V	IRESET_B=-5uA,V_{SB}=5V
	V_{OLR}	-	0.28	0.4	V	IRESET_B=3mA,V_{SB}=0V
		-	0.38	0.5	V	IRESET_B=10mA,V_{SB}=0V
RESET_B output sink current	IRESET_B	20	40	-	mA	VRESET_B=1.0V,V_{SB}=0V
CT charge current	I_{CT}	9	12	16	uA	VSB=5V, V_{CT}=0.5V
OUTC output leakage current	I_{OHC}	-	0	1.0	uA	V_{OUTC}=18V
OUTC output voltage	V_{OLC}	-	0.15	0.4	V	I_{OUTC}=4mA,V_{SC}=5V
OUTC sink current	I_{OUTC}	6	15	-	mA	V_{OUTC}=1.0V,V_{SC}=5V
RESET operation minimum supply voltage	V_{CCL}	-	0.8	1.2	V	IRESET_B =200uA,VRESET≦0.4V,
VSA,VSB input pulse width	t_{PI}	5.0	-	-	us	
Reset hold time	t_{PO}	0.5	1.0	1.5	ms	
RESET_B rise time	t_r	-	1.0	1.5	us	RL(VCC-RESET_B)=2.2kΩ CL(RESET_B-GND)=100pF
RESET_B fall time	t_f	-	0.1	0.5	us	
Propagation delay time	t_{PD} *(NOTE 2)*	-	2	10	us	
	t_{PHL} *(NOTE 3)*	-	0.5	-	us	RL(VCC-OUTC)=2.2kΩ CL(OUTC-GND)=100pF
	t_{PLH} *(NOTE 3)*	-	1.0	-	us	

(NOTE 2) In case of VSB termination.
(NOTE 3) In case of VSC termination.
◎ Not designed withstand radiation.

●Typical Performance Curve

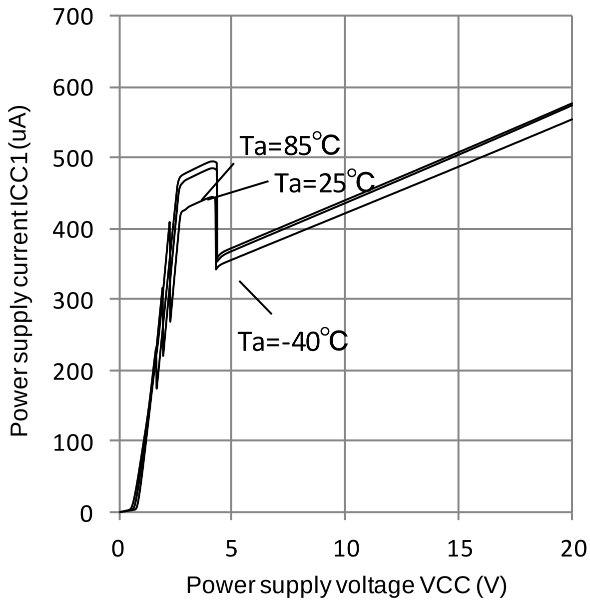


Figure 6. Power supply current vs. power supply voltage

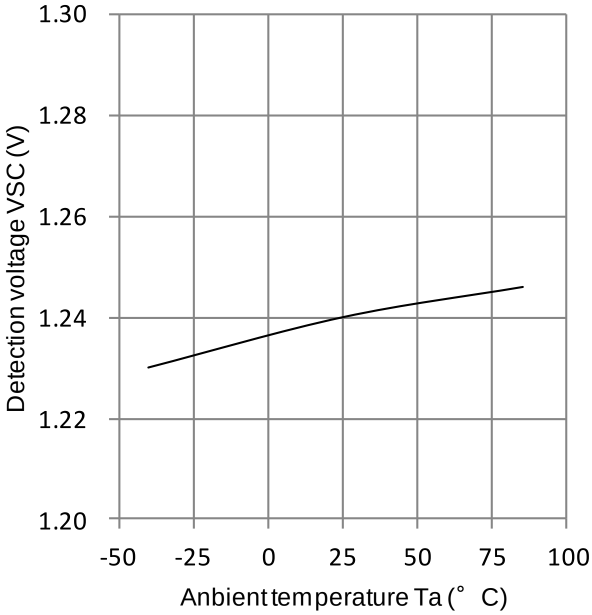


Figure 7. Detection voltage (VSC) vs. ambient temperature

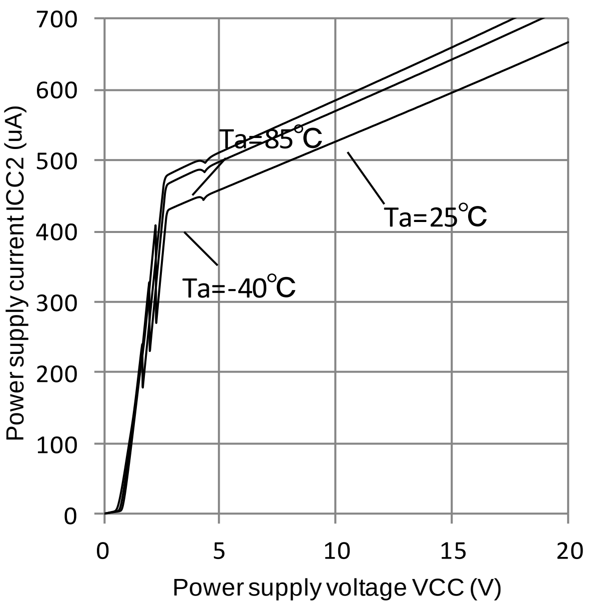


Figure 8. Power supply current vs. power supply voltage

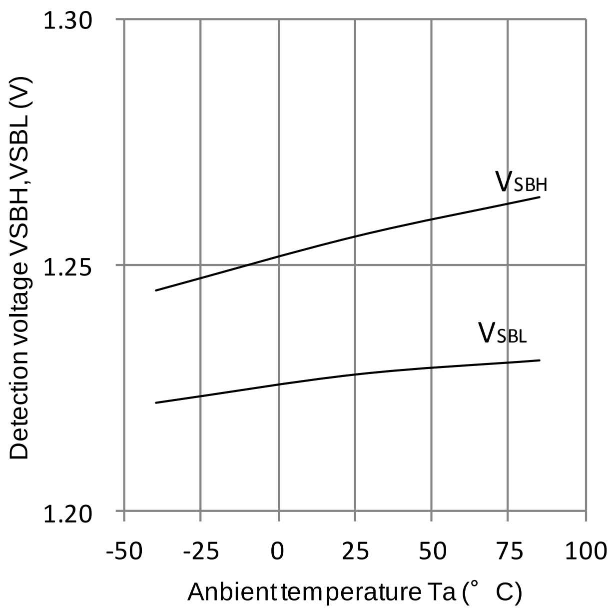


Figure 9. Detection voltage (VSB) vs. ambient temperature

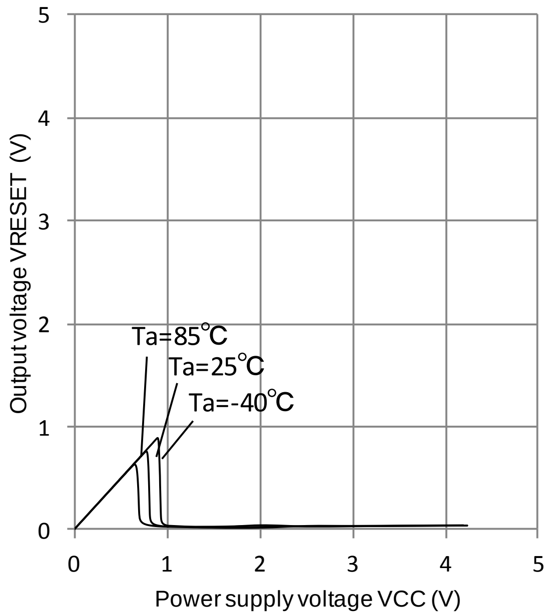


Figure 10. Output (RESET) voltage vs. power supply voltage

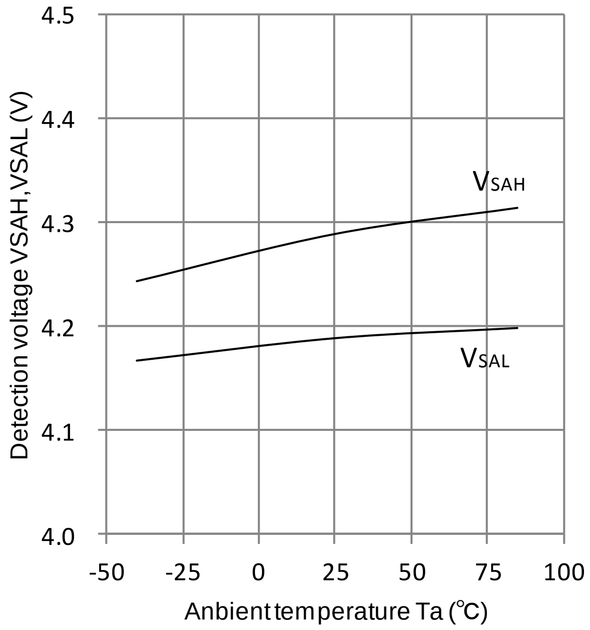


Figure 11. Detection voltage (VSA) vs. ambient temperature

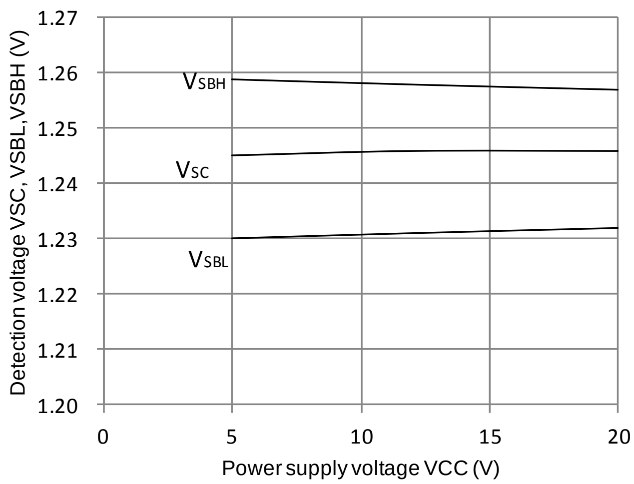


Figure 12. Detection voltage (VSB, VSC) vs. Power supply voltage

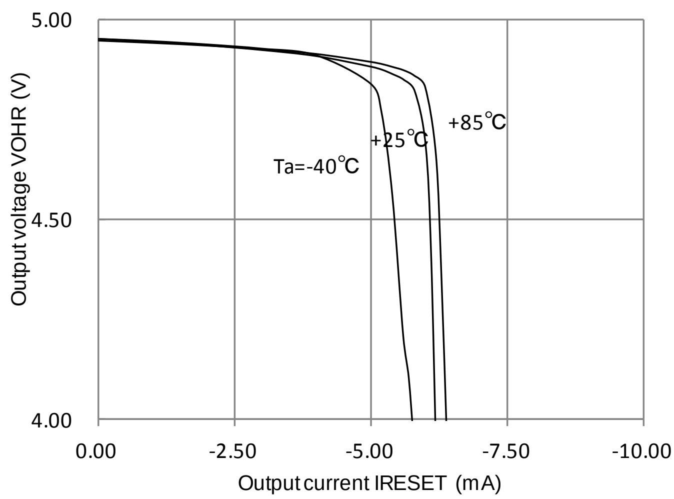


Figure 13. Reset voltage (RESET) vs. output current

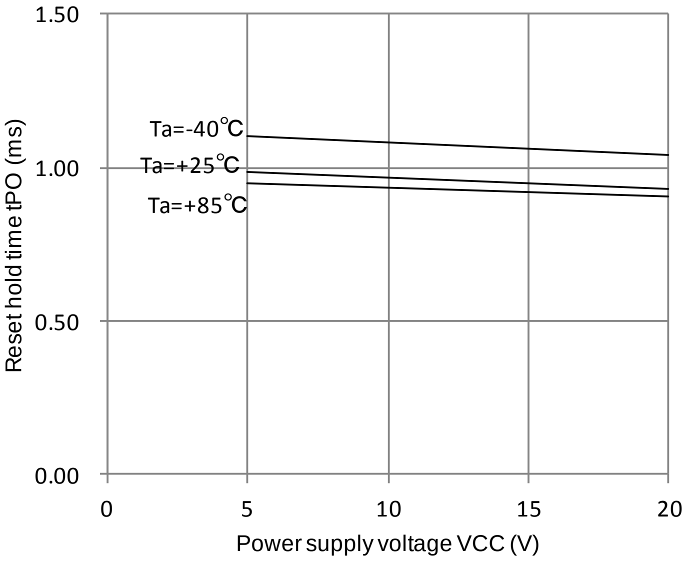


Figure 14. Reset hold time vs. power supply voltage
(CT = 0.01μF)

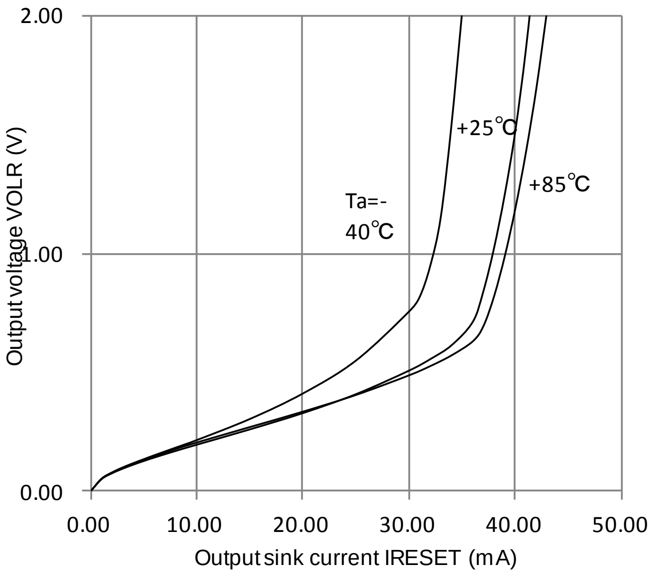


Figure 15. Output (RESET) voltage vs. output current

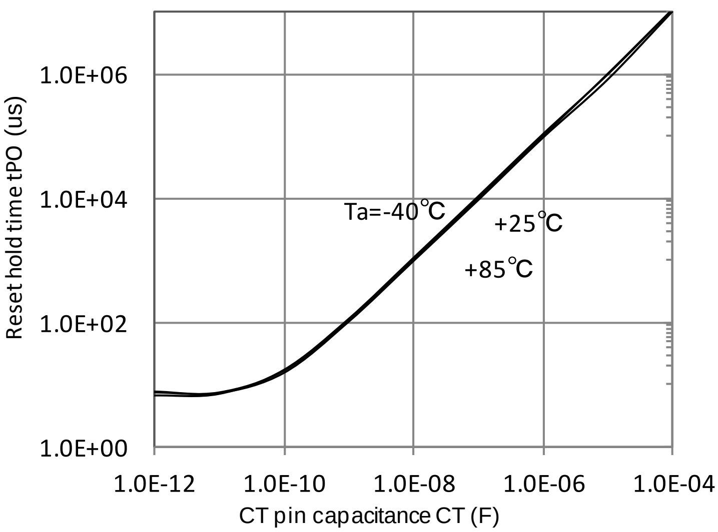


Figure 16. CT pin capacitance vs. reset hold time

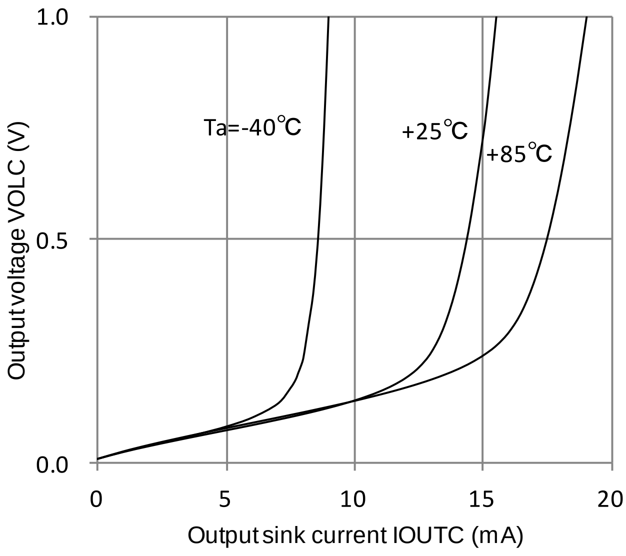


Figure 17. Output voltage (OUTC) vs. output current

● Application Examples

①5V Power Supply Monitor

Monitored by VSA. Detection threshold voltage is VSAL and VSAH

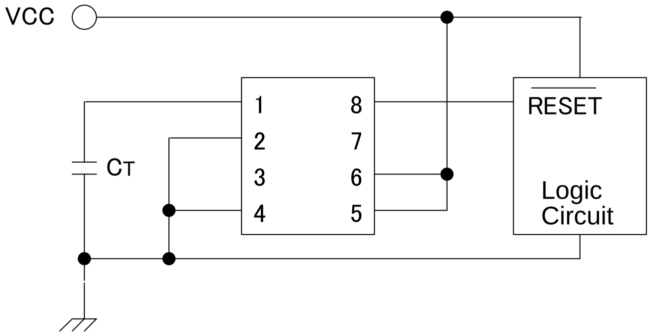


Figure 18. Application Example1

②5V Power Supply Voltage Monitor (Externally Fine-Tuned Type)

The VSA detection voltage can be adjusted externally.

External resistance R1 and R2 are set sufficiently lower than the IC internal partial voltage resistance (120kΩ, 50kΩ), so that the detection voltage can be set using the ratio between external resistance R1 and R2. External resistance R1 and R2 should be set to values that can cansel the variation of temperature variations and internal resistance characteristics of the IC.(below 10kΩ)

・R_1,R_2 calculation formula (when R_1<<120kΩ, R_2<<50kΩ)

$V_{SAL} \fallingdotseq (R_1+R_2) \times V_{SB}/R_2$[V], $V_{SAH} \fallingdotseq (R_1+R_2) \times (V_{SB}+V_{HYSB})/R_2$[V]

R_1 (kΩ)	R_2 (kΩ)	Detection voltage: V_{SAL}(V)	Detection voltage:V_{SAH} (V)
10	3.9	4.37	4.47
9.1	3.9	4.11	4.20

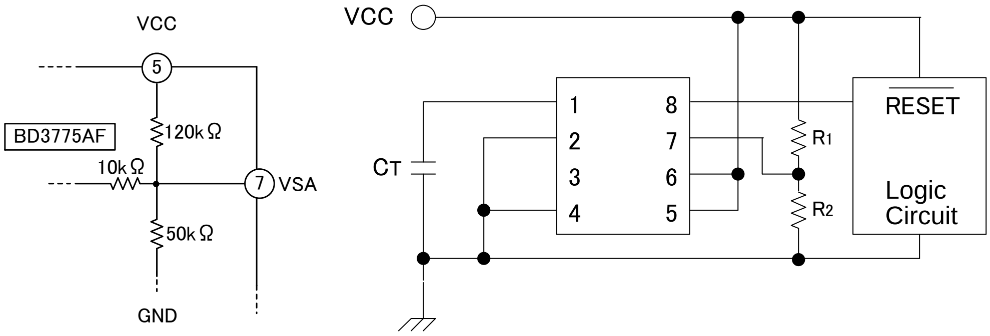


Figure 19. Application Example 2

③Arbitrary Voltage Supply Monitor

(1)Case: VCC ≤ 18V

・Detection Voltage can be set by R1 and R2.
Detection Voltage =$(R_1+R_2) \times V_{SB}/R_2$

・Connect Pin 7 to VCC when VCC less than 4.45V.

・Pin 7 can be opened when VCC greater than 4.45V
Power Dissipation can be reduced.

Note : Hysteresis of 28mV at VSB at termination is available.
Hysteresis width dose not depend on (R1 + R2).

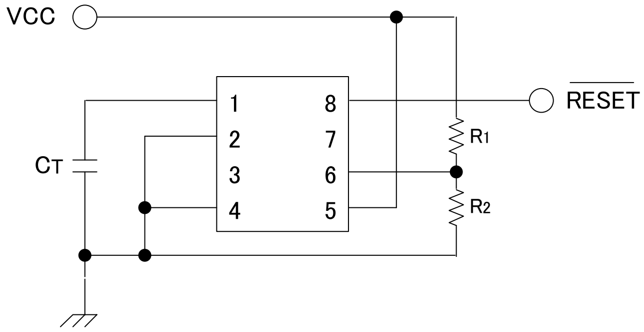


Figure 20. Application Example 3-1

(2) Monitoring VCC > 18V

・Detection Voltage can be set by R1 and R2.
Detection Voltage =$(R_1+R_2) \times V_{SB}/R_2$

・The RESET_B signal output is ≅0V (low level) and ≅5V (high level). VCC voltage cannot be output. Do not pull up RESET_B to VCC
Changing the resistance ratio between R4 and R5 changes the constant voltage output, thereby changing the voltage of the high level RESET_B output. Note that the constant voltage output should not exceed 18V.・R_4, R_5

・The 5V output can be used as a power supply for control circuits with low current consumption.

・In setting the R3 resistance level, caution should be given to the power consumption in the resistor. The table below lists sample resistance values for reference (using 1/4 Ω resistance).

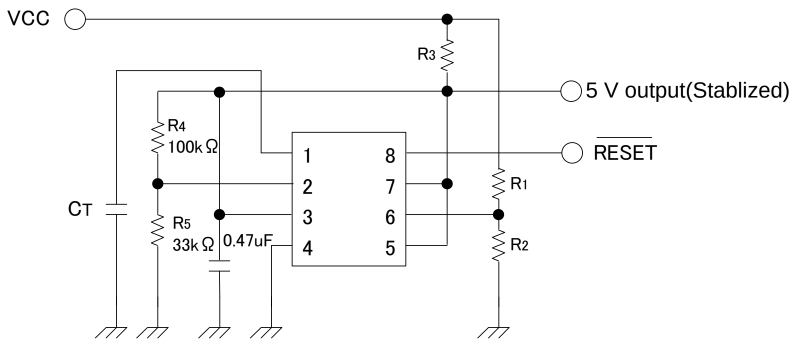


Figure 21. Application Example 3-2

④5V and 12V Power Supply Monitor (2 types of power supply monitor VCC1 = 5V, VCC2 =12V)
・5V is monitored by VSA. Detection voltage is about 4.2V
・12V is monitored by VSB. When R1 = 390 kΩ and R2 = 62 kΩ, Detection voltage is about 9.0V. Generally the detection voltage is determined by the following equation.

Detection Voltage $=(R_1+R_2)\times V_{SB}/R_2$

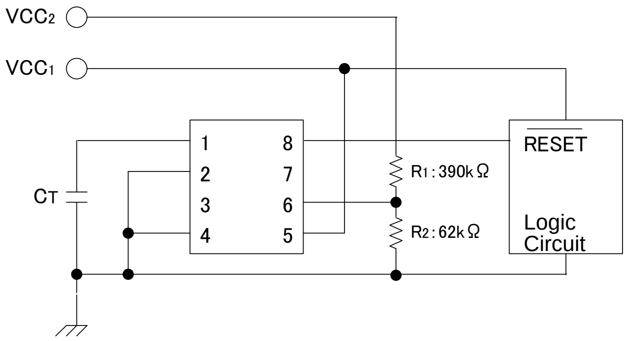


Figure 22. Application Example 4

⑤ 5V and 12V Power Supply Monitor (RESET_B signal is generated by 5V, VCC1 = 5V, VCC2 = 12V)
・5V is monitored by VSA, and generates RESET_B signal when VSA detects voltage sagging.
・12V is monitored by VSC, and generates its detection signal at OUTC
・The detection voltage of 12V monitoring and its hysteresis is determined by the following equations.

Detection voltage $= \dfrac{R_1+R_2+R_3}{R_2+R_3} \times V_{SC}$ (8.95V in the circuit above)

Hysteresis width $= \dfrac{R_1(R_3-R_3//R_4)}{(R_2+R_3)(R_2+R_3//R_4)} \times V_{SC}$ (200mV in the circuit above)

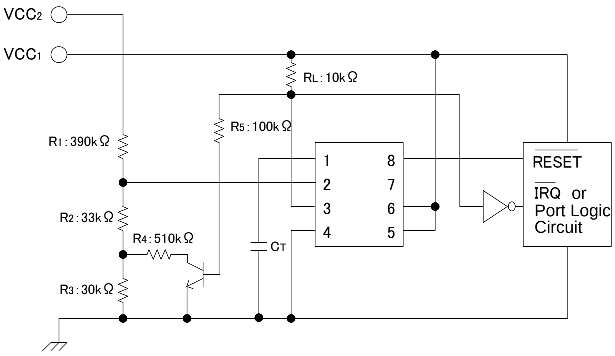


Figure 23. Application Example 5

⑥5V Power Supply Monitor with forced RESET input (VCC = 5V)
RESIN is a TTL compatible input

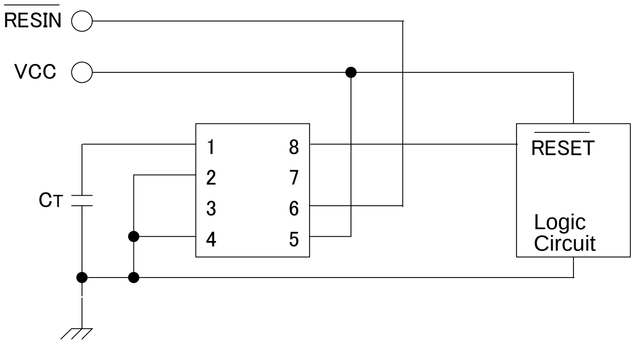


Figure 24. Application Example 6

⑦5V Power Supply Monitor with Non-inverted RESET

In this case, Comparator C is used to invert RESET signal. OUTC is an open-collector output.
RL is used a pull-up resistor.

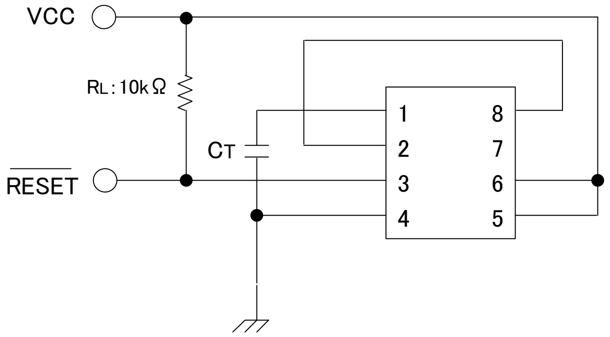


Figure 25. Application Example 7

⑧Supply Voltage Monitoring with Delayed Trigger

When the voltage shown in the diagram below is applied at VCC, the minimum value of the input pulse width is increased to 65µs (when C1 = 1000pF).

The formula for calculating the minimum value of the input pulse width [Tp] is:

Tp [µs] ≒ $6.5 \times 10^{-2} \times C_1$[pF]

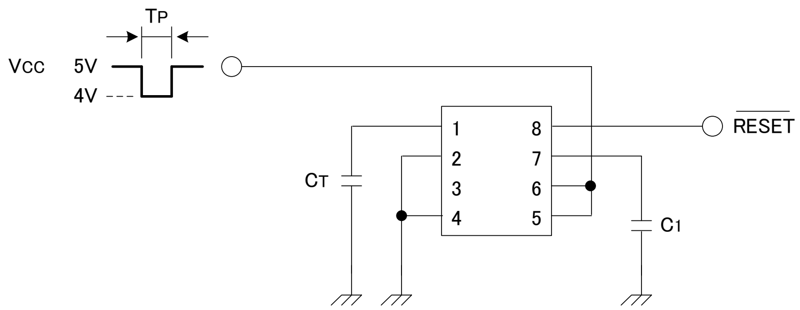


Figure 26. Application Example 8

⑨Dual (Positive/Negative) Power Supply Voltage Monitoring (VCC = 5V, VEE = Negative Power Supply)

Monitors a 5V and a negative (any given level) power supply. R1, R2, and R3 should be the same value.

Detection Voltage = $V_{SB} - V_{SB} \times R_4/R_3$

Example if $V_{EE} = -5V$, R4=91kΩ

Then the detected voltage =-4.37V

In cases where VEE may be output when VCC is not output, it is necessary to use a Schottky barrier diode (SBD).

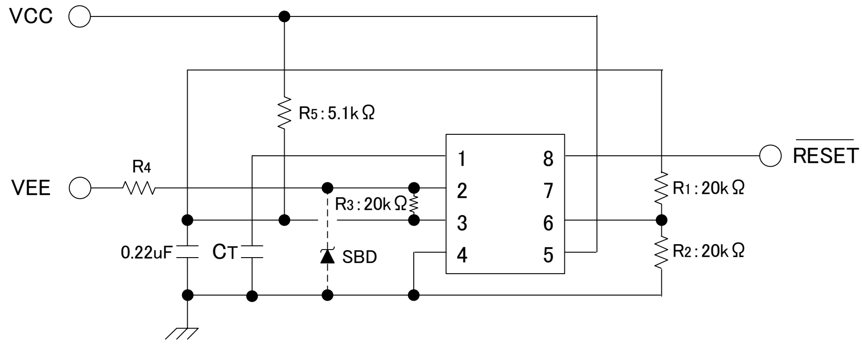


Figure 27. Application Example 9

⑩Reference Voltage Generation and Voltage Sagging Detection

(1) 9V Reference Voltage Generation and 5V/9V Monitoring

Detection Voltage = 7.2V

In the above examples, the output voltage and the detection voltage are determined by the following equations:

Detection Voltage =$(R_1 + R_2) \times V_{SB} / R_2$

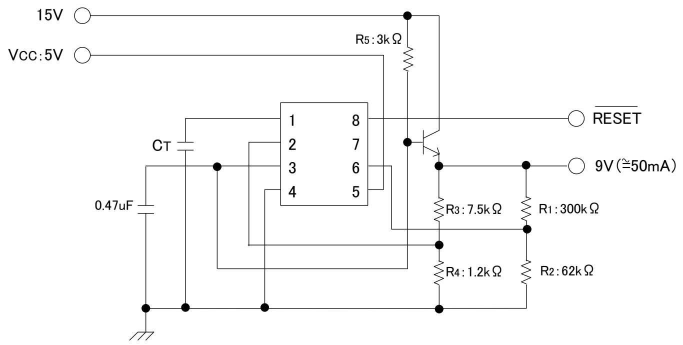


Figure 28. Application Example 10-1

(2) 5V Reference Voltage Generation and 5V Monitoring (No.1)

Detection Voltage =4.2V

In the above examples, the output voltage and the detection voltage are determined by the following equations:

Detection Voltage = $(R_3+R_4) \times V_{SC}/R_4$

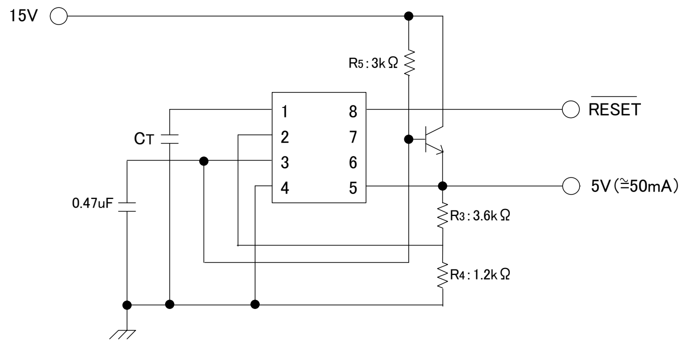


Figure 29. Application Example 10-2

(3) 5V Reference Voltage Generation and 5V Monitoring (No. 2)

The value of R1 should be calculated from the current consumption of the MB3771, the current flowing at R2 and R3, and the 5V output current.

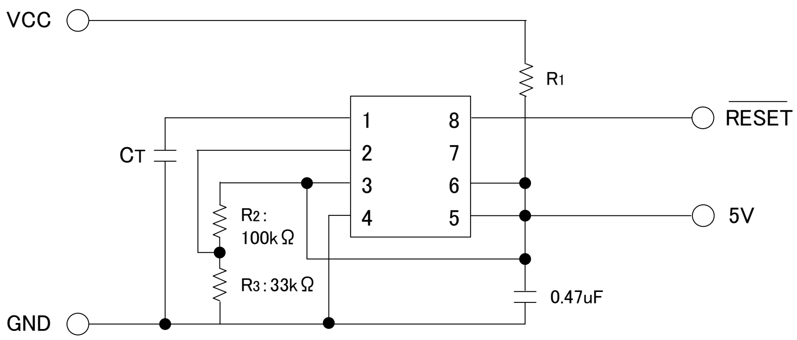


Figure 30. Application Example 10-3

(4) 1.245V Reference Voltage Generation and 5V Monitoring
Resistor R1 determines Reference current. Using 1.2kΩ as R1, reference current is about 2mA.

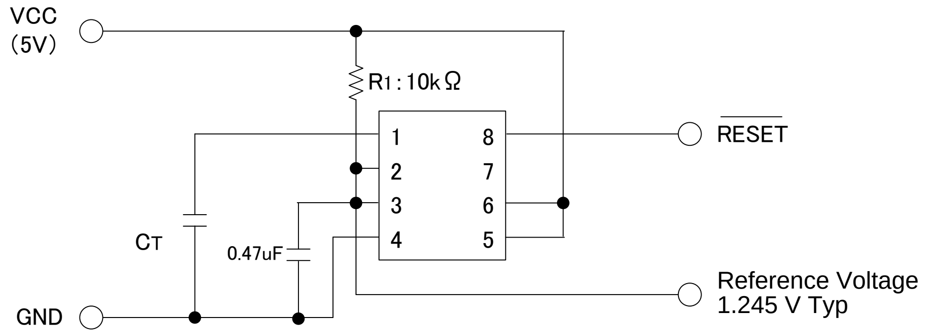


Figure 31. Application Example 10-4

●Power Dissipation

It is shown below reducing characteristics of power dissipation to mount 70mm × 70mm × 1.6mm^t, 1layer PCB.
Junction temperature must be designed not to exceed 150℃.

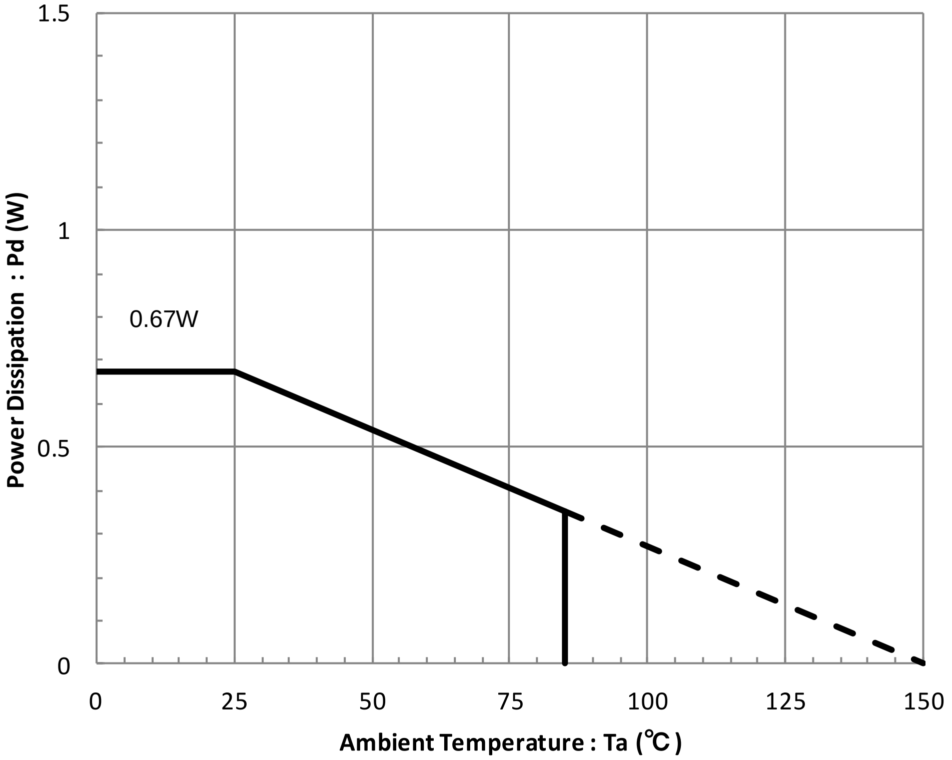


Figure 32. Power Dissipation(70mm × 70mm × 1.6mm^t 1layer PCB)

●I/O equivalent circuit

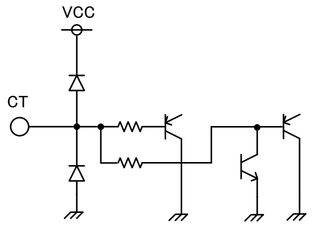
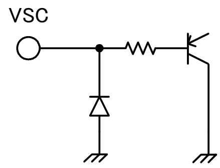
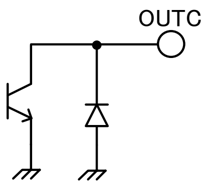
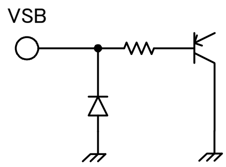
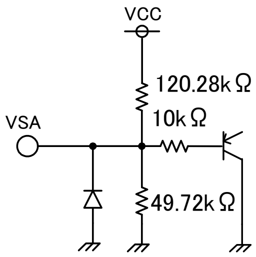
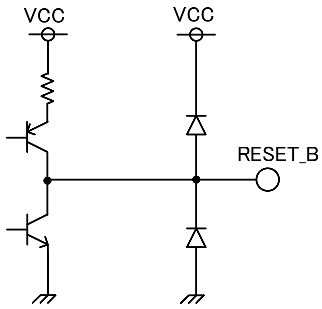
Pin.No	Pin Name	Pin Equivalent Circuit	Pin.No	Pin Name	Pin Equivalent Circuit
1	CT		2	VSC	
3	OUTC		6	VSB	
7	VSA		8	RESET_B	

Figure 33. I/O equivalent circuit

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

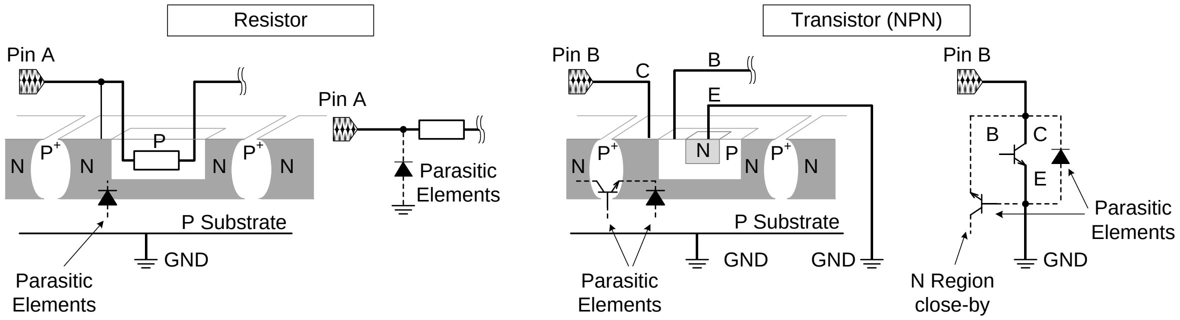


Figure 34. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

●Ordering part number

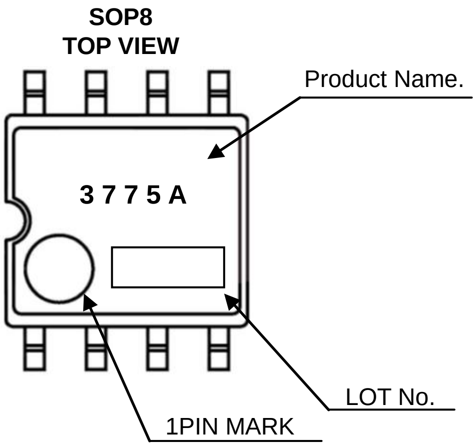
B D 3 7 7 5 A F E 2

Part Number

package
F: SOP8

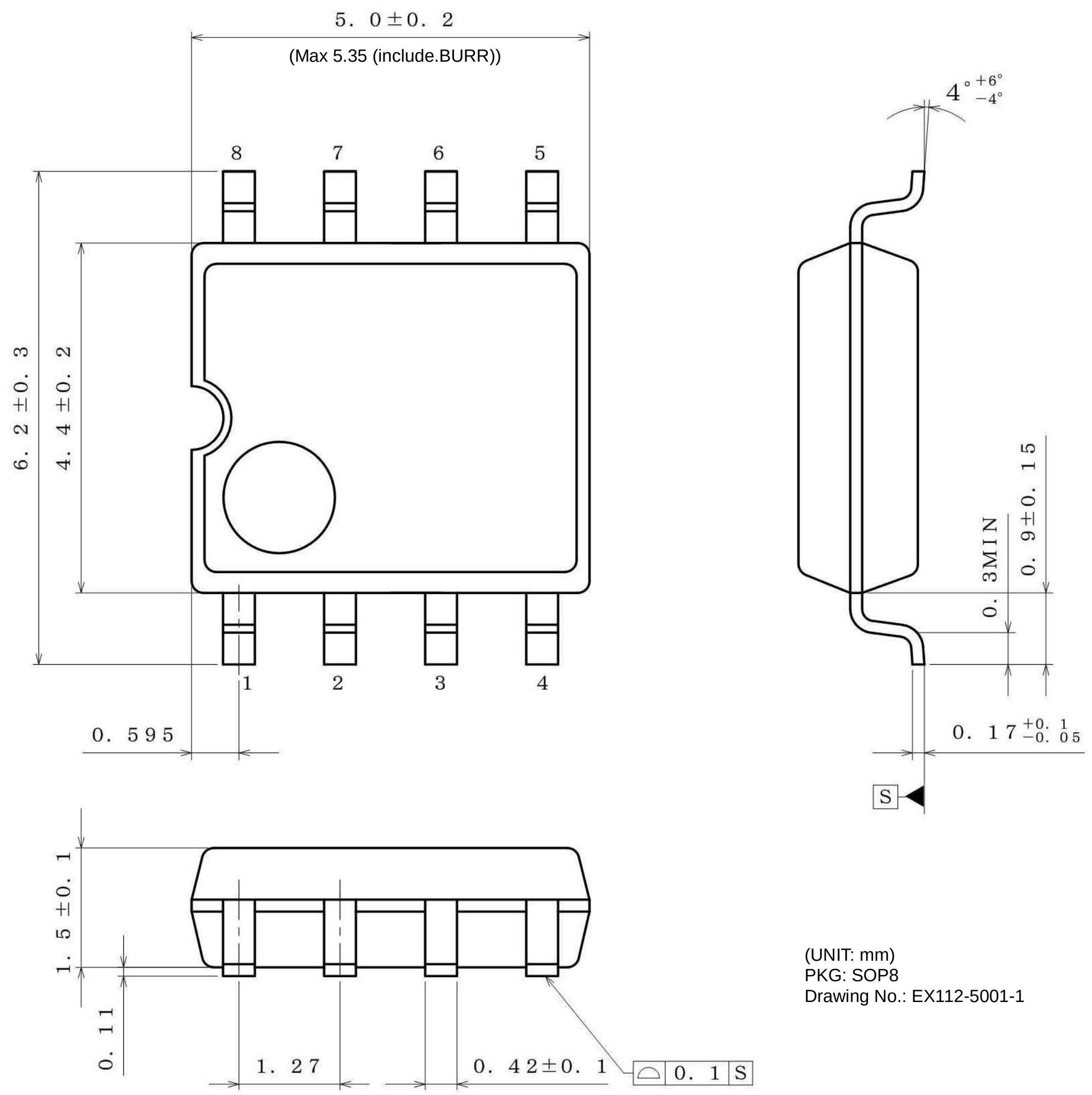
Packaging and forming specification
E2: Embossed tape and reel

●Marking Diagram



●Physical Dimension and Packing Information

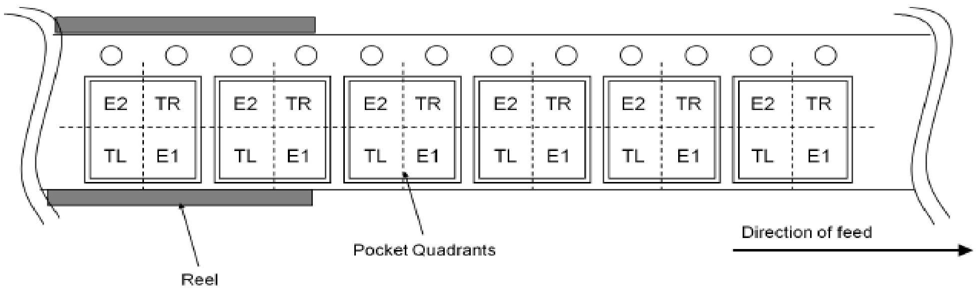
Package Name	SOP8



(UNIT: mm)
PKG: SOP8
Drawing No.: EX112-5001-1

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



●Revision History

Date	Revision	Changes
21.Nov.2012	001	New Release
26.Nov.2012	002	Correction of Typographical Error
11.SEP.2017	003	Correction of Typographical Error

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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