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BD429
ARINC 429/RS-422 Line Driver
Integrated Circuit

Features:

- ARINC 429 Line Driver for HI speed (100 kHz) and LOW speed (12.5 kHz) data rates
- Pin for Pin replacement part for industry standard ARINC 429 Line Drivers
- Available in a 16 Pin SOIC (WB), 16 Pin CERDIP and 28L PLCC
- Low EMI RS-422 line driver mode for data rates up to 100 kHz
- Adjustable slew rates via two external capacitors
- Inputs are TTL and CMOS compatible
- Low quiescent power of 125mW (typical)
- Programmable output differential range via V_{REF} pin
- Outputs are fused for failsafe overvoltage protection
- Drives full ARINC load of 400Ω and 30,000pF
- -55°C to +125°C operating temperature range
- 100% Final Testing

General Description:

The BD429 ARINC Line Driver Circuit is a bipolar monolithic IC designed to meet the requirements of several general aviation serial data bus standards. These include the differential bipolar RZ types such as ARINC 429, ARINC 571, and ARINC 575, as well as the differential NRZ types such as the RS-422 standard.

Table 1: Product Matrix Table

Product Matrix Table		
Part Number	Package Type	# of Pins
BD429	CERDIP	16
BD429A	SOIC WB	16
BD429B	PLCC	28

Functional Description:

Modes: The BD429 operates in either a 429 mode or a 422 mode as controlled by the 429/422´ pin.

429 Mode: In 429 mode, the serial data is presented on the DATA(A) and DATA(B) inputs in the dual rail format defined in the *MARK 33 Digital Information Transfer System – ARINC Specification 429-10*. The driver is enabled by the SYNC and CLOCK inputs. The output voltage level is programmed by the V_{REF} input and is normally tied to +5VDC along with V_1 to produce output levels of +5 volts, 0 volts, and –5 volts on each output for ±10 volts differential outputs. *See figure 2.

422 Mode: In 422 mode, the serial data is presented on DATA(A) input. The driver is enabled by the SYNC and CLOCK inputs. The outputs swings between 0 volts and +5 volts if V_{REF} is at +5VDC. *See figure 3.

Output Resistance: The driver output resistance is 75Ω ±20% at room temperature; 37.5Ω on each output. The outputs are also fused for failsafe protection against shorts to aircraft power. The output slew rate is controlled by external timing capacitors on C_A and C_B. Typical values are 75pF for 100 KHz data and 500pF for 12.5 KHz data.

Table 2: Pin Descriptions

Pin Name	Description
V_{REF}	Analog Input. The voltage on V_{REF} sets the output voltage levels on A_{OUT} and B_{OUT}. The output logic levels swing between $+V_{REF}$, 0 volts, and $–V_{REF}$ volts.
NC	No Connect
SYNC	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
DATA(A) DATA(B)	Logic inputs. These signals contain the Serial Data to be transmitted on the ARINC 429 data bus. Refer to Figures 2 and 3.
C_A C_B	Analog Nodes. External timing capacitors are tied from these points to ground to establish the output signal slew rate. Typical $C_A = C_B = 75pF$ for 100 kHz data and $C_A = C_B = 500pF$ for 12.5 kHz data. *
A_{OUT} B_{OUT}	Outputs. These are the line driver outputs which are connected to the aircraft serial data bus.
-V	Negative Supply Input. –15VDC nominal.
GND	Ground.
+V	Positive Supply Input. +15VDC nominal.
CLOCK	Logic input. Logic 0 forces outputs to NULL state. Logic 1 enables data transmission.
429/422'	Logic Input. Mode control for ARINC 429 and RS-422 modes. An internal 10KΩ pull up resistor keeps the chip in ARINC 429 mode when there is no external connection. This creates a default logic 1, enabling the ARINC 429 mode. A forced logic 0 enables the RS-422 mode.
V_1	Logic Supply Input. +5VDC nominal.

*C_A and C_B pin voltages swing between ±5 volts. Any electronic switching of the capacitor on the pins must not inhibit the full voltage swings.

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Table 3: Truth Table								
	429/422' NOTE 1	SYNC NOTE 2	CLOCK NOTE 2	DATA(A) NOTE 2	DATA(B) NOTE 2	A_{OUT}	B_{OUT}	COMMENTS
429 MODE	H	L	X	X	X	0	0	NULL
	H	X	L	X	X	0	0	NULL
	H	H	H	L	L	0	0	NULL
	H	H	H	H	H	0	0	NULL
	H	H	H	H	L	$+V_{REF}$	$-V_{REF}$	LOGIC 1
	H	H	H	L	H	$-V_{REF}$	$+V_{REF}$	LOGIC 0
422 MODE	L	L	X	X	X	$+V_{REF}$	0	NULL
	L	X	L	X	X	$+V_{REF}$	0	NULL
	L	H	H	L	X	0	$+V_{REF}$	LOGIC 0
	L	H	H	H	X	$+V_{REF}$	0	LOGIC 1

NOTES:

1. The 429/422' pin is internally pulled up to V_1 through a 10kΩ resistor. So, if no external connection is made to this pin, it will force the chip into the 429 mode.
2. X = Don't care.

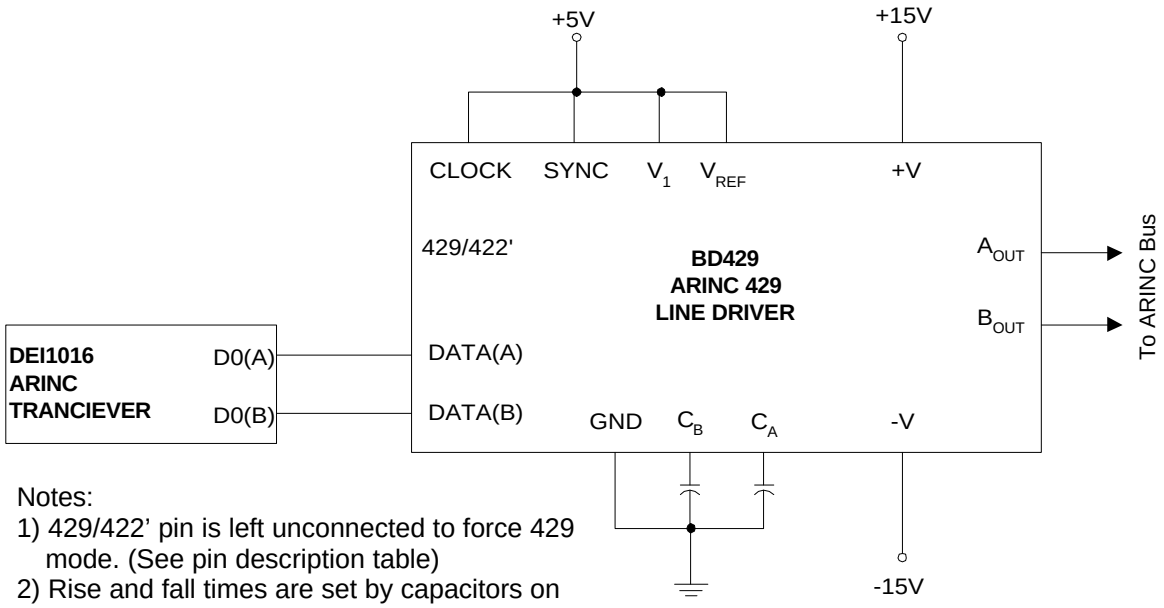
Table 4: Absolute Maximum Ratings			
PARAMETER	SYMBOL	RATING	UNITS
Voltage between pins +V and –V		40	V
V_1 Maximum Voltage	V_1	7	V
V_{REF} Maximum Voltage	V_{REF}	6	V
DATA(A) Max Input Voltage DATA(B) Max Input Voltage	$V_{DATA(A)}$ $V_{DATA(B)}$	(GND-0.3V) to (V_1 + 0.3V)	V
Output Short Circuit Duration		Note1	
Output Over-voltage Protection		Note2	
Lead Soldering Temperature (10 sec duration)	T_{SLD}	280	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation	See Power Dissipation Table		

Notes.
1. One output at a time can be shorted to ground indefinitely.
2. Both outputs are fused at between 0.5 Amp DC and 1.0 Amp DC to prevent an over-voltage fault from coupling onto the system power bus.

Table 5: Operating Range					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Positive Supply Voltage	+V	+11.4		16.5	VDC
Negative Supply Voltage	-V	-11.4		-16.5	VDC
V_1	V_1	+4.75	+5	+5.25	VDC
V_{REF} (For ARINC 429)	V_{REF}	+4.75	+5	+5.25	VDC
V_{REF} (For other applications)	V_{REF}	+3		+6	VDC
Operating Temperature	T_A	-40		+85	°C
Max Operating Junction Temperature	T_J			+175	°C

Table 6: Power Dissipation Table						
Full Load = 400Ω/30,000pF Half Load = 4,000Ω/10,000pF						
DATA RATE	LOAD	+V @ 15V	-V @ -15V	$V_1 + V_{REF}$ @5V	429 POWER	LOAD POWER
0 to 100kbps	NONE	2.0mA	-5.0mA	4mA	125mW	0.0mW
12.5kbps	FULL	16.0mA	19.0mA	4mA	485mW	60.0mW
100kbps	FULL	48.0mA	51.0mA	4mA	1194mW	325.0mW
12.5kbps	HALF	6.0mA	8.0mW	4mA	196mW	30.0mW
100kbps	HALF	22.0mA	25.0mA	4mA	561mW	162.5mW

Table 7: Thermal Characteristics			
Parameter	BD429	BD429A	BD429B
Storage Temp (min/max)	-65/+150 °C	-65/+150 °C	-65/+150 °C
Ambient Operating Temp	-55 °C to +125 °C	-40 °C to +85 °C	-40 °C to +85 °C
Junction to ambient (θ_{JA})	75°C/W	75°C/W	55°C/W
Max Junction Temp.	175 °C	175 °C	175 °C



Notes:
1) 429/422' pin is left unconnected to force 429 mode. (See pin description table)
2) Rise and fall times are set by capacitors on C_A and C_B pins. (See pin description table)

Figure 1: BD429 Typical Application

Table 8: DC Electrical Characteristics						
Conditions: Temperature: -40°C to +85°C; +V = +11.4VDC to +16.5VDC, –V = -11.4VDC to –16.5VDC; $V_1 = V_{REF}$ = +5VDC ±5%, 429/422' = Open Circuit (unless otherwise noted.)						
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
IQ+V	Quiescent +V supply current	-	2	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
IQ-V	Quiescent -V supply current	-	5	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
IQV_1	Quiescent V_1 supply current	-	4	-	mA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
IQV_{REF}	Quiescent V_{REF} supply current	-	10	-	µA	No Load. 429 mode. DATA = CLOCK = SYNC = LOW
V_{IH}	Logic 1 Input V	2.0	-	-	V	No Load.
V_{IL}	Logic 0 Input V	-	-	0.6	V	No Load.
I_{IH}	Logic 1 Input I	-	-	10	µA	No Load.
I_{IL}	Logic 0 Input I	-	-	-20	µA	No Load. (429/422´ Pin I_{IL} = -2mA max)
I_{OHSC}	Output Short Circuit Current (Output High)	-80	-	-	mA	Short to Ground
I_{OLSC}	Output Short Circuit Current (Output Low)	80	-	-	mA	Short to Ground
V_{OH}	Output Voltage HIGH. (+1)	V_{REF} - 250mV	V_{REF}	V_{REF} + 250mV	V	No Load. 429 Mode.
V_{NULL}	Output Voltage NULL. (0)	-250	-	+250	mV	No Load. 429 Mode.
V_{OL}	Output Voltage LOW. (-1)	$-V_{REF}$ – 250mV	$-V_{REF}$	$-V_{REF}$ + 250mV	V	No Load. 429 Mode.
I_{CT} + -	Timing Capacitor Charge Current C_A (+1) C_B (-1) C_A (-1) C_B (+1)	-	 +200 –200	-	 µA µA	No Load. 429 Mode. SYNC = CLOCK = HIGH C_A and C_B held at zero volts.
ISC (+V)	+V Short Circuit Supply Current	-	-	+150	mA	Output short to ground
ISC (-V)	-V Short Circuit Supply Current	-	-	-150	mA	Output short to ground
R_{OUT}	Resistance on each output	-	37.5	-	Ω	Room Temp Only
C_{IN}	Input Capacitor	-	-	15	pF	-

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AC ELECTRICAL CHARACTERISTICS

Figures 2 and 3 show the output waveforms for the ARINC 429 and RS-422 modes of operation.

The output slew rates are controlled by timing capacitors C_A and C_B. They are charged by ±200µA (nom.) Slew rate (SR) measured as V/µsec, is calculated by:

SR = 200/C
where C is in pF.

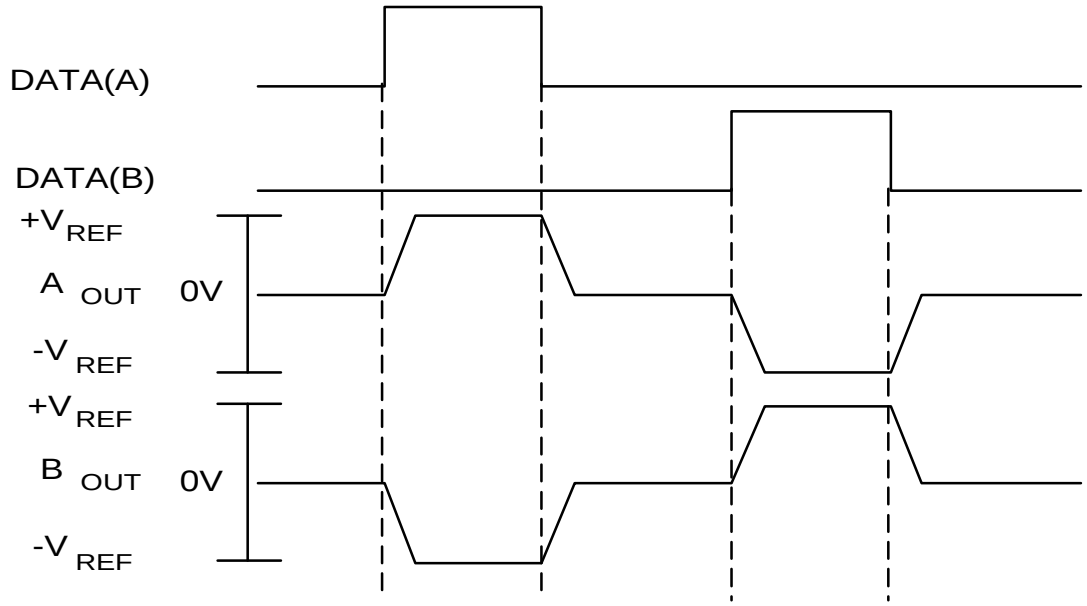


Figure 2: ARINC 429 Waveforms

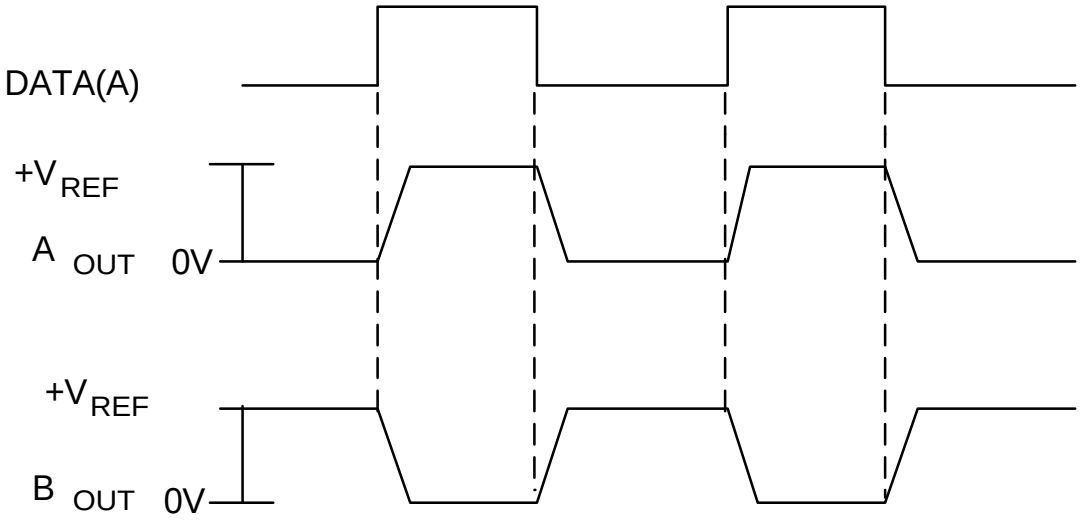
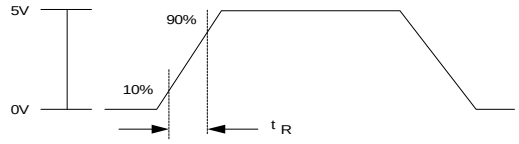
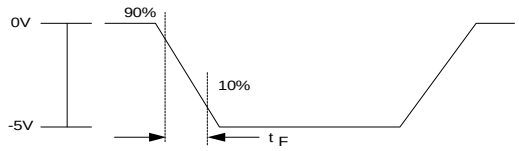


Figure 3: RS-422 Waveforms

Table 9: AC Electrical Characteristics					
Parameter	Symbol	MIN	MAX	UNITS	NOTES
Output Rise Time A_{OUT} or B_{OUT} $C_A = C_B = 75pF$ $C_A = C_B = 500pF$	 t_R t_R	 1.0 5.0	 2.0 15.0	 µsec µsec	
Output Fall Time A_{OUT} or B_{OUT} $C_A = C_B = 75pF$ $C_A = C_B = 500pF$	 t_F t_F	 1.0 5.0	 2.0 15.0	 µsec µsec	
Input to Output Propagation Delay	t_{PNH} t_{PNL}	-	3.0	µsec	See Figure 4 below
A_{OUT} / B_{OUT} Skew Spec.	-	-	500	nsec	

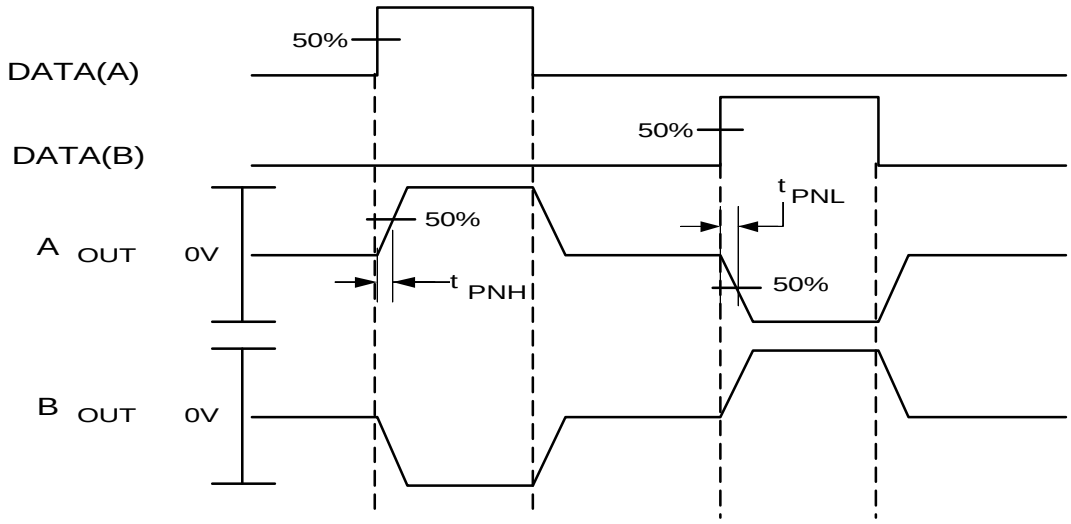


Figure 4: Propagation Delay

Table 10: Package Description Table			
	BD429	BD429A	BD429B
No. of Pins	16	16	28
Package Type	CERDIP	WB SOIC	PLCC
Marking	BD429 Lot Code Date Code	BD429A Lot Code Date Code	BD429B Lot Code Date Code
Screening Procedure	A	B	B

Component Screening

Screening Procedure A: All components tested under this procedure shall be screened as follows:

Thermal cycle:
MIL-STD-883B Method 1010.4 test condition B.

Burn-in (minimum):
96 hrs @ 125°C per MIL-STD-883 method 1015 condition A.

DC parametric and functional test:
All burned in components will be tested @ 25°C per manufacturer's specification. Tests will be completed within 96 hours of removal from burn-in.

Screening Procedure B: All components tested under this procedure shall be screened as follows:

DC parametric and functional test.
All components will be tested @ 25°C per manufactures specification.

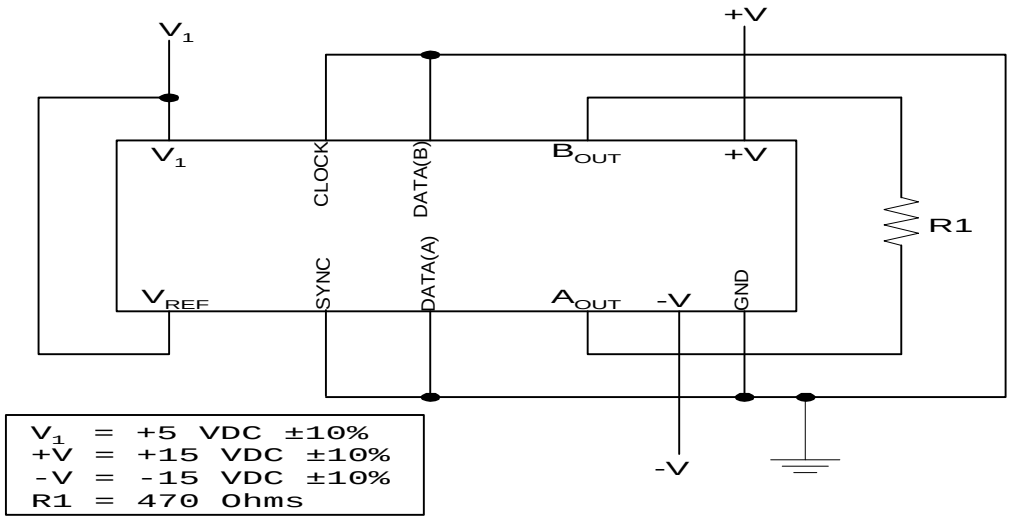
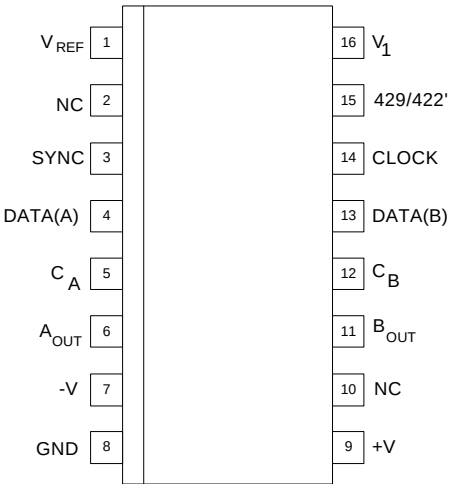
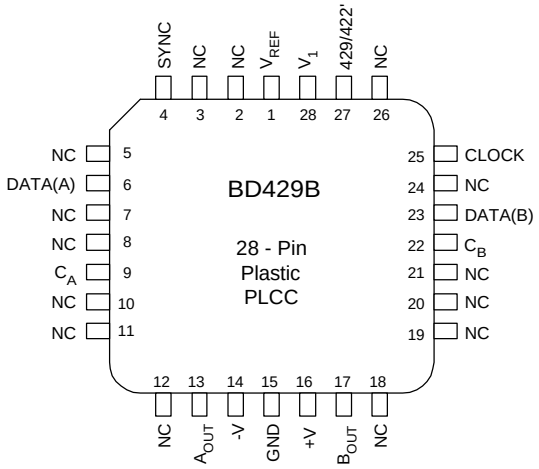


Figure 5: Burn-in Schematic

Table 11: Package Pinout Table					
PIN #	BD429 (16L CERDIP)	BD429A (16L WB SOIC)	BD429B (28L PLCC)	PIN #	BD429B (28L PLCC)
1	V_{REF}	V_{REF}	V_{REF}	17	B_{OUT}
2	NC	NC	NC	18	NC
3	SYNC	SYNC	NC	19	NC
4	DATA(A)	DATA(A)	SYNC	20	NC
5	C_A	C_A	NC	21	NC
6	A_{OUT}	A_{OUT}	DATA(A)	22	C_B
7	-V	-V	NC	23	DATA(B)
8	GND	GND	NC	24	NC
9	+V	+V	C_A	25	CLOCK
10	NC	NC	NC	26	NC
11	B_{OUT}	B_{OUT}	NC	27	429/422'
12	C_B	C_B	NC	28	V_1
13	DATA(B)	DATA(B)	A_{OUT}		
14	CLOCK	CLOCK	-V		
15	429/422'	429/422'	GND		
16	V_1	V_1	+V		



BD429 (16L CERDIP) and
BD429B (16L SOIC WB)



BD429B Pinout (28L PLCC)

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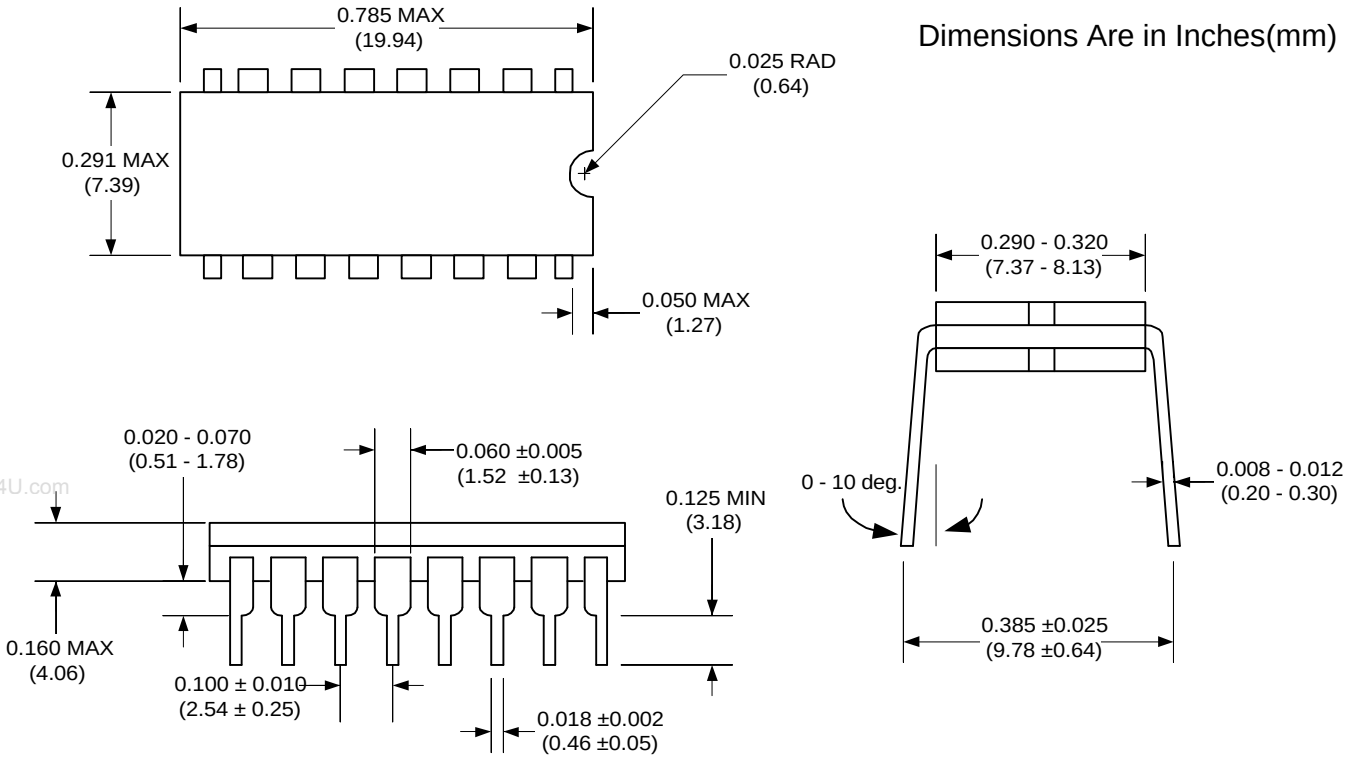
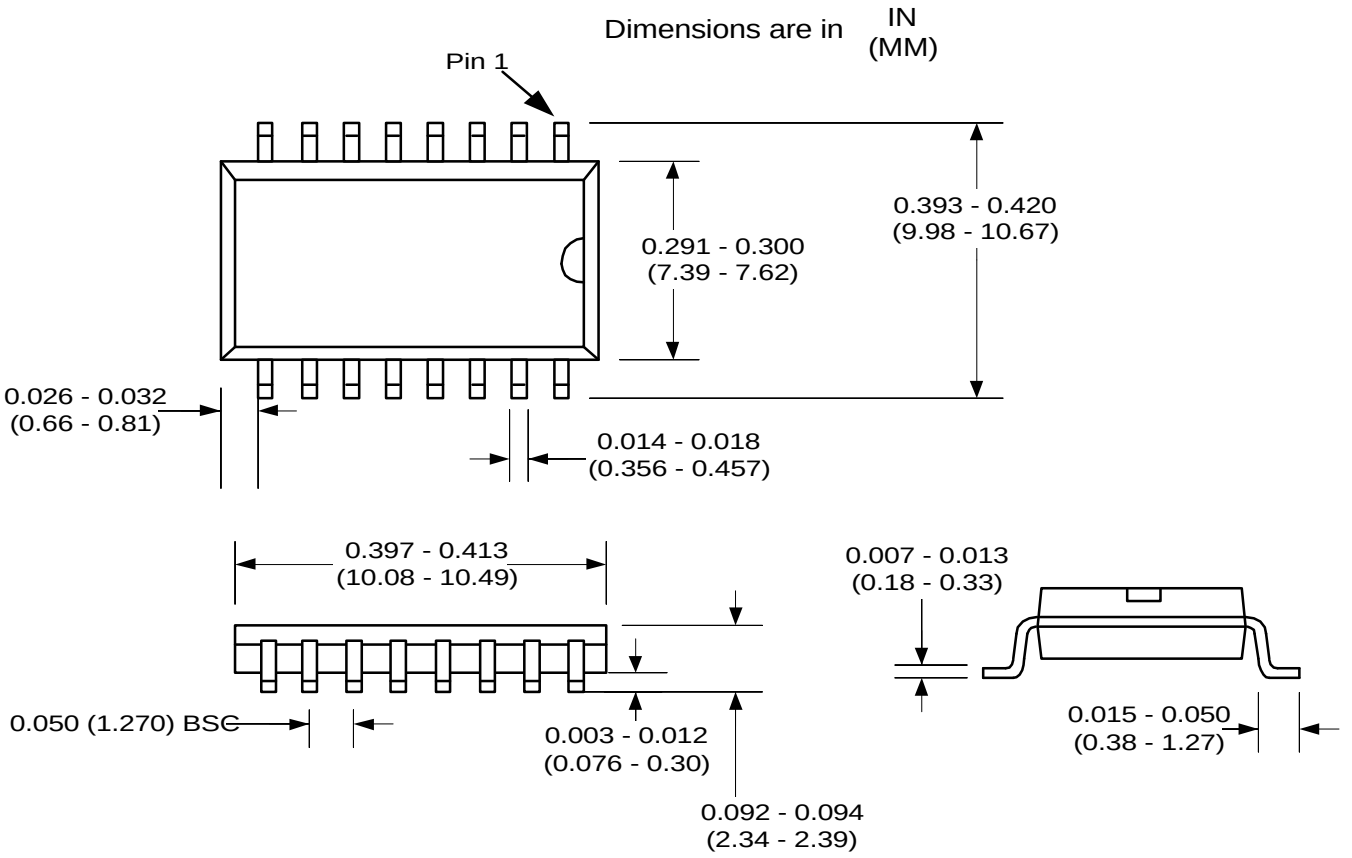
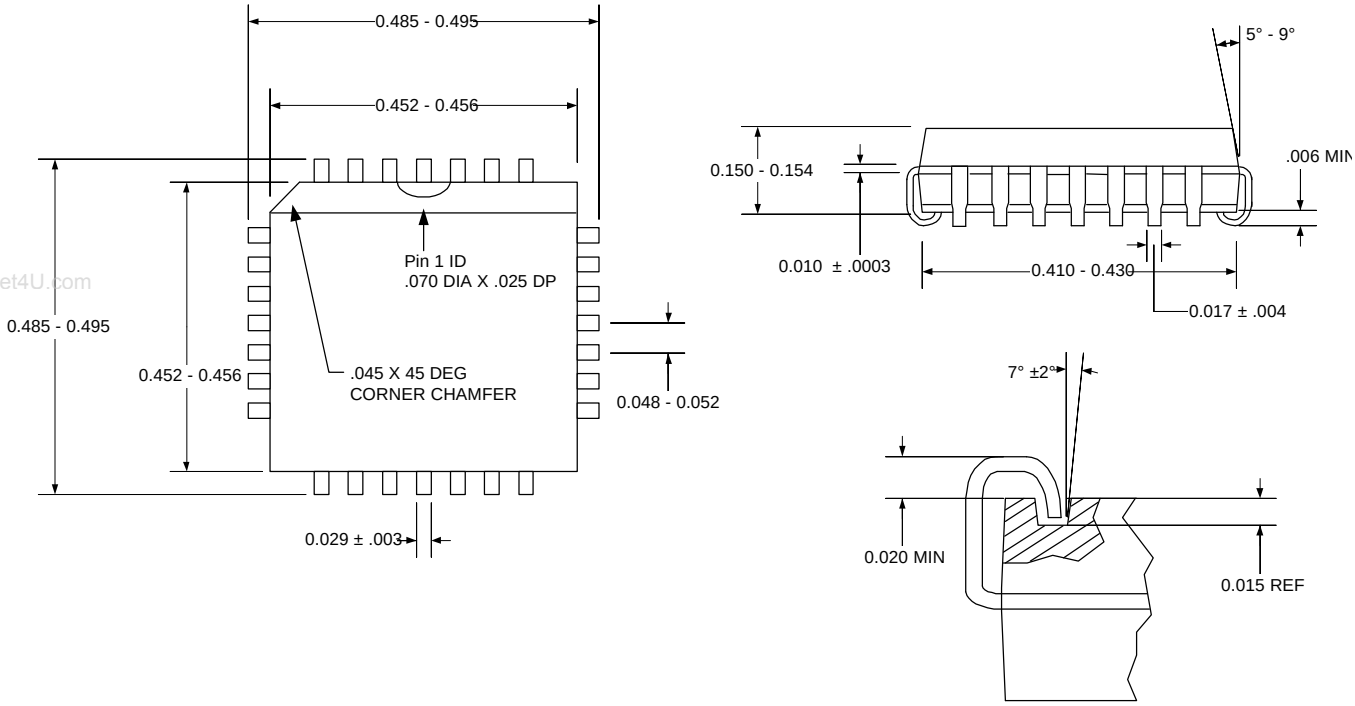


16 Pin CERDIP Package Dimensions



16 Pin SOIC WB Package Dimensions

NOTES: 1. ALL DIMENSIONS IN INCH.
2. SURFACE FINISH, MATTE, CHARMILLE #24-27
3. LEAD COPLANARITY AFTER FORM TO BE WITHIN .004.



28 Lead PLCC Package Dimensions