100mA Fixed Output for Automotive
LDO Regulator

BDxxFA1MG-M

● General Description

BDxxFA1MG-M is an LDO regulator with output current capability of 0.1A and output voltage of 5.0V. The SSOP5 package can contribute to the downsizing of the set. As protective function to prevent IC from destruction, this chip has built-in over current protection circuit to protect the device when output is shorted and built-in thermal shutdown circuit to protect the IC during thermal over load conditions. This regulator can use ceramic capacitor, which have smaller size and longer life than other capacitors.

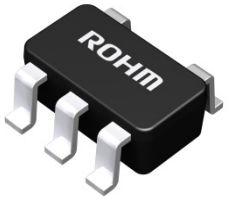
● Features

- AEC-Q100 Qualified *(Note1)*
- Built-in high accuracy reference voltage circuit
- Built-in Over current protection circuit (OCP)
- Built-in Temperature protection circuit (TSD)
- Zero μA shutdown mode
- Soft start function

(Note1 Grade2)

●Package

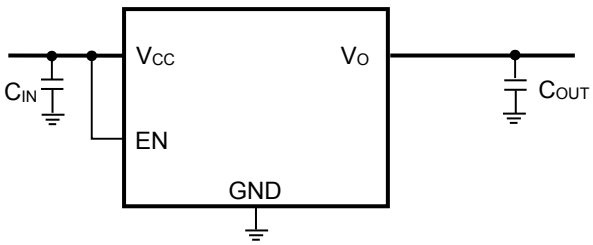
	W(Typ.)	D(Typ.)	H(Max.)
SSOP5	2.90mm	x2.80mm	x 1.25mm



● Key Features

- Input power supply voltage range: Vo+3.0V to 25.0V
- Output voltage: 5.0V
- Output current: 0.1A (Max)
- Shutdown current: 0μA (Typ)
- Operating temperature range: -40°C to +105°C

●Typical Application Circuit



C_{IN}, C_{OUT} : Ceramic Capacitor

●Ordering Information

B	D	x	x	F	A	1	M	G	-	MTR

Part Number	Output voltage	Input Voltage	Output Current	"M" Series	Package	Product Rank / Packaging Specification
	50:5.0V	F:30V	A1:0.1A		G:SSOP5	M:for Automotive TR: Embossed tape and reel

○ Product structure : Silicon monolithic integrated circuit ○This product is not designed to have protection against radioactive rays.

● **Block Diagram**

BDxxFA1MG-M

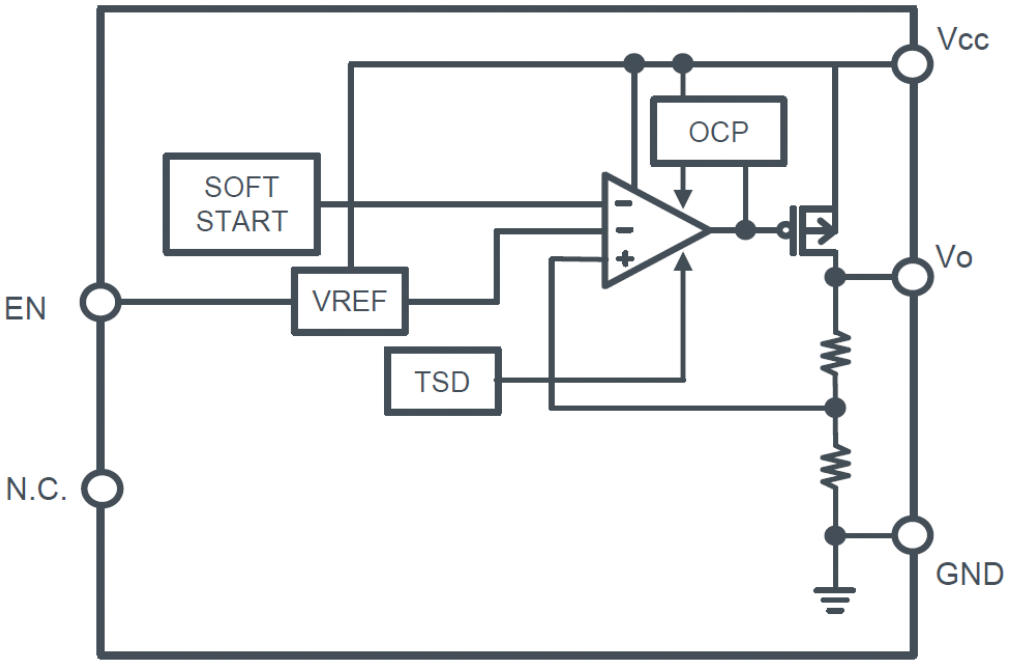
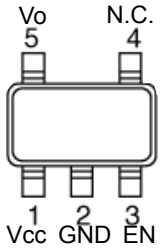


Figure 1. Block Diagram

●**Pin Description**

Pin No.	Pin name	Pin Function
1	V_{CC}	Input pin
2	GND	GND pin
3	EN	Enable pin
4	N.C. *(Note1)*	No Connection (Connect to GND or leave OPEN)
5	Vo	Output pin

(Note 1) N.C. Pin can be open since it is not connected inside of IC



● **Absolute Maximum Ratings (Ta=-40°C to +105°C)**

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{CC}	-0.3 to +30.0 *(Note1)*	V
EN voltage		V_{EN}	-0.3 to +30.0	V
Power dissipation	SSOP5	Pd	332 *(Note2)*	mW
Operating temperature range		Topr	-40 to +105	°C
Storage temperature range		Tstg	-55 to +150	°C
Maximum junction temperature		Tjmax	+150	°C

(Note1) Not to exceed Pd.
(Mote2) In case Ta≧25°C (When mounted on a single-layer glass epoxy board with 114.3mm×76.2mm×1.57mm dimension) is reduced by 2.66mW/°C

● **Recommended Operating Conditions (Ta=-40°C to +105°C)**

Parameter	Symbol	Min.	Max.	Unit
Input power supply voltage	V_{CC}	Vo+3.0	25.0	V
EN voltage	V_{EN}	0.0	25.0	V
Output voltage setting range	V_O	3.0	12.0	V
Output current	I_O	0.0	0.1	A

●**Recommended Operating Condition**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Capacitor	C_{IN}	1.0 *(Note3)*	2.2	-	μF	Ceramic capacitor recommended
Output Capacitor	C_{OUT}	1.0 *(Note3)*	2.2	-	μF	Ceramic capacitor recommended

(Note3) The minimum value of capacitor must meet this specification over full operating conditions. (Ex: Temperature, DC bias)

● **Electrical Characteristics (Unless otherwise specified, Vcc=10V, EN=3V, Ta=-40°C to +105°C)**

Parameter	Symbol	Temp	Min.	Typ.	Max.	Unit	Conditions
Circuit current at shutdown mode	I_{SD}	25℃	-	0	5	μA	V_{EN}=0V, OFF mode
		-40℃ to +105℃	-	-	5		
Bias current	I_{CC}	25℃	-	300	450	μA	
		-40℃ to +105℃	-	-	500		
Line Regulation	Reg.I	25℃	-1	+0.5	+1	%	V_{CC} =(Vo+3V)→25.0V
		-40℃ to +105℃	-1	+0.5	+1		
Load Regulation	Reg I_O	25℃	-1.5	+0.5	+1.5	%	I_O=0→0.1A
		-40℃ to +105℃	-1.5	+0.5	+1.5		
Minimum dropout voltage	V_{CO}	25℃	-	2	3	V	I_O=0.1A
		-40℃ to +105℃	-	-	3		
Output Voltage	Vo	25℃	Vo x 0.985	Vo	Vo x 1.015	V	I_O=0.1A
		-40℃ to +105℃	Vo x 0.98	Vo	Vo x 1.02		
EN Low voltage	V_{EN} (Low)	25℃	0	-	0.8	V	
		-40℃ to +105℃	0	-	0.8		
EN High voltage	V_{EN} (High)	25℃	2.4	-	25.0	V	
		-40℃ to +105℃	2.4	-	25.0		
EN Bias current	I_{EN}	25℃	1	3	9	μA	
		-40℃ to +105℃	-	-	9		

●Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SSOP5				
Junction to Ambient	θ_{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	40	30	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air).
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 4)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm^2 (Square)	35µm	74.2mm^2(Square)	70µm

(Note 5) This thermal via connects with the copper pattern of all layers

●**Performance Curve (Reference Data)**

■**BD50FA1MG-M**

(Unless otherwise specified, Ta=25°C, Vcc=10V, EN=3V, C_{IN}=C_{OUT}=2.2µF)

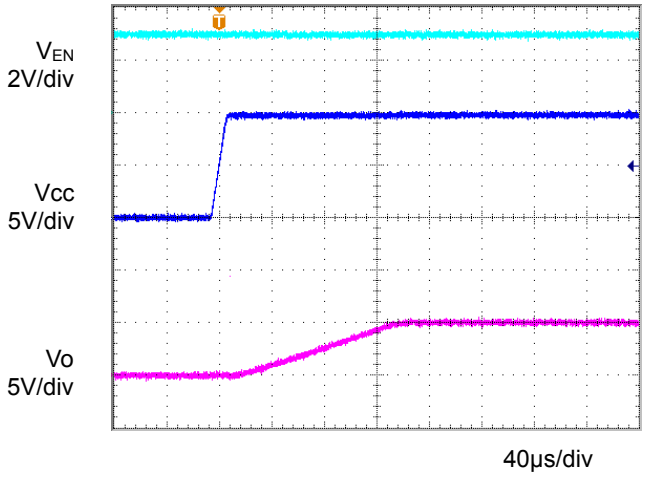


Figure 2. Input sequence (25°C)
(C_{OUT} = 1µF)

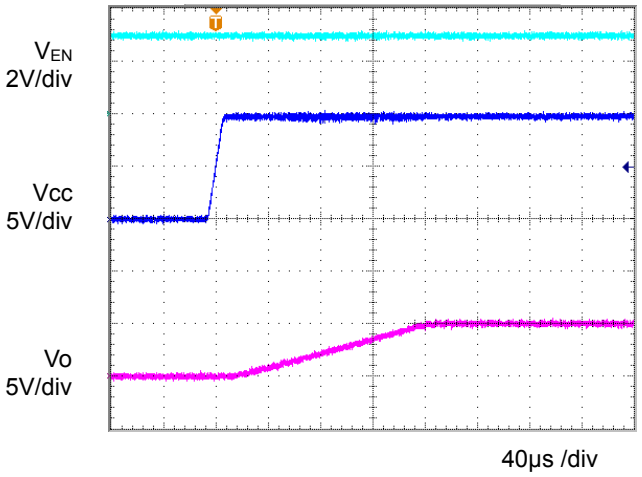


Figure 3. Input sequence (-40°C)
(C_{OUT} = 1µF)

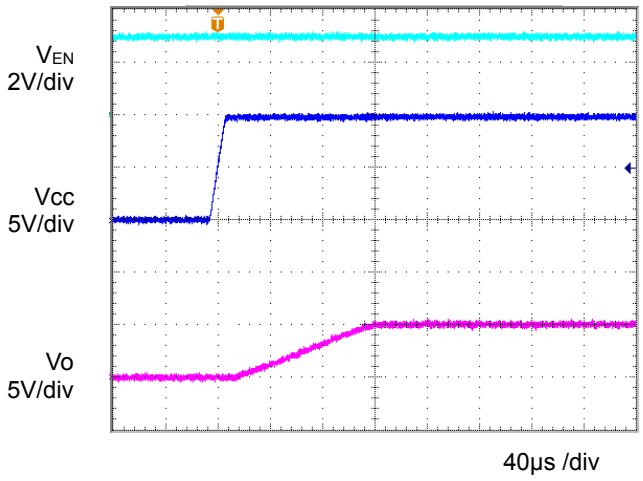


Figure 4. Input sequence (105°C)
(C_{OUT} = 1µF)

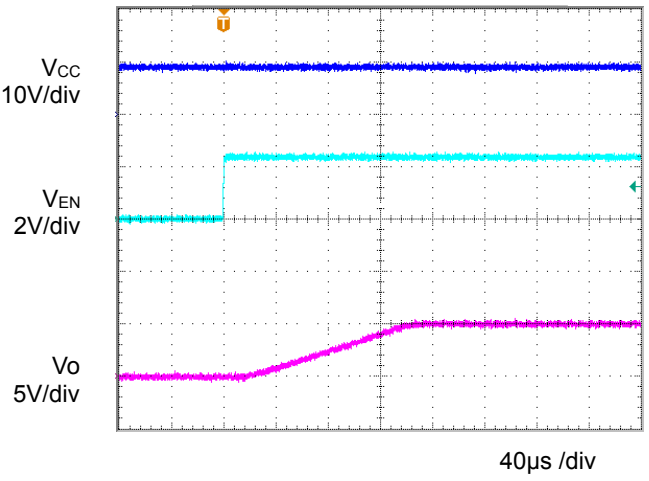


Figure 5. Input sequence (25°C)
(C_{OUT} = 1µF)

●**Performance Curve (Reference Data)**

■**BD50FA1MG-M**

(Unless otherwise specified, Ta=25°C, Vcc=10V, EN=3V, C_{IN}=C_{OUT}=2.2µF)

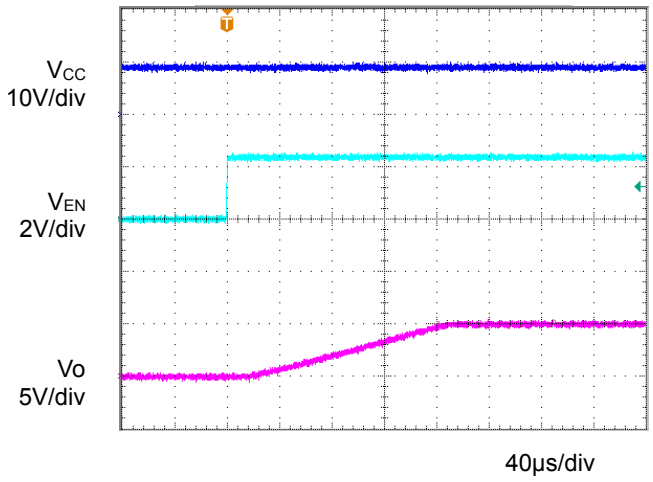


Figure 6. Input sequence (-40°C)
(C_{OUT} = 1µF)

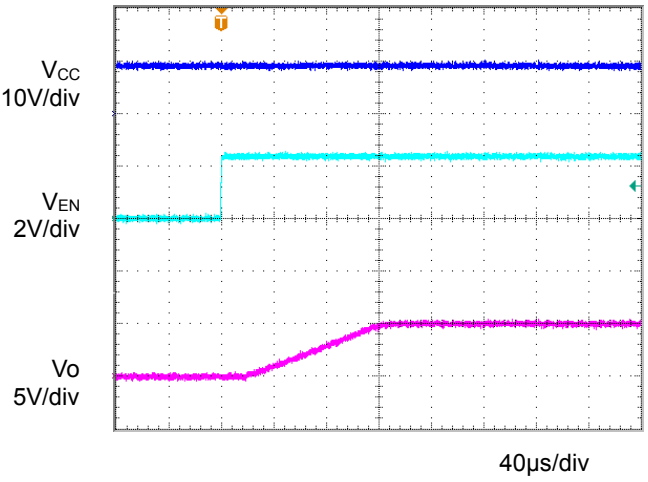


Figure 7. Input sequence (105°C)
(C_{OUT} = 1µF)

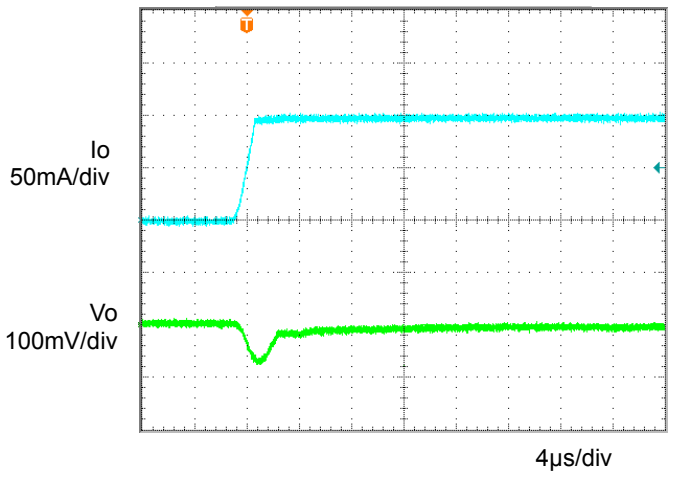


Figure 8. Transient Response (25°C)
(Io = 0A→0.1A)
(C_{OUT} = 1µF)

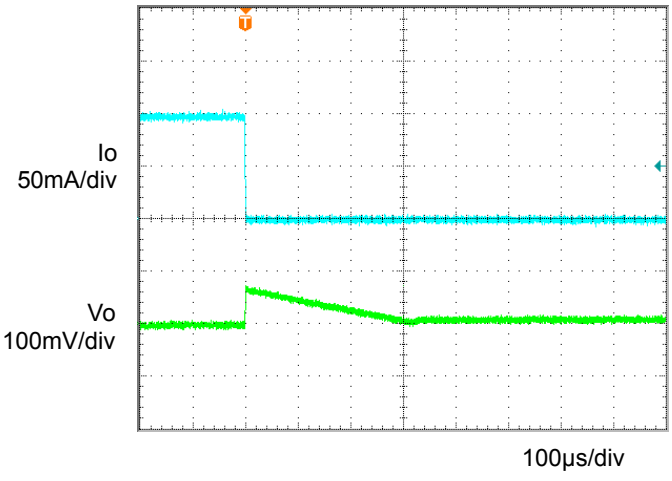


Figure 9. Transient Response (25°C)
(Io = 0.1A→0A)
(C_{OUT} = 1µF)

●**Performance Curve (Reference Data)**

■**BD50FA1MG-M**

(Unless otherwise specified, Ta=25°C, Vcc=10V, EN=3V, C_{IN}=C_{OUT}=2.2µF)

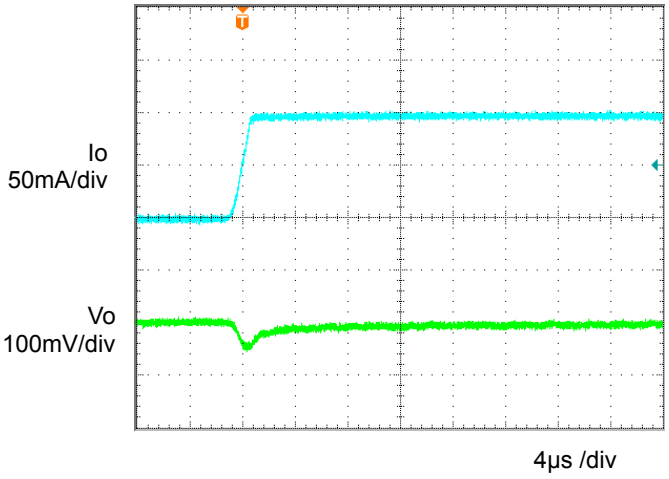


Figure 10. Transient Response (-40°C)
(Io = 0A→0.1A)
(C_{OUT} = 1µF)

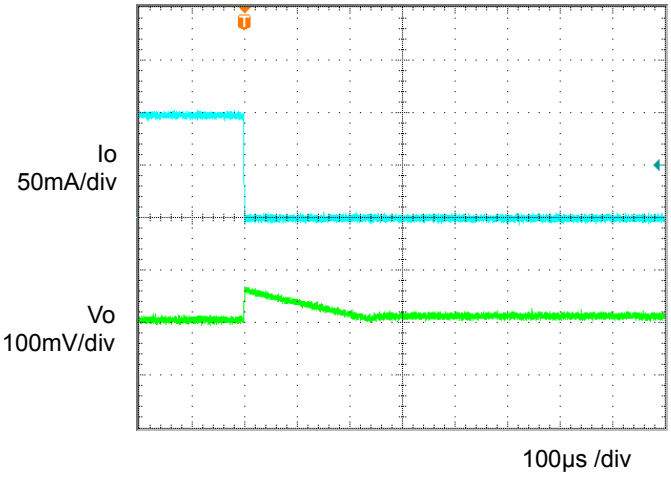


Figure 11. Transient Response (-40°C)
(Io = 0.1A→0A)
(C_{OUT} = 1µF)

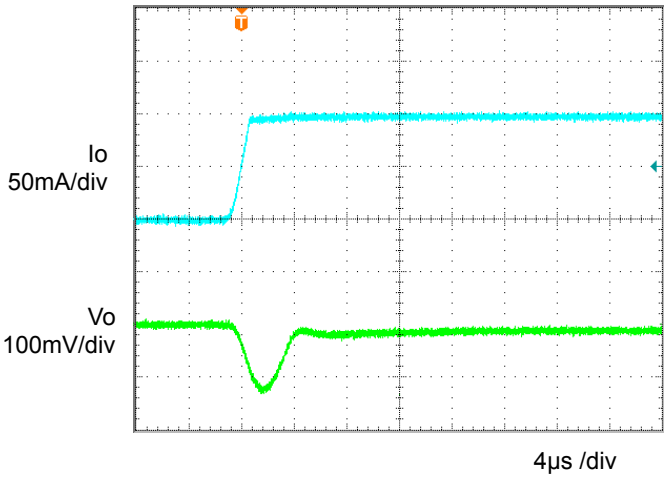


Figure 12. Transient Response (105°C)
(Io = 0A→0.1A)
(C_{OUT} = 1µF)

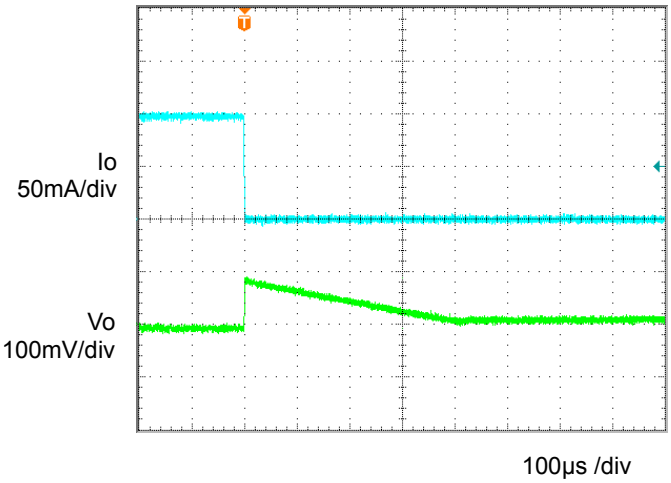


Figure 13. Transient Response (105°C)
(Io = 0.1A→0A)
(C_{OUT} = 1µF)

●**Performance Curve (Reference Data)**

■**BD50FA1MG-M**

(Unless otherwise specified, Ta=25°C, Vcc=10V, EN=3V, C_{IN}=C_{OUT}=2.2μF)

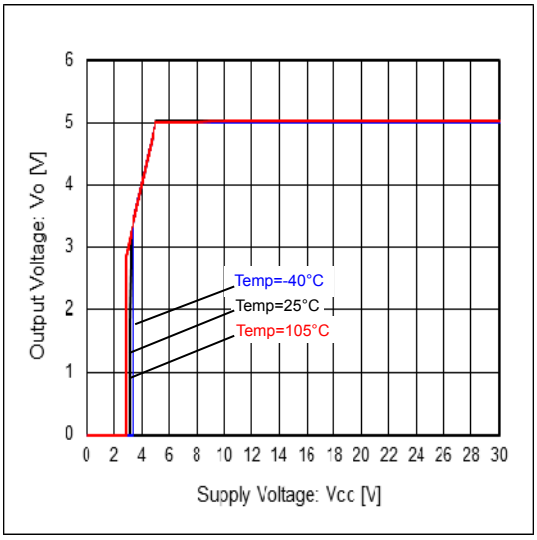


Figure 14. Vcc - Vo

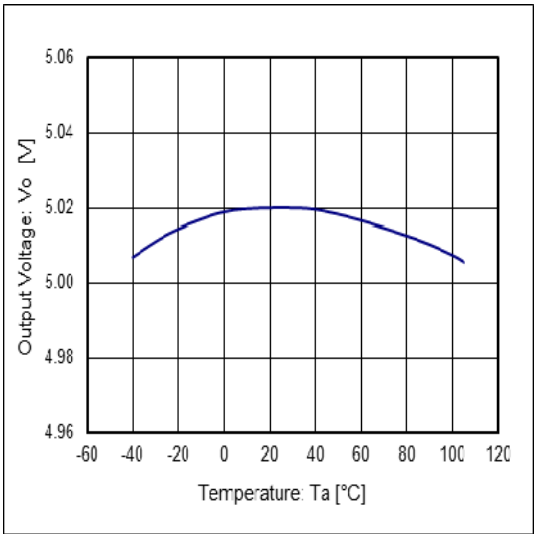


Figure 15. Ta - Vo
(Io = 0mA)

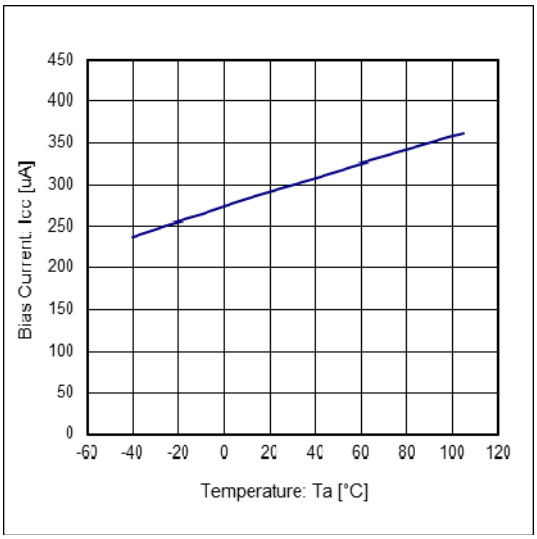


Figure 16. Ta - Icc

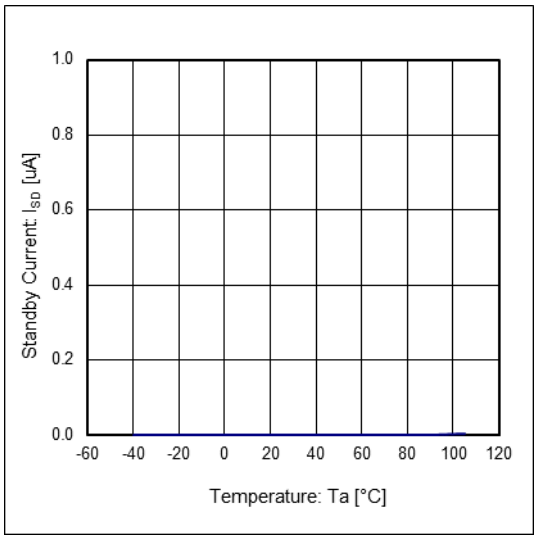


Figure 17. Ta-I_{SD}
(V_{EN}=0V)

●**Performance Curve (Reference Data)**

■**BD50FA1MG-M**

(Unless otherwise specified, Ta=25°C, Vcc=10V, EN=3V, C_{IN}=C_{OUT}=2.2µF)

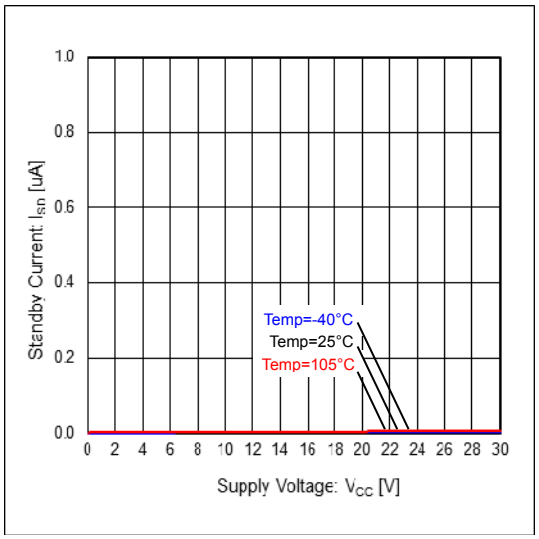


Figure 18. V_{CC}-I_{SD}
(V_{EN}=0V)

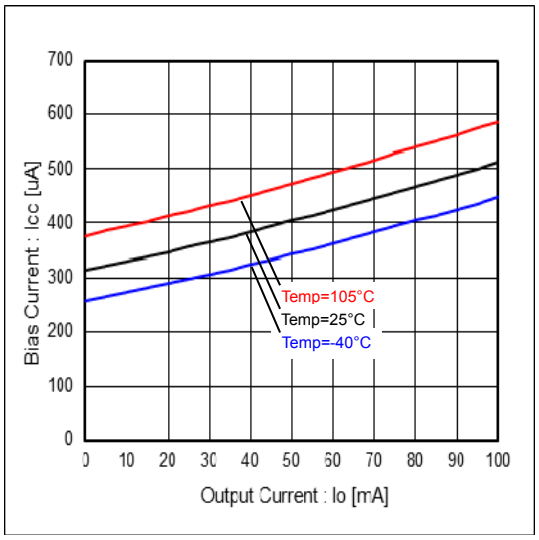


Figure 19. Io - Icc

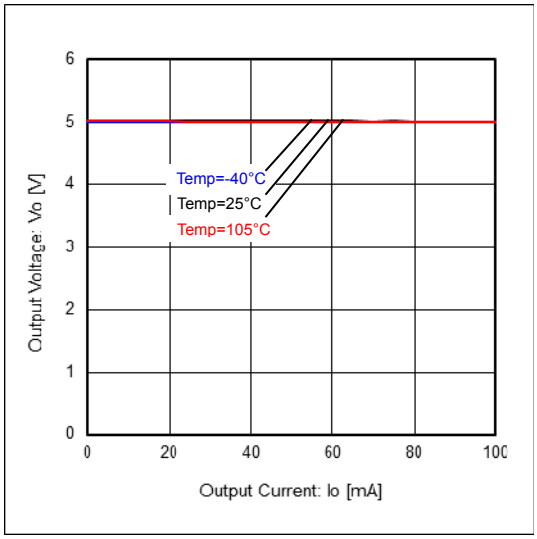


Figure 20. Io - Vo

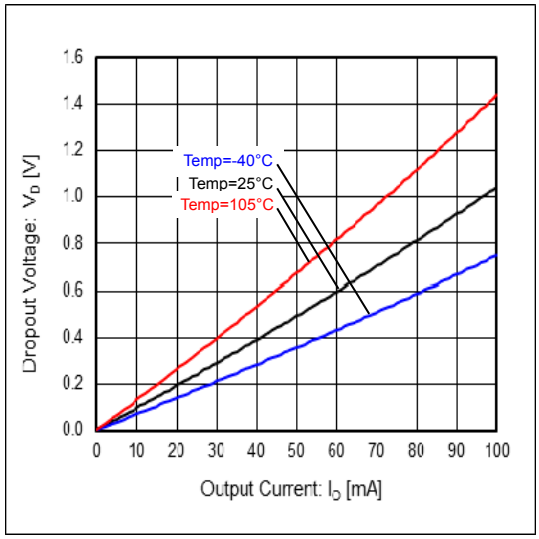


Figure 21. Minimum Dropout Voltage

●**Performance Curve (Reference Data)**

■**BD50FA1MG-M**

(Unless otherwise specified, Ta=25°C, Vcc=10V, EN=3V, C_{IN}=C_{OUT}=2.2µF)

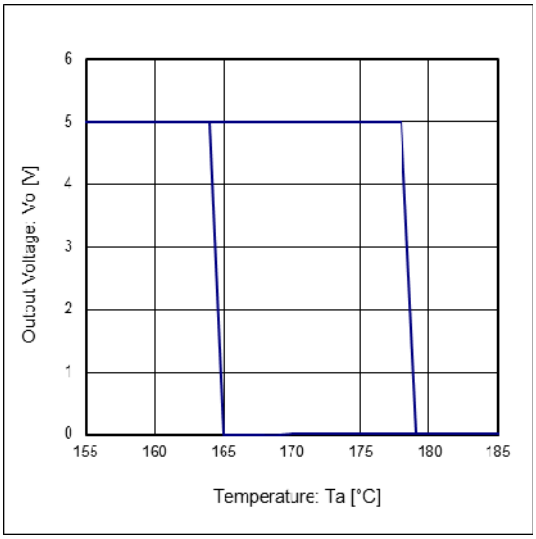


Figure 22. TSD
(Io = 0mA)

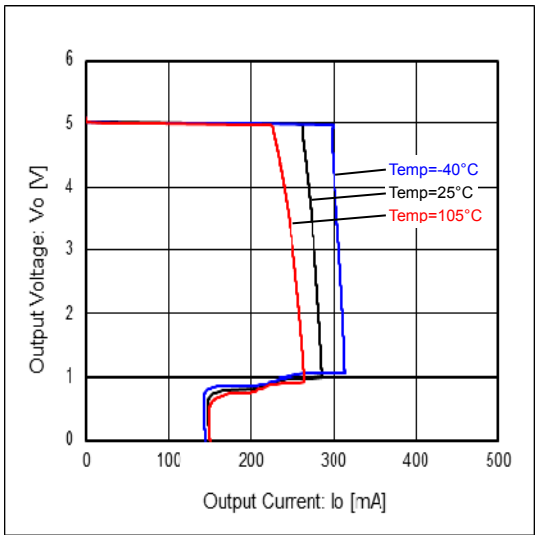


Figure 23. OCP

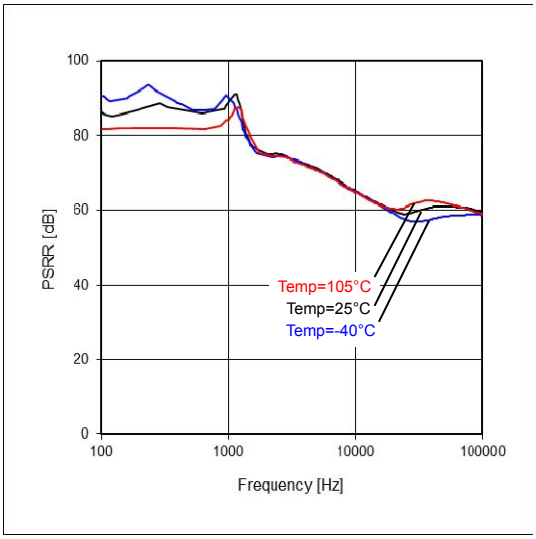


Figure 24. PSRR
(Io = 0mA)

●**Power Dissipation**

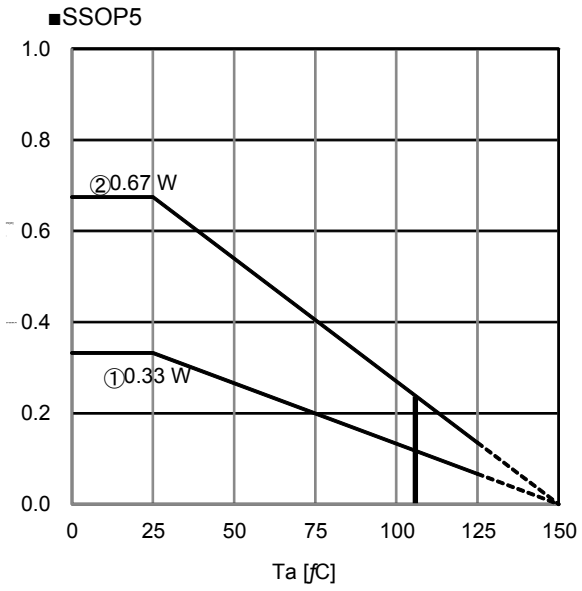


Figure 25 SSOP5 Power Dissipation Data(reference)

IC mounted on ROHM standard board based on JEDEC.
Board material: FR4
Board size:

1s	114.3 mm x 76.2 mm x 1.57 mmt
2s2p	114.3 mm x 76.2 mm x 1.6 mmt

Mount condition: PCB and exposed pad are soldered.
Top copper foil: The footprint ROHM recommend.
+ wiring to measure.

①: 1-layer PCB (Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
②: 4-layer PCB (2 inner layers and copper foil area on the reverse side of PCB: 74.2mm x 74.2 mm)

Condition①: θ_{JA} = 376.5 °C/W, Ψ_{JT}=40 °C/W
Condition②: θ_{JA} = 185.4 °C/W, Ψ_{JT}=30 °C/W

●**Thermal Design**

Within this IC, the power consumption is decided by the dropout voltage condition, the load current and the circuit current. Refer to power dissipation curves illustrated in Figure 25 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25 °C, depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be Tj ≤ Tjmax = 150 °C in all possible operating temperature range.
Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature Tj.
Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj.

$$Tj = Ta + P_C \times \theta_{JA}$$

Where:

Tj	: Junction Temperature
Ta	: Ambient Temperature
P_C	: Power Consumption
θ_{JA}	: Thermal Impedance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj.

$$Tj = T_T + P_C \times \Psi_{JT}$$

Where:

Tj	: Junction Temperature
T_T	: Top Center of Case's (mold) Temperature
P_C	: Power consumption
Ψ_{JT}	: Thermal Impedance (Junction to Top Center of Case)

The following method is used to calculate the power consumption Pc (W).

$$Pc = (Vcc - Vo) \times I_O + Vcc \times IGND$$

Where:

P_C	: Power Consumption
Vcc	: Input Voltage
Vo	: Output Voltage
I_O	: Load Current
$IGND$	: Circuit Current

・Calculation Example (SSOP5)

If Vcc = 8.0 V, Vo = 5.0 V, I_O = 50 mA, IGND = 400 μA, the power consumption Pc can be calculated as follows:

$$P_C = (Vcc - Vo) \times I_O + Vcc \times IGND$$
$$= (8.0\ V - 5.0\ V) \times 50\ mA + 8.0\ V \times 400\ \mu A$$
$$= 0.153\ W$$

At the ambient temperature Tamax = 105°C, the thermal Impedance (Junction to Ambient)θ_{JA} = 185.4 °C / W (4-layer PCB),

$$Tj = Tamax + P_C \times \theta_{JA}$$
$$= 105\ ℃ + 0.153\ W \times 185.4\ ℃ / W$$
$$= 133.4\ ℃$$

When operating the IC, the top center of case's (mold) temperature T_T = 100 °C、Ψ_{JT} = 40 °C / W (1-layer PCB),

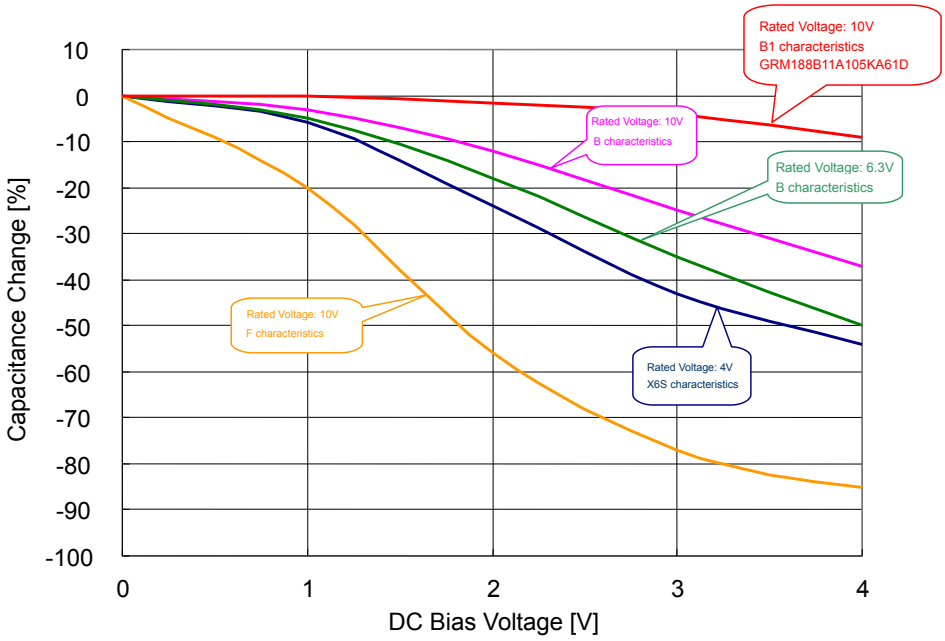
$$Tj = T_T + P_C \times \Psi_{JT}$$
$$= 100\ ℃ + 0.153\ W \times 40\ ℃ / W$$
$$= 106.1\ ℃$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

● **Input/Output Capacitor**

It is recommended that a capacitor is placed close to pin between input pin and GND as well as output pin and GND. The input capacitor becomes more necessary when the power supply impedance is high or when the PCB trace has significant length. Moreover, the higher the capacitance of the output capacitor the more stable the output will be, even with load and line voltage variations. However, please check the actual functionality by mounting on a board for the actual application. Also, ceramic capacitors usually have different thermal and equivalent series resistance characteristics and may degrade gradually over continued use.

For additional details, please check with the manufacturer and select the best ceramic capacitor for your application.



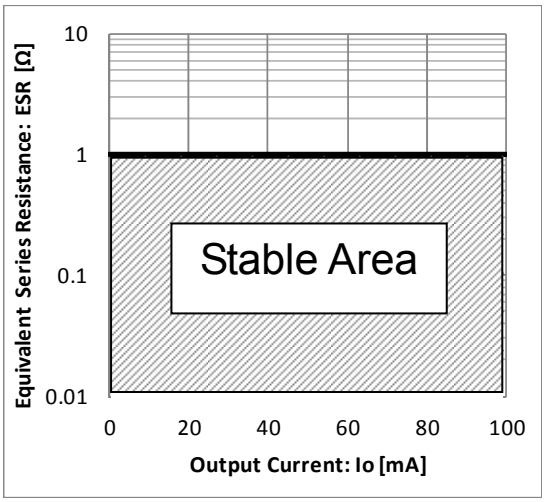
Ceramic Capacitor Capacitance Value— DC Bias Characteristics
(Characteristics Example)

●**Output Capacitor Equivalent Series Resistance**

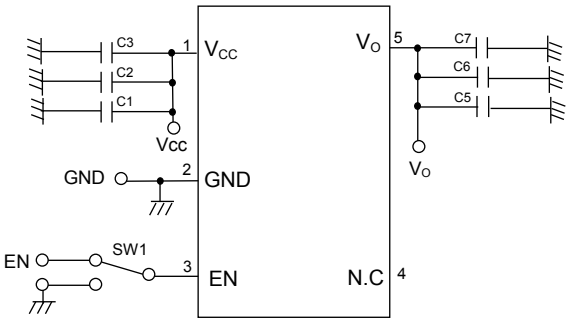
To prevent oscillation, please attach a capacitor between V_O and GND. Generally, capacitor has ESR (Equivalent Series Resistance). Operation will be stable in ESR-Io range shown in the right.

The 2.2µF ceramic capacitor and resistor at output in this characteristic data are connected in series and measured. Generally, ESR of ceramic capacitor, tantalum capacitor and electrolytic capacitor is different. Check the ESR of capacitor to be used and use it within the range of stable region.

However, please take note that for the same value of capacitance of different electrolytic capacitor, ESR are not always the same. In addition, ESR characteristics may also change due to wiring impedance of board, input power impedance and load impedance; therefore check the behavior in actual application.



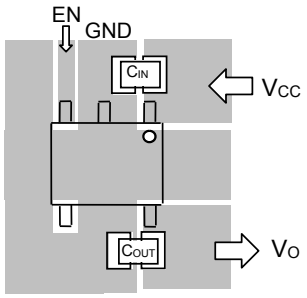
●**Evaluation Board Circuit**



●**Evaluation Board Parts List**

Designation	Value	Part No.	Company	Designation	Value	Part No.	Company
R1		-	-	C4	-	-	-
R2		-	-	C5	2.2μF	CGA4J1X7R1V225M	TDK
R3	-	-	-	C6			
R4	-	-	-	C7	-	-	-
R5	-	-	-	C8	-	-	-
R6	-	-	-	C9	-	-	-
C1	2.2μF	CGA4J1X7R1V225M	TDK	C10	-	-	-
C2	-	-		U1	-	BD50FA1MG-M	ROHM
C3	-	-		U2	-	-	-

●**Board Layout**



・Input capacitor C_{IN} connected to V_{CC} should be placed as close as possible to V_{CC} pin and use wide layout.
Output capacitor C_{OUT} should also be placed as close as possible to IC pin. In case connected to inner layer GND plane, please use several through hole.
・Please make GND pattern wide enough to handle the power dissipation of the chip.

●**Operational Notes**

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

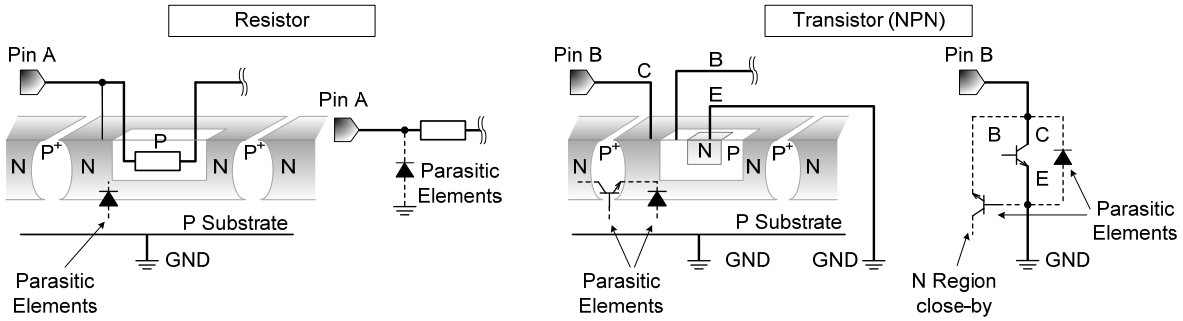


Figure xx. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

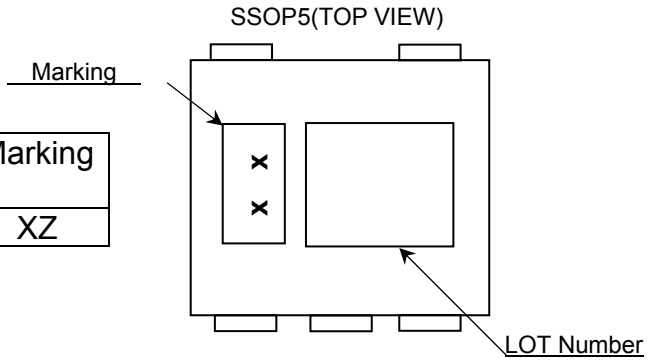
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

17. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

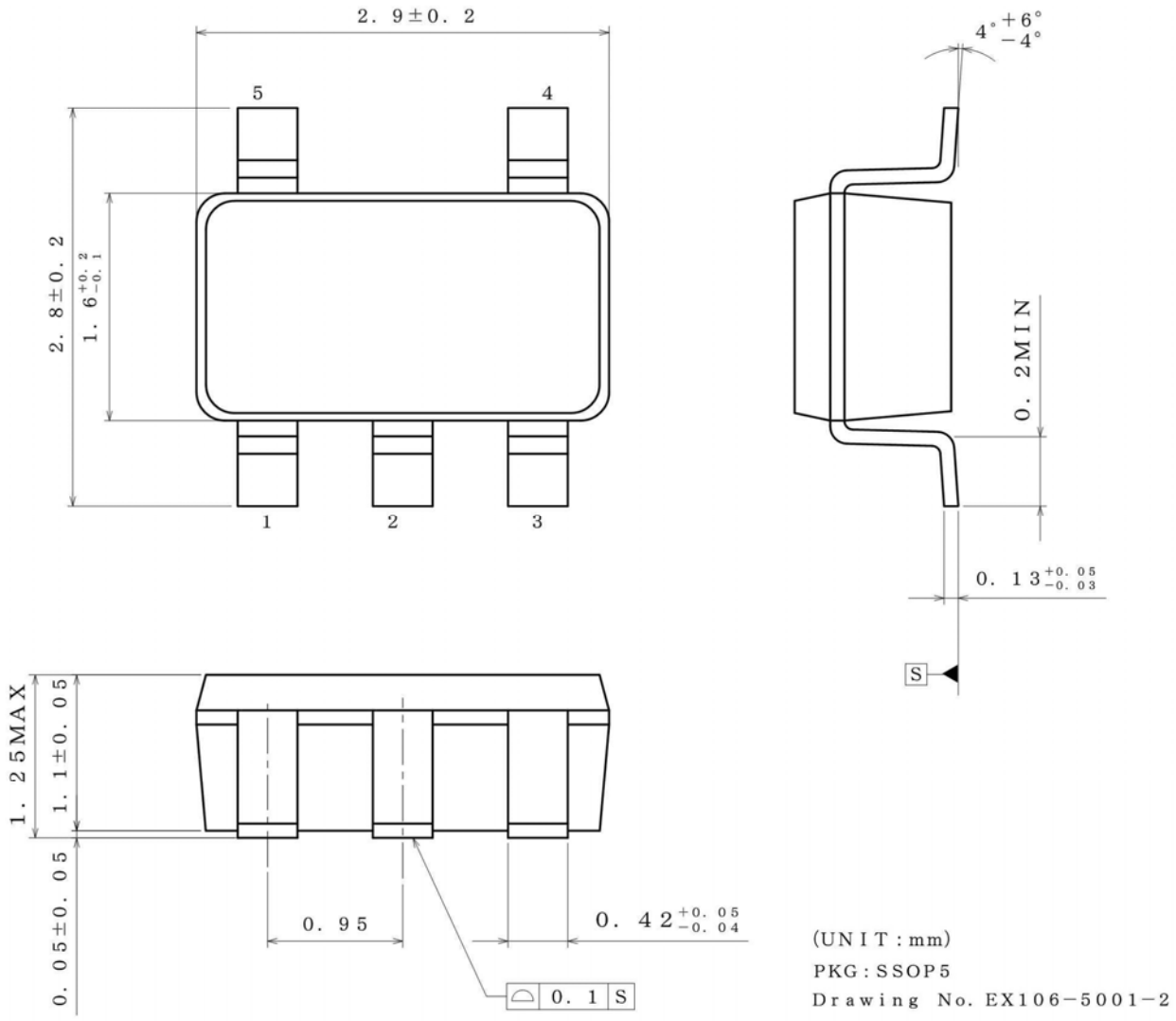
●**Marking Diagram**

xx	Output Voltage	Marking
50	5.0V typ.	XZ



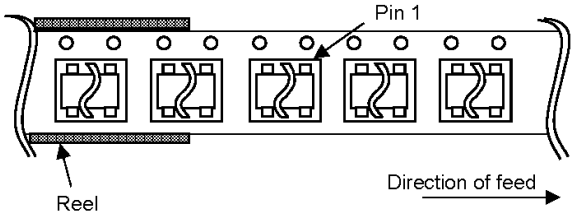
●**Physical Dimension Tape and Reel Information**

Package Name	SSOP5



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



●Revision History

Date	Revision	Revision contents
11.Nov.2015	001	New release
3.Feb.2016	002	P3 output voltage limit modified All input voltage symbol changed into Vcc All Output voltage symbol changed into Vo

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BD50FA1MG-M - Web Page

Part Number	BD50FA1MG-M
Package	SSOP5
Unit Quantity	3000
Minimum Package Quantity	3000
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes