Three-Phase Brushless Motor Driver

BD63006MUV

General Description

BD63006MUV is a Three-Phase Brushless Motor Driver with a 33V power supply voltage rating and a 1.5A output current rating. It generates a driving signal from the Hall sensor and drives PWM through the input control signal. In addition, the power supply can use 12V or 24V and it has various controls and built-in protection functions, making it useful for variety of purposes. Since the IC adopts small packages, it can be used on small diameter motors.

Features

- Built-in 120° Commutation Logic Circuit
- Low ON Resistance DMOS Output
- PWM Control Mode (low side arm switching)
- Built-in Power-saving Circuit
- CW/CCW Function
- Short Brake Function
- FG Output (1FG/3FG conversion)
- Built-in Protection Circuit for Current Limiting (CL), Overheating (TSD), Over Current (OCP), Under Voltage (UVLO), Over Voltage (OVLO), Motor Lock (MLP)

Applications

- OA machines
- Other consumer products

Key Specifications

- Power supply voltage rating: 33V
- Output current rating: 1.5A
- Operating temperature range: -40 to +85°C
- Stand-by current: 1.7mA(Max)
- Current limit detect voltage: 0.2V±10%
- Output ON Resistance (top & bottom total): 0.8Ω (Typ)
- UVLO lockout voltage: 6.0V (Typ)

Package

	W(Typ) x D(Typ) x H(Max)
VQFN024V4040	4.00mm x 4.00mm x 1.00mm

Typical Application Circuit(s)

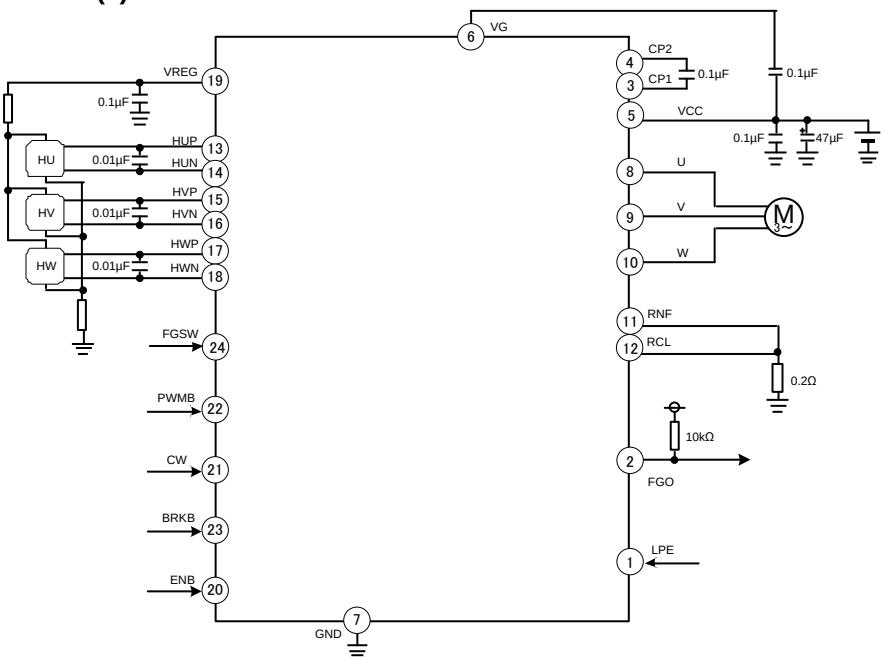

Figure 1. Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin Configuration

(TOP VIEW)

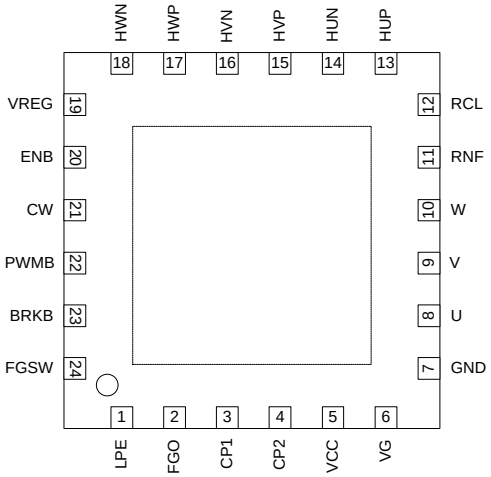

Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	LPE	Setting about motor lock protection (H/M/L input)	13	HUP	U phase Hall input＋
2	FGO	FG output (1FG or 3FG)	14	HUN	U phase Hall input－
3	CP1	Charge pump setting 1	15	HVP	V phase Hall input＋
4	CP2	Charge pump setting 2	16	HVN	V phase Hall input－
5	VCC	Power supply	17	HWP	W phase Hall input＋
6	VG	Charge pump output	18	HWN	W phase Hall input－
7	GND	Ground	19	VREG	Regulator output (OFF at stand-by)
8	U	U phase output	20	ENB	Enable input (negative logic)
9	V	V phase output	21	CW	CW/CCW input (H:CW, L:CCW)
10	W	W phase output	22	PWMB	PWM input (negative logic)
11	RNF	Detect resistor for over current	23	BRKB	Brake input (negative logic)
12	RCL	Detect voltage input for over current	24	FGSW	1FG/3FG switching (H:3FG, L:1FG)

Block Diagram

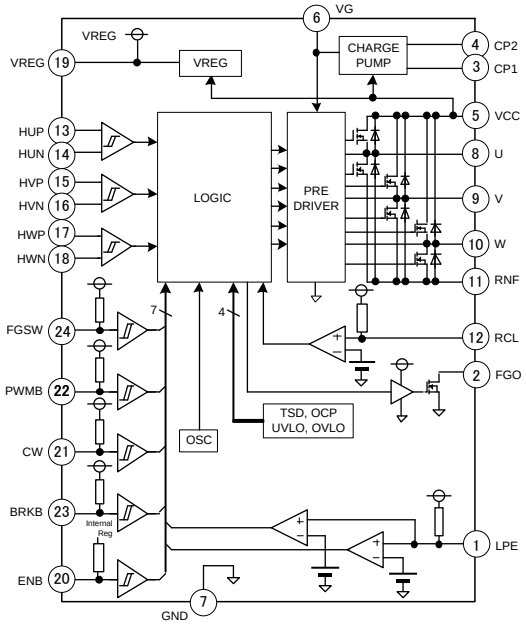

Figure 3. Block Diagram

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Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Limit	Unit
Power Supply Voltage	V_{CC}	-0.3 to +33.0	V
VG Voltage	V_G	-0.3 to +38.0	V
Control Input Voltage	V_{IN},V_{IN2}	-0.3 to +5.5	V
FGO Terminal Voltage	V_{FGO}	-0.3 to +7.0	V
RNF Maximum Apply Voltage	V_{RNF}	0.7	V
VREG Output Current	I_{VREG}	-30(Note 1)	mA
FGO Output Current	I_{FGO}	5(Note 1)	mA
Driver Output Current	$I_{OUT(DC)}$	1.5(Note 1)	A/Phase
Operating Temperature Range	T_{OPR}	-40 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
Junction Temperature	T_{jmax}	150	°C

(Note 1) Do not exceed T_j=150°C.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +85°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	8	24	28	V

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Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
VQFN024V4040				
Junction to Ambient	θ_{JA}	150.6	37.9	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	20	9	°C/W

*(Note 1)*Based on JESD51-2A(Still-Air)
*(Note 2)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 3)*Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

*(Note 4)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

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Description of Block(s)

1. Commutation Logic
   This IC adopts 120° commutation mode, and the truth table is as follows:

HU	HV	HW	CW (CW=H or Open)			CCW (CW=L)			FGO	
			U	V	W	U	V	W	1FG	3FG
H	L	H	PWM*	H	Hi-z	H	PWM*	Hi-z	L	Hi-z
H	L	L	PWM*	Hi-z	H	H	Hi-z	PWM*	L	L
H	H	L	Hi-z	PWM*	H	Hi-z	H	PWM*	L	Hi-z
L	H	L	H	PWM*	Hi-z	PWM*	H	Hi-z	Hi-z	L
L	H	H	H	Hi-z	PWM*	PWM*	Hi-z	H	Hi-z	Hi-z
L	L	H	Hi-z	H	PWM*	Hi-z	PWM*	H	Hi-z	L

* When PWMB="L"，PWM="L"，When PWMB="H"，PWM="H".

2. Regulator Output Terminal (VREG)
   This is constant voltage output terminal of 5V(Typ). It is recommended to connect capacitors of 0.01μF to 1μF. Please be careful that VREG current does not exceed ratings in case of being used for bias power supply of hall elements.

3. Enable Input Terminal (ENB)
   Output of each phase can be set to ON/OFF (negative logic) through ENB terminal. When applied voltage is V_{ENA}, the motor is driven (enable). When applied voltage is V_{STBY} or OPEN, the motor stops (stand-by). Stand-by mode has precedence to other control input signal and VREG output is OFF. In addition, ENB terminal is pulled up by internal power supply through a resistance of 100kΩ (Typ) ±30kΩ.

ENB	Operation
H or OPEN	Stand-by
L	Enable

4. PWM Input Terminal (PWMB)
   Speed can be controlled by inputting PWM signal into PWMB terminal (negative logic). Synchronous rectifier PWM can be achieved through lower switching. When PWMB=" L", driver output that belongs to Hall input logic is “L”. When PWMB="H" or open, driver output is "H". When PWMB="H" or OPEN status is detected 104μs (Typ), the synchronous rectifier is OFF (Hi-z). Synchronous rectifier is ON through falling edges of subsequent PWMB. Additionally, PWMB terminal is pulled up by VREG through a resistance of 100kΩ (Typ) ±30kΩ.

PWMB	Driver Output
H or OPEN	H (Hi-z)
L	L

5. Brake Input Terminal (BRKB)
   Motor rotation can be quickly stopped by BRKB terminal (negative logic). When BRKB="L", all driver outputs are "L" (short brake). When BRKB="H" or OPEN, then short brake action is released. In addition, BRKB terminal is pulled up by VREG through a resistance of 100kΩ (Typ) ±30kΩ.

BRKB	Operation
H or OPEN	Normal
L	Short brake

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6. CW/CCW Input Terminal (CW)
Rotation direction can be switched with CW terminal. When CW="H" or OPEN, the direction is Clockwise. When CW="L", the direction is Counterclockwise. We do not recommend changing the direction of rotation while the motor is rotating. However if direction of rotation is changed while rotating, a short brake action is active until the rotation speed becomes equal to the hall frequency, which is less than approximately 40Hz (Typ). After a short brake, the rotation direction will switch to a new setting. In addition, CW terminal is pulled up by VREG through resistance of 100kΩ (Typ) ±30kΩ.

CW	Direction
H or OPEN	Clockwise
L	Counterclockwise

7. 1FG/3FG Switching Terminal (FGSW)
FG signal that is output from FGO terminal can be switched to 1FG/3FG. It becomes 3FG by FGSW="H" or OPEN, and 1 FG by FGSW="L". Moreover, FGSW terminal is pulled up by VREG through resistance of 100kΩ (Typ)±30kΩ.

FGSW	FGO
H or OPEN	3FG
L	1FG

8. Hall Input (HALL: HUP, HUN, HVP, HVN, HWP, HWN)
Hall comparator is designed with hysteresis (±15mV (Typ)) in order to prevent incorrect action due to noise inside. So please set bias current for Hall element to make amplitude of Hall input voltage over minimum input voltage ($V_{HALLMIN}$). Here, we recommend you to connect the ceramic capacitor with about 100pF to 0.01μF between difference input terminals of Hall comparator. The in-phase input voltage range designed for Hall comparator is $V_{HALLCM1,2}$, so please set within this range when applying bias to Hall element.
Moreover, "H" or "L" of HU, HV and HW in Commutation Logic means the following.

HU	HV	HW	HUP	HUL	HVP	HVN	HWP	HWN
H	L	H	H	L	L	H	H	L
H	L	L	H	L	L	H	L	H
H	H	L	H	L	H	L	L	H
L	H	L	L	H	H	L	L	H
L	H	H	L	H	H	L	H	L
L	L	H	L	H	L	H	H	L

When HU, HV and HW become all "H" or "L", detect circuit detects these Hall input abnormalities and makes all driver outputs "Hi-z".

9. FG Output Terminal (FGO)
1FG or 3FG signal that is reshaped by hall signal is output from FGO terminal. It is does not have output in stand-by mode. In addition, because FG terminal is output from open drain, please use resistance of about 10kΩ to 100kΩ pulled up from outside. In that case, please be careful that FGO voltage or current never exceed rating.

10. Power Supply Terminal (VCC)
Please make low impedance thick and short since motor drive current flows. Please stabilize V_{CC} by placing bypass capacitor near terminal as much as possible because V_{CC} might be changed considerably by motor BEMF and PWM switching. Please add capacity of capacitor as necessary when using large current and motor with large BEMF. Moreover, it is recommended to place laminated ceramic capacitor of around 0.01μF to 0.1μF in parallel on the purpose of decreasing impedance of power supply broadband. Please be careful that V_{CC} never exceeds ratings. VCC terminal has clamp element for preventing ESD damage. If applying steep pulse signal and voltage such as surge more than ratings, this clamp element operates, which might be a cause of destruction. It is effective to put zener diode that corresponds to V_{CC} absolute maximum ratings. Diode for preventing ESD damage is inserted between VCC and GND terminals. Please note that IC might be destroyed when the backward voltage is applied to VCC and GND terminals.

11. Ground Terminal (GND)
Wiring impedance from this terminal should be as low as possible for reducing noise of switching current and stabilizing basic voltage inside of IC, and the impedance also should be the lowest potential in any operating condition. In addition, please do pattern design not to have common impedance as other GND pattern.

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12. Driver Output Terminal (U, V, W)
When driver output converts "L"→"H" or "H"→"L", for example when synchronous rectification PWM is operating, a dead time (1μs(Typ)) will be set to prevent simultaneous ON of output top & bottom MOS.
Please be careful about the following points in using driver output.
- Wiring should be thick, short, and low Impedance due to motor drive current.
- In applying steep pulse signal or voltage that will surge more than ratings, the clamp element which is built-in the driver output terminal operates in order to prevent ESD damage. Then it might cause destruction of IC. Do not exceed ratings.

When using large current, in case that driver current changes considerably toward positive and negative (when BEMF is large), malfunction or destruction of IC might occur. Please add Schottky diode to the driver output terminal.

13. Capacitor Connection Terminal for Boosting, Boosting Output Terminal (CP1, CP2, VG)
Charge pump is built-in for upper Nch MOS drive signal of driver output. Boosting voltage of V_{CC}+5V (Typ) occurs in VG terminal by connecting capacitor between CP1 to CP2 terminals and VG to VCC terminals. It is recommended to use capacitor more than 0.1μF. In addition, because there is built-in protection circuit for insufficient booster, when VG voltage is below V_{GUVON} (VCC+2V (Typ.)), driver outputs all become “Hi-z”.

14. Resistor Connection Terminal for Detecting Output Current (RNF)
Please insert resistor for detecting current 0.15Ω to 0.5Ω between RNF and GND. When deciding resistor value, it should be careful that consumption electricity of resistor for detecting current $I_{OUT}^2 \cdot R$[W] does not exceed rating of resistor. In addition, please do not have common impedance as other GND patterns by using low impedance wiring, since motor drive current flows into pattern of RNF terminal to resistor for detecting current to GND. In case that RNF voltage goes over rating (0.7V), circuit malfunction might occur. Therefore please do not exceed rating. When RNF terminal is shorted to GND, big current flows due to a lack of normal current limit operation. Please be careful that OCP or TSD might operate in that case. Similarly, if RNF terminal is OPEN, output current might not flow, which also becomes a cause of malfunction.

15. Comparator Input Terminal for Detecting Output Current (RCL)
RCL terminal is placed individually as input terminal of current detect comparator in order to avoid deterioration of current detect accuracy by wire impedance inside IC of RNF terminal. Therefore, when operating current limit, please be sure to connect RNF terminal and RCL terminal. Moreover, it is possible to reduce deterioration of current detect accuracy by impedance of board pattern between RNF terminal and resistor for detecting current by connecting wiring from RCL terminal most adjacent to resistor for detecting current. Please design pattern considering wiring that is less influenced by noise. Additionally, when RCL terminal is shorted to GND, big current might flow due to a lack of normal current limit operation. Please be careful that OCP or TSD might operate in that case.

16. Control Signal Sequence
Though we recommend you input control signals of ENB, PWMB, BRKB, FGSW, CW, LPE terminals after inputting V_{CC}, there is no problem if you input control signals before inputting V_{CC}. If LPE terminal is set to "H" or "M" when being started, please be informed that if motor rotation cannot be detected within the set time (edge of FGO signal cannot be input), then the MLP circuit starts and motor fails to start. Moreover, the order of priority is set to control signal and IC internal signal. Please refer to the following table.

Priority of Control Signal

Priority	Input / Internal Signals
1st	ENB, UVLO
2nd	BRKB↑↓,CW↑↓,PWMB ↓
3rd	TSD, OCP, MLP, HALLERR
4th	OVLO
5th	VG_UVLO
6th	BRKB
7th	CL
8th	PWMB, CW

Note）↑↓ means rising and falling edges of signal.
For signal name, please see state transition diagram.

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Protection Circuit

1. Current Limit Circuit (CL circuit)
   Current limit of output (Current Limit: CL) can be achieved by changing voltage of output current with resistor between RNF and GND, and then inputting the voltage into RCL terminal. In order to avoid error detection of current detection comparator by RNF spike noise that occurs at output ON, using mask time (0.5µs (Typ)) can be efficient. Current detection is invalid during mask time after RCL voltage becomes more than 0.2V (Typ). Then please turn OFF all lower MOS of driver output, which is returned automatically after specified time (32µs (Typ)). This operation is not synchronized with PWM signal that is input into PWMB terminal.

2. Thermal Shut Down Circuit (TSD Circuit)
   When chip temperature of driver IC rises and exceeds the set temperature (175°C (Typ)), the thermal shut down circuit (Thermal Shut Down: TSD) begins to work. At this time, the driver outputs all become "Hi-z". In addition, the TSD circuit is designed with hysteresis (25°C (Typ)), therefore, when the chip temperature drops, it returns to normal working condition. Moreover, the purpose of the TSD circuit is to protect driver IC from thermal breakdown, therefore, temperature of this circuit will be over working temperature when it is started up. Thus, thermal design should have sufficient margin, so do not take continuous use and action of the circuit as a precondition.

3. Over Current Protection Circuit (OCP Circuit)
   Over current protection (Over Current Protection : OCP) is built-in in order to prevent from destruction when being shorted between output terminals and also being VCC/GND shorted. Therefore output current exceeds ratings and specified current flows. In that case, driver outputs are all latched to Hi-z condition. Latch can be released by going through stand-by condition or switching BRKB/CW logic. However, output current rating is exceeded when this circuit operates. Thus, please design sufficient margin not to take continuous use and action of the circuit as a precondition.

4. Under Voltage Lock Out Circuit (UVLO Circuit)
   There is a built-in under voltage lock out circuit (Under Voltage Lock Out: UVLO) used to ensure the lowest power supply voltage for drive IC to work and to prevent error action of IC. When V_{CC} declines to V_{UVL} (6V (Typ)), all of the driver outputs should be "Hi-z". At the same time, UVLO circuit is designed with hysteresis (1V (Typ)), so when V_{CC} reaches more than V_{UVH} (7V (Typ)), it enters normal working condition.

5. Over Voltage Lock Out Circuit (OVLO circuit)
   There is built-in over voltage lock out circuit (Over Voltage Lock Out: OVLO) used to restrain rise of V_{CC} when motor is decelerating. When LPE terminal is at "M" and V_{CC} is over V_{OVH1} (16V (Typ)), and when LPE terminal is at "H" or "L" and V_{CC} is over V_{OVH2} (31V (Typ)), a certain time (4ms (Typ)) of short brake action is conducted. What's more, because OVLO circuit is designed with hysteresis, therefore, when V_{OVH1} is below V_{OVL1} (15V (Typ)) and when V_{OVH2} is below V_{OVL2} (30.5V (Typ)), it can return to normal working condition after a certain time of short brake action.

6. Motor Lock Protection Circuit (MLP circuit)
   There is built-in motor lock protection circuit (Motor Lock Protection: MLP). The Enable/Disable of MLP circuit and OVLO threshold can be set by the LPE terminal.
   In monitoring Hall signals, when the LPE = "H" or "M" and Hall signal logic does not change to more than 1.1sec(Typ), all driver outputs are latched as "Hi-z".
   There are three ways to release the latch.
   - The latch is released by putting IC in standby mode.
   - The latch is released by changing BRKB/CW logic.
   - After PWMB = "H" or OPEN state is detected for about 15ms(Typ), the latch is released by falling edge of subsequent PWMB.

   However, when LPE = "L", short brake action (including switching rotation direction) enables or TSD circuit works, MLP circuit does not work.
   LPE terminal is pulled up by VREG through a resistance of 100kΩ (Typ) ±30 kΩ.

LPE	Monitoring Time	OVLO Threshold
H or OPEN	1.1sec(Typ) ±30%	V_{OVH2}, V_{OVL2}
M	1.1sec(Typ) ±30%	V_{OVH1}, V_{OVL1}
L	Disable	V_{OVH2}, V_{OVL2}

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Electrical Characteristics (Unless otherwise specified Ta=25°C, VCC=24V)

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
[Whole]						
Circuit Current	I_{CC}	-	4.4	8.4	mA	V_{ENB}=0V
Stand-by Current	I_{STBY}	-	1.1	1.7	mA	ENB=OPEN
VREG Voltage	V_{REG}	4.5	5.0	5.5	V	I_{VREG}=-10mA
[Driver output]						
Output On Resistance	R_{ON}	-	0.8	1.2	Ω	I_{OUT}=±1.0A(Upper + Lower)
[Hall input]						
Input Bias Current	I_{HALL}	-2.0	-0.1	+2.0	μA	V_{HALL}=0V
Range of In-phase Input Voltage1	$V_{HALLCM1}$	0	-	V_{REG}-1.7	V	
Range of In-phase Input Voltage2	$V_{HALLCM2}$	0	-	V_{REG}	V	When one hall Input is bias
Minimum Input Voltage	$V_{HALLMIN}$	50	-	-	mV_{p-p}	
HYS Level ＋	$V_{HALLHY+}$	5	15	25	mV	
HYS Level －	$V_{HALLHY-}$	-25	-15	-5	mV	
[Input of Control：ENB]						
Input Current	I_{ENB}	-75	-45	-25	μA	V_{ENB}=0V
Standby Voltage	V_{STBY}	2.0	-	V_{REG}	V	
Enable Voltage	V_{ENA}	0	-	0.8	V	
[Input of Control：PWMB, CW, BRKB, FGSW]						
Input Current	I_{IN}	-80	-50	-30	μA	V_{IN}=0V
Voltage Input H	V_{INH}	2.0	-	V_{REG}	V	
Voltage Input L	V_{INL}	0	-	0.8	V	
Minimum Input Pulse Width	t_{PLSMIN}	1	-	-	msec	CW, BRKB
[Input of Control：LPE]						
Input Current	I_{IN2}	-80	-50	-30	μA	V_{IN2}=0V
Input Voltage "H"	V_{INH2}	$0.8 \times V_{REG}$	-	V_{REG}	V	
Input Voltage "M"	V_{INM2}	$0.4 \times V_{REG}$	-	$0.6 \times V_{REG}$	V	
Input Voltage "L"	V_{INL2}	0	-	$0.2 \times V_{REG}$	V	
[FG Output：FGO]						
Output Voltage L	V_{FGOL}	0	0.1	0.3	V	I_{FGO}=2mA
[Current Limit]						
Detect Voltage	V_{CL}	0.18	0.20	0.22	V	
[UVLO]						
Release Voltage	V_{UVH}	6.5	7.0	7.5	V	
Lockout Voltage	V_{UVL}	5.5	6.0	6.5	V	
[OVLO]						
Release Voltage1	V_{OVL1}	14.0	15.0	16.0	V	LPE="M"
Lockout Voltage1	V_{OVH1}	15.0	16.0	17.0	V	LPE="M"
Release Voltage2	V_{OVL2}	29.0	30.5	32.0	V	LPE="H" or "L"
Lockout Voltage2	V_{OVH2}	29.5	31.0	32.5	V	LPE="H" or "L"

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Timing Chart

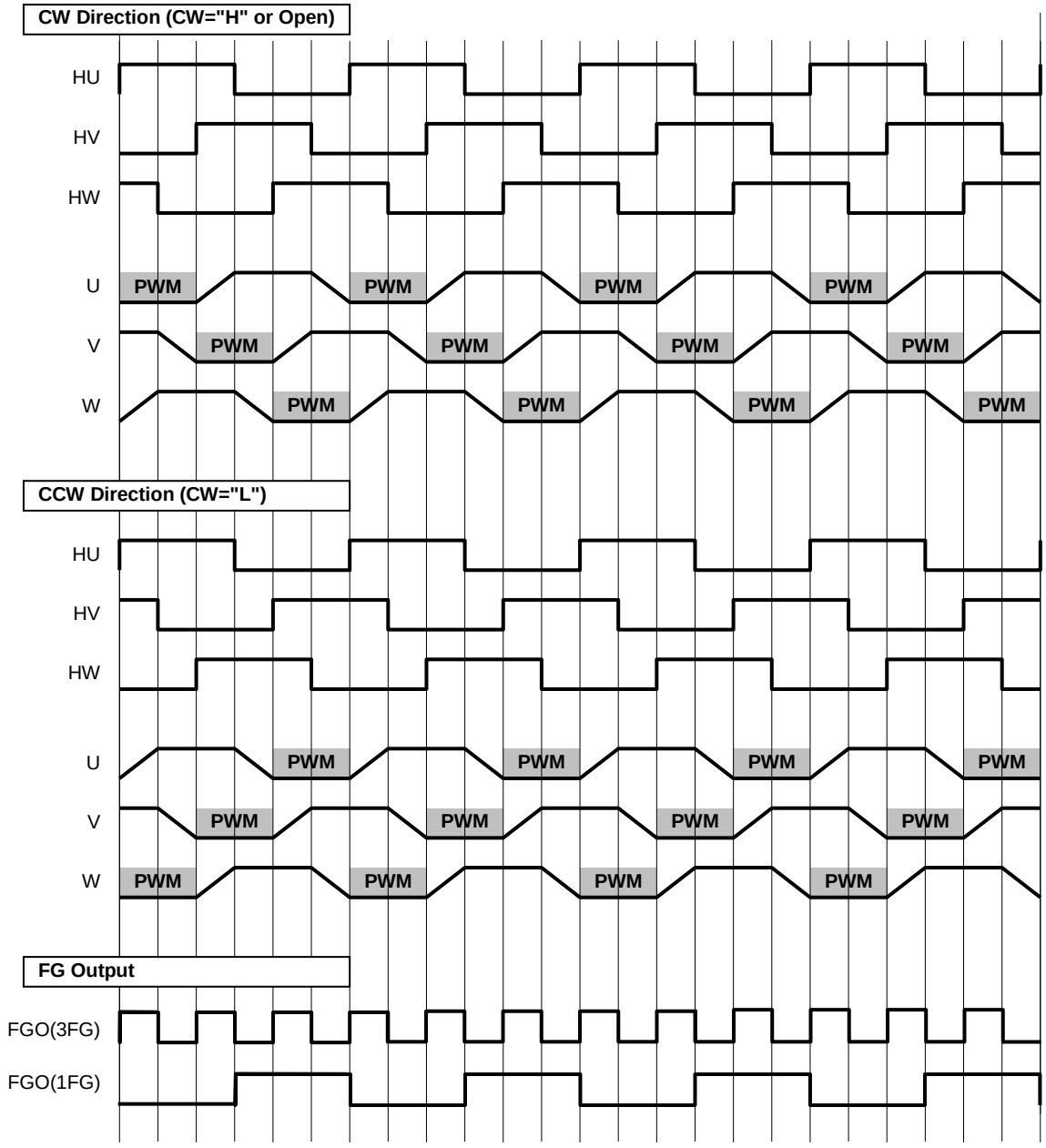

Figure 4. Timing Chart

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State Transition Diagram

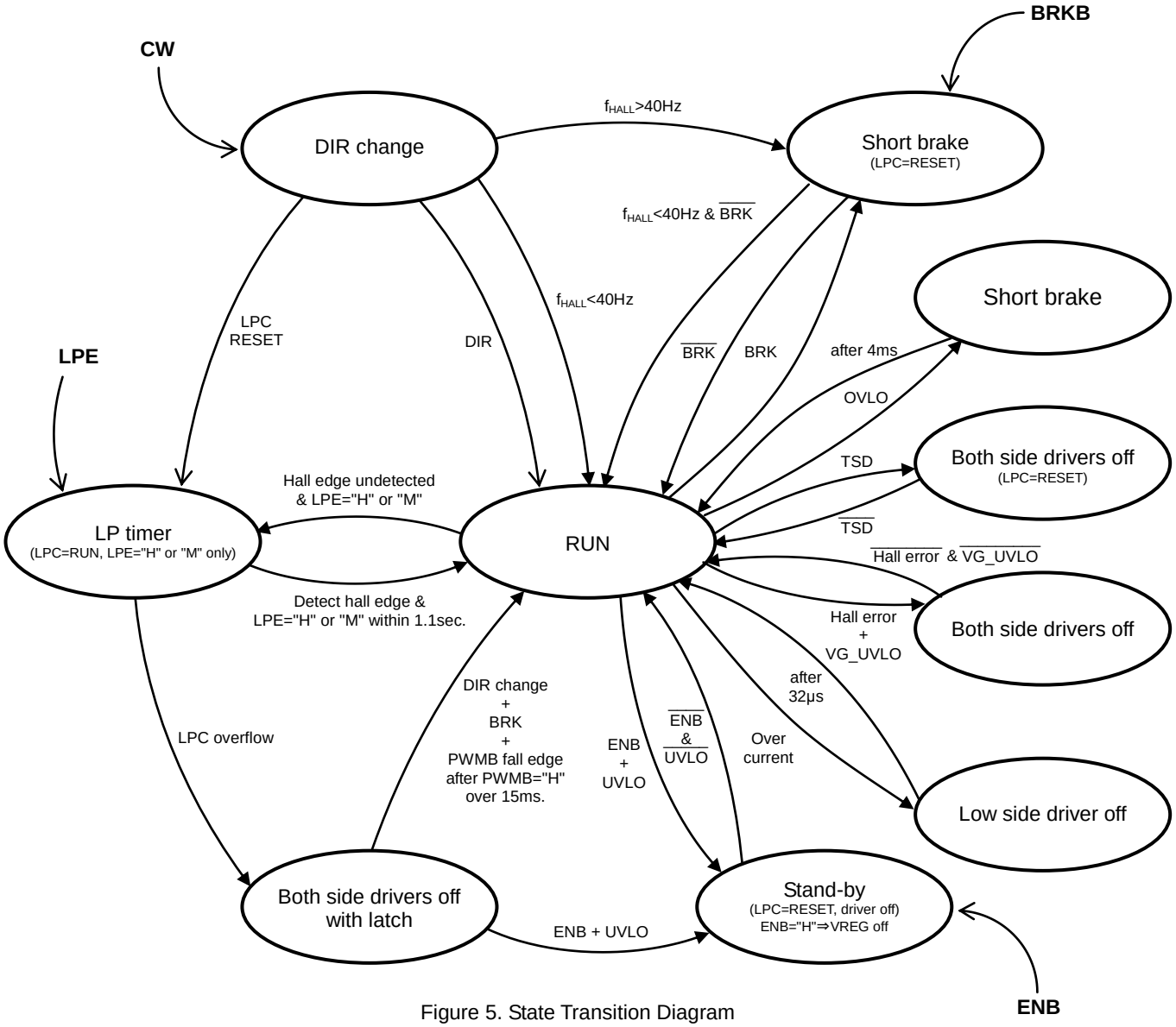

Figure 5. State Transition Diagram

Legend:
DIR: motor rotational direction
LP: motor lock protection
LPC: internal counter for the motor lock protection (watch-dog timer)
f_{HALL}: hall signal frequency
Hall error: HU=HV=HW
&: logical "AND"
+: logical "OR"

State transition
Command signal

Note) All values are typical

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I/O Equivalence Circuits

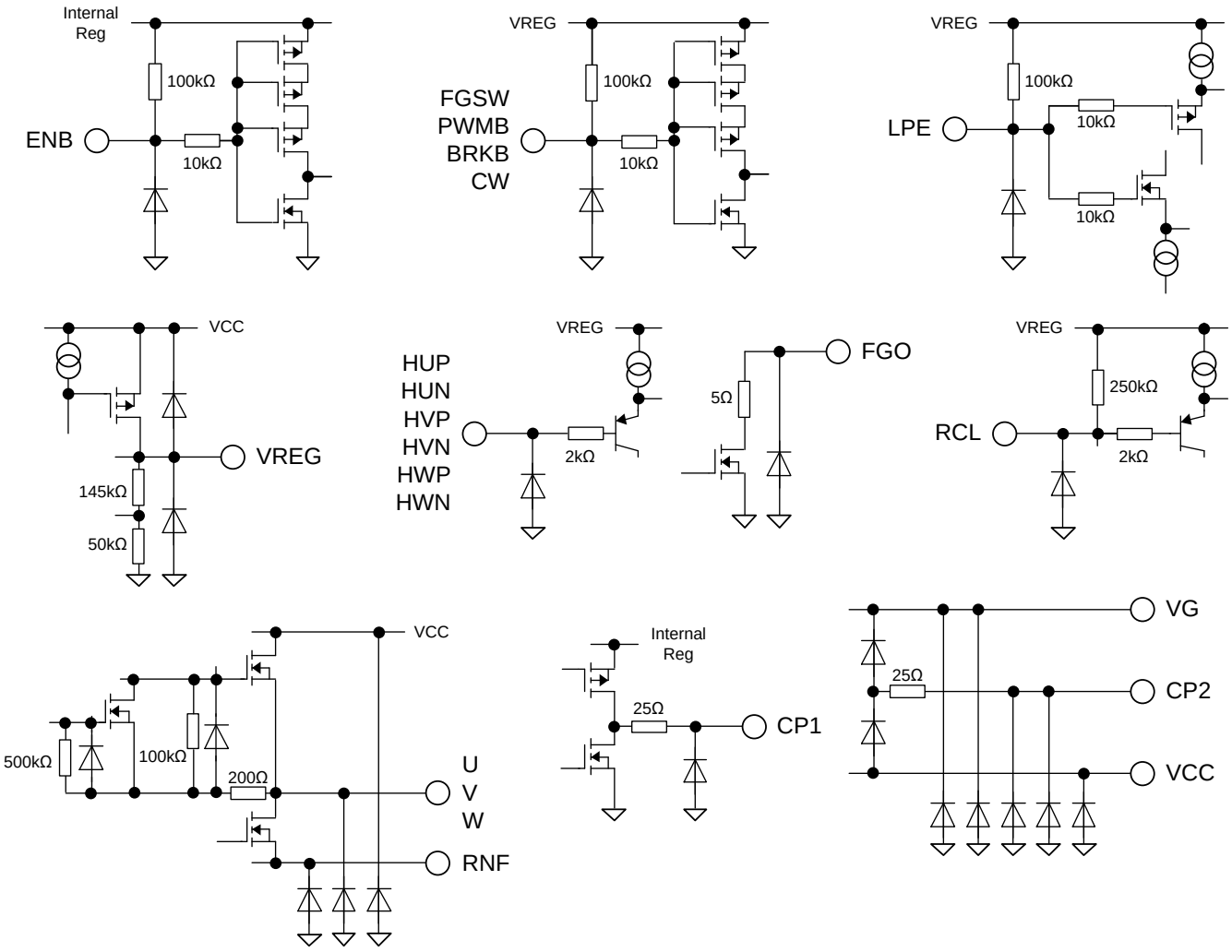

Figure 6. I/O Equivalence Circuits

Application Operational Notes

1. **CP1-CP2 shorted**
   When CP1 (3pin) and CP2 (4pin) are shorted incorrectly, they result in damaging the IC. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

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Operational Notes – continued

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

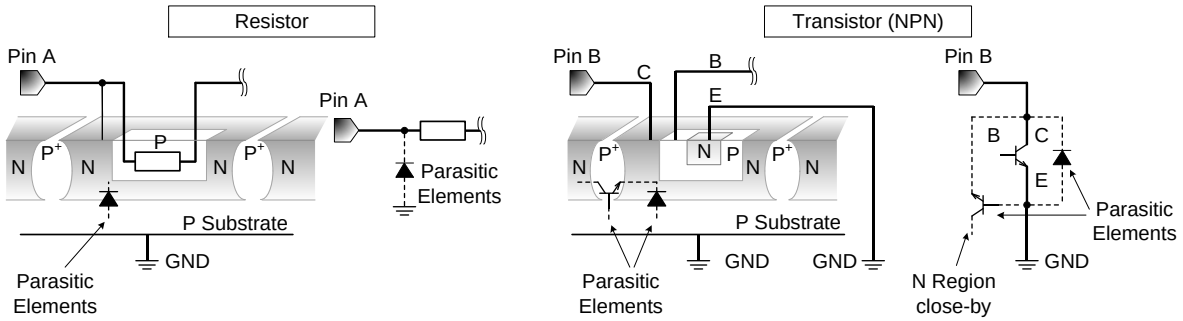

Figure 7. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

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Operational Notes – continued

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

17. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

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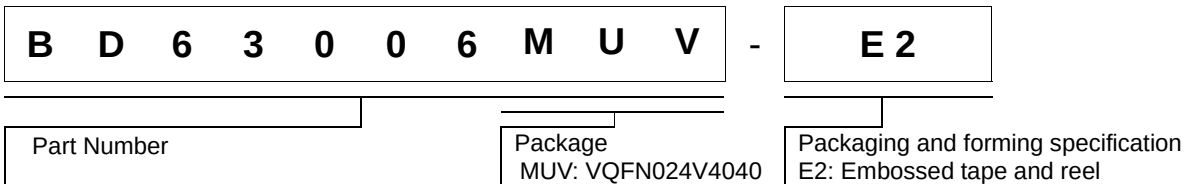
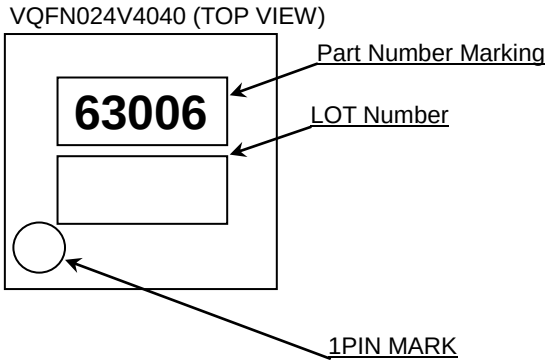
Ordering Information



Marking Diagrams



Part Number Marking	Package	Orderable Part Number
63006	VQFN024V4040	BD63006MUV-E2

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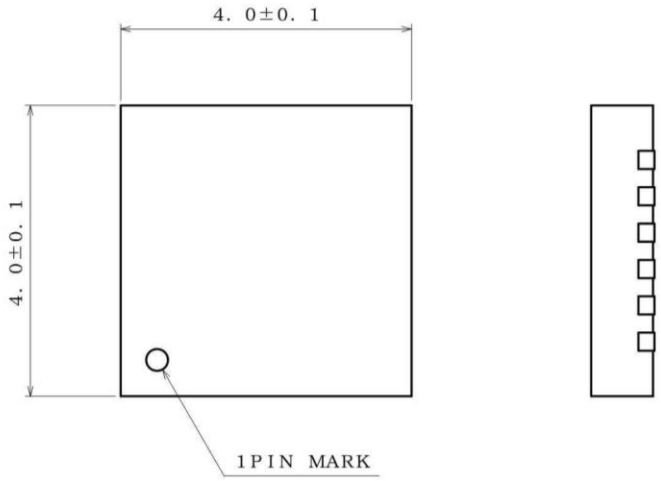
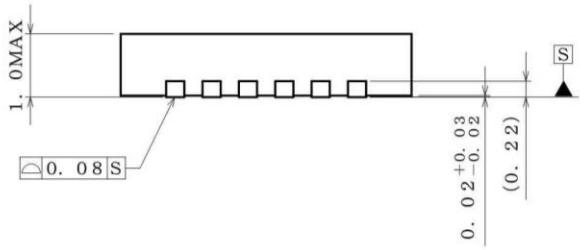
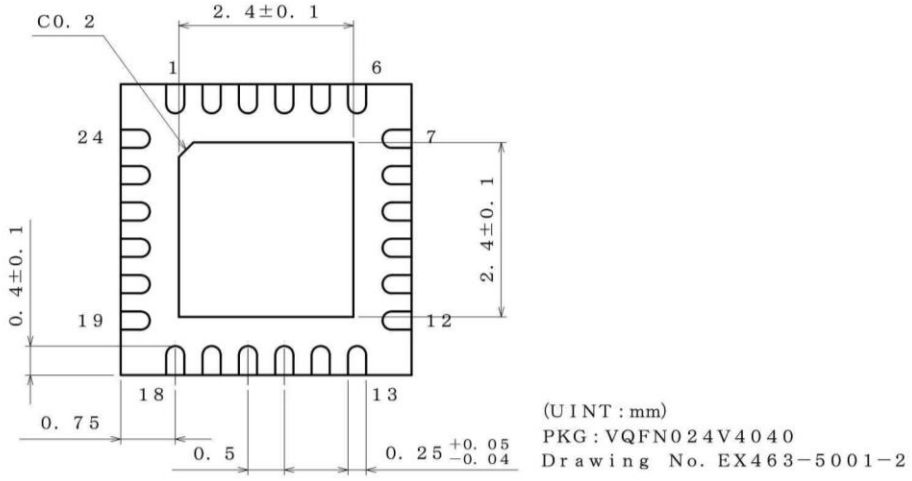
Physical Dimension Tape and Reel Information

Package Name	VQFN024V4040

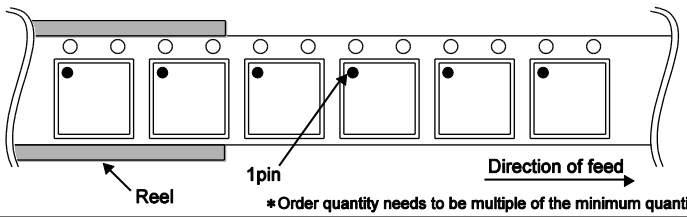






<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
14.Jul.2015	001	New Release
2.Jun.2016	002	P1. Chenge the symbol of Application circuit P3. Change block diagram ,add Internal Reg P4 delete Power dissipation P5 add thermal Resistance P6 PWM input terminal : Hi-z ⇒ “H” OFF ⇒ OFF(Hi-z) P7 (V_{HALLCM}、0V~V_{REG}-1.7V) ⇒ ($V_{HALLCM1,2}$) P8 U,V,W output : dead time (1μs to 2μs(Typ)) ⇒ 1us (Typ) 14.Resistor Connection Terminal for Detecting Output Current (RNF) 0.05Ω to 0.5Ω ⇒ 0.15Ω to 0.5Ω P9 I/O Equivalence Circuits : change symbol Delete power dissipation

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BD63006MUV - Web Page

Part Number	BD63006MUV
Package	VQFN024V4040
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes