System Lens Driver Series for Digital Still Cameras / Single-lens Reflex Cameras

6ch System Lens Drivers for Digital Still Cameras / Single-lens Reflex Cameras

BD6373GW,BD6873KN,BD6753KV

No.09014EAT02

●Description

The BD6373GW motor driver provides 6 Full-ON Drive H-bridge channels. The BD6873KN motor driver provides 5 Full-ON Drive H-bridge channels and 1 Linear Constant-Current Drive H-bridge channel, while the BD6753KV provides 4 Full-ON Drive channels and 2 PWM Constant-Current Drive H-bridge channels.

Stepping motors can be used for auto focus, and either zoom or iris. A new drive type (lens barrier) is also available. Three types of drivers for shutter are offered: a simple Full-ON type, a high-precision linear constant current type, or a high-efficiency PWM constant current type, enabling selection of the ideal solution based on the application.

●Features

1) Subminiature 31PIN Wafer-level CSP (Chip Size Package): 2.6 x 2.6 x 0.85mm^3 (BD6373GW)
2) DMOS output allowing a range power supply: 4.5V to 10.5V (BD6753KV; VM1), 2.0V to 10.5V (BD6753KV; VM2 to VM4)
3) Low ON-Resistance Power MOS output:
   Full-ON Drive block with 1.2Ω Typ. (BD6373GW)
   Full-ON Drive block with 1.2Ω Typ. and Linear Constant-Current Drive block with 1.0Ω Typ. (BD6873KN)
   Full-ON Drive block with 1.2Ω Typ. and PWM Constant-Current Drive block with 1.2Ω Typ. (BD6753KV)
4) Serial interface 3-line bus control input (BD6753KV)
5) Built-in two-step output current setting switch for the Linear Constant-Current Drive block (BD6873KN)
6) Drive mode switching function
7) 1.2V±3% high-precision reference voltage output (BD6873KN)
8) Constant-Current Drive block features phase compensation capacitor-free design (BD6873KN)
9) Built-in ±3% high-precision Linear Constant-Current Driver (BD6873KN)
10) Built-in peak current control PWM Constant-Current Driver (BD6753KV)
11) Built-in charge pump circuit for the DMOS gate voltage drive (BD6753KV)
12) UVLO (Under Voltage Lockout Protection) function
13) Built-in TSD (Thermal Shut Down) circuit
14) Standby current consumption: 0μA Typ.

●Absolute Maximum Ratings

Parameter	Symbol	Limit			Unit
		BD6373GW	BD6873KN	BD6753KV	
Power supply voltage	VCC	-0.5 to +6.5	0 to +7.0	-0.5 to +7.0	V
Motor power supply voltage	VM	-0.5 to +6.5	0 to +7.0	-0.5 to +12.5	V
Charge pump voltage	VG	-	-	18.0	V
Control input voltage	VIN	-0.5 to VCC+0.5	0 to VCC	-0.5 to VCC+0.5	V
Power dissipation	Pd	940※1	950※2	1125※3	mW
Operating temperature range	Topr	-25 to +85	-25 to +85	-25 to +75	°C
Junction temperature	Tjmax	+150	+150	+150	°C
Storage temperature range	Tstg	-55 to +150	-55 to +150	-55 to +150	°C
H-bridge output current	Iout	-800 to +800※4	-800 to +800※4	-800 to +800※4	mA/ch

※1 Reduced by 7.52mW/°C over 25°C, when mounted on a glass epoxy board (50mm x 58mm x 1.75mm; 8layers).
※2 Reduced by 7.6mW/°C over 25°C, when mounted on a glass epoxy board (70mm x 70mm x 1.6mm).
※3 Reduced by 9.0mW/°C over 25°C, when mounted on a glass epoxy board (70mm x 70mm x 1.6mm).
※4 Must not exceed Pd, ASO, or Tjmax of 150°C.

●**Operating Conditions (Ta=-25 to +85°C(BD6373GW, BD6873KN), -25 to +75°C(BD6753KV))**

Parameter	Symbol	Limit			Unit
		BD6373GW	BD6873KN	BD6753KV	
Power supply voltage	VCC	2.5 to 5.5	2.5 to 5.5	2.7 to 5.5	V
Motor power supply voltage	VM	2.5 to 5.5	2.5 to 5.5	4.5 to 10.5 (VM1) 2.0 to 10.5 (VM2 to VM4)	V
Control input voltage	VIN	0 to VCC	0 to VCC	0 to VCC	V
Output current control input voltage range	VLIM	-	0 to VCC	0 to 0.5	V
PWM signal input frequency	FPWM	-	-	0 to 0.1	MHz
H-bridge output current	Iout	-500 to +500※5	-500 to +500※5	-500 to +500※5	mA/ch

※5 Must not exceed Pd or ASO.

●**Electrical Characteristics**

1) BD6373GW Electrical Characteristics (Unless otherwise specified, Ta=25°C, VCC=3.0V, VM=5.0V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
Circuit current	ICC	-	1.0	1.9	mA	no signal and no load
Control input (IN=ENABLExx, INPUTx, and BRAKEx)						
High level input voltage	VINH	2.0	-	VCC	V	
Low level input voltage	VINL	0	-	0.7	V	
High level input current	IINH	15	30	60	μA	VINH=3V
Low level input current	IINL	-1	0	-	μA	VINL=0V
UVLO						
UVLO voltage	VUVLO	1.6	-	2.4	V	
Full-ON Drive block (ch1 to ch6)						
Output ON-Resistance 1	RON1	-	1.2	1.5	Ω	Io=±400mA on high and low sides In total (VM=5V)
Output ON-Resistance 2	RON2	-	1.5	2.0	Ω	Io=±400mA on high and low sides In total (VM=3V)
Turn on time	ton	-	0.55	1.95	μs	RL=20Ω
Turn off time	toff	-	0.08	0.5	μs	RL=20Ω
Rise time	tr	0.1	0.15	1.0	μs	RL=20Ω
Fall time	tf	-	0.03	0.2	μs	RL=20Ω

2) BD6873KN Electrical Characteristics (Unless otherwise specified, Ta=25°C, VCC=3.0V, VM=5.0V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
Circuit current during standby operation	ICCST	-	0	10	μA	PS=0V
Circuit current	ICC	-	1.2	2.3	mA	PS=VCC with no signal and no load
Power-saving (PS)						
High level input voltage	VPSH	2.0	-	-	V	
Low level input voltage	VPSL	-	-	0.7	V	
High level input current	IPSH	15	30	60	μA	VPS=3V
Low level input current	IPSL	-1	0	-	μA	VPS=0V
Control input (IN=IN1A to IN5B, SEL1 to 3, BRK1, EN1, IN6, and VLIMS)						
High level input voltage	VINH	2.0	-	-	V	
Low level input voltage	VINL	-	-	0.7	V	
High level input current	IINH	15	30	60	μA	VINH=3V
Low level input current	IINL	-1	0	-	μA	VINL=0V
Pull-down resistance	RIN	50	100	200	kΩ	
UVLO						
UVLO voltage	VUVLO	1.6	-	2.4	V	
Full-ON Drive block (ch1 to ch5)						
Output ON-Resistance	RON	-	1.2	1.5	Ω	Io=±400mA on high and low sides In total
Linear Constant-Current Drive block (ch6)						
Output ON-Resistance	RON	-	1.0	1.25	Ω	Io=±400mA on high and low sides in total
VREF output voltage	VREF	1.16	1.20	1.24	V	Iout=0~1mA
Output limit voltage	VOL	194	200	206	mV	RNF=0.5Ω, VLIM=0.2V

3) BD6753KV Electrical Characteristics (Unless otherwise specified, Ta=25°C, VCC=3.3V, VM=10.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
Circuit current during standby operation	ICCST	-	0	10	μA	PS=0V
Circuit current	ICC	-	2.2	3.0	mA	PS=VCC with no signal; CRx open
Power-saving (PS)						
High-level input voltage	VPSH	2.0	-	-	V	
Low-level input voltage	VPSL	-	-	0.7	V	
High-level input current	IPSH	25	50	100	μA	VPSH=3.3V
Low-level input current	IPSL	-1	0	-	μA	VPSL=0V
Control input (IN=STROBE, CLK, DATA, and PWM1 to 6)						
High-level input voltage	VINH	2.0	-	-	V	
Low-level input voltage	VINL	-	-	0.7	V	
High-level input current	IINH	16.5	33	66	μA	VINH=3.3V
Low-level input current	IINL	-1	0	-	μA	VINL=0V
Pull-down resistance	RIN	50	100	200	kΩ	
Charge pump						
Charge pump voltage	VCP	16	16.5	-	V	
UVLO						
UVLO voltage	VUVLO	1.6	-	2.5	V	
Full-ON Drive block (ch1 to ch4)						
Output ON-Resistance	RON	-	1.2	1.5	Ω	Io=±400mA, VG=16.5V on high and low sides in total
PWM Linear Constant-Current Drive block (ch5 and ch6)						
Output ON-Resistance	RON	-	1.2	1.5	Ω	Io=±400mA, VG=16.5V on high and low sides in total
VLIM pin input current	IVLIM	-1	-0.2	-	μA	VLIMx=0V, SENSEx=0.5V
SENSE pin input current	ISENSE	-1	-0.2	-	μA	VLIMx=0.5V, SENSEx=0V
Output limit voltage	VOL	485	500	515	mV	VLIMx=500mV
CR clamp voltage	VCR	0.8	0.9	1.0	V	R=10kΩ
CR switching high voltage	VCRH	0.72	0.80	0.88	V	
CR switching low voltage	VCRL	0.36	0.40	0.44	V	
Minimum ON time	TMINON	0.1	0.5	1.0	μs	C=470pF, R=10kΩ
Constant voltage power supply						
VREF output voltage	VREF	0.81	0.90	0.99	V	Iout=0~1mA

●Electrical Characteristic Diagrams

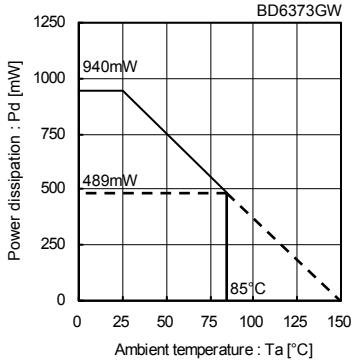


Fig.1 Power Dissipation Reduction

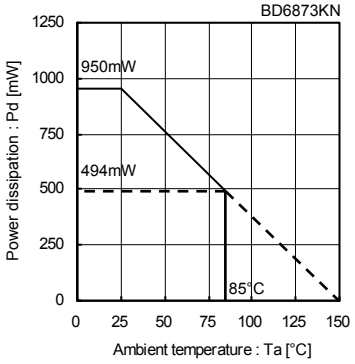


Fig.2 Power Dissipation Reduction

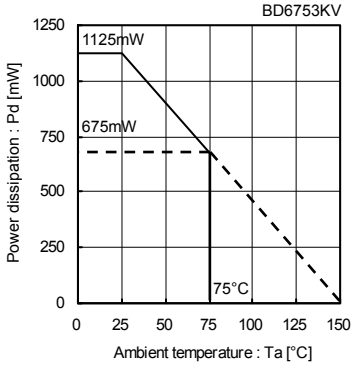


Fig.3 Power Dissipation Reduction

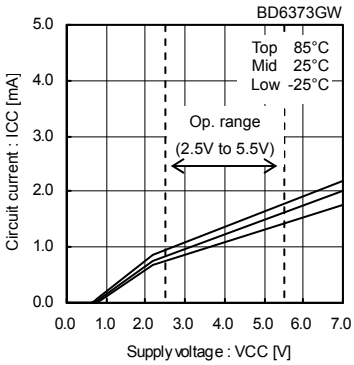


Fig.4 Circuit current

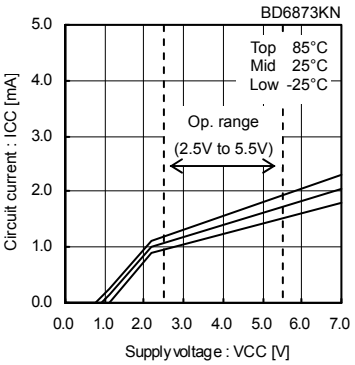


Fig.5 Circuit current

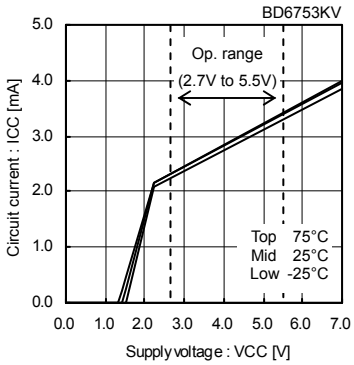


Fig.6 Circuit current

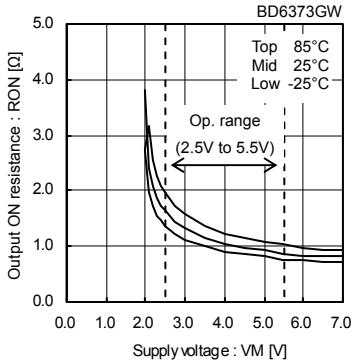


Fig.7 Output ON-Resistance
(Full-ON Drive block)

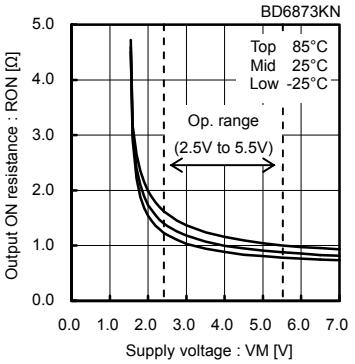


Fig.8 Output ON-Resistance
(Full-ON Drive block)

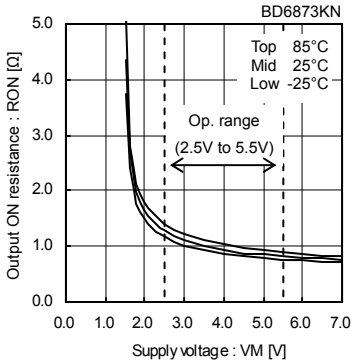


Fig.9 Output ON-Resistance
(Linear Constant-Current Drive

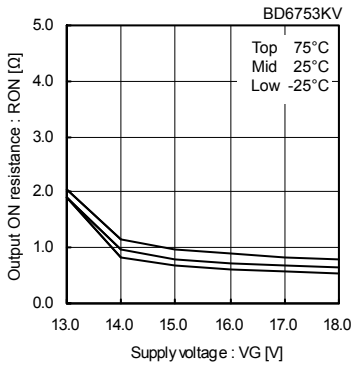


Fig.10 Output ON-Resistance
(VM=10.5V)

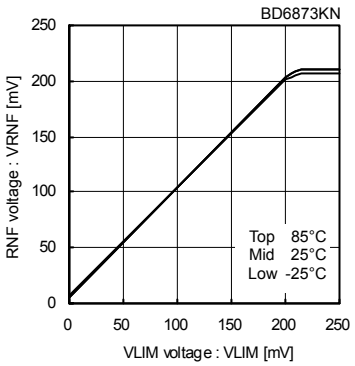


Fig.11 Output limit voltage
(RNF=0.5Ω)

●Block Diagram, Pin Arrangement, and Pin Function

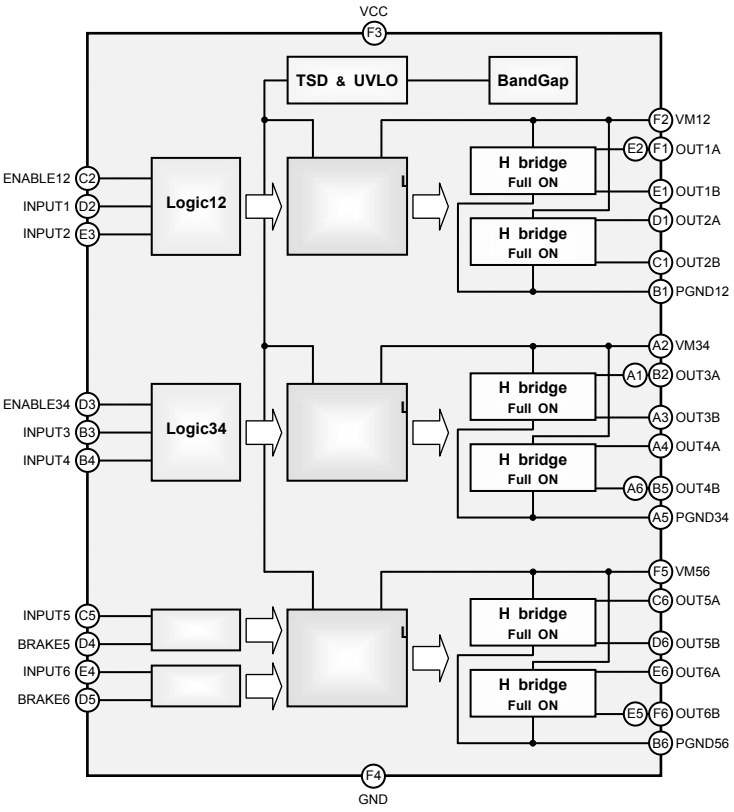


Fig.12 BD6373GW Block Diagram

	1	2	3	4	5	6
A	OUT3A	VM34	OUT3B	OUT4A	PGND34	OUT4B
B	PGND12	OUT3A	INPUT3	INPUT4	OUT4B	PGND56
C	OUT2B	ENABLE12	INDEX POST		INPUT5	OUT5A
D	OUT2A	INPUT1	ENABLE34	BRAKE5	BRAKE6	OUT5B
E	OUT1B	OUT1A	INPUT2	INPUT6	OUT6B	OUT6A
F	OUT1A	VM12	VCC	GND	VM56	OUT6B

OUT3A, OUT4B, OUT1A, and OUT6B, which are 2 function pins, are shorted on printed circuit boards.

Fig.13 BD6373GW Pin Arrangement (Top View)
UCSP75M2 Package

BD6373GW Pin Function Table

No.	Pin Name	Function	No.	Pin Name	Function
A1	OUT3A	H-bridge output pin ch3 A	D1	OUT2A	H-bridge output pin ch2 A
A2	VM34	Motor power supply pin ch3 and ch4	D2	INPUT1	Control input pin ch1 INPUT
A3	OUT3B	H-bridge output pin ch3 B	D3	ENABLE34	Control input pin ch3 and ch4 ENABLE
A4	OUT4A	H-bridge output pin ch4 A	D4	BRAKE5	Control input pin ch5 BRAKE
A5	PGND34	Motor ground pin ch3 and ch4	D5	BRAKE6	Control input pin ch6 BRAKE
A6	OUT4B	H-bridge output pin ch4 B	D6	OUT5B	H-bridge output pin ch5 B
B1	PGND12	Motor ground pin ch1 and ch2	E1	OUT1B	H-bridge output pin ch1 B
B2	OUT3A	H-bridge output pin ch3 A	E2	OUT1A	H-bridge output pin ch1 A
B3	INPUT3	Control input pin ch3 INPUT	E3	INPUT2	Control input pin ch2 INPUT
B4	INPUT4	Control input pin ch4 INPUT	E4	INPUT6	Control input pin ch6 INPUT
B5	OUT4B	H-bridge output pin ch4 B	E5	OUT6B	H-bridge output pin ch6 B
B6	PGND56	Motor ground pin ch5 and ch6	E6	OUT6A	H-bridge output pin ch6 A
C1	OUT2B	H-bridge output pin ch2 B	F1	OUT1A	H-bridge output pin ch1 A
C2	ENABLE12	Control input pin ch1 and ch2 ENABLE	F2	VM12	Motor power supply pin ch1 and ch2
C3	INDEX POST	-	F3	VCC	Power supply pin
C4		-	F4	GND	Ground pin
C5	INPUT5	Control input pin ch5	F5	VM56	Motor power supply pin ch5 and ch6
C6	OUT5A	H-bridge output pin ch5 A	F6	OUT6B	H-bridge output pin ch6 B

OUT3A, OUT4B, OUT1A, and OUT6B, which are 2 function pins, are shorted on printed circuit boards.

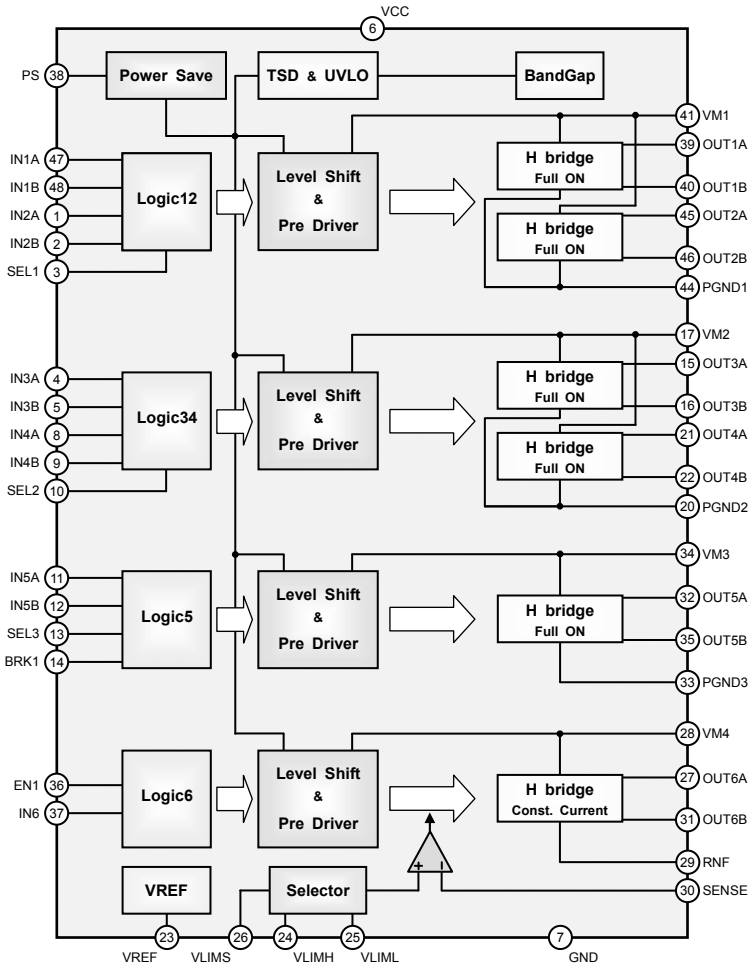


Fig.14 BD6873KN Block Diagram

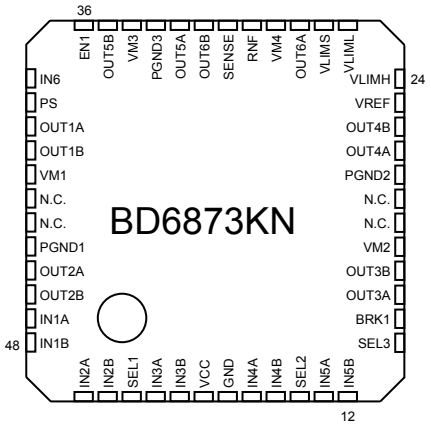


Fig.15 BD6873KN Pin Arrangement (Top View)
UQFN48 Package

BD6873KN Pin Function Table

No.	Pin name	Function	No.	Pin name	Function
1	IN2A	Control input pin ch2 A	25	VLIML	Output current setting pin 2 ch6
2	IN2B	Control input pin ch2 B	26	VLIMS	Output current selection pin ch6
3	SEL1	Input mode selection pin ch1 and ch2	27	OUT6A	H-bridge output pin ch6 A
4	IN3A	Control input pin ch3 A	28	VM4	Motor power supply pin ch6
5	IN3B	Control input pin ch3 B	29	RNF	Resistance connection pin for output current detection ch6
6	VCC	Power supply pin	30	SENSE	Output current detection pin ch6
7	GND	Ground pin	31	OUT6B	H-bridge output pin ch6 B
8	IN4A	Control input pin ch4 A	32	OUT5A	H-bridge output pin ch5 A
9	IN4B	Control input pin ch4 B	33	PGND3	Motor ground pin ch5
10	SEL2	Input mode selection pin ch3 and ch4	34	VM3	Motor power supply pin ch5
11	IN5A	Control input pin ch5 A	35	OUT5B	H-bridge output pin ch5 B
12	IN5B	Control input pin ch5 B	36	EN1	Control input pin ch6 ENABLE
13	SEL3	Input mode selection pin ch5	37	IN6	Control input pin ch6 INPUT
14	BRK1	Control input pin ch5 BRAKE	38	PS	Power-saving pin
15	OUT3A	H-bridge output pin ch3 A	39	OUT1A	H-bridge output pin ch1 A
16	OUT3B	H-bridge output pin ch3 B	40	OUT1B	H-bridge output pin ch1 B
17	VM2	Motor power supply pin ch3 and ch4	41	VM1	Motor power supply pin ch1 and ch2
18	N.C.	-	42	N.C.	-
19	N.C.	-	43	N.C.	-
20	PGND2	Motor ground pin ch3 and ch4	44	PGND1	Motor ground pin ch1 and ch2
21	OUT4A	H-bridge output pin ch4 A	45	OUT2A	H-bridge output pin ch2 A
22	OUT4B	H-bridge output pin ch4 B	46	OUT2B	H-bridge output pin ch2 B
23	VREF	Reference voltage output pin	47	IN1A	Control input pin ch1 A
24	VLIMH	Output current setting pin 1 ch6	48	IN1B	Control input pin ch1 B

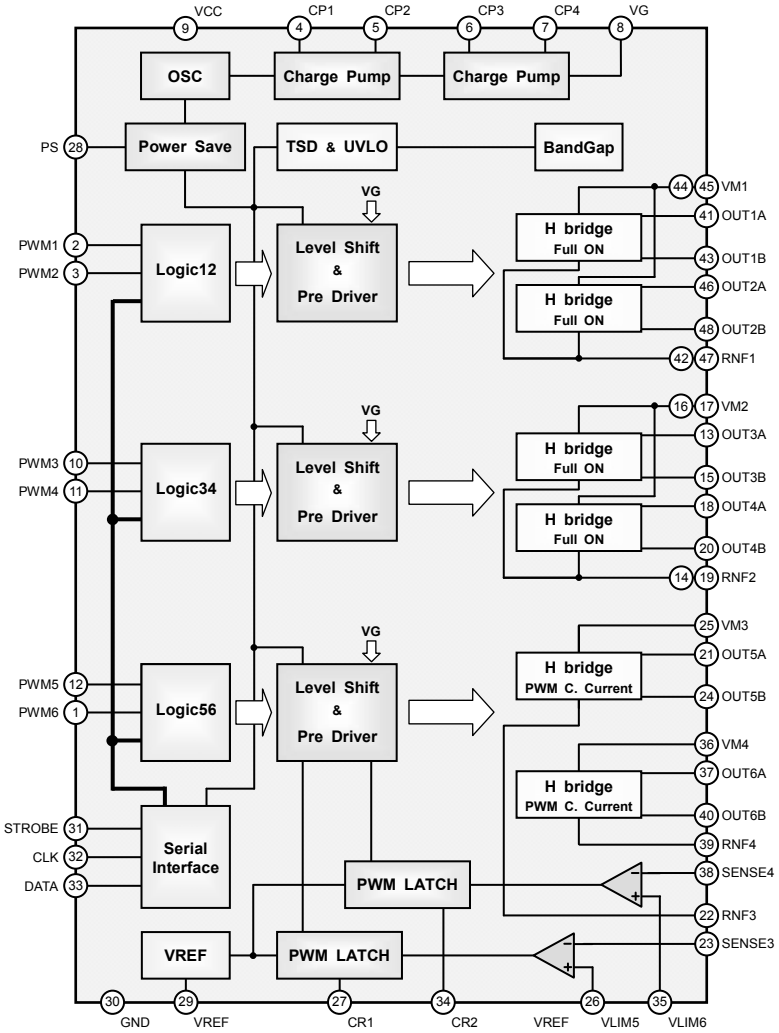


Fig.16 BD6753KV Block Diagram

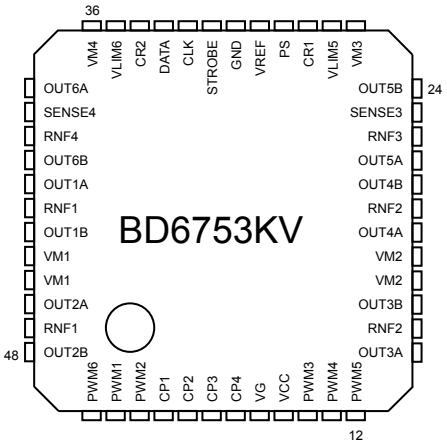


Fig.17 BD6753KV Pin Arrangement (Top View)
VQFP8C Package

BD6753KV Pin Function Table

No.	Pin name	Function	No.	Pin name	Function
1	PWM6	PWM control input pin ch6	25	VM3	Motor power supply pin ch5
2	PWM1	PWM control input pin ch1	26	VLIM5	Output current setting pin ch5
3	PWM2	PWM control input pin ch2	27	CR1	CR timer setting element connection pin ch5
4	CP1	Charge pump capacitor connection pin 1	28	PS	Power-saving pin
5	CP2	Charge pump capacitor connection pin 2	29	VREF	Reference voltage output pin
6	CP3	Charge pump capacitor connection pin 3	30	GND	Ground pin
7	CP4	Charge pump capacitor connection pin 4	31	STROBE	Serial enable input pin
8	VG	Charge pump output pin	32	CLK	Serial clock input pin
9	VCC	Power supply pin	33	DATA	Serial data input pin
10	PWM3	PWM control input pin ch3	34	CR2	CR timer setting element connection pin ch6
11	PWM4	PWM control input pin ch4	35	VLIM6	Output current setting pin ch6
12	PWM5	PWM control input pin ch5	36	VM4	Motor power supply pin ch6
13	OUT3A	H-bridge output pin ch3 A	37	OUT6A	H-bridge output pin ch6 A
14	RNF2	Motor ground pin ch3 and ch4	38	SENSE4	Output current detection pin ch6
15	OUT3B	H-bridge output pin ch3 B	39	RNF4	Resistance connection pin for output current detection ch6
16	VM2	Motor power supply pin ch3 and ch4	40	OUT6B	H-bridge output pin ch6 B
17	VM2	Motor power supply pin ch3 and ch4	41	OUT1A	H-bridge output pin ch1 A
18	OUT4A	H-bridge output pin ch4 A	42	RNF1	Motor ground pin ch1 and ch2
19	RNF2	Motor ground pin ch3 and 4	43	OUT1B	H-bridge output pin ch1 B
20	OUT4B	H-bridge output pin ch4 B	44	VM1	Motor power supply pin ch1 and ch2
21	OUT5A	H-bridge output pin ch5 A	45	VM1	Motor power supply pin ch1 and ch2
22	RNF3	Resistance connection pin for output current detection ch5	46	OUT2A	H-bridge output pin ch2 A
23	SENSE3	Output current detection pin ch5	47	RNF1	Motor ground pin ch1 and ch2
24	OUT5B	H-bridge output pin ch5 B	48	OUT2B	H-bridge output pin ch2 B

●Application Circuit Diagram and Function Explanation

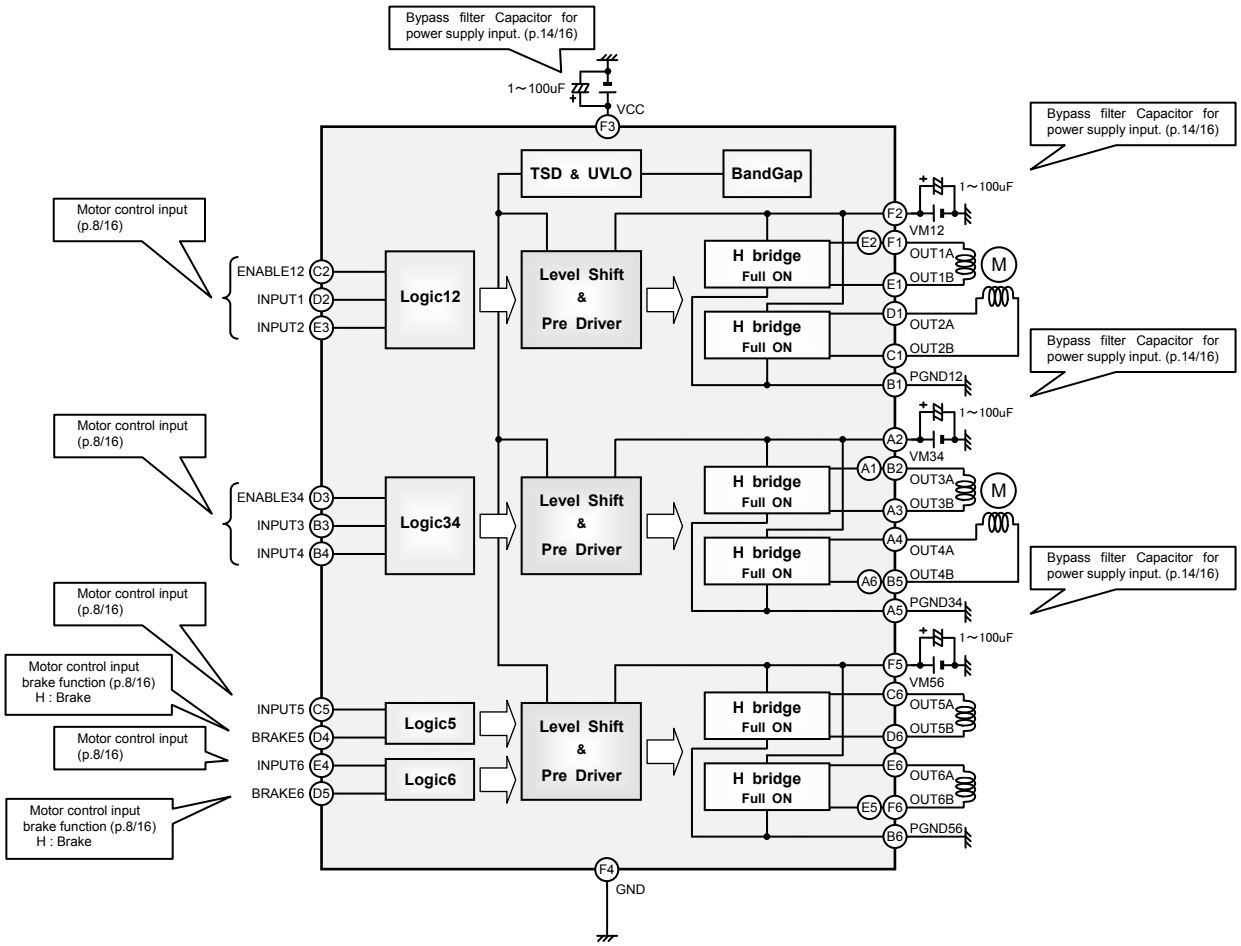


Fig.18 BD6373GW Application Circuit Diagram

1) Power-saving function
When Low-level voltage is applied to PS pin, the IC will be turned off internally and the circuit current will be 0μA (Typ.). During operating mode, PS pin should be High-level. (See the Electrical Characteristics; p.2/16)

2) Motor Control input
(1) ENABLExx and INPUTx pins (BD6373GW), INxA, INxB, EN1 and IN6 pins (BD6873KN), and PWMx pins (BD6753KV)
These pins are used to program and control the motor drive modes. (See the Electrical Characteristics; p.2/16 and p.3/16 and I/O Truth Table; p.12/16 and p.13/16)
(2) SELx pins (BD6873KN)
When the Low-level voltage is applied to the SELx pins, the I/O logic can be set to EN/IN mode. However, when the High-level voltage is applied, the I/O logic can be set to IN/IN mode. The same selection made with the BD6873KN's SELx pin can be made for the BD6753KV, using serial control. (See the Electrical Characteristics; p.2/16 and p.3/16 and I/O Truth Table)
(3) BRAKEx pins (BD6373GW) and BRK1 pin (BD6873KN)
Applying the High-level voltage pin will set the brake mode. The same selection made with the brake mode can be made for the BD6753KV, using serial control. (See the Electrical Characteristics; p.2/16 and p.3/16 and I/O Truth Table; p.12/16 and p.13/16)

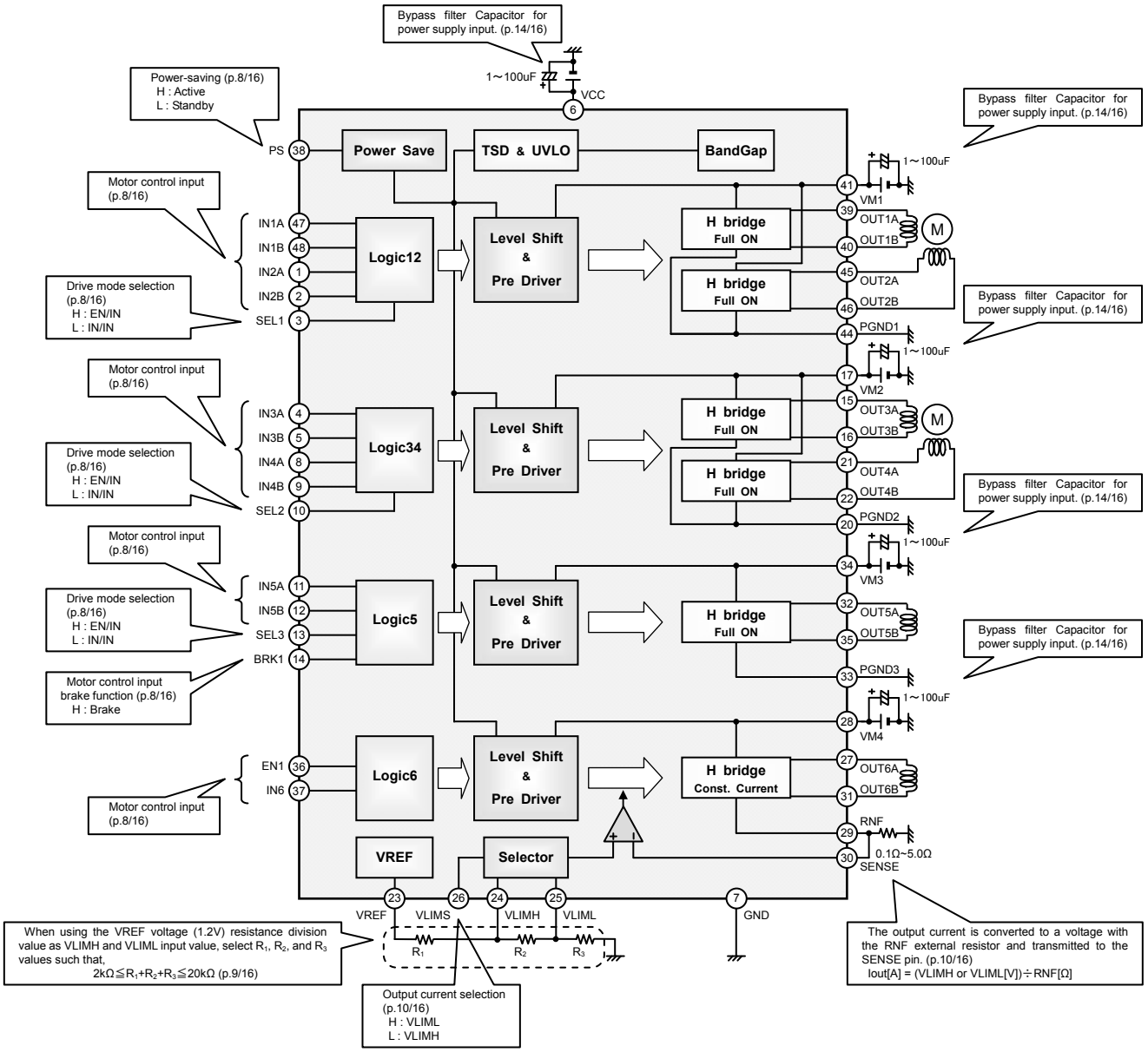


Fig.19 BD6873KN Application Circuit Diagram

3) H-bridge

The 6-channel H-bridges of can be controlled independently. For this reason, it is possible to drive the H-bridges simultaneously, as long as the package thermal tolerances are not exceeded.

The H-bridge output transistors of the BD6373GW, BD6873KN and BD6753KV consist of Power CMOS, with the motor power supply VM, and Power DMOS, with the charge pump step-up power supply VG, respectively. The total H-bridge ON-Resistance on the high and low sides varies with the VM and VG voltages, respectively. The system must be designed so that the maximum H-bridge current for each channel is 800mA or below.

4) Drive system of Linear Constant-Current H-bridge (BD6873KN: ch6)

BD6873KN (ch6) enables Linear Constant-Current Driving.

(1) Reference voltage output (with a tolerance of ±3%)

The VREF pin outputs 1.2V, based on the internal reference voltage. The output current of the Constant-Current Drive block is controllable by connecting external resistance to the VREF pin of the IC and applying a voltage divided by the resistor to the output current setting pins (VLIMH and VLIML pins). It is recommended to set the external resistance to 2kΩ or above in consideration of the current capacity of the VREF pin, and 20kΩ or below in order to minimize the fluctuation of the set value caused by the base current of the internal transistor of the IC.

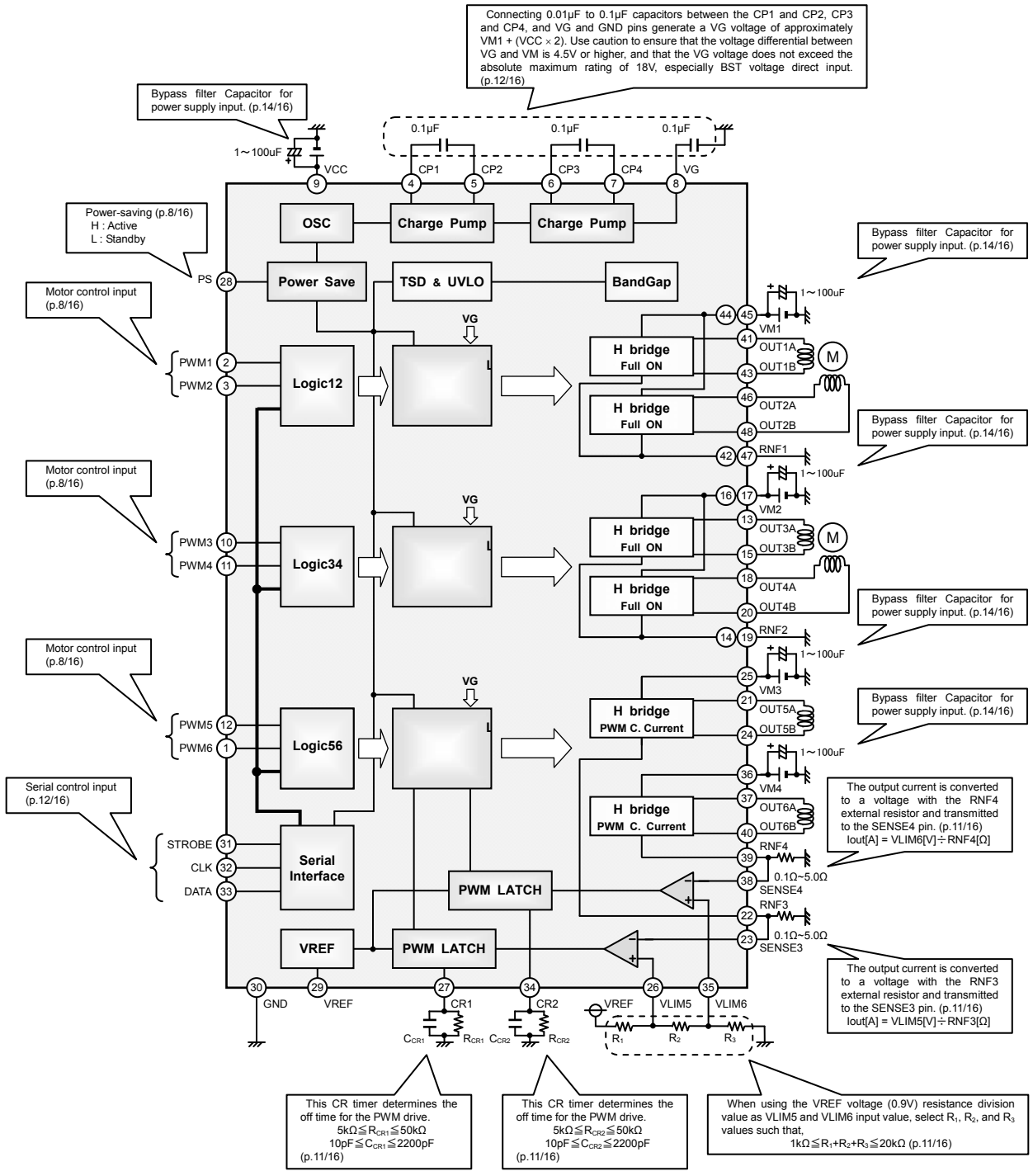


Fig.20 BD6753KV Application Circuit Diagram

(2) Output current settings and setting changes

When the Low-level control voltage is applied to the VLIMS pin, the value on the VLIMH pin will be used as an output current set value to control the output current. When the High-level control voltage is applied to the VLIMS pin, the value on the VLIML pin will be used as an output current set value to control the output current. (See the Electrical Characteristics; P.2/16)

(3) Output current detection and current settings

By connecting external resistor (0.1Ω to 5.0Ω) to the RNF pin of the IC, the motor drive current will be converted into voltage in order to be detected. The output current is kept constant by shorting the RNF and SENSE pins and comparing the voltage with the VLIMH or VLIML voltage. To perform output current settings more precisely, trim the external RNF resistance if needed, and supply a precise voltage externally to the VLIMH or VLIML pin of the IC. In that case, open the VREF pin.

$$\text{Output current value Iout[A]} = \frac{\text{VLIMH[V] or VLIML[V]}}{\text{RNF[Ω]}} \quad \begin{pmatrix}\text{Select VLIMH when VLIMS is Low-level}\\ \text{Select VLIML when VLIMS is High-level}\end{pmatrix} \cdots\cdots(1)$$

The output current is 400mA±3% if 0.2V is applied to the VLIMH or VLIML pin and a 0.5Ω resistor is connected externally to the RNF pin.

If the VLIMH and VLIML pins are shorted to the VCC pin (or the same voltage level as the VCC is applied) and the SENSE and RNF pins are shorted to the ground, this channel can be used as a Full-ON Drive H-bridge like the other five channels.

5) Drive system of PWM Constant-Current H-bridge (BD6753KV: ch5 and ch6)
BD6753KV (ch5 and ch6) enable peak current control PWM Constant-Current Driving.

(1) Output current detection and current settings

By connecting external resistance (0.1Ω to 5.0Ω) to the RNF3 and RNF4 pins of the IC, the motor drive current will be converted into voltage in order to be detected. The output current is kept constant by shorting the RNF3 and RNF4 pins with the SENSE3 and SENSE4 pins, respectively, and comparing the voltage to the set voltage input from outside the IC to the VLIM5 and VLIM6 pins. As with the BD6873KN, the reference voltage generated inside the IC (VREF pin: 0.9V±10%) can be divided using external resistors (from 1kΩ to 20kΩ). The resulting value can be input as the set voltage.
It is also necessary to connect a resistor and capacitor to the CR1 and CR2 pins, to determine the PWM drive off time.

(2) PWM Constant-Current control operation

When the output current in output ON mode increases, and the RNF3 or RNF4 voltage reaches the value set with the VLIM5 or VLIM6 voltage, the internal current limiting comparator operates to set the IC to short mode. This caused the current to be attenuated so that the H-bridge's low-side DMOS is ON. Once the off time (Toff) ends, as measured by the CR timer, the IC returns to output ON mode. By repeating this cycle, the IC maintains a fixed current due to the motor's inductance characteristics.

(3) Noise cancellation function

In order to avoid false detections by the current limiting comparator (caused by spike noise generated when output is turned on), the IC uses the noise cancellation time (Tn) to disable current detection. This begins from the time output turns on, until the noise cancellation time elapses. The noise cancellation time represents the minimum on time, and is determined by the CR pin's internal resistor, external resistor, and capacitor.

(4) CR timer

When output turns on, the CR pin is clamped at approximately 0.9V. When the mode changes to short mode, it discharges to approximately 0.4V. The interval over which this 0.5V voltage differential is discharged, is determined by the off time (Toff). Once the CR pin voltage reaches 0.4V, the pin begins to charge as the output turns on, until it reaches 0.9V. The interval over which the pin charges from 0.4V to approximately 0.8V is given by the noise cancellation time (Tn). Toff and Tn are determined by the external resistor and capacitor connected to the CR pin.
A low resistance value to the CR pin will prevent it from reaching the clamp voltage. Therefore a resistor from 5 kΩ to 50kΩ should be used. Capacitors should be from 10pF to 2200pF. The use of a capacitance in excess of 2200pF will lengthen the noise cancellation time and may cause the output current to exceed the set current. Setting a longer off time may increase the output current ripple, reducing both the average current and the motor's rotational efficiency.

$$\text{Output current value Iout[A]} = \frac{\text{VLIM5[V]}}{\text{RNF3[Ω]}} \text{ or } \frac{\text{VLIM6[V]}}{\text{RNF4[Ω]}} \quad \cdots\cdots(2)$$

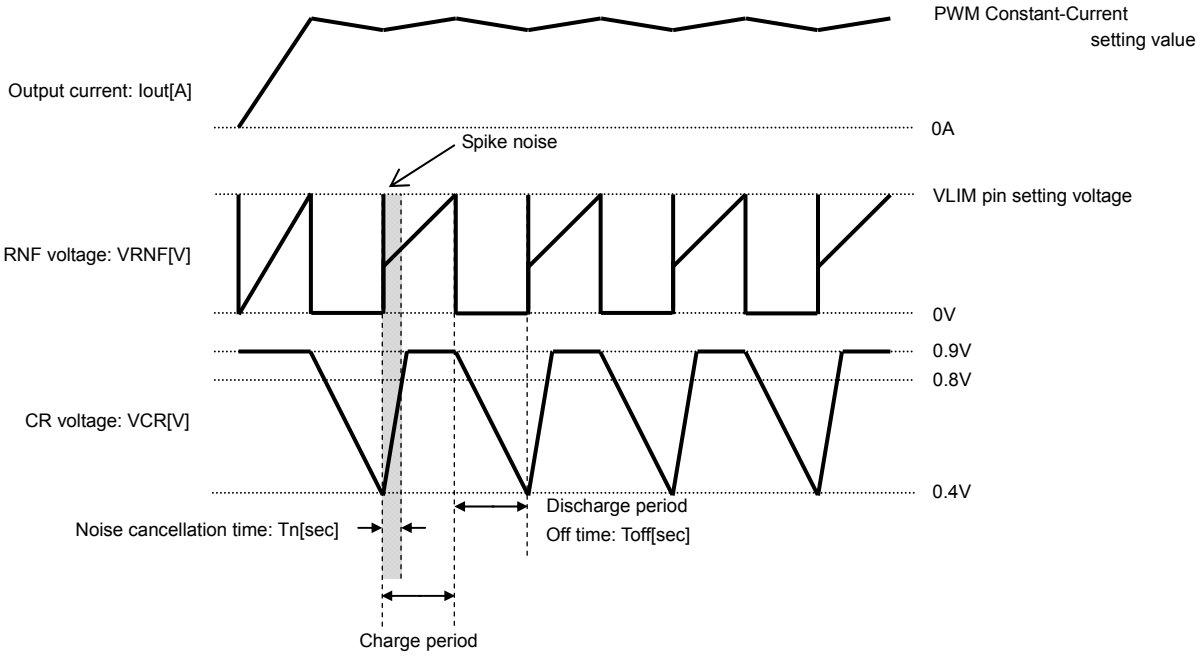


Fig.21 BD6753KV Peak Current Control PWM Constant-Current Drive Using the CR Timer

If the VLIM5 or VLIM6 is shorted to the VCC pin (or the same voltage level as the VCC is applied) and the SENSE3 or SENSE4 and RNF3 or RNF4 pins are shorted to the ground, this channel can be used as a Full-ON Drive H-bridge like the other four channels.

6) Charge pump (BD6753KV)

Each output H-bridge of the BD6753KV on the high and low sides consists of Nch DMOS. Therefore, the gate voltage VG should be higher than the VM voltage to drive the Nch DMOS on the high side.The BD6753KV has a built-in charge pump circuit that generates VG voltage by connecting an external capacitor (0.01μF to 0.1μF).

If a 0.1μF capacitor is connected between: CP1 and CP2, CP3 and CP4, VG and GND
Then, VG pin output voltage will be: VM1 + (VCC × 2)

If a 0.1μF capacitor is connected between: CP1 and CP2, VG and GND
CP4 and VG pins are shorted, and CP3 pin is open
Then, VG pin output voltage will be: VM1 + VCC

The VM1 to VM4 respectively can be set to voltages different to one another. In order to ensure better performance, the voltage differential between VG and VM must be 4.5V or higher, and the VG voltage must not exceed the absolute maximum rating of 18V.

7) Serial interface (BD6753KV)

The BD6753KV provides an 8-bit, 3-line serial interface for setting output modes. DATA is sent to the internal shift register during the STROBE low interval at the CLK rising edge. Shift register data is written to the IC's internal 6-bit memory at the STROBE rising edge, according to the addresses stored in Bit[7] and Bit[6]. The serial data input order is Bit[0] to Bit[7]. Serial settings are reset when the PS pin changes to Low-level control voltage, triggering standby mode. Serial settings are also reset when the UVLO circuit operates.

BD6753KV Serial Resistor Bit Map

No.	ADDRESS BIT		DATA BIT					
	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00H	0	0	mod2	mod1	p2a	p2b	p1a	p1b
01H	0	1	mod4	mod3	p4a	p4b	p3a	p3b
02H	1	0	mod6	mod5	p6a	p6b	p5a	p5b

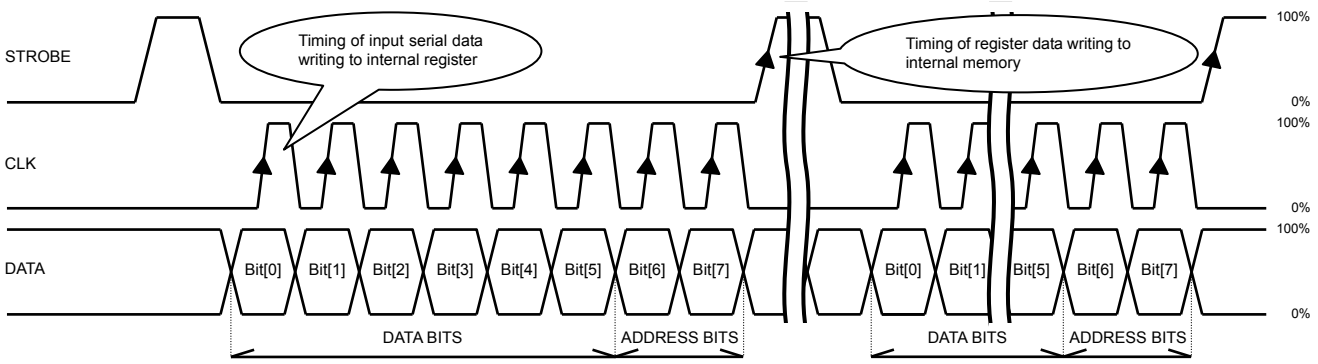


Fig.22 BD6753KV Sequence of Serial Control Input

●I/O Truth Table

BD6373GW Full-ON Driver ch1 to ch2 I/O Truth Table

Drive mode	INPUT		OUTPUT		Output mode
	ENABLE12	INPUTx	OUTxA	OUTxB	
EN/IN	H	X	Z	Z	Standby
	L	L	H	L	CW
	L	H	L	H	CCW

BD6373GW Full-ON Driver ch3 to ch4 I/O Truth Table

Drive mode	INPUT		OUTPUT		Output mode
	ENABLE34	INPUTx	OUTxA	OUTxB	
EN/IN	H	X	Z	Z	Standby
	L	L	H	L	CW
	L	H	L	H	CCW

BD6373GW Full-ON Driver ch5 to ch6 I/O Truth Table

Drive mode	INPUT		OUTPUT		Output mode
	INPUTx	BRAKEx	OUTxA	OUTxB	
IN/IN	L	L	H	L	CW
	H	L	L	H	CCW
	X	H	L	L	Brake

L: Low, H: High, X: Don't care, Z: High impedance
At CW, current flows from OUTA to OUTB. At CCW, current flows from OUTB to OUTA.

BD6873KN Full-ON Driver ch1 to ch4 I/O Truth Table

Drive mode	INPUT			OUTPUT		Output mode
	SELx	INxA	INxB	OUTxA	OUTxB	
EN/IN	L	H	X	Z	Z	Standby
		L	L	H	L	CW
		L	H	L	H	CCW
IN/IN	H	L	L	Z	Z	Standby
		H	L	H	L	CW
		L	H	L	H	CCW
		H	H	L	L	Brake

L: Low, H: High, X: Don't care, Z: High impedance
At CW, current flows from OUTA to OUTB. At CCW, current flows from OUTB to OUTA.

BD6873KN Full-ON Driver ch5 I/O Truth Table

Drive mode	INPUT				OUTPUT		Output mode
	SEL3	IN5A	IN5B	BRK1	OUT5A	OUT5B	
EN/IN	L	H	X	X	Z	Z	Standby
		L	L	L	H	L	CW
		L	H	L	L	H	CCW
		L	X	H	L	L	Brake
IN/IN	H	L	L	X	Z	Z	Standby
		H	L	X	H	L	CW
		L	H	X	L	H	CCW
		H	H	X	L	L	Brake

L: Low, H: High, X: Don't care, Z: High impedance
At CW, current flows from OUTA to OUTB. At CCW, current flows from OUTB to OUTA.

BD6873KN Linear Constant-Current Driver ch6 I/O Truth Table

Drive mode	INPUT		OUTPUT		Output mode
	EN1	IN6	OUT6A	OUT6B	
EN/IN	H	X	Z	Z	Standby
	L	L	H	L	CW
	L	H	L	H	CCW

L: Low, H: High, X: Don't care, Z: High impedance
At CW, current flows from OUTA to OUTB. At CCW, current flows from OUTB to OUTA.

BD6753KV ch1 to ch6 I/O Truth Table

Drive mode	INPUT				OUTPUT		Output mode
	Serial data			Terminal			
	modx	pxa	pxa	PWMx	OUTxA	OUTxB	
IN/IN	L	L	L	X	Z	Z	Standby
		L	H	L	L	H	CCW
		L	H	H	L	L	Brake
		H	L	L	H	L	CW
		H	L	H	L	L	Brake
		H	H	X	L	L	Brake
EN/IN	H	L	X	X	Z	Z	Standby
		H	L	L	H	L	CW
		H	L	H	L	H	CCW
		H	H	X	L	L	Brake

L: Low, H: High, X: Don't care, Z: High impedance
At CW, current flows from OUTA to OUTB. At CCW, current flows from OUTB to OUTA.

●**I/O Circuit Diagram**

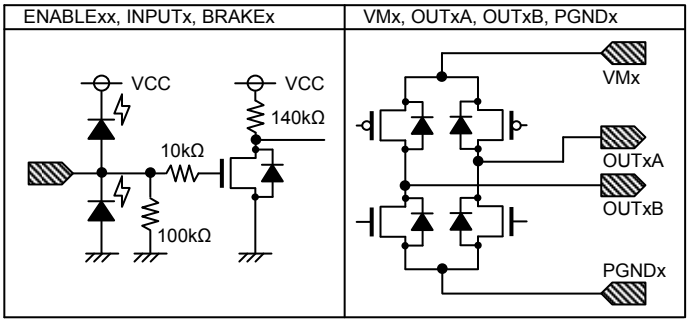


Fig.23 BD6373GW I/O Circuit Diagram (Resistance values are typical ones)

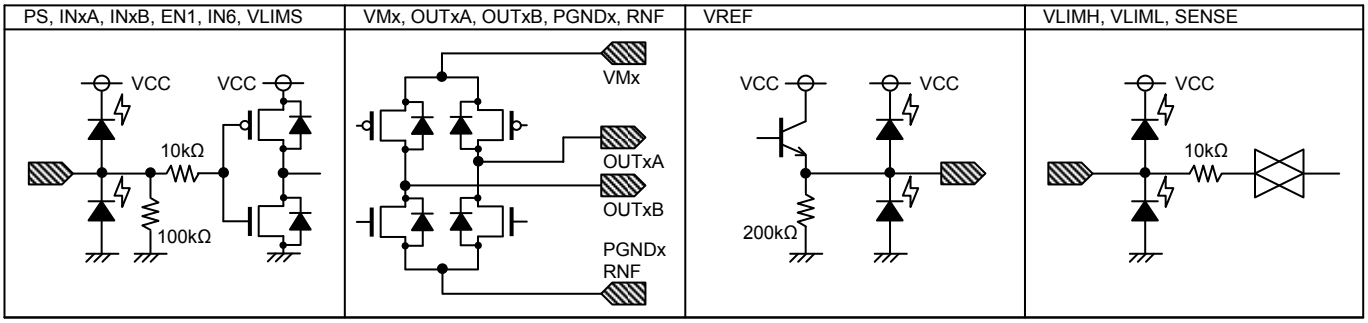


Fig.24 BD6873KN I/O Circuit Diagram (Resistance values are typical ones)

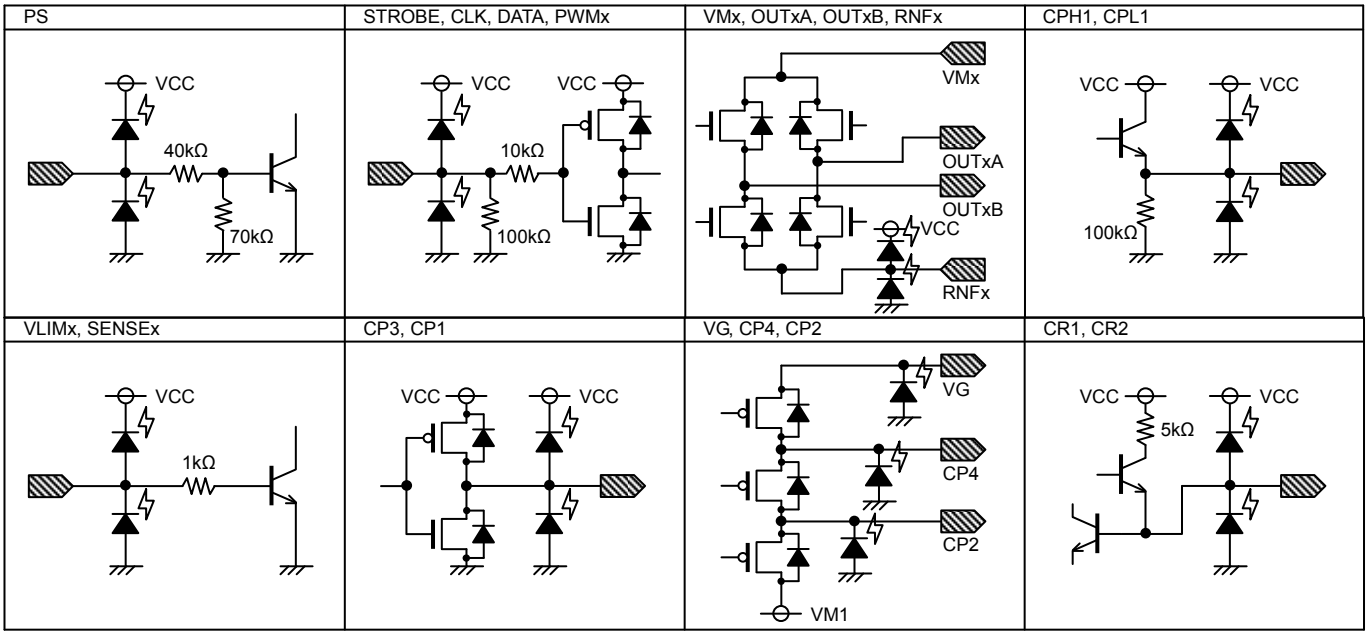


Fig.25 BD6753KV I/O Circuit Diagram (Resistance values are typical ones)

●**Operation Notes**

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) Storage temperature range
As long as the IC is kept within this range, there should be no problems in the IC's performance. Conversely, extreme temperature changes may result in poor IC performance, even if the changes are within the above range.

3) Power supply pins and lines
None of the VM line for the H-bridges is internally connected to the VCC power supply line, which is only for the control logic or analog circuit. Therefore, the VM and VCC lines can be driven at different voltages. Although these lines can be connected to a common power supply, do not open the power supply pin but connect it to the power supply externally.
Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may loose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and ground pins.
For this IC with several power supplies and a part consists of the CMOS block, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays, and to the unstable internal logic, respectively. Therefore, give special consideration to power coupling capacitance, width of power and ground wirings, and routing of wiring.

4) Ground pins and lines
Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.
When using both small signal GND and large current MGND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.
The power supply and ground lines must be as short and thick as possible to reduce line impedance.

5) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6) Pin short and wrong direction assembly of the device
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.

7) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

8) ASO
When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

9) Thermal shutdown circuit
If the junction temperature (Tjmax) reaches 175°C, the TSD circuit will operate, and the coil output circuit of the motor will open. There is a temperature hysteresis of approximately 25°C (BD6373GW and BD6873KN Typ.) and 25°C (BD6753KV Typ.). The TSD circuit is designed only to shut off the IC in order to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. The performance of the IC's characteristics is not guaranteed and it is recommended that the device is replaced after the TSD is activated.

10) Serial data input
In the BD6753KV, DATA input string start with LSB first.
The serial settings are reset during standby mode operation and whenever the UVLO or TSD circuits are operating.

11) Power saving terminal
Be cancelled power saving mode after turned on power supply VCC and VM, because of PS terminal combines power saving with serial reset function. If the case of power saving terminal always shorted power supply terminal, reset function may not be well, and it may cause the IC to malfunction.

12) Testing on application board
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

13) Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics. When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

14) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
When GND > Pin A, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic diode and transistor.
Parasitic elements can occur inevitably in the structure of the IC. The operation of parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic elements operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

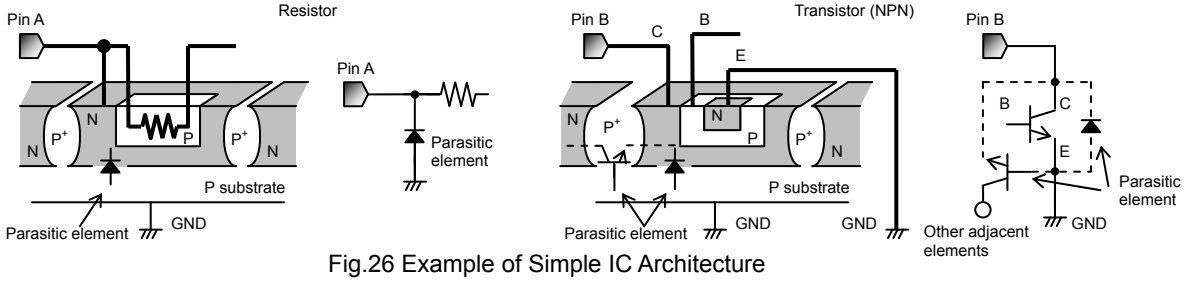


Fig.26 Example of Simple IC Architecture

●**Ordering part number**

B	D	6	3	7	3	G	W	-	E	2

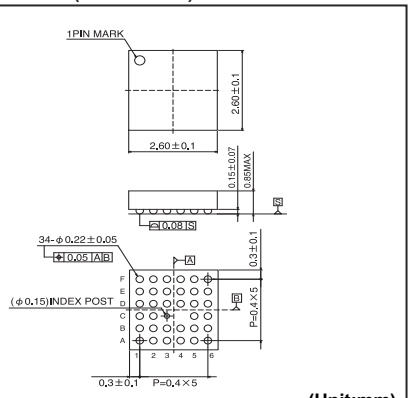
Part No.

Part No.
6373 : F.ON 6ch
6873 : F.ON 5ch+C.C. 1ch
6753 : F.ON 4ch+PWM 2ch

Package
GW : UCSP75M2
KN : UQFN48
KV : VQFP48C

Packaging and forming specification
E2: Embossed tape and reel
(UCSP75M2/ UQFN48))
None: Tray
(VQFP48C)

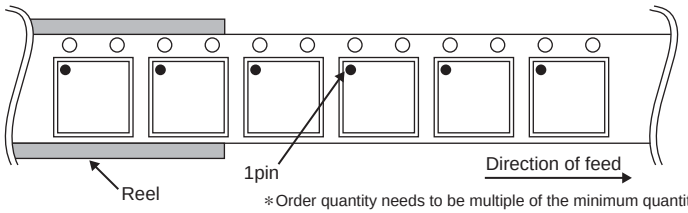
UCSP75M2 (BD6373GW)



(Unit:mm)

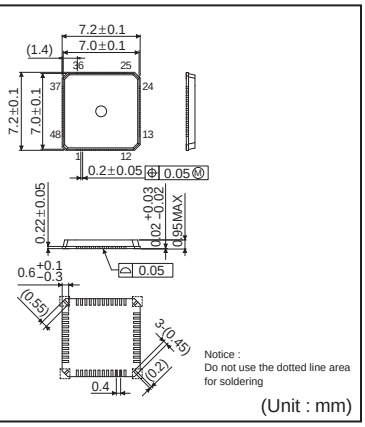
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

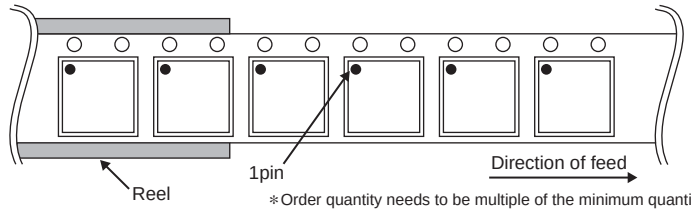
UQFN48



(Unit : mm)

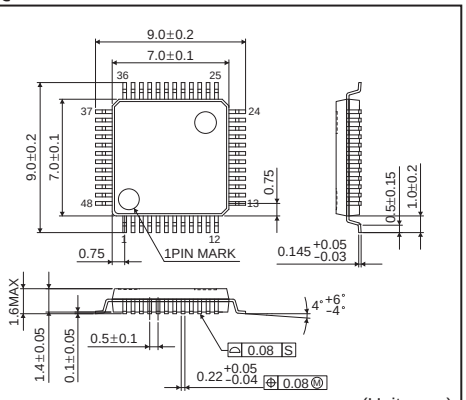
<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

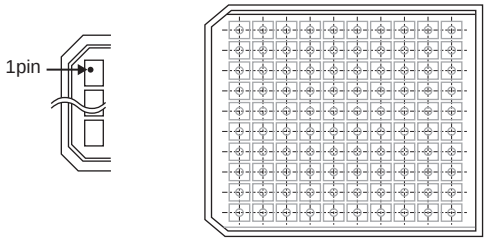
VQFP48C



(Unit : mm)

<Tape and Reel information>

Container	Tray
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray



∗Order quantity needs to be multiple of the minimum quantity.

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