

STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCT SERIES	Single-Phase Full-Wave Motor Driver for Fan Motor
TYPE	B D 6 9 7 3 F V
FEATURES	Pre-driver compatible for external Tr Speed controllable by DC/PWM input PWM soft switching drive

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit	Unit
Supply voltage	Vcc	20	V
Power dissipation	Pd	874.7 *	mW
Operating temperature	Topr	-40 to +100	°C
Storage temperature	Tstg	-55 to +150	°C
High side output voltage	VOH	36	V
Low side output voltage	VOL	15	V
Low side output current	IOL	10	mA
FG output current	IFG	10	mA
FG output voltage	VFG	20	V
REF current ability	IREF	12	mA
HB current ability	IHB	12	mA
Input voltage(H+, H-, TH, MIN, CS, SS)	VIN	7	V
Junction temperature	Tjmax	150	°C

* Reduce by 7.0mW/°C over Ta=25°C.
(On 70.0mm × 70.0mm × 1.6mm glass epoxy board)

OPERATING CONDITIONS

Parameter	Symbol	Limit	Unit
Operating supply voltage range	Vcc	4.3 to 17.0	V
Hall input voltage range	VH	0 to Vcc-2.0	V
		0 to 7.0	V
TH input voltage range	VTH	0 to REF	V
MIN input voltage range	VMIN	0 to REF	V

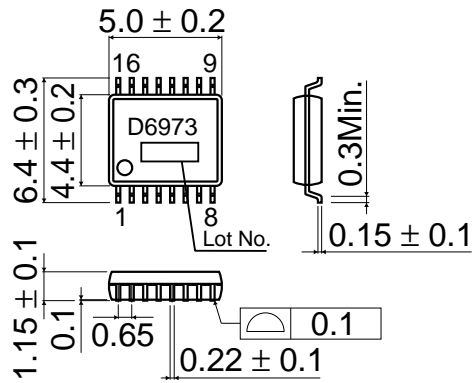
less than Vcc=9.0V
more than Vcc=9.0V

* This product is not designed for production against radioactive rays.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta=25°C, Vcc=12V)

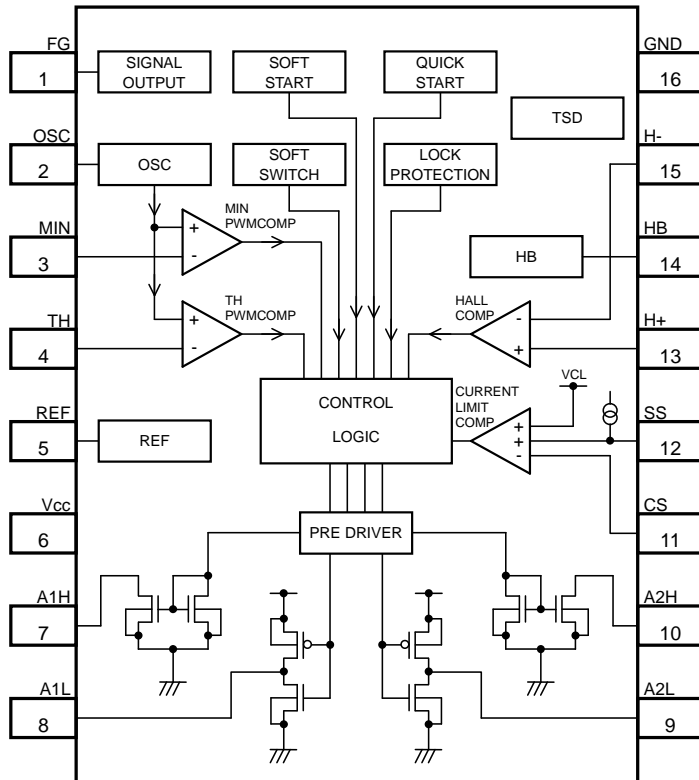
Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Circuit current	Icc	3	5	8	mA	
Hall input hysteresis	VHYS	±5	±10	±15	mV	
High side output current	IH	9.0	12.0	16.5	mA	VOH=12V
High side output leak current	IHL	-	-	10	µA	VOH=36V
Low side output high voltage	VLH	9.3	9.5	-	V	IOL=-5mA
Low side output low voltage	VLL	-	0.5	0.7	V	IOL=5mA
Lock detection ON time	TON	0.2	0.3	0.45	s	
Lock detection OFF time	TOFF	4.0	6.0	9.0	s	
FG output low voltage	VFGL	-	-	0.3	V	IFG=5mA
FG output leak current	IFGL	-	-	10	µA	VFG=17V
OSC low voltage	VOSCL	0.8	1.0	1.2	V	
OSC high voltage	VOSCH	2.3	2.5	2.7	V	
OSC charge current	ICOSC	-55	-40	-25	µA	
OSC discharge current	IDOSC	25	40	55	µA	
Output ON duty 1	DUTY1	75	80	85	%	VTH=VREF × 0.26 (H side pull up R=1kΩ, COSC=470pF)
Output ON duty 2	DUTY2	45	50	55	%	VTH=VREF × 0.35 (H side pull up R=1kΩ, COSC=470pF)
Output ON duty 3	DUTY3	15	20	25	%	VTH=VREF × 0.44 (H side pull up R=1kΩ, COSC=470pF)
REF voltage	VREF	4.8	5.0	5.2	V	IREF=-2mA
Hall bias voltage	VHB	1.10	1.26	1.50	V	IHB=-2mA
Current limit voltage	VCL	120	150	180	mV	
SS charge current	ISS	50	120	300	nA	VSS=0V
TH bias current	ITH	-	-	0.2	µA	
MIN bias current	IMIN	-	-	0.2	µA	
CS bias current	ICS	-	-	0.2	µA	

OPACKAGE OUTLINES



SSOP-B16 (UNIT: mm)

OBLOCK DIAGRAM



OTERMINAL NAME

PIN No.	Terminal name
1	FG
2	OSC
3	MIN
4	TH
5	REF
6	V _{cc}
7	A1H
8	A1L
9	A2L
10	A2H
11	CS
12	SS
13	H+
14	HB
15	H-
16	GND

CAUTIONS ON USE

1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3) Power supply line

Back electromotive force causes regenerated current to power supply line, therefore take a measure such as placing a capacitor between power supply and GND for routing regenerated current. And fully ensure that the capacitor characteristics have no problem before determine a capacitor value. (when applying electrolytic capacitors, capacitance characteristic values are reduced at low temperatures)

4) GND potential

It is possible that the motor output terminal may deflect below GND terminal because of influence by back electromotive force of motor. The potential of GND terminal must be minimum potential in all operating conditions, except that the levels of the motor outputs terminals are under GND level by the back electromotive force of the motor coil. Also ensure that all terminals except GND and motor output terminals do not fall below GND voltage including transient characteristics. Malfunction may possibly occur depending on use condition, environment, and property of individual motor. Please make fully confirmation that no problem is found on operation of IC.

5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9) Thermal shut down circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). Operation temperature is 175°C (typ.) and has a hysteresis width of 25°C (typ.). When IC chip temperature rises and TSD circuit works, the output terminal becomes an open state. TSD circuit is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operation this circuit or use the IC in an environment where the operation of this circuit is assumed.

10) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

11) GND wiring pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

12) Capacitor between output and GND

When a large capacitor is connected between output and GND, if Vcc is shorted with 0V or GND for some cause, it is possible that the current charged in the capacitor may flow into the output resulting in destruction. Keep the capacitor between output and GND below 100uF.

13) IC terminal input

When Vcc voltage is not applied to IC, do not apply voltage to each input terminal. When voltage above Vcc or below GND is applied to the input terminal, parasitic element is actuated due to the structure of IC. Operation of parasitic element causes mutual interference between circuits, resulting in malfunction as well as destruction in the last. Do not use in a manner where parasitic element is actuated.

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