TECHNICAL NOTE

## For LCD Panel Backlight Applications

# White LED Driver IC

## BD8118FM

rev. 1.50

**● Outline**

BD8118FM is a white LED driver featuring a high input voltage range (36V MAX), an integrated step-up DC/DC converter and four constant-current output drivers on a single chip. Brightness can be controlled by either PWM or VDAC methods.

**● Features**

1) Input voltage range 4.5 – 30 V
2) Integrated step-up DC/DC controller
3) Four integrated LED current driver channels (150 mA max. each channel)
4) Compatible with PWM light-modulation (0.38 – 99.5%)
5) Built-in protection functions (UVLO, OVP, TSD, OCP)
6) Abnormal status detection function (open)
7) HSOP-M28 package

**● Applications**

Car navigation system backlights, small/medium-sized LCD panels, etc.

**● Absolute maximum ratings** (Ta = 25 ℃)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage (Pin 1) | $V_{CC}$ | 36 | V |
| Load switch output voltage (Pin 2) | $V_{LOADSW}$ | 36 | V |
| LED output voltage (Pin 12,14,15,17) | $V_{LED}$ | 36 | V |
| FAIL output voltage (Pin 3,20) | $V_{OL}$ | 7 | V |
| Input voltage (Pin 5,6,10,11,24) | $V_{IN}$ | -0.3～7 < $V_{CC}$ | V |
| VDAC input voltage (Pin 8) | $V_{DAC}$ | -0.3～7 < $V_{CC}$ | V |
| Power Consumption | Pd | 2.20 ※1 | W |
| Junction temperature | Tjmax | 150 | ℃ |
| Operating temperature range | Topr | -40～+95 | ℃ |
| Storage temperature range | Tstg | -55～+150 | ℃ |
| LED maximum output current (Pin : 12,14,15,17) | $I_{LED}$ | 150 ※2 ※3 | mA |

※1 IC mounted on glass epoxy board measuring 70mm×70mm×1.6mm, power dissipated at a rate of 17.6mw/℃ at temperatures above 25℃.

※2 Dispersion figures for LED maximum output current and $V_F$ are correlated. Please refer to data on separate sheet.

※3 Amount of current per channel.

**● Operating conditions** (Ta = 25 ℃)

| Parameter | Symbol | Target value | Unit |
|---|---|---|---|
| Power supply voltage (Pin 1) | $V_{CC}$ | 4.5～30 | V |
| Oscillating frequency range | $F_{OSC}$ | 50～550 | kHz |
| External synchronization frequency range (Pin 6) ※4 ※5 | $F_{SYNC}$ | fosc～550 | kHz |
| External synchronization pulse duty range (Pin 6) | $F_{SDUTY}$ | 40～60 | % |

※4 Connect SYNC to GND when not using external frequency synchronization.

※5 Do not switch between internal and external synchronization when an external synchronization signal is input to the device.

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● **Electrical Characteristics** (unless otherwise specified, VCC=12V Ta=25℃)

| Parameter | Symbol | Target value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Circuit current | $I_{CC}$ | 2.5 | 6 | 10 | mA | EN=Hi, SYNC=VREG, RT=OPEN PWM=OPEN, ISET=OPEN, $C_{IN}$=1μF |
| Standby current | $I_{ST}$ | - | 0 | 2 | μA | EN=Low |
| **[VREG Block (VREG)]** | | | | | | |
| Reference voltage | $V_{REG}$ | 4.5 | 5 | 5.5 | V | $I_{REG}$=-10mA, $C_{REG}$=1μF |
| **[SW Block (SWOUT,CS)]** | | | | | | |
| SWOUT high-side ON resistance | $R_{ONH}$ | 0.05 | 3 | 7 | Ω | $I_{ON}$=-10mA |
| SWOUT low-side ON resistance | $R_{ONL}$ | 0.05 | 2 | 5 | Ω | $I_{ON}$=10mA |
| Over-current protection operating voltage | $V_{DCS}$ | 0.3 | 0.4 | 0.5 | V | $V_{CS}$=sweep up |
| **[Error Amplifier (COMP,SS)]** | | | | | | |
| LED control voltage | $V_{LED}$ | 0.7 | 0.8 | 0.9 | V | |
| COMP sink current | $I_{SKCP}$ | 40 | 100 | 200 | μA | $V_{LED}$=2V, Vcomp=1V |
| COMP source current | $I_{SCCP}$ | -200 | -100 | -40 | μA | $V_{LED}$=0V, Vcomp=1V |
| SS charging current | $I_{SS}$ | -14 | -10 | -6 | μA | $V_{SS}$＝1.0V |
| SS maximum voltage | $V_{MXSS}$ | 2.0 | 2.5 | 3.0 | V | EN＝High |
| SS standby current | $I_{STSS}$ | - | 0 | 2 | μA | EN＝Low |
| **[Oscillator Block (RT, SWOUT)]** | | | | | | |
| Oscillating frequency | $F_{OSC}$ | 250 | 300 | 350 | KHz | $R_T$=100kΩ |
| **[OVP Block (OVP)]** | | | | | | |
| Over-voltage detection reference voltage | $V_{DOVP}$ | 1.86 | 2.0 | 2.14 | V | $V_{OVP}$=Sweep up |
| OVP hysteresis width | $V_{DOHS}$ | 0.35 | 0.45 | 0.55 | V | $V_{OVP}$=Sweep down |
| **[UVLO Block (VREG)]** | | | | | | |
| Reduced-voltage detection reference voltage | $V_{DUVLO}$ | 2.5 | 2.8 | 3.1 | V | $V_{REG}$=Sweep down |
| UVLO hysteresis width | $V_{DUHS}$ | 50 | 100 | 200 | mV | $V_{REG}$=Sweep up |
| **[Load Switch Block (open-drain) (LOADSW)]** | | | | | | |
| Load switch LOW voltage | $V_{LDL}$ | 0.05 | 0.15 | 0.3 | V | $I_{LOAD}$=10mA |
| **[LED Output Block (LED1-4, ISET, PWM, VDAC, OVP)]** | | | | | | |
| LED current relative dispersion width | $\triangle I_{LED1}$ | 0 | 3 | 6 | % | $I_{LED}$=50mA ※1 |
| LED current absolute dispersion width | $\triangle I_{LED2}$ | -6 | 0 | 6 | % | $I_{LED}$=50mA |
| ISET voltage | $V_{ISET}$ | 1.96 | 2.0 | 2.04 | V | |
| PWM light modulation | Duty | 0.38 | - | 99.5 | % | $F_{PWM}$=150Hz, $I_{LED}$=50mA ※2, 3, 4, |
| PWM frequency | $F_{PWM}$ | 0 | - | 20 | KHz | Duty=50%, $I_{LED}$=50mA ※3 |
| VDAC gain | $G_{VDAC}$ | 20 | 25 | 30 | mA/V | $V_{DAC}$=0～2V, $I_{LED}$=50mA ※3 |
| Open detection voltage 1 | $V_{DOP1}$ | 0.05 | 0.15 | 0.3 | V | $V_{LED}$= Sweep down, $V_{OVP}$＞$V_{DOP2}$, $V_{SS}$≧$V_{MXSS}$ |
| Open detection voltage 2 | $V_{DOP2}$ | 1.56 | 1.7 | 1.84 | V | $V_{OVP}$= Sweep up, $V_{LED}$＞$V_{DOP1}$, $V_{SS}$≧$V_{MXSS}$ |
| **[Logic Inputs (EN, SYNC, PWM, LEDEN1, LEDEN2)]** | | | | | | |
| Input HIGH voltage | $V_{INH}$ | 2.6 | - | 5.5 | V | |
| Input LOW voltage | $V_{INL}$ | GND | - | 0.8 | V | |
| Input current 1 | $I_{IN}$ | 18 | 35 | 53 | μA | $V_{IN}$=5V(SYNC,PWM,LEDEN1,LEDEN2) |
| Input current 2 | $I_{EN}$ | 13 | 25 | 38 | μA | $V_{EN}$=5V (EN) |
| **[FAIL Output (open drain) (FAIL1, FAIL2)]** | | | | | | |
| FAIL LOW voltage | $V_{FLL}$ | 0.05 | 0.1 | 0.2 | V | $I_{OL}$=1mA |

◎ This product is not designed for use in radioactive environments.

※1 (MAX(ILED)-MIN(ILED))/(AVE(ILED)x100

※2 $I_{LED}$=$V_{ISET}$÷$R_{ISET}$×3300, $V_{DAC}$＞$V_{ISET}$

※3 $I_{LED}$=$V_{DAC}$÷$R_{ISET}$×3300

※4 0%/100%-input capable

● **Reference data** (unless otherwise specified, Ta=25℃)

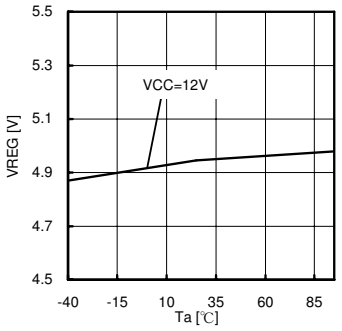



Fig.1 VREG temperature characteristic

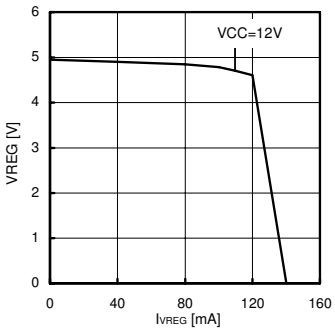



Fig.2 VREG current capacity

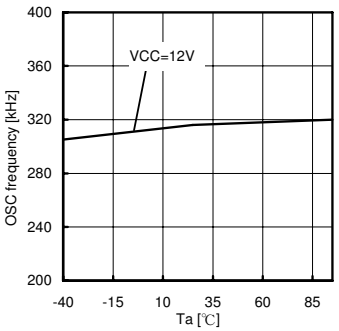



Fig.3 OSC temperature characteristic

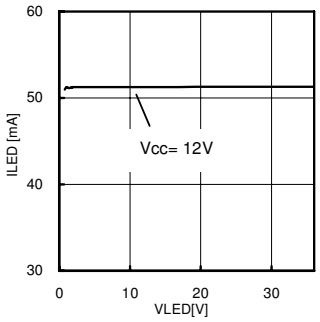



Fig.4 ILED's dependence on VLED

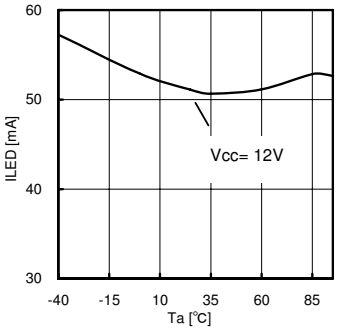



Fig.5 ILED temperature characteristic

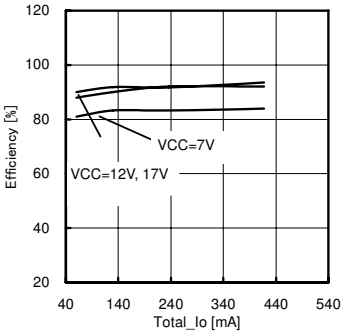



Fig.6 efficiency

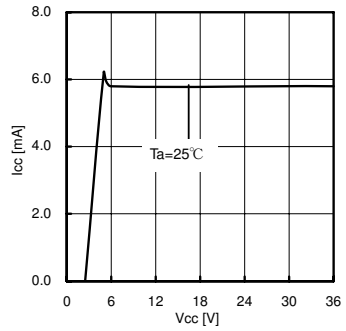



Fig.7 ICC-VCC

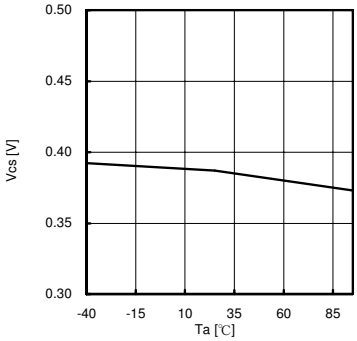



Fig.8 Overcurrent detecting voltage temperature characteristic

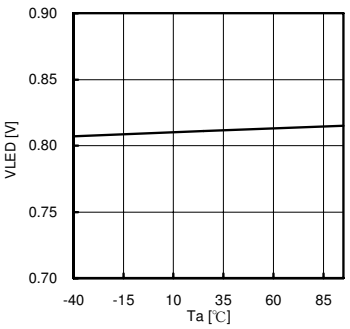



Fig.9 VLED temperature characteristic

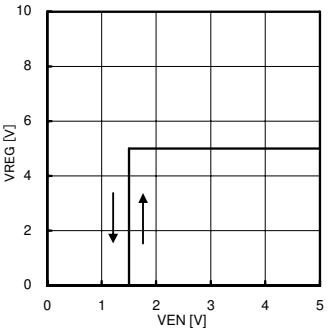



Fig.10 EN threshold voltage

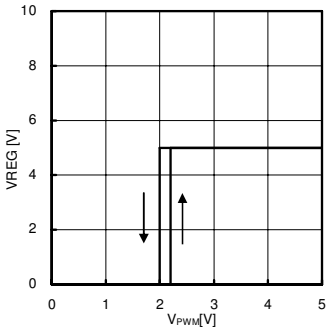



Fig.11 PWM threshold voltage

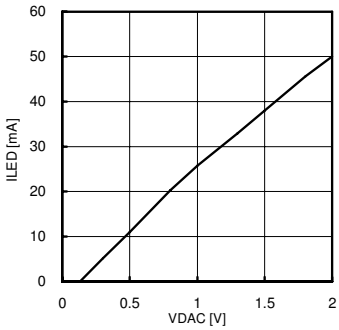



Fig.12 VDAC gain

● **Block diagram**

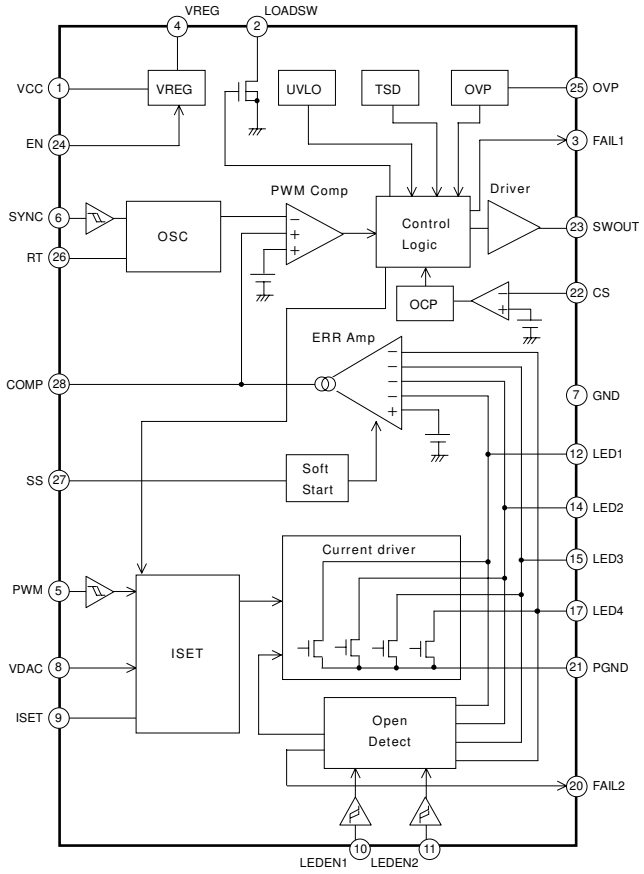



Fig.13

● **Pin layout**

BD8118FM (HSOP-M28)

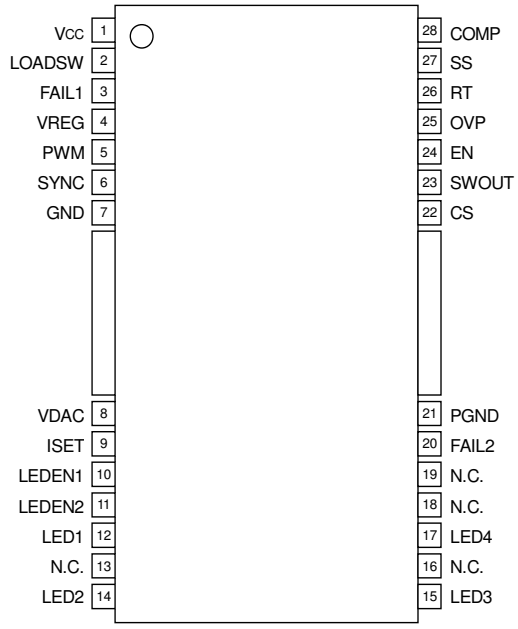



Fig.14

● **Pin function table**

| Pin | Symbol | Function |
|---|---|---|
| 1 | VCC | Input power supply |
| 2 | LOADSW | FET connection for load switch |
| 3 | FAIL1 | Failure signal output |
| 4 | VREG | Internal reference voltage output |
| 5 | PWM | PWM light modulation input |
| 6 | SYNC | External synchronization signal input |
| 7 | GND | Small-signal GND |
| 8 | VDAC | DC variable light modulation input |
| 9 | ISET | LED output current-setting resistance input |
| 10 | LEDEN1 | LED output enable pin 1 |
| 11 | LEDEN2 | LED output enable pin 2 |
| 12 | LED1 | LED output 1 |
| 13 | - | N.C. |
| 14 | LED2 | LED output 2 |
| 15 | LED3 | LED output 3 |
| 16 | - | N.C |
| 17 | LED4 | LED output 4 |
| 18 | - | N.C. |
| 19 | - | N.C. |
| 20 | FAIL2 | LED open detection signal output |
| 21 | PGND | LED output GND |
| 22 | CS | DC/DC output current detection input |
| 23 | SWOUT | DC/DC switching output |
| 24 | EN | Enable input |
| 25 | OVP | Over-voltage detection input |
| 26 | RT | Oscillation frequency-setting resistance input |
| 27 | SS | Soft start time-setting capacitance input |
| 28 | COMP | Error amplifier output |

**• 5V voltage reference (VREG)**

5V (Typ.) is generated from the VCC input voltage when the enable pin is set high. This voltage is used to power internal circuitry, as well as the voltage source for device pins that need to be fixed to a logical HIGH.

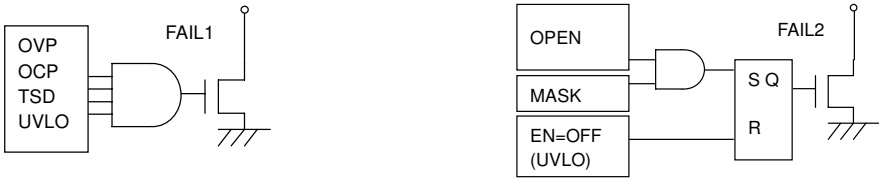
UVLO protection is integrated into the VREG pin. The voltage regulation circuitry operates uninterrupted for output voltages higher than 2.9 V (Typ.), but if output voltage drops to 2.8 V (Typ.) or lower, UVLO engages and turns the IC off.

Connect a capacitor (Creg = 10uF Typ.) to the VREG terminal for phase compensation. Operation may become unstable if Creg is not connected.

**• Self-diagnostic functions**

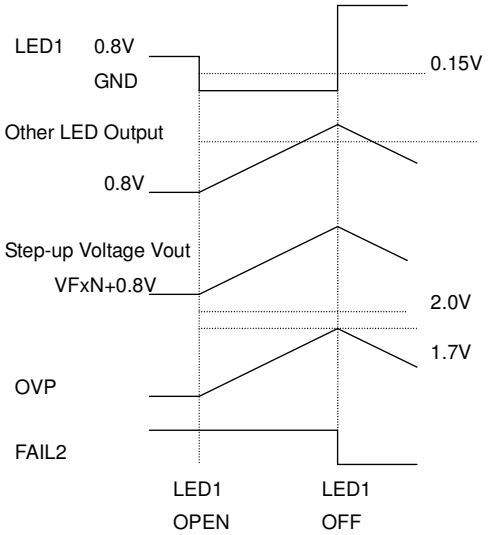
The operating status of the internal protection circuitry is transmitted via the FAIL1 and FAIL2 output pins (open drain).

When UVLO, OVP, OCP or TSD protection is engaged, FAIL1 and SWOUT output are pulled low, and step-up DC/DC conversion is stopped. For OCP, SWOUT is pulled low for only 1 cycle of FOSC, as the protection is activated on a pulse-by-pulse basis. If UVLO, OVP or TSD protection is engaged, LED output pins are held open (Hi-Z). The TSD, OVP and OCP functions also serve to protect the VREG terminal. Additionally, FAIL1 and LOADSW outputs are internally inverted; thus, if FAIL1 engages (i.e. is pulled low), then LOADSW will turn off.




FAIL2 output is pulled low when an open circuit is detected. The open circuit detection engages via a latch, which is cycled via the ON/OFF (UVLO) signal from the EN terminal. The device detects an open circuit if the LED output is lower than 0.15V (Typ.), or if the voltage at the OVP pin reaches 1.7V (Typ.) or more.

FAIL output pins are open-drain, so ensure pull-up resistors are connected to both for proper operation.




**• Constant-current LED drivers**

If less than four constant-current drivers are used, unused channels should be switched off via the LEDEN pin configuration. The truth table for these pins is shown below. If a driver output is enabled but not used (i.e. left open), the IC's open circuit-detection circuitry will operate. Do not connect the driver output to GND as the inputs of the error amplifier cannot be deactivated via the LEDEN pin. Instead, keep the driver output floating or connect it to VREG. The LEDEN terminals are pulled down internally in the IC, so if left open, the IC will recognize them as logic LO. However, they should be connected directly to VREG or fixed to a logic HI when in use.

| LED EN | | LED | | | |
|---|---|---|---|---|---|
| 〈1〉 | 〈2〉 | 1 | 2 | 3 | 4 |
| L | L | ON | ON | ON | ON |
| H | L | ON | ON | ON | OFF |
| L | H | ON | ON | OFF | OFF |
| H | H | ON | OFF | OFF | OFF |

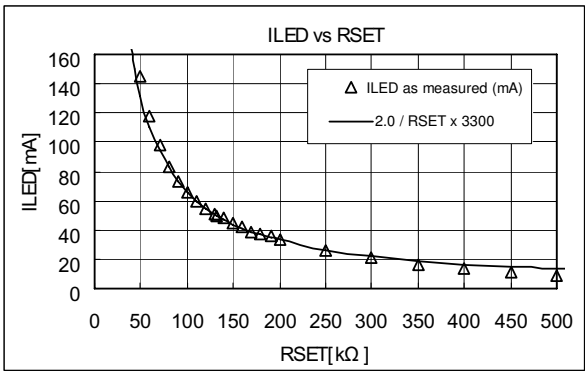
**・Output current setting**

LED current is computed via the following equation:

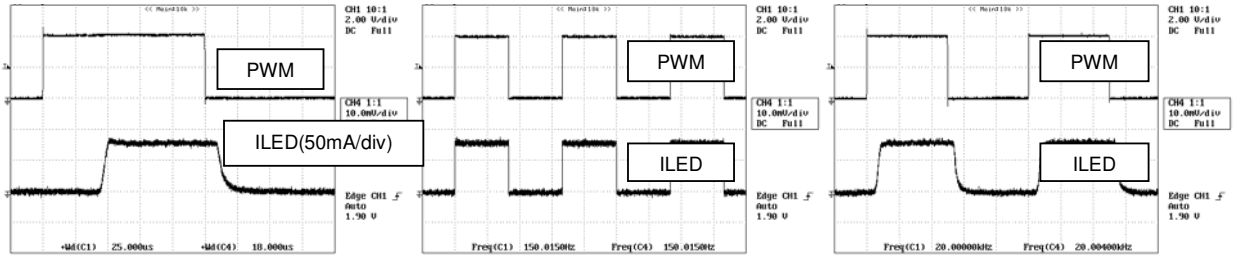
$$I_{LED} = \mathbf{min}[\mathbf{VDAC}\ ,\ \mathbf{VISET}(=2.0V)] / \mathbf{RSET} \times \mathbf{3300}\ [mA]$$

(min[VDAC , 2.0V] = the smaller value of either VDAC or VISET; 3300 (Typ.) = constant set by internal circuitry.)
In applications where an external signal is used for output current control, a control voltage in the range of 0.1 to 2.0 V can be connected on the VDAC pin to control according to the above equation. If an external control signal is not used, connect the VDAC pin to VREG (do not leave the pin open as this may cause the IC to malfunction). Also, do not switch individual channels on or off via the LEDEN pin while operating in PWM mode.

The following diagram illustrates the relation between RISET and ISET.




In PWM intensity control mode, the ON/OFF state of each current driver is controlled directly by the input signal on the PWM pin; thus, the duty ratio of the input signal on the PWM pin equals the duty ratio of the LED current. When not controlling intensity via PWM, fix the PWM terminal to a high voltage (100%). Output light intensity is greatest at 100% input. Inserting a low-pass filter (cut off frequency: 30 kHz) on the PWM pin is recommended.




PWM=150Hz Duty=0.38% | PWM=150Hz Duty=50% | PWM=20kHz Duty=50%

**● Step-up DC/DC controller**

**・Number of LEDs in series connection**

Output voltage of the step-up converter is controlled such that the forward voltage over each of the LEDs on the output is set to 0.8V (Typ.). Step-up operation is performed only when the LED output is operating. When two or more LED outputs are operating simultaneously, the LED voltage output is held at 0.8V (Typ.) per LED over the column of LEDs with the highest VF value. The voltages of other LED outputs are increased only in relation to the fluctuation of voltage over this column. Consideration should be given to the change in power dissipation due to variations in VF of the LEDs.

The number of LEDs that can be connected in series is limited due to the open-circuit protection circuit, which engages at 85% of the set OVP voltage. Therefore, the maximum output voltage of the under normal operation becomes **30.6** V (= **36** V x **0.85**, where (**30.6** V – **0.8** V) / **VF** > **N** [maximum number of LEDs in series]).

**・ Over-voltage protection circuit (OVP)**

The output of the step-up converter should be connected to the OVP pin via a voltage divider. In determining an appropriate trigger voltage of for OVP function, consider the total number of LEDs in series and the maximum variation in VF. Also, bear in mind that open detection is triggered at 0.85 x OVP trigger voltage. If the OVP function engages, it will not release unless the step-up voltage drops to 77.5% of the OVP trigger voltage. For example, if ROVP1 (step-up voltage side), ROVP2 (GND side), and step-up voltage VOUT are conditions for OVP, then: **VOUT** ≥ (**ROVP1** + **ROVP2**) / **ROVP2** x **2.0** V.
OVP will engage when **VOUT** > **32** V if **ROVP1** = **330** kΩ and **ROVP2** = **22** kΩ.

**▪ Step-up DC/DC converter oscillation frequency (FOS)**

The regulator's internal triangular wave oscillation frequency can be set via a resistor connected to the RT pin (pin 26). This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillating frequency. Refer to the following theoretical formula when setting RT:

$$f_{OSC} = \frac{30 \times 10^6}{RT\ [\Omega]} \times \alpha\ [kHz]$$

$30 \times 10^6$ (V/A/S) is a constant (±16.6%) determined by the internal circuitry, and α is a correction factor that varies in relation to RT:

{ RT: α = 50kΩ: 0.98, 60kΩ: 0.985, 70kΩ: 0.99, 80kΩ: 0.994, 90kΩ: 0.996, 100kΩ: 1.0, 50kΩ: 1.01, 200kΩ: 1.02, 300kΩ: 1.03, 400kΩ: 1.04, 500kΩ: 1.045 }

A resistor in the range of 62.6kΩ～523kΩ is recommended. Settings that deviate from the frequency range shown below may cause switching to stop, and proper operation cannot be guaranteed.

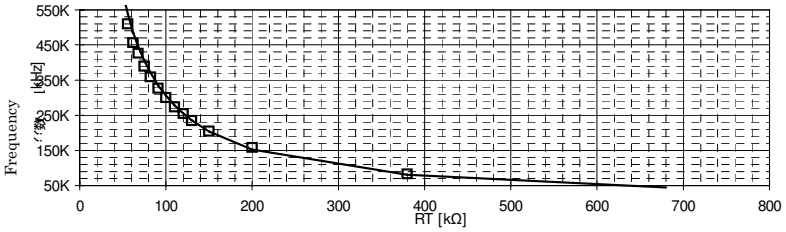



Fig.15 RT versus switching frequency

**▪ External DC/DC converter oscillating frequency synchronization (FSYNC)**

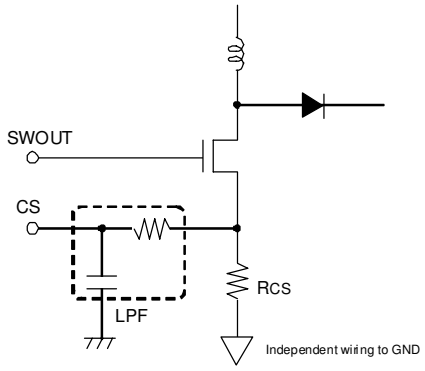
Do not switch from external to internal oscillation of the DC/DC converter if an external synchronization signal is present on the SYNC pin. When the signal on the SYNC terminal is switched from high to low, a delay of about 30 µS (typ.) occurs before the internal oscillation circuitry starts to operate (only the rising edge of the input clock signal on the SYNC terminal is recognized). Moreover, if external input frequency is less than the internal oscillation frequency, the internal oscillator will engage after the above-mentioned 30 µS (typ.) delay; thus, do not input a synchronization signal with a frequency less than the internal oscillation frequency.

**▪ Over-Current protection circuit (OCP)**

Insert a current-sense resistor $R_{CS}$ between GND and the source of the n-MOSFET for current detection at the output of the DC/DC converter. A low-pass filter (LPF) with a cutoff frequency of 1-2 MHz should also be inserted between the CS pin and $R_{CS}$ in order to reduce switching noise. Ensure, however, that the time constant of this filter does not reduce the rise time of the CS pin signal such that it erroneously engages the OCP function (for example, if FOSC = 300 kHz, then RLPF = 100 Ω, CLPF = 1000 pF are appropriate values). Current detection is executed according to the following relation:

**IOCP** = **VOLIMIT** (0.4V) / **RCS** [A]

As OCP engages on a pulse-by-pulse basis, SWOUT is pulled low for only 1 cycle of FOSC when engaged. Special consideration should be given to the design of the trace from RCS to system ground as this path conducts a significantly large amount of current. Independent wiring to the system GND is recommended.



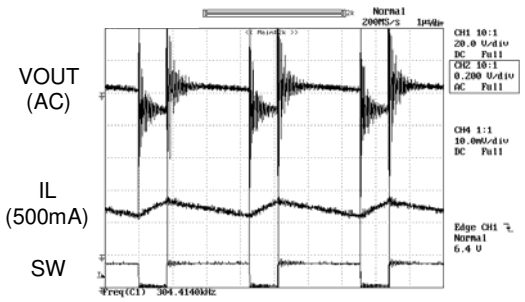




Fig.16 Ripple current & voltage

**▪ Soft start (SS)**

The SS-pin of this IC is for having the soft start function and disabling the LED-open detection. The soft start function operates with the rising edge of the EN but not with the PWM, therefore keep the SS pin open. Also, note the LED-open detection is disabled until the voltage of the SS-pin reaches to the VSS clamp voltage of 2.5V (typ.).

**● Selection of External Parts**

1. Coil Inductor (L)

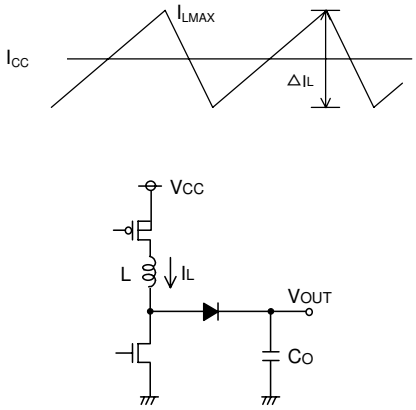



Fig.17 Output ripple current

The inductor's value directly influences the output ripple current. As formula (1) indicates below, the higher the inductance or switching frequency, the lower the ripple current $\Delta I_L$:

$$\Delta I_L = \frac{(V_{OUT}-V_{CC}) \times V_{CC}}{L \times V_{OUT} \times f} \quad [A] \cdot \cdot \cdot (1)$$

If efficiency is represented as in (2), the input peak current is as shown in (3).

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{CC} \times I_{CC}} \quad \cdot \cdot \cdot (2)$$

$$I_{LMAX} = I_{CC} + \frac{\Delta I_L}{2} = \frac{V_{OUT} \times I_{OUT}}{V_{CC} \times \eta} + \frac{\Delta I_L}{2} \quad [A] \cdot \cdot \cdot (3)$$

※ Passing a current through the inductor in excess of its rated current value will cause magnetic saturation in the coil, thereby decreasing overall system efficiency. In selecting an inductor, allow enough margin to ensure that peak current does not exceed the inductor's rated current value.

※ To minimize power loss and improve efficiency, select a coil with low resistive components (DCR and ACR).

2. Output Capacitor (Co)

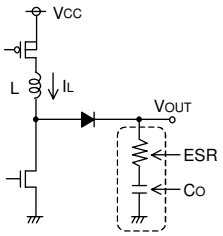



Fig.18 Output capacitor

The output capacitor should be selected after careful consideration of output voltage stability range and desired level of output voltage ripple.

The output ripple voltage $\triangle V_{OUT}$ is computed as shown in formula (4).

$$\triangle V_{OUT} = I_{LMAX} \times R_{ESR} + \frac{1}{C_O} \times \frac{I_{OUT}}{\eta} \times \frac{1}{f} \quad [V] \cdot \cdot \cdot (4)$$

(ESR = equivalent series resistance of Co, $\eta$ = efficiency)

※ When selecting the capacitor's voltage rating, maintain a suitable margin for both output voltage and ripple voltage.

3. Input Capacitor (Cin)

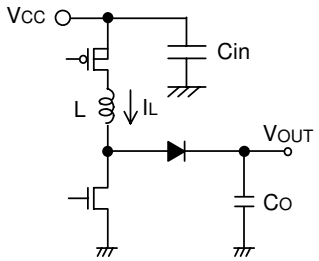



Fig.19 Input capacitor

In order to prevent excess voltage output, select a low-ESR input capacitor that can adequately respond to large ripples in output current.
The ripple current $I_{RMS}$ is derived from formula (5).

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{(V_{OUT} - V_{CC}) \times V_{OUT}}}{V_{OUT}} \quad [A] \cdot \cdot \cdot (5)$$

This figure is also highly dependent upon the characteristics of the power supply input, the wiring pattern of the substrate, and the MOSFET gate-drain capacitance. It is highly recommended that operating temperature range, load range and MOSFET conditions are adequately considered throughout the design process.

4. MOSFET Load Switch and Soft-Start

In normal boost applications, no switch exists between VCC and VO; therefore, a short circuit on the output could burn out the rectifying diode. To avoid this, a PMOSFET can be inserted as a load switch between VCC and the coil. A PMOSFET that can handle a voltage higher than VCC between both the gate-source and drain-source junctions should be selected.
If a soft-start is desired, insert a capacitor between the gate and source. Refer to figure 21 to determine the soft-start time. Keep in mind, however, that soft-start time can vary depending on the gate capacitance of the FET.

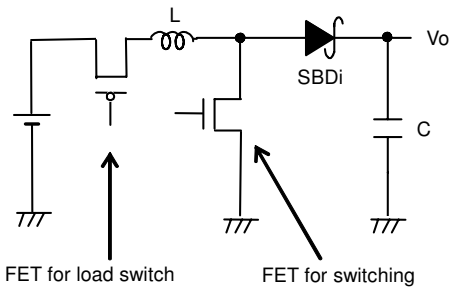



Fig.20 Load Switch Circuit Diagram

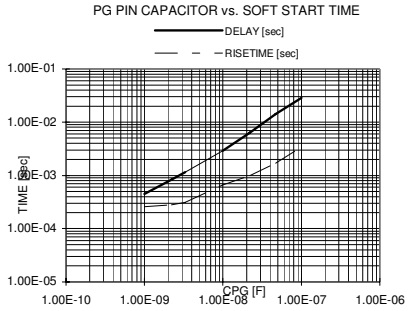



Fig.21 PG Capacitance vs. Soft-Start Time

5. Switching MOSFET

As long as the absolute maximum rating of the FET is greater than or equal to the current rating of the inductor and the voltage rating of the output capacitor and rectifying diode, the circuit will function properly. However, to attain high-speed switching, a FET with small gate capacitance should be selected.

※ The FET's current rating should be higher than the over-current protection limit
※ Lower ON resistance yields higher overall efficiency

6. Rectification Diode

Select a Schottky barrier diode with a current rating greater than the inductor's current rating, and with a reverse-voltage rating greater than the capacitor's voltage rating. A lower forward-voltage (VF) rating is better.

- **Phase Compensation Guidelines**

In general, the negative feedback loop is stable when the following condition is met:

- Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., a phase margin of 40º or more)

However, as the DC/DC converter constantly samples the switching frequency, the gain-bandwidth (GBW) product of the entire series should be set to 1/10 the switching frequency of the system. Therefore, the overall stability characteristics of the application are as follows:

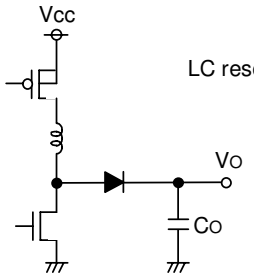
- Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., a phase margin of 40º or more)
- GBW (frequency at gain 0dB) of 1/10 the switching frequency

Thus, to improve response within the GBW product limits, the switching frequency must be increased.

A trick to secure stability with phase compensation is to cancel the second phase-lag (-180º) caused by the LC resonance with a second phase lead (i.e. insert two phase-leads). Phase lead is caused by the ESR component of the output capacitor and the RC filter on the error amp output pin (COMP).

In DC/DC converter applications, a -180º phase lag is always present due to the LC resonance circuit at the output.
If the output capacitor is has a large ESR component (several Ω, such as an aluminum electrolytic capacitor), this ESR component also causes a phase lead of +90º, yielding an overall phase lag of -90º. When an output capacitor with low ESR (such as a ceramic capacitor) is used, a physical resistor for the ESR component should be inserted to compensate the circuit correctly.

LC Resonance

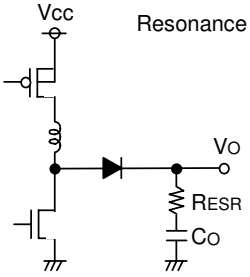



LC resonance phase lag (-180º):

$$fr = \frac{1}{2\pi\sqrt{LCO}} \quad [Hz]$$

Fig.22

With ESR




Resonance point at: $fr = \frac{1}{2\pi\sqrt{LCO}}$ [Hz]

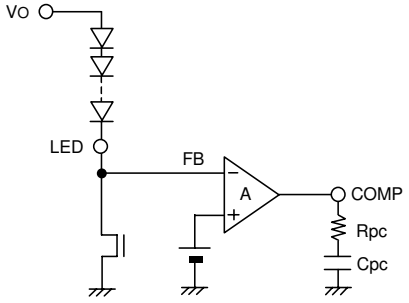
Phase lead at:

$$fESR = \frac{1}{2\pi RESRCO} \quad [Hz]$$

Phase lag -90°

Fig.23

Because of the changes in phase characteristics caused by the capacitor's ESR component, one phase-lead should be inserted.



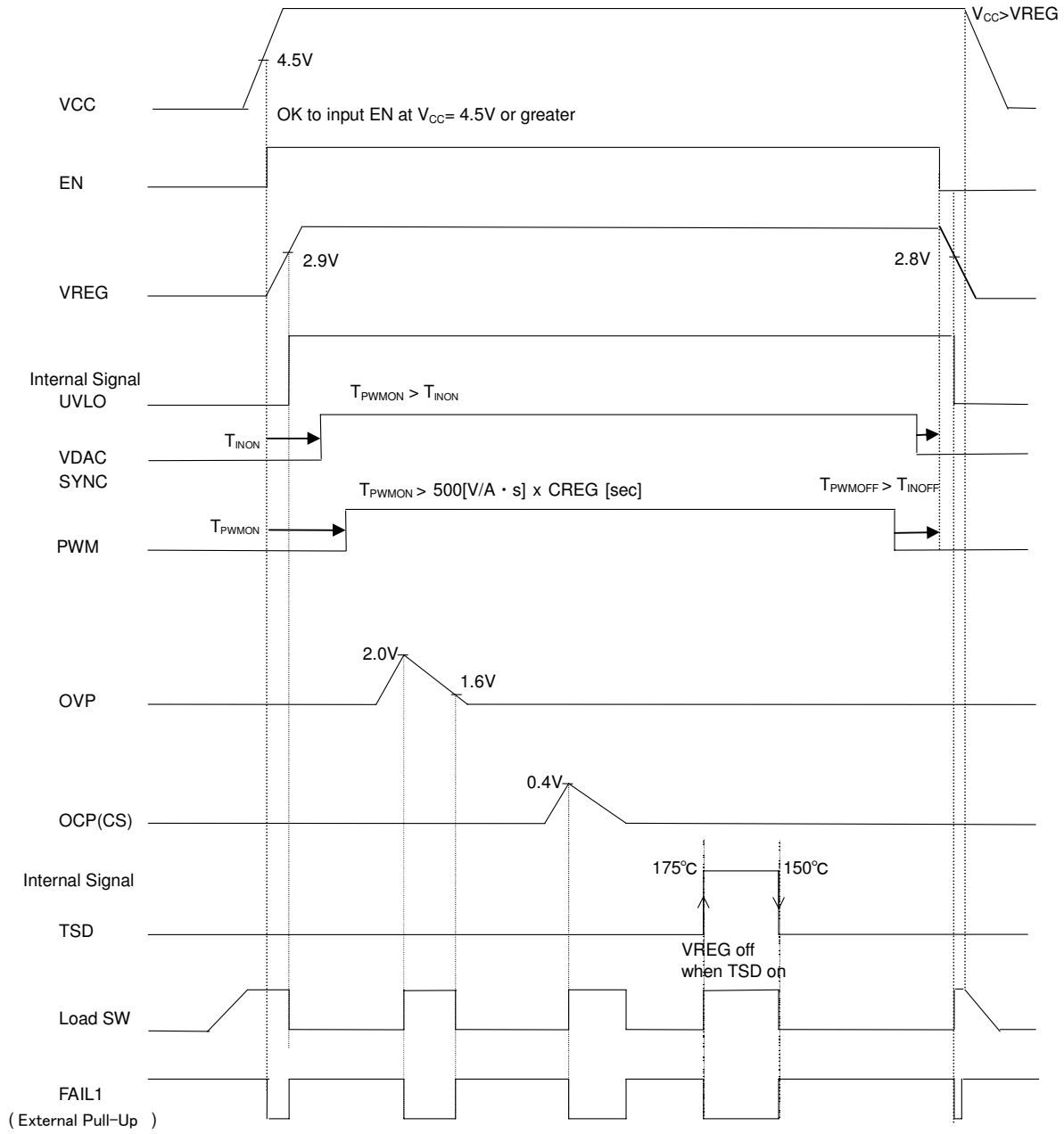

Phase-lead $fz = \frac{1}{2\pi CpcRpc}$ [Hz]

Fig.24

The phase-lead component should ideally be set equal to the resonance frequency of the LC circuit in order to cancel it out.

It is important to keep in mind that these are very loose guidelines, and adjustments may have to be made to ensure stability in the actual circuitry. It is also important to note that stability characteristics can change greatly depending on factors such as substrate layout and load conditions. Therefore, when designing for mass-production, stability should be thoroughly investigated and confirmed in the actual physical design.

● **Timing Chart**




※Fix LEDEN1 and 2 before input.

Fig.25

## • Power Dissipation Calculation

Power dissipation can be calculated as follows:

$$Pd(N) = I_{CC} \cdot V_{CC} + C_{iss} \cdot V_{sw} \cdot f_{sw} \cdot V_{sw} + R_{load} \cdot I_{load}^2 + [\, V_{LED} \cdot N + \Delta V_f \cdot (N - 1)\, ] \cdot I_{LED}$$

| | |
|---|---|
| $I_{CC}$ | Maximum circuit current |
| $V_{CC}$ | Supply power voltage |
| $C_{iss}$ | External FET capacitance |
| $V_{sw}$ | SW gate voltage |
| $F_{sw}$ | SE frequency |
| $R_{load}$ | LOAD SW ON resistance |
| $I_{load}$ | LOAD SW maximum input current |
| $V_{LED}$ | LED control voltage |
| N | LED parallel numeral |
| $\Delta V_f$ | LED $V_f$ fluctuation |
| $I_{LED}$ | LED output current |

Sample Calculation:

Pd(4) = 10mA × 30V + 500pF × 5V × 300kHz × 5V + 15Ω × (10mA)$^2$ + [0.8V × 4 + △Vf × 3] × 100mA

If △Vf = 3.0V, Pd(4) = 324mW + 1220mW = 1544mW.

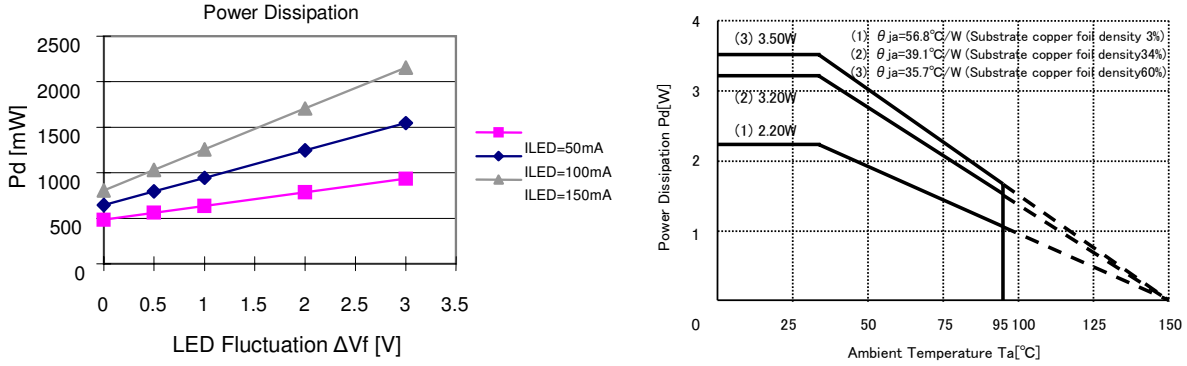



Fig.26

Pd=2200mW (968mW): Substrate copper foil density 3%

Pd=3200mW (1408mW): Substrate copper foil density34%

Pd=3500mW (1540mW): Substrate copper foil density 60% (Value within parentheses represents power dissipation when Ta=95℃)

Note 1: Power dissipation calculated when mounted on 70mm X 70mm X 1.6mm glass epoxy substrate (1-layer platform/copper thickness 18μm)

Note 2: Power dissipation changes with the copper foil density of the board. This value represents only observed values, not guaranteed values.

## • Efficiency of Switching Power Supply

Efficiency $\eta$ is characterized by the following formula:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{Vin \times Iin} \times 100[\%] = \frac{P_{OUT}}{Pin} \times 100[\%] = \frac{P_{OUT}}{P_D(IC) + P_D\alpha} \times 100[\%]$$

The main causes of power dissipation in the switching regulator $P_D\alpha$ are listed below. Efficiency can be improved by optimizing these factors.

1) Dissipation from ON resistance of coil and FET: PD-($I^2R$) *1
2) Gate charge-discharge dissipation: PD-(Gate) *2
3) Switch dissipation: PD(SW) *3
4) Capacitor ESR dissipation: PD-(ESR) *4
5) IC operation current dissipation: PD-(IC) *5

*1: $P_D(I^2R) = I_{OUT}^2 \times (R_{COIL} \times R_{ON})$ ($R_{COIL}$[Ω]: coil resistance, $R_{ON}$[Ω]: ON resistance of FET, $I_{OUT}$[A]: Output current)

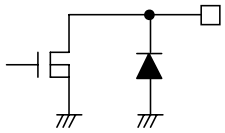
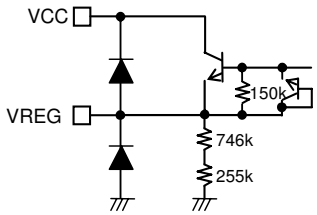
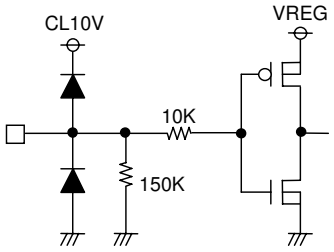
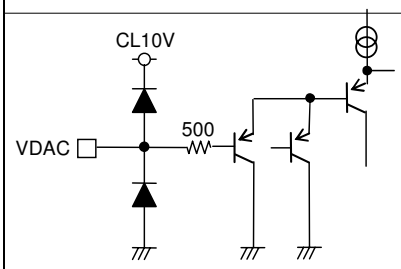
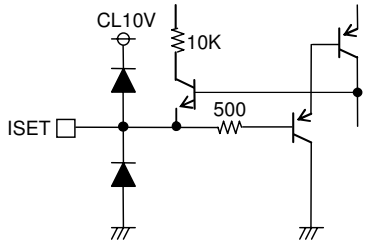
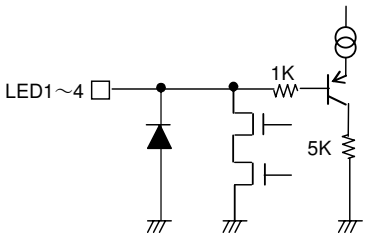
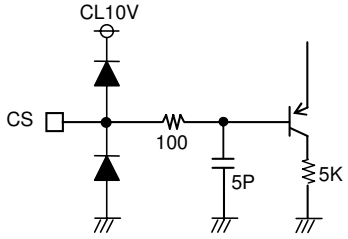
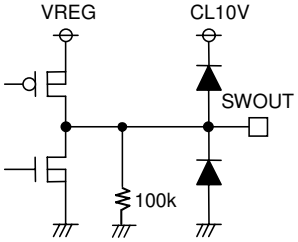
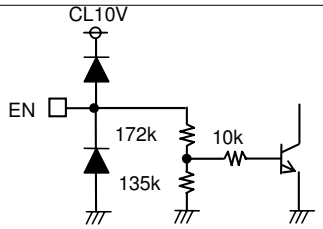
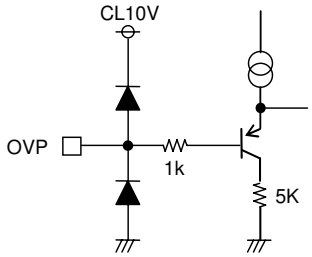
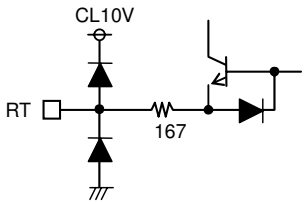
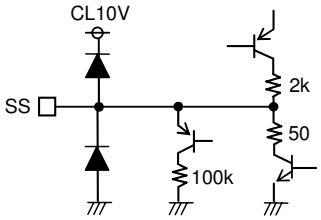
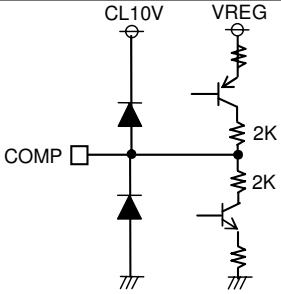
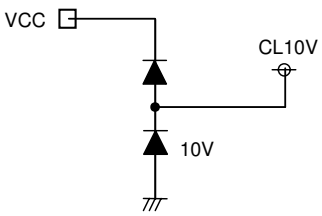
*2: $P_D(Gate) = C_{SW} \times f_{SW} \times V_{SW}$ ($C_{SW}$[F]: Gate capacity of FET, $f_{SW}$[Hz]: Switching frequency, $V_{SW}$[V]: Gate drive voltage of FET)

*3: $P_D(SW) = \frac{Vin^2 \times C_{RSS} \times I_{OUT} \times f_{SW}}{I_{Drive}}$ ($C_{RSS}$[F]: Reciprocal transmission capacitance of FET, $I_{Drive}$[A]: Peak current of gate

*4: $P_D(ESR) = I_{RMS}^2 \times ESR$ ($I_{RMS}$[A]: Ripple current of condenser, ESR[Ω]: Equivalent Series Resistance)

*5: $P_D(IC) = Vin \times I_{CC}$ ($I_{CC}$[A] : Circuit Current)

● **Input/output Equivalent Circuits** (terminal name follows pin number)

| 2. LOADSW, 3. FAIL1, 20. FAIL2 | 4. VREG | 5. PWM, 6. SYNC,<br>10. LEDEN1, 11. LEDEN2 |
|---|---|---|
|  |  |  |
| 8. VDAC | 9. ISET | 12. LED1, 14. LED2,<br>15. LED3, 17. LED4 |
|  |  |  |
| 22. CS | 23. SWOUT | 24. EN |
|  |  |  |
| 25. OVP | 26. RT | 27. SS |
|  |  |  |
| 28. COMP | 13, 16, 18, 19 N.C. | CL10V |
|  |  <br>N.C. = no connection (open) |  |

※All values typical.

● **Sample Application Circuit**

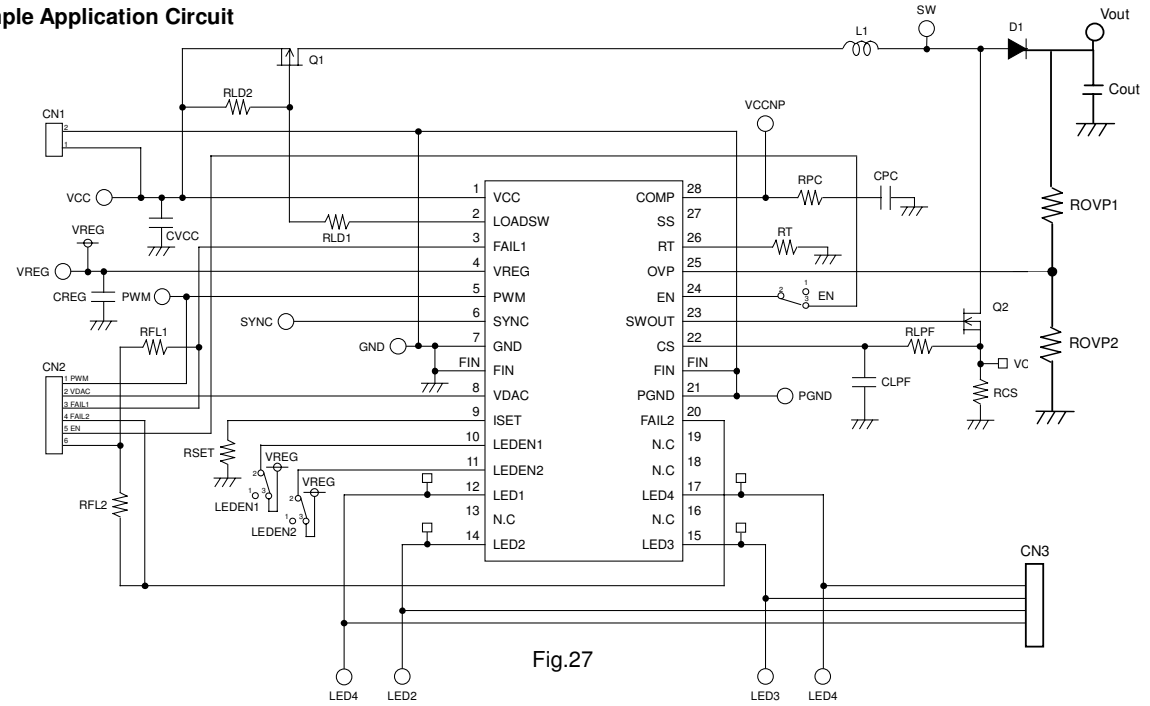



Fig.27

- The coupling capacitors CVCC and CREG should be mounted as close as possible to the IC's pins.
- Large currents may pass through CSGND and PGND, so each should have its own low-impedance routing to the system ground.
- Noise should be minimized as much as possible on pins 8 (VDAC), 9 (ISET), 26 (RT) and 28 (COMP).
- Pins 5 (PWM), 6 (SYNC) and 12-17 (LED1-4) carry switching signals, so ensure during layout that surrounding traces are not affected by crosstalk.
- Connections depicted above with thicker lines should be laid out with traces that are as short and wide as possible.

● **Application Board Part List**

| Label | Value | Product Part No. | Manufacturer |
|---|---|---|---|
| RLD1 | 5.1kΩ | MCR03Series5101 | ROHM |
| RLD2 | 5.1kΩ | MCR03Series5101 | ROHM |
| RFL1 | 5.1kΩ | MCR03Series5101 | ROHM |
| RFL2 | 5.1kΩ | MCR03Series5101 | ROHM |
| RPC | 330Ω | MCR03Series3300 | ROHM |
| RT | 100kΩ | MCR03Series1003 | ROHM |
| ROVP1 | 330kΩ | MCR03Series3303 | ROHM |
| ROVP2 | 22kΩ | MCR03Series2202 | ROHM |
| RCS | 0.1Ω | MCR10SeriesR10 | ROHM |
| RSET | 100kΩ | MCR03Series1003 | ROHM |
| CPC | 1uF | GRM188B10J105KA01B | Murata |
| CSS | - | - | - |
| CVCC | 10uF | GRM21BB31C106KE15 | Murata |
| CREG | 10uF | GRM21BB31C106KE15 | Murata |
| Q1 | - | RSS090P03FU6TB | ROHM |
| Q2 | - | SP8K22FU6TB | ROHM |
| L1 | 47uH | CDRH8D38NP-470NC | Sumida |
| D1 | - | RB160L-60TE25 | ROHM |
| CVOUT | 220uF | 25YK220M0611 | Rubycon |
| RLPF | 100Ω | MCR03Series1000 | ROHM |
| CLPF | 1000pF | GRM1882C1H102JA01 | Murata |
| CLD2 | 1uF | GRM21BB31C105KE12 | Murata |

- The above values are fixed numbers for confirmed operation with the following conditions: VCC = 12V, four parallel channels of five series-connected LEDs, and ILED=50mA.
- Optimal values of external components depend on the actual application; these values should only be used as guidelines and should be adjusted to fit the operating conditions of the actual application.

● **Operating Notes**

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

2) GND potential

Ensure that the GND pin is held at the minimum potential in all operating conditions.

3) Thermal Design

Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by poor soldering or foreign objects may result in damage to the IC.

5) Operation in strong electromagnetic fields

Exercise caution when using the IC in the presence of strong electromagnetic fields as doing so may cause the IC to malfunction.

6) Testing on application boards

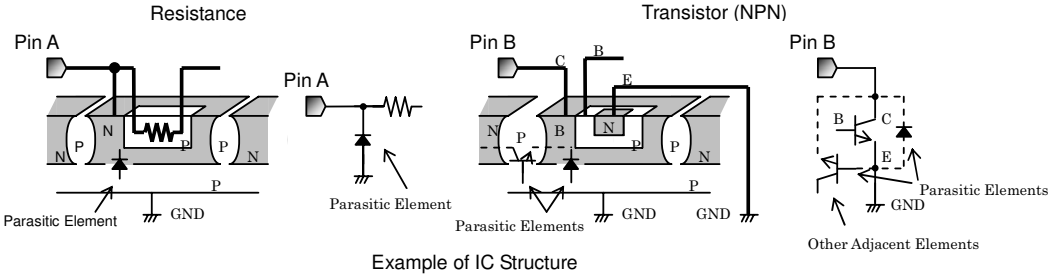
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

7) Ground wiring patterns

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.

8) IC input pins and parasitic elements

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):




Example of IC Structure

- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

9) Over-current protection circuits

An over-current protection circuit (designed according to the output current) is integrated into the IC to prevent damage in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected overloads on the output. However, the IC should not be used in applications where operation of the OCP function is anticipated or assumed

10) Thermal shutdown circuit (TSD)

This IC also incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the rise in the chip's junction temperature $T_j$ will trigger the TSD circuit, shutting off all output power elements. The circuit automatically resets itself once the junction temperature $T_j$ drops down to normal operating temperatures. The TSD protection will only engage when the IC's absolute maximum ratings have been exceeded; therefore, application designs should never attempt to purposely make use of the TSD function.

● **Part Number Selection**



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