Single-chip Type with Built-in FET Switching Regulators

Low Noise High Efficiency Step-down Switching Regulator with Built-in Power MOSFET

BD8960NV

No.10027EBT21

●Description

ROHM's high efficiency step-down switching regulator BD8960NV is a power supply designed to produce a low voltage including 1 volts from 5.5/3.3 volts power supply line. Offers high efficiency with synchronous rectifier. Employs a current mode control system to provide faster transient response to sudden change in load.

●Features

1) Offers fast transient response with current mode PWM control system.
2) Offers highly efficiency for all load range with synchronous rectifier (Nch/Pch FET)
3) Incorporates soft-start function.
4) Incorporates thermal protection and ULVO functions.
5) Incorporates short-current protection circuit with time delay function.
6) Incorporates shutdown function
7) Employs small surface mount package : SON008V5060

●Applications

Power supply for LSI including DSP, Micro computer and ASIC

●Line up

Parameter	Symbol	Limits	Unit
VCC Voltage	V_{CC}	-0.3～+7 [*1]	V
PVCC Voltage	PV_{CC}	-0.3～+7 [*1]	V
EN Voltage	V_{EN}	-0.3～+7	V
SW,ITH Voltage	V_{SW}, V_{ITH}	-0.3～+7	V
Power Dissipation 1	Pd1	900 [*2]	mW
Power Dissipation 2	Pd2	3900 [*3]	mW
Operating temperature range	Topr	-25 ~ +105	℃
Storage temperature range	Tstg	-5 ~ +150	℃
Maximum junction temperature	Tjmax	+150	℃

＊1　Pd should not be exceeded.
＊2　Derating in done 7.2mW/℃ for temperatures above Ta=25℃, Mounted on 70mm×70mm×1.6mm Glass Epoxy PCB.
＊3　Derating in done 31.2mW/℃ for temperatures above Ta=25℃, Mounted on JESD51-7.

●Operating Conditions (Ta=25℃)

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
V_{CC} Voltage	V_{CC} [*4]	2.7 [*5]	3.3	5.5	V
PV_{CC} Voltage	P_{VCC} [*4]	2.7 [*5]	3.3	5.5	V
EN Voltage	V_{EN}	0	-	VCC	V
SW average output current	Isw [*4]	-	-	2.0	A
Output voltage Setting Range	V_{OUT}	1.0	-	2.5	V

＊4　Pd should not be exceeded.
＊5　In case set output voltage 1.6V or more, VccMin. = Vout + 1.3V.

2010.04 - Rev.B

●**Electrical Characteristics**
◎(Ta=25℃, Vcc=PVcc=3.3V, EN=Vcc, R1=10k

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Standby current	ISTB	-	0	10	μA	EN=GND
Bias current	ICC	-	250	400	μA	
EN Low voltage	VENL	-	GND	0.8	V	Standby mode
EN High voltage	VENH	2.0	Vcc	-	V	Active mode
EN input current	IEN	-	1	10	μA	VEN=3.3V
Oscillation frequency	FOSC	0.8	1	1.2	MHz	
Pch FET ON resistance	RONP	-	200	400	mΩ	Pvcc=3.3V
Nch FET ON resistance	RONN	-	160	350	mΩ	Pvcc=3.3V
ADJ Voltage	VADJ	0.788	0.800	0.812	V	
Output voltage	VOUT	-	1.200	-	V	
ITH sink current	ITHSI	10	20	-	μA	VADJ=1.0V
ITH source current	ITHSO	10	20	-	μA	VADJ=0.6V
UVLO threshold voltage	VUVLO1	2.400	2.500	2.600	V	Vcc=3→0V
UVLO release voltage	VUVLO2	2.425	2.550	2.700	V	Vcc=0→3V
Soft start time	TSS	0.5	1	2	ms	
Timer latch time	TLATCH	1	2	3	ms	SCP/TSD operated
Output Short circuit Threshold Voltage	VSCP	-	$V_{OUT} \times 0.5$	$V_{OUT} \times 0.7$	VOUT	VOUT=1.2→0V

Ω, R2=5kΩ, unless otherwise specified.)

●**Block Diagram, Application Circuit**
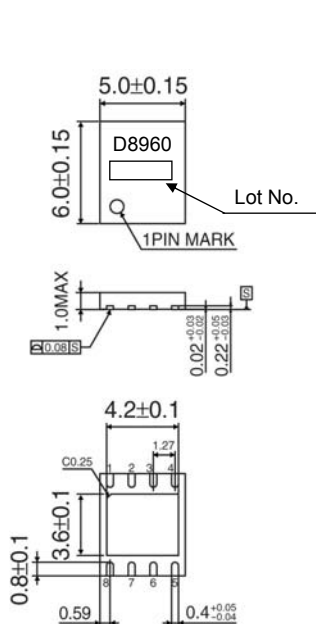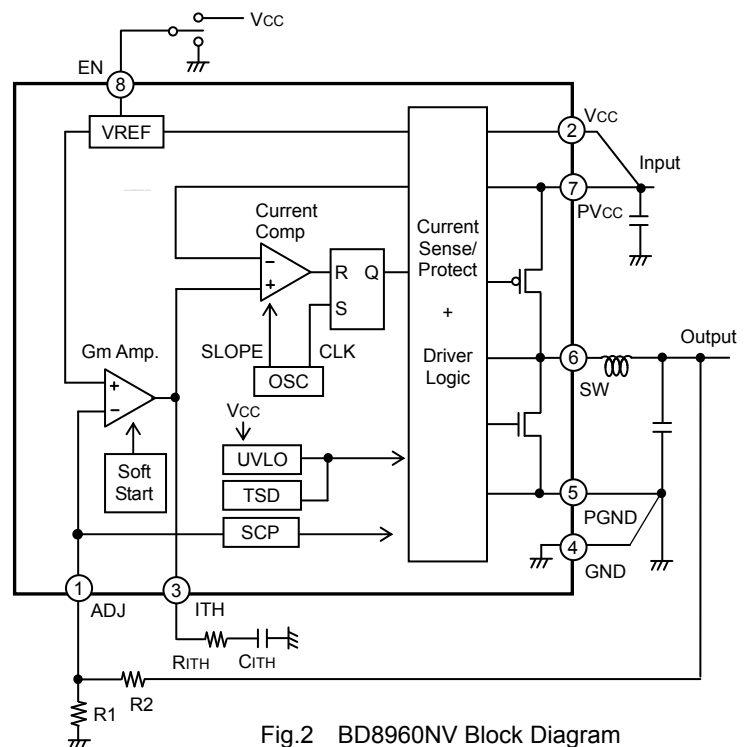

Fig.1   BD8960NV TOP View

Fig.2   BD8960NV Block Diagram

●**Pin No. & function table**

Pin No.	Pin name	PIN function
1	ADJ	Output voltage detect pin
2	Vcc	Vcc power supply input pin
3	ITH	GmAmp output pin/Connected phase compensation capacitor
4	GND	Ground
5	PGND	Nch FET source pin
6	SW	Pch/Nch FET drain output pin
7	PVcc	Pch FET source pin
8	EN	Enable pin(Active High)

●**Characteristics data (Reference data)**
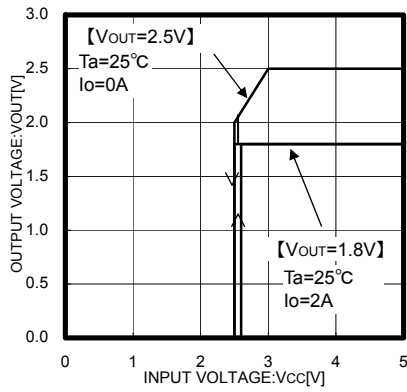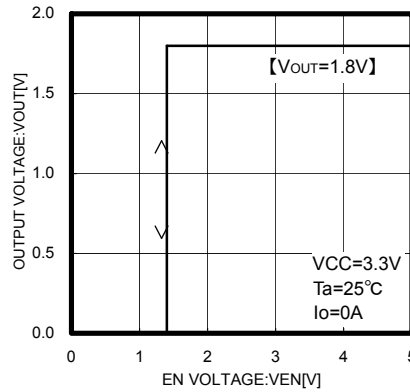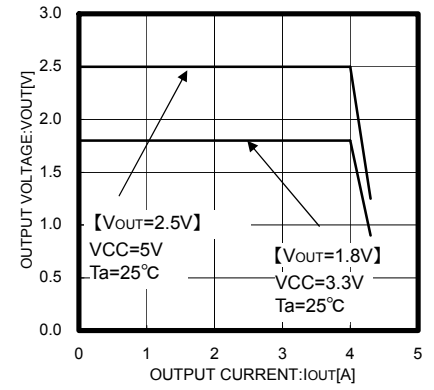

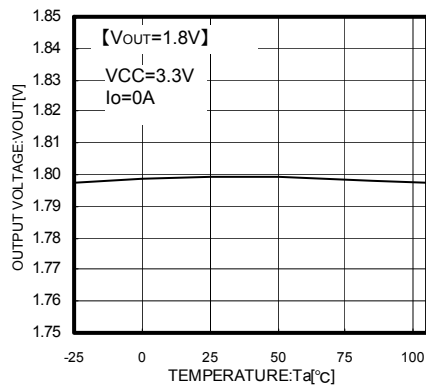
Fig.3 Vcc-Vout

Fig.4 Ven-Vout

Fig.5 Iout-Vout

Fig. 6 Ta-V$_{OUT}$
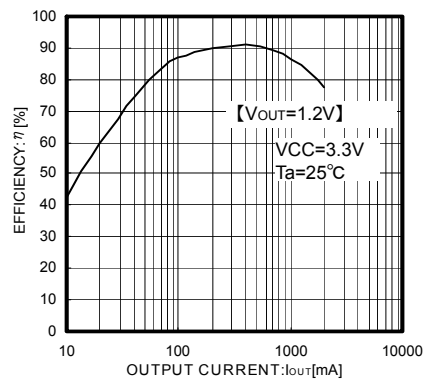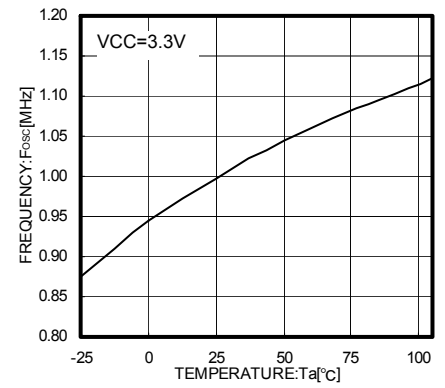

Fig.7 Efficiency

Fig.8 Ta-F$_{OSC}$
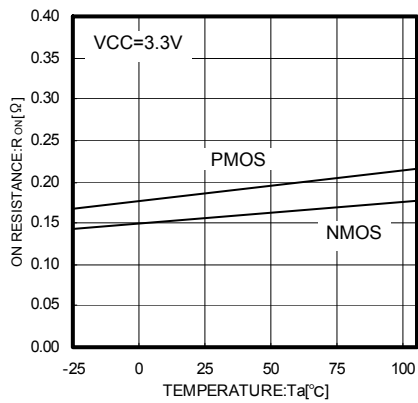
Fig.9 Ta-R$_{ONN}$, R$_{ONP}$
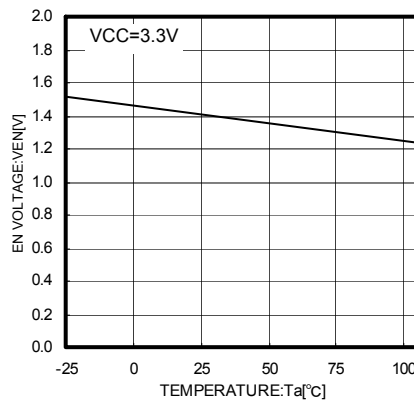
Fig.10 Ta-V$_{EN}$
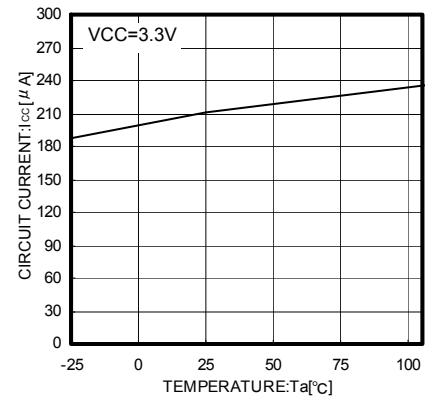
Fig.11 Ta-I$_{CC}$

●**Characteristics data (Reference data) – Continued**

Fig.12 Vcc-Fosc

Fig.13 Soft start waveform

Fig.14 SW waveform Io=10mA

Fig. 15 Transient response
Io=1A→2A(10μs)

Fig.16 Transient response
Io=2A→1A(10μs)
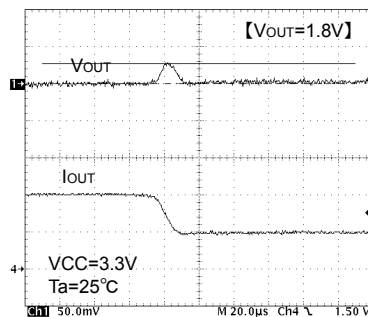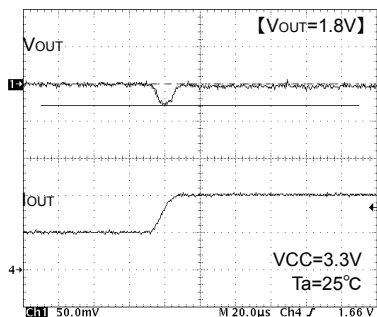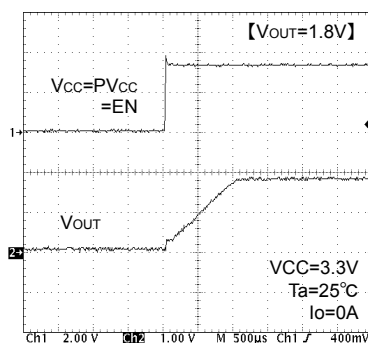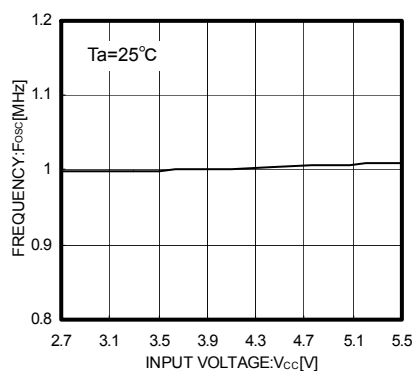
●**Information on advantages**

Advantage 1 : Offers fast transient response with current mode control system.
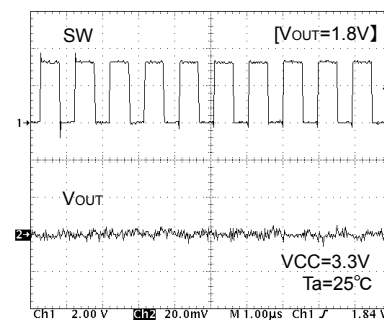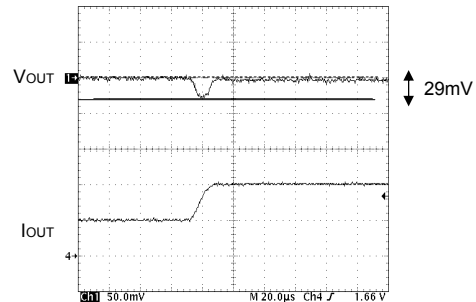
Conventional product (Load response Io=0.1A→0.6A)   <u>BD8960NV</u> (Load response Io=1A→2A)
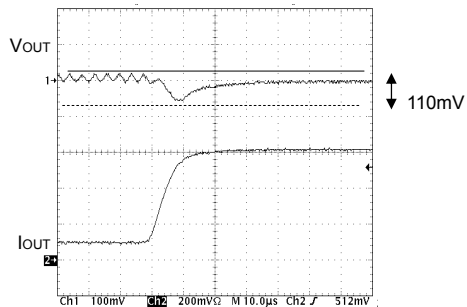
Voltage drop due to sudden change in load was reduced by about 50%.

Fig.17 Comparison of transient response

Advantage 2 : Offers high efficiency with synchronous rectifier

Utilizes the synchronous rectifying mode and the low on-resistance MOS FETs incorporated as power transistor.

⎧ ON resistance of P-channel MOS FET : 200mΩ(Typ.)
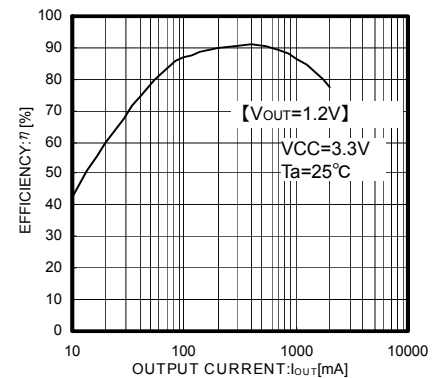⎩ ON resistance of N-channel MOS FET : 160mΩ(Typ.)

Fig.18 Efficiency

Advantage 3 : ・Supplied in smaller package due to small-sized power MOS FET incorporated.

・Output capacitor Co required for current mode control: 22μF ceramic capacitor
・Inductance L required for the operating frequency of 1 MHz: 2.2μH inductor
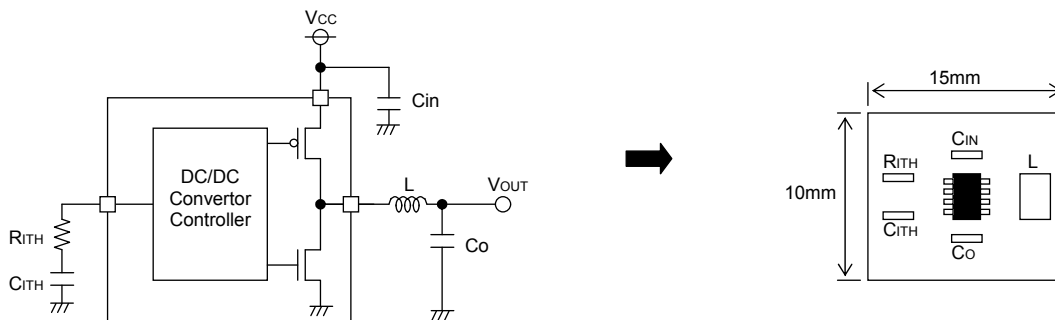
Reduces a mounting area required.

Fig.19 Example application

●**Operation**
BD8960NV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system.

○Synchronous rectifier
It does not require the power to be dissipated by a rectifier externally connected to a conventional DC/DC converter IC, and its P.N junction shoot-through protection circuit limits the shoot-through current during operation, by which the power dissipation of the set is reduced.

○Current mode PWM control
Synthesizes a PWM control signal with a inductor current feedback loop added to the voltage feedback.
・PWM (Pulse Width Modulation) control
The oscillation frequency for PWM is 1 MHz. SET signal form OSC turns ON a P-channel MOS FET (while a N-channel MOS FET is turned OFF), and an inductor current I_L increases. The current comparator (Current Comp) receives two signals, a current feedback control signal (SENSE: Voltage converted from I_L) and a voltage feedback control signal (FB), and issues a RESET signal if both input signals are identical to each other, and turns OFF the P-channel MOS FET (while a N-channel MOS FET is turned ON) for the rest of the fixed period. The PWM control repeat this operation.
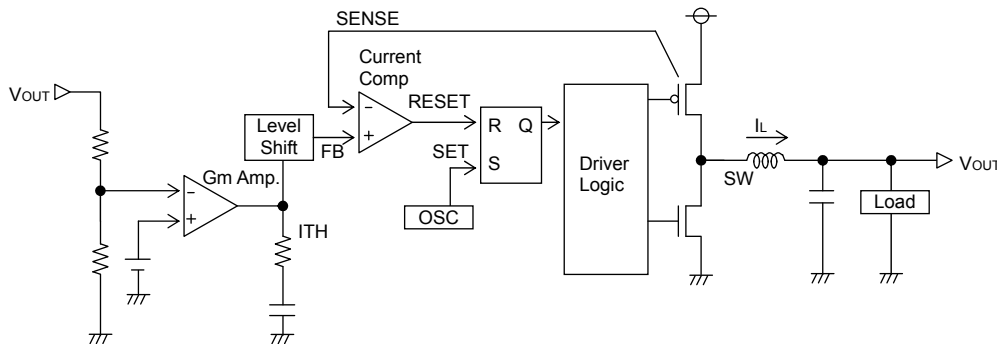

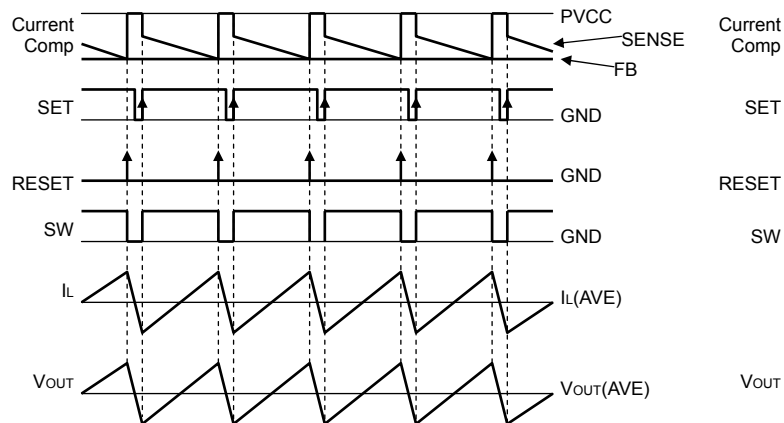Fig.20 Diagram of current mode PWM control

Fig.21 PWM switching timing chart

●**Description of operations**

・Soft-start function
EN terminal shifted to "High" activates a soft-starter to gradually establish the output voltage with the current limited during startup, by which it is possible to prevent an overshoot of output voltage and an inrush current.

・Shutdown function
With EN terminal shifted to "Low", the device turns to Standby Mode, and all the function blocks including reference voltage circuit, internal oscillator and drivers are turned to OFF.　Circuit current during standby is 0μF (Typ.).

・UVLO function
Detects whether the input voltage sufficient to secure the output voltage of this IC is supplied.　And the hysteresis width of 50mV (Typ.) is provided to prevent output chattering.

Fig.22 Soft start, Shutdown, UVLO timing chart
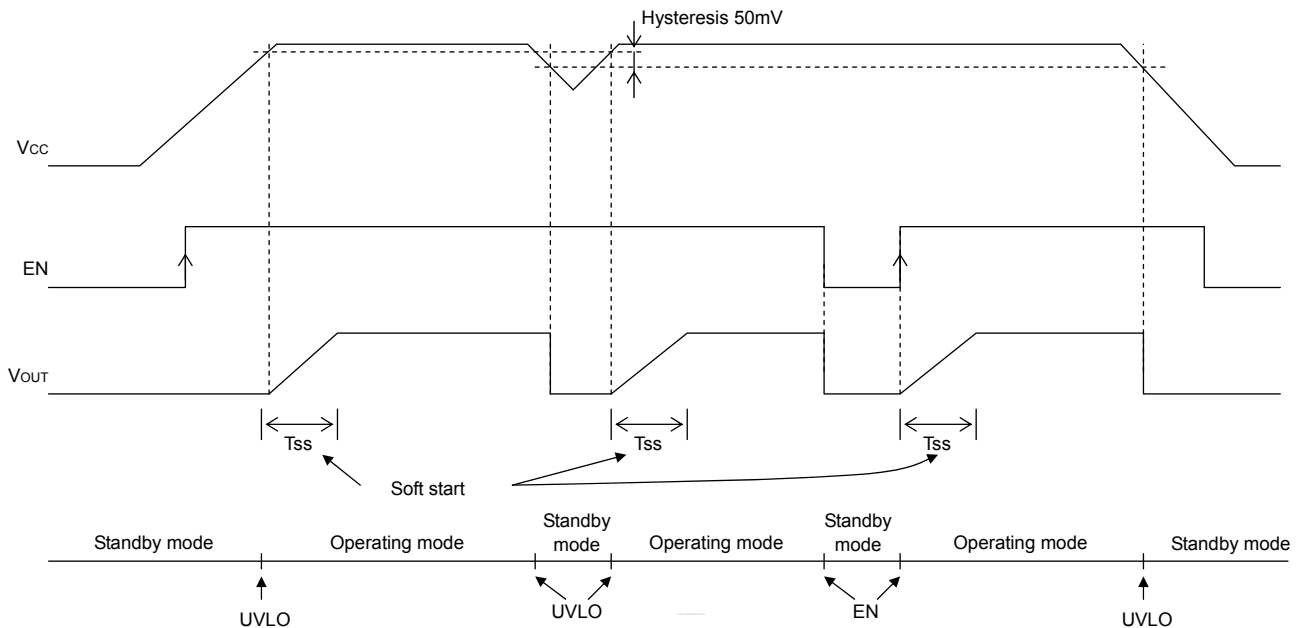
・Short-current protection circuit with time delay function
Turns OFF the output to protect the IC from breakdown when the incorporated current limiter is activated continuously for the fixed time(T_{LATCH}) or more.　The output thus held tuned OFF may be recovered by restarting EN or by re-unlocking UVLO.
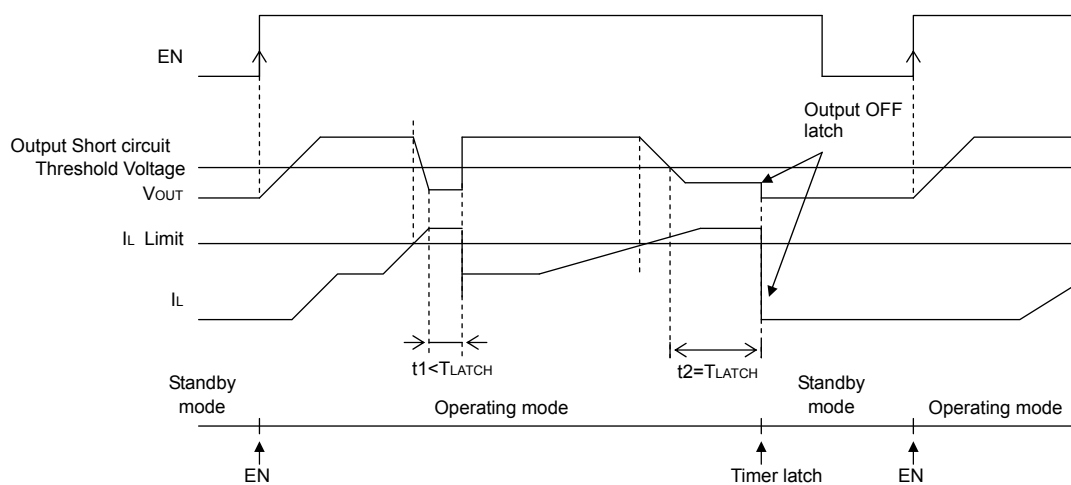
Fig.23 Short-current protection circuit with time delay timing chart

●**Switching regulator efficiency**

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{in} \times I_{in}} \times 100[\%] = \frac{P_{OUT}}{P_{in}} \times 100[\%] = \frac{P_{OUT}}{P_{OUT} + P_{D\alpha}} \times 100[\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors $P_{D\alpha}$ as follows:

Dissipation factors:
1) ON resistance dissipation of inductor and FET：PD(I^2R)
2) Gate charge/discharge dissipation：PD(Gate)
3) Switching dissipation：PD(SW)
4) ESR dissipation of capacitor：PD(ESR)
5) Operating current dissipation of IC：PD(IC)

1)PD(I^2R)=$I_{OUT}^2 \times$(R$_{COIL}$+R$_{ON}$)　(R$_{COIL}$[Ω]：DC resistance of inductor, R$_{ON}$[Ω]：ON resistance of FET, I$_{OUT}$[A]：Output current.)
2)PD(Gate)=Cgs×f×V　(Cgs[F]：Gate capacitance of FET, f[H]：Switching frequency, V[V]：Gate driving voltage of FET)

3)PD(SW)= $\dfrac{V_{in}^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$ 　(C$_{RSS}$[F]：Reverse transfer capacitance of FET, I$_{DRIVE}$[A]：Peak current of gate.)

4)PD(ESR)=I$_{RMS}^2 \times$ESR　(I$_{RMS}$[A]：Ripple current of capacitor, ESR[Ω]：Equivalent series resistance.)
5)PD(IC)=V$_{in} \times$I$_{CC}$　(I$_{CC}$[A]：Circuit current.)

●**Consideration on permissible dissipation and heat generation**

As this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation.　In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON resistance of FET are considered. Because the conduction losses are considered to play the leading role among other dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.

①for SON008V5060
　JEDEC 4 layer board 76.2×114.3×1.6mm
　θj-a=32.1℃/W
②for SON008V5060
　ROHM standard 1 layer board 70×70×1.6mm
　θj-a=138.9℃/W
③ IC only
　θj-a=195.3℃/W
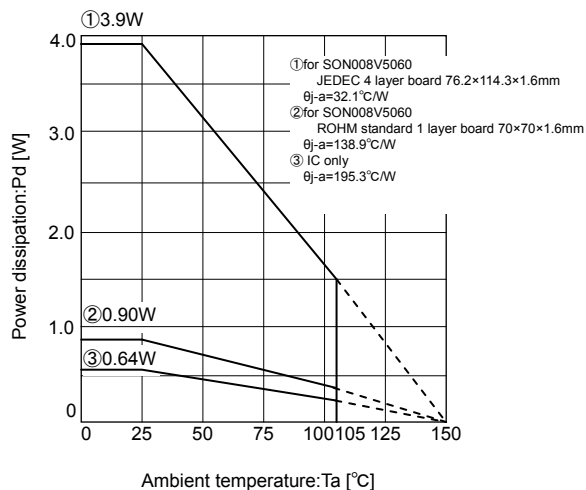
Fig.24 Thermal derating curve (SON008V5060)

$P = I_{OUT}^2 \times R_{ON}$
$R_{ON} = D \times R_{ONP} + (1-D) R_{ONN}$

D：ON duty (=V$_{OUT}$/V$_{CC}$)
R$_{COIL}$：DC resistance of coil
R$_{ONP}$：ON resistance of P-channel MOS FET
R$_{ONN}$：ON resistance of N-channel MOS FET
I$_{OUT}$：Output current

If V$_{CC}$=3.3V, V$_{OUT}$=1.8V, R$_{ONP}$=0.2Ω, R$_{ONN}$=0.16Ω
　I$_{OUT}$=2A, for example,
　　D=V$_{OUT}$/V$_{CC}$=1.8/3.3=0.545
　　R$_{ON}$=0.545×0.20+(1-0.545)×0.16
　　　=0.109+0.0728
　　　=0.1818[Ω]

　　P=$2^2 \times$0.1818＝0.7272W]

As R$_{ONP}$ is greater than R$_{ONN}$ in this IC, the dissipation increases as the ON duty becomes greater.　With the consideration on the dissipation as above, thermal design must be carried out with sufficient margin allowed.

●**Selection of components externally connected**

1. Selection of inductor (L)

Fig.25 Output ripple current

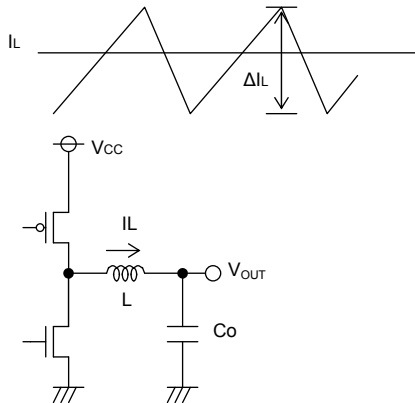The inductance significantly depends on output ripple current. As seen in the equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{L\times V_{CC}\times f} \ [A]\cdot\cdot\cdot(1)$$

Appropriate ripple current at output should be 20% more or less of the maximum output current.

$$\Delta I_L = 0.2\times I_{OUT}max. \ [A]\cdot\cdot\cdot(2)$$

$$L = \frac{(V_{CC}-V_{OUT})\times V_{OUT}}{\Delta I_L\times V_{CC}\times f} \ [H]\cdot\cdot\cdot(3)$$

(ΔI_L: Output ripple current, and f: Switching frequency)

* Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=3.3V, V_{OUT}=1.8V, f=1MHz, ΔI_L=0.2×2A=0.4A, for example,(BD8960NV)

$$L = \frac{(3.3-1.8)\times 1.8}{0.4\times 3.3\times 1M} = 2.05\mu \rightarrow 2.2[\mu H]$$

*Select the inductor of low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

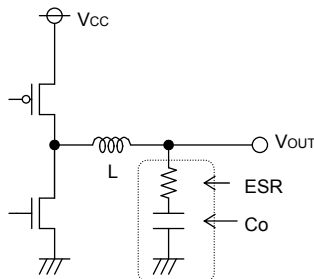2. Selection of output capacitor (C_O)

Fig.26 Output capacitor

Output capacitor should be selected with the consideration on the stability region and the equivalent series resistance required to smooth ripple voltage.

Output ripple voltage is determined by the equation (4) :

$$\Delta V_{OUT} = \Delta I_L \times ESR \ [V]\cdot\cdot\cdot(4)$$

(ΔI_L: Output ripple current, ESR: Equivalent series resistance of output capacitor)

*Rating of the capacitor should be determined allowing sufficient margin against output voltage. A 22μF to 100μF ceramic capacitor is recommended.
Less ESR allows reduction in output ripple voltage.

3. Selection of input capacitor (Cin)
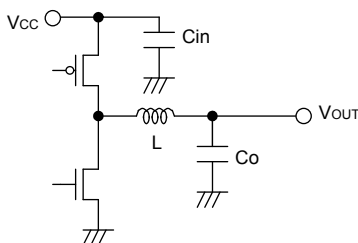
Fig.27 Input capacitor

Input capacitor to select must be a low ESR capacitor of the capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (5):

$$I_{RMS} = I_{OUT}\times \frac{\sqrt{V_{OUT}(V_{CC}-V_{OUT})}}{V_{CC}} \ [A]\cdot\cdot\cdot(5)$$

< Worst case > $I_{RMS(max.)}$

When Vcc is twice the V_{OUT}, $I_{RMS} = \dfrac{I_{OUT}}{2}$

If V_{CC}=3.3V, V_{OUT}=1.8V, and $I_{OUT}max.$=2A, (BD8960NV)

$$I_{RMS} = 2\times \frac{\sqrt{1.8(3.3-1.8)}}{3.3} = 0.99[A_{RMS}]$$

A low ESR 22μF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

4. Determination of RITH, CITH that works as a phase compensator

As the Current Mode Control is designed to limit a inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consisting of a output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR.   So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.
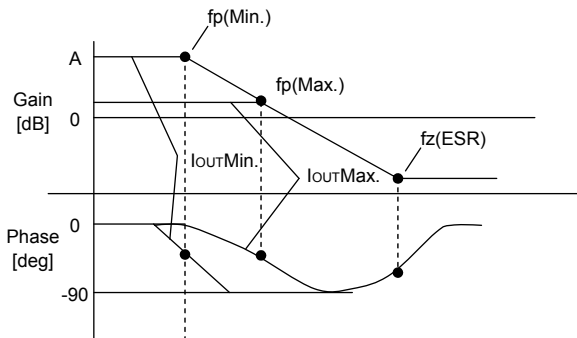

Fig.28 Open loop gain characteristics

$$fp = \frac{1}{2\pi \times R_O \times C_O}$$

$$fz_{(ESR)} = \frac{1}{2\pi \times E_{SR} \times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency lowers.

$$fp_{(Min.)} = \frac{1}{2\pi \times R_{OMax.} \times C_O} \text{ [Hz]} \leftarrow \text{with lighter load}$$

$$fp_{(Max.)} = \frac{1}{2\pi \times R_{OMin.} \times C_O} \text{ [Hz]} \leftarrow \text{with heavier load}$$
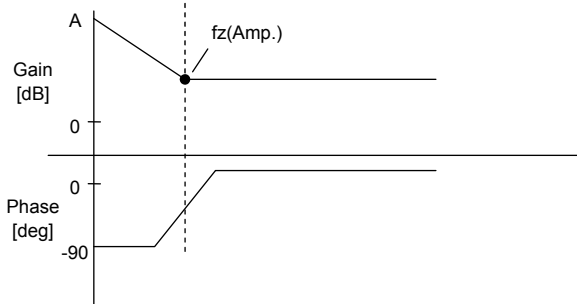
Fig.29 Error amp phase compensation characteristics

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change.   (This is because when the capacitance is doubled, the capacitor ESR reduces to half.)

$$fz_{(Amp.)} = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$
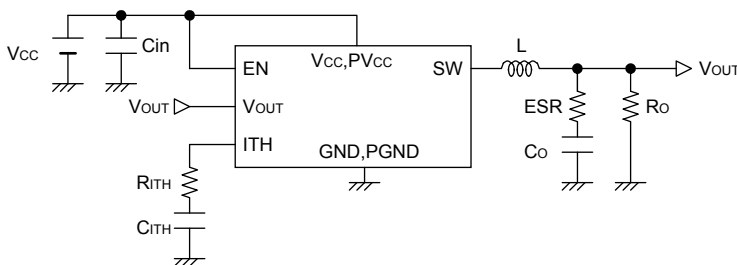
Fig.30 Typical application

Stable feedback loop may be achieved by canceling the pole fp (Min.) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$fz_{(Amp.)} = fp_{(Min.)}$$

$$\longrightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{OMax.} \times C_O}$$

5. Determination of output voltage

The output voltage V_{OUT} is determined by the equation (6):
$V_{OUT}=(R2/R1+1) \times V_{ADJ}$ ・・・(6) V_{ADJ}: Voltage at ADJ terminal (0.8V Typ.)
With R1 and R2 adjusted, the output voltage may be determined as required.

$\left[\text{Adjustable output voltage range : 1.0V} \sim \text{2.5V} \right]$
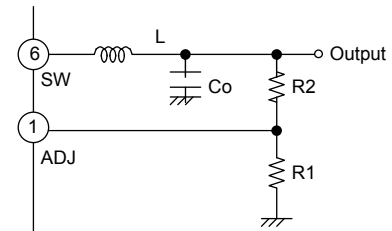
Fig.31 Determination of output voltage

Use 1 kΩ～100 kΩ resistor for R1.   If a resistor of the resistance higher than 100 kΩ is used, check the assembled set carefully for ripple voltage etc.

The lower limit of input voltage depends on the output voltage.
Basically, it is recommended to use in the condition :
     VCCmin = VOUT+1.3V.
Fig.32. shows the necessary output current value at the lower limit of input voltage. (DCR of inductor : 0.1Ω)
This data is the characteristic value, so it' doesn't guarantee the operation range,
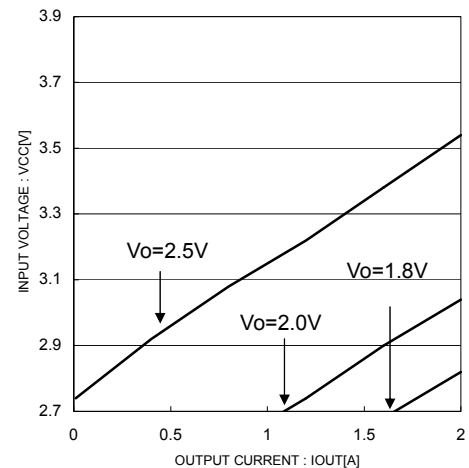
Fig.32 minimum input voltage in each output voltage

● **BD8960NV   Cautions on PC Board layout**
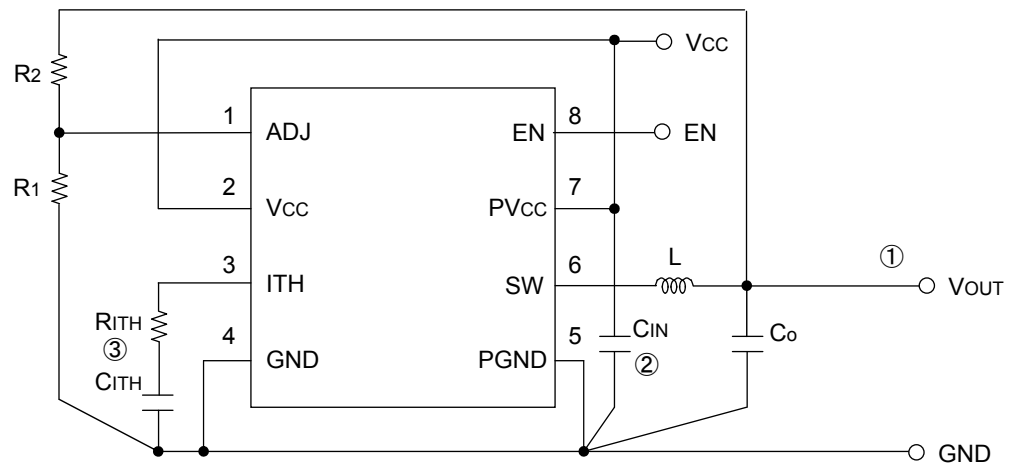
Fig.33 Layout diagram

①For the sections drawn with heavy line, use thick conductor pattern as short as possible.
②Lay out the input ceramic capacitor CIN closer to the pins PVCC and PGND, and the output capacitor Co closer to the pin PGND.
③Lay out CITH and RITH between the pins ITH and GND as neat as possible with least necessary wiring.
  * SON008V5060 (BD8960NV) has thermal FIN on the reverse of the package.
   The package thermal performance may be enhanced by bonding the FIN to GND plane which take a large area of PCB.

●**Recommended components Lists on above application**

Symbol	Part	Value		Manufacturer	Series
L	Coil	2.2μH		TDK	LTF5022-2R2N3R2
C$_{IN}$	Ceramic capacitor	22μF		Kyocera	CM32X5R226M10A
C$_O$	Ceramic capacitor	22μF		Kyocera	CM316B226M06A
C$_{ITH}$	Ceramic capacitor	V$_{OUT}$=1.0V	680pF	murata	GMR18 Serise
		V$_{OUT}$=1.2V	560pF	murata	GMR18 Serise
		V$_{OUT}$=1.5V	470pF	murata	GMR18 Serise
		V$_{OUT}$=1.8V	330pF	murata	GMR18 Serise
		V$_{OUT}$=2.5V	330pF	murata	GMR18 Serise
R$_{ITH}$	Resistance	V$_{OUT}$=1.0V	10kΩ	Rohm	MCR03 Serise
		V$_{OUT}$=1.2V	12kΩ	Rohm	MCR03 Serise
		V$_{OUT}$=1.5V	15kΩ	Rohm	MCR03 Serise
		V$_{OUT}$=1.8V	18kΩ	Rohm	MCR03 Serise
		V$_{OUT}$=2.5V	18kΩ	Rohm	MCR03 Serise

* The parts list presented above is an example of recommended parts. Although the parts are sound, actual circuit characteristics should be checked on your application carefully before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the VCC and PVCC pins, and a schottky barrier diode established between the SW and PGND pins.
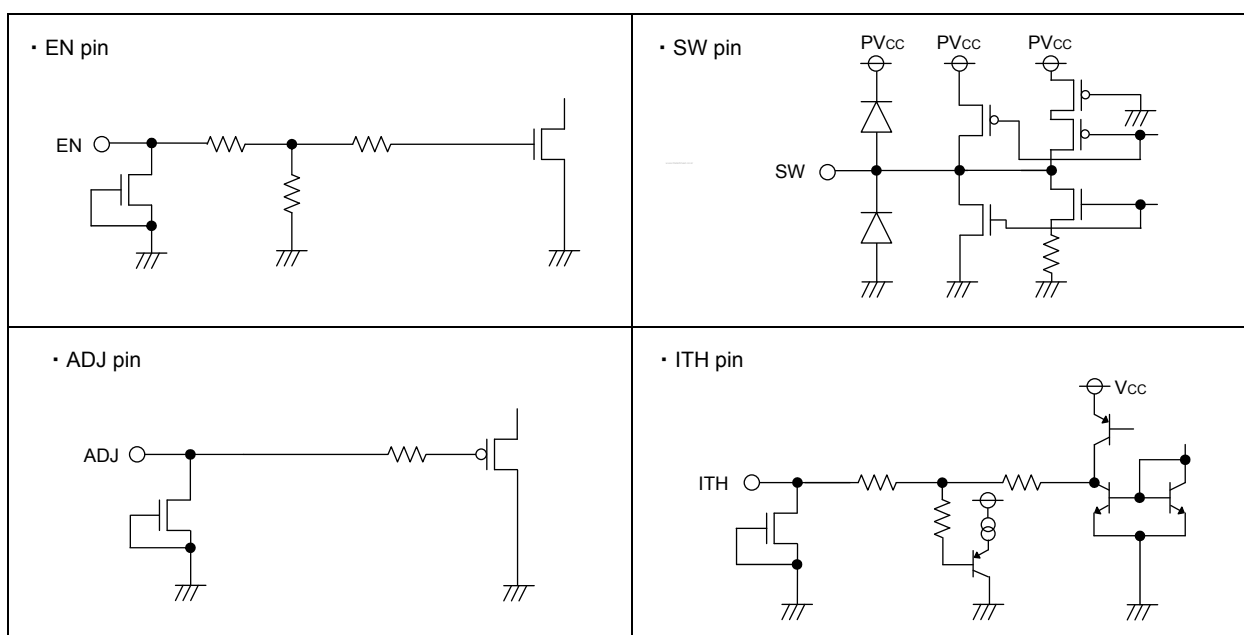
●**I/O equivalence circuit**

Fig.34 I/O equivalence circuit

●**Notes of use**

1. Absolute Maximum Ratings

While utmost care is taken to quality control of this product, any application that may exceed some of the absolute maximum ratings including the voltage applied and the operating temperature range may result in breakage. If broken, short-mode or open-mode may not be identified. So if it is expected to encounter with special mode that may exceed the absolute maximum ratings, it is requested to take necessary safety measures physically   including insertion of fuses.

2. Electrical potential at GND

GND must be designed to have the lowest electrical potential In any operating conditions.

3. Short-circuiting between terminals, and mismounting

When mounting to pc board, care must be taken to avoid mistake in its orientation and alignment.   Failure to do so may result in IC breakdown.   Short-circuiting due to foreign matters entered between output terminals, or between output and power supply or GND may also cause breakdown.

4. Operation in Strong electromagnetic field

Be noted that using the IC in the strong electromagnetic radiation can cause operation failures.

5. Thermal shutdown protection circuit

Thermal shutdown protection circuit is the circuit designed to isolate the IC from thermal runaway, and not intended to protect and guarantee the IC.   So, the IC the thermal shutdown protection circuit of which is once activated should not be used thereafter for any operation originally intended.

6. Inspection with the IC set to a pc board

If a capacitor must be connected to the pin of lower impedance during inspection with the IC set to a pc board, the capacitor must be discharged after each process to avoid stress to the IC.   For electrostatic protection, provide proper grounding to assembling processes with special care taken in handling and storage.   When connecting to jigs in the inspection process, be sure to turn OFF the power supply before it is connected and removed.

7. Input to IC terminals

This is a monolithic IC with P$^+$ isolation between P-substrate and each element as illustrated below.   This P-layer and the N-layer of each element form a P-N junction, and various parasitic element are formed.

If a resistor is joined to a transistor terminal as shown in Fig 35.

○P-N junction works as a parasitic diode if the following relationship is satisfied;

GND>Terminal A (at resistor side), or GND>Terminal B (at transistor side); and

○if GND>Terminal B (at NPN transistor side),

a parasitic NPN transistor is activated by N-layer of other element adjacent to the above-mentioned parasitic diode.

The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown.   It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.
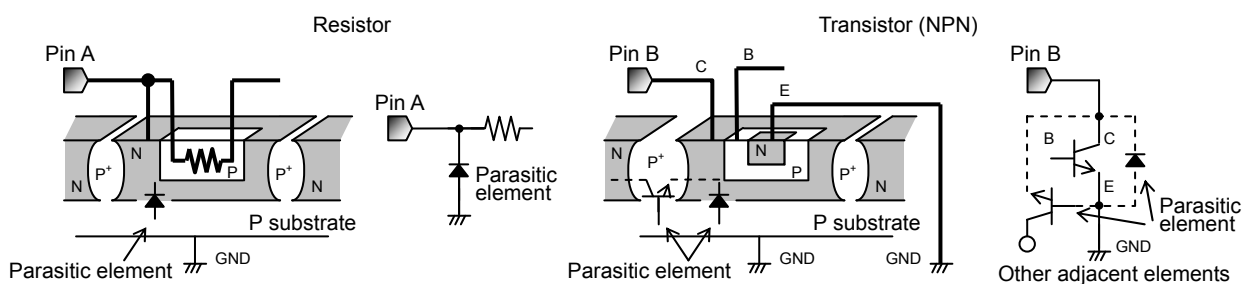

Fig.35 Simplified structure of monorisic IC

8. Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

9 . Selection of inductor

It is recommended to use an inductor with a series resistance element (DCR) 0.1Ω or less. Especially, in case output voltage is set 1.6V or more, note that use of a high DCR inductor will cause an inductor loss, resulting in decreased output voltage. Should this condition continue for a specified period (soft start time + timer latch time), output short circuit protection will be activated and output will be latched OFF. When using an inductor over 0.1Ω, be careful to ensure adequate margins for variation between external devices and this IC, including transient as well as static characteristics. Furthermore, in any case, it is recommended to start up the output with EN after supply voltage is within operation range.

●**Ordering part number**

| B | D | | 8 | 9 | 6 | 0 | | N | V | - | E | 2 |

Part No.   Part No.   Package   Packaging and forming specification
                                              NV : SON008V5060   E2: Embossed tape and reel

SON008V5060

5.0±0.15

6.0±0.15

1PIN MARK

1.0MAX

0.08 S

4.2±0.1

1.27

C0.25

0.8±0.1

3.6±0.1

0.59   0.4 +0.05 -0.04

(Unit : mm)

<Tape and Reel information>
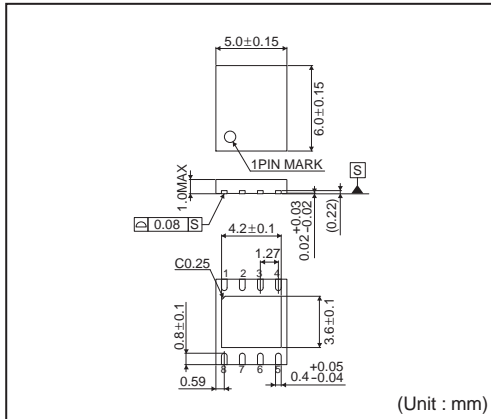
Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand

1pin

Direction of feed

Reel

＊Order quantity needs to be multiple of the minimum quantity.
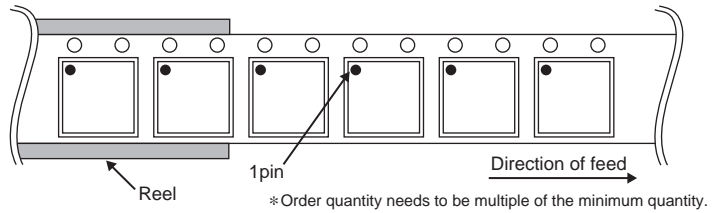
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