STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **ＢＤ９２４４ＡＦＶ**

FUNCTION
- 36V High voltage process
- 1ch control with Full-Bridge
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out and Over Voltage Protection
- Mode-selectable the operating or stand-by mode by stand-by pin
- BURST mode controlled by PWM and DC input

○Absolute Maximum Ratings（Ｔａ＝２５℃）

Parameter	Symbol	Limits	Unit
Supply Voltage	VCC	36	V
BST PIN	BST	40	V
SW PIN	SW	36	V
BST-SW voltage difference	BST-SW	15	V
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃
Power Dissipation	Pd	1024*	mW

*Pd derate at 5.6mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○Operating condition

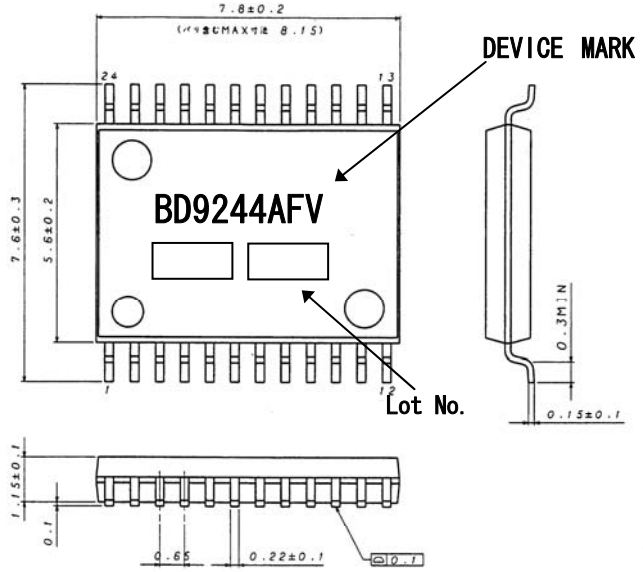
Parameter	Symbol	Limits	Unit
Supply voltage	VCC	9.0～30.0	V
BST voltage	BST	5.0～37.5	V
BST-SW voltage difference	BST-SW	5.0～14.0	V
oscillation frequency	FOUT	30～110	kHz
BCT oscillation frequency	fBCT	0.05～1.00	kHz

○Electric Characteristics (Ta=25℃、VCC=24V、STB=3.0V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
((WHOLE DEVICE))						
Operating current	Icc1	—	2.2	5.0	mA	FOUT=60kHz, FB=SW=GND, BST=OPEN
Stand-by current	Icc2	—	0	10	μA	
((STAND BY CONTROL))						
Stand-by voltage H	VstH	2.0	—	VCC	V	System ON
Stand-by voltage L	VstL	-0.3	—	1.0	V	System OFF
((VCC UVLO BLOCK))						
Operating voltage (VCC)	V_VCCUVP	6.17	6.50	6.83	V	
Hesteresis width (VCC UVLO)	⊿V_VCCUVP	0.37	0.50	0.63	V	
Operating voltage (UVLO)	V_UVP	1.80	1.85	1.90	V	
Hesteresis width(UVLO)	⊿V_UVP	0.15	0.20	0.25	V	
Operating voltage (OVP)	V_OVP	3.10	3.20	3.30	V	
Hesteresis width(OVP)	⊿V_OVP	0.15	0.20	0.25	V	
((REG BLOCK))						
REG output voltage	VREG	7.35	7.50	7.65	V	VCC>8.5V
REG source current	IREG	20	—	—	mA	
((OSC BLOCK)						
RT Output Voltage	VRT	1.05	1.50	1.95	V	
SRT ON Resistor value	RSRT	—	100	200	Ω	
((SOFT START BLOCK))						
Soft start time	TSS	2.5	5.0	10.0	ms	FOUT=60kHz
((BOSC BLOCK))						
BOSC Max voltage	VBCTH	2.16	2.25	2.34	V	fBCT=0.3kHz
BOSC Min voltage	VBCTL	0.6	0.7	0.8	V	fBCT=0.3kHz
BOSC frequency	FBCT	291	300	309	Hz	BCT=10000pF
((FEED BACK BLOCK))						
IS threshold voltage	VIS1	1.225	1.250	1.275	V	
VS threshold voltage	VVS	1.215	1.250	1.285	V	
IS source current 1	IIS1	—	—	0.9	μA	DUTY=2.45V
IS source current 2	IIS2	40	50	60	μA	DUTY=0V IS=1.0V
VS source current	IVS	—	—	0.9	μA	
IS COMP detect voltage	VISCOMP	0.606	0.625	0.644	V	
((OUTPUT BLOCK))						
LN output sink resistance	RsinkLN	1.5	3	6	Ω	
LN output source resistance	RsourceLN	5	10	20	Ω	
HN output sink resistance	RsinkHN	1.5	3	6	Ω	VBST-VSW=7.0V
HN output source resistance	RsourceHN	5	10	20	Ω	VBST-VSW=7.0V
MAX DUTY	MAX DUTY	46.0	48.5	49.5	%	FOUT=60kHz
OFF period	TOFF	100	200	400	ns	
Drive output frequency	FOUT	57.9	60	62.1	kHz	RT=100kΩ
((TIMER LATCH BLOCK)						
CP timer latch detect voltage	VCP	1.9	2.0	2.1	V	
CP timer latch charge current	ICP	0.85	1.0	1.15	μA	
FAIL ON Resistor value	RFAIL	—	125	250	Ω	
((COMP BLOCK))						
COMP over voltage detect voltage	VCOMP	3.88	4.0	4.12	V	
Hysteresis width (COMP)	⊿VCOMP	0.15	0.20	0.25	V	

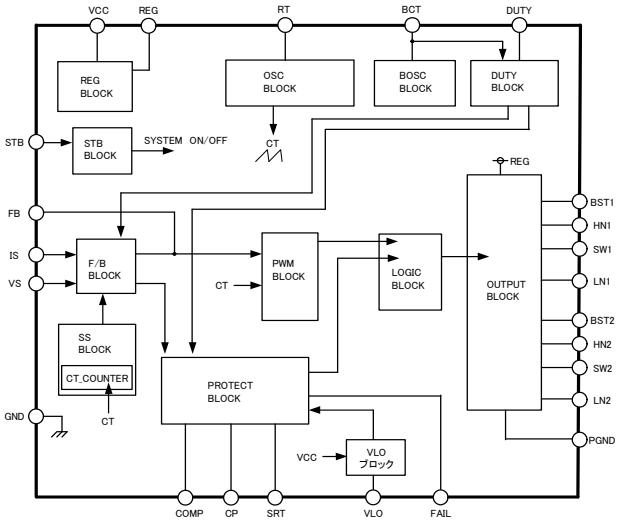
(This product is not designed to be radiation-resistant.)

○Package Dimensions



SSOP-B24 (UNIT:mm)

○Block Diagram



○Pin Description

PIN No.	PIN NAME	FUNCTION	PIN No.	PIN NAME	FUNCTION
1	PGND	Power Ground for FET drivers	13	FAIL	Error Indication signal output (Normal : L, Error : OPEN)
2	LN2	NMOS FET driver (Ch. 2)	14	CP	External capacitor between CP and GND for timer latch
3	BST2	Boot-strap input for HN2 output	15	FB	Error amplifier output
4	HN2	NMOS FET driver (Ch. 2)	16	IS	Error amplifier input 2
5	SW2	Lower rail voltage for HN2 output	17	VS	Error amplifier input 1
6	VCC	Power supply input with UVLO Protection	18	COMP	Input of over voltage detector
7	STB	Stand-by switch	19	VLO	External Under Voltage Lock Out and Over Voltage Protection
8	SRT	External resister from SRT to RT for adjusting the start-up Triangle oscilator	20	SW1	Lower rail voltage for HN1 output
9	RT	External resistor between RT and GND for adjustment frequency of saw tooth wave	21	HN1	NMOS FET driver (Ch. 1)
10	GND	Ground	22	BST1	Boot-strap input for HN1 output
11	BCT	External capacitor between BCT and GND for adjusting the BURST triangle oscillator	23	REG	regulator output
12	DUTY	Control Burst-dimming by PWM signal or DC	24	LN1	NMOS FET driver (Ch. 1)

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and IC. Use adequate margins for steady state and transient characteristics.
2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND pin.
6. If the voltage between VCC and I/O pins or GND and I/O pins is in opposite from the normal potential difference, unusual current flow into pins may occur which can destroy the IC. To avoid such occurrence it is recommended to place protection diodes for prevention against backward current flow.
7. BD9244AFV incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
8. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
9. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
10. By STB voltage, BD9244AFV are changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (1.0～2.0V).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
12. This IC is a monolithic IC which (as shown is Fig.4)has P^+ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,
    - ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)
    - ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin

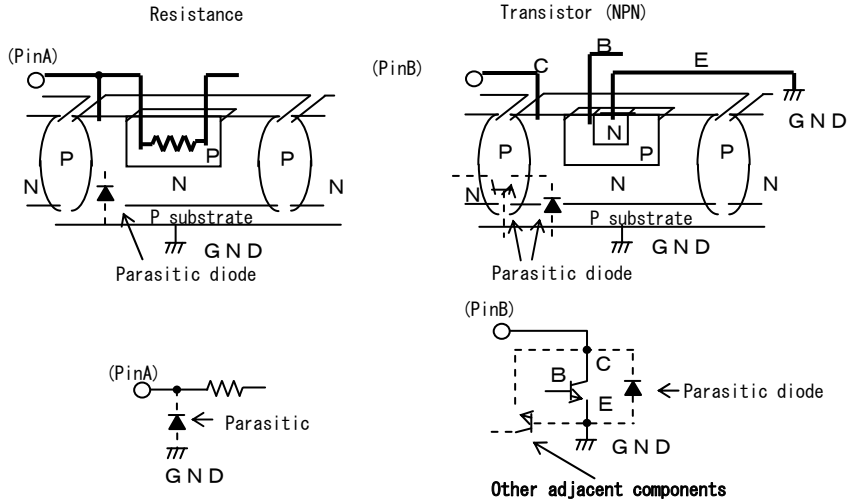


Fig.4. Simplified structure of a Bipolar IC

Notes

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