DATA SHEET

BF1109; BF1109R; BF1109WR
N-channel dual-gate MOS-FETs

Product specification
Supersedes data of 1997 Sep 03
File under Discrete Semiconductors, SC07

1997 Dec 08

Philips
Semiconductors

PHILIPS

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

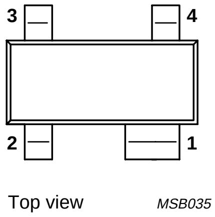
- VHF and UHF applications with 9 V supply voltage, such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1109, BF1109R and BF1109WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

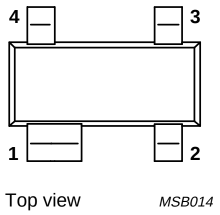
PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



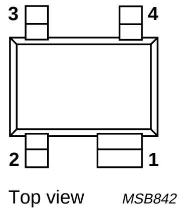
BF1109R marking code: NBp.

Fig.2 Simplified outline (SOT143R).



BF1109 marking code: NFp.

Fig.1 Simplified outline (SOT143B).



BF1109WR marking code: NB.

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	11	V
I_D	drain current (DC)		–	–	30	mA
P_{tot}	total power dissipation	$T_{amb} \leq 80$ °C	–	–	200	mW
$\|y_{fs}\|$	forward transfer admittance		–	30	–	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1		–	2.2	2.7	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	25	40	fF
F	noise figure	f = 800 MHz	–	1.5	2.5	dB
X_{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	100	–	–	dBμV
T_j	operating junction temperature		–	–	150	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	11	V
I_D	drain current (DC)		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	$T_{amb} \leq 80$ °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

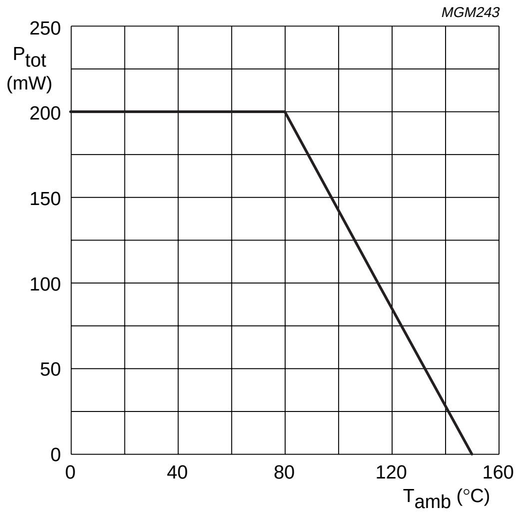


Fig.4 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		200	K/W

Note

1. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

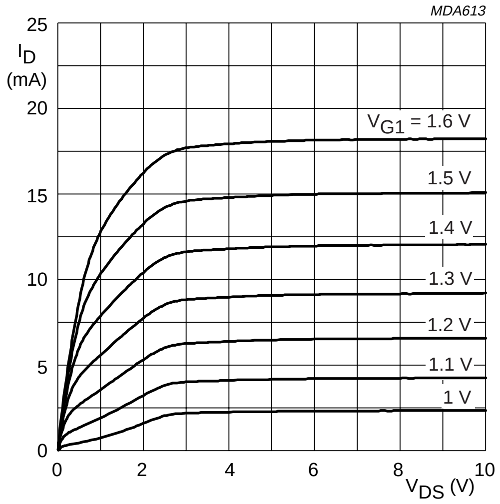
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1\text{-}S} = V_{G2\text{-}S} = 0$; $I_D = 10\ \mu A$	11	–	V
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S} = 0$; $I_{G1\text{-}S} = 10\ \mu A$; $I_D = 0$	11	–	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S} = V_{DS} = 0$; $I_{G2\text{-}S} = 10\ \mu A$	11	–	V
$V_{G2\text{-}S\ (th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S} = 9$ V; $V_{DS} = 9$ V; $I_D = 20\ \mu A$	0.3	1.2	V
I_{DSX}	self-biasing drain current	$V_{G2\text{-}S} = 4$ V; $V_{DS} = 9$ V	8	16	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G1\text{-}S} = 9$ V; $V_{G2\text{-}S} = 0$; $I_D = 0$	–	20	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S} = V_{DS} = 0$; $V_{G2\text{-}S} = 9$ V	–	20	nA

DYNAMIC CHARACTERISTICS

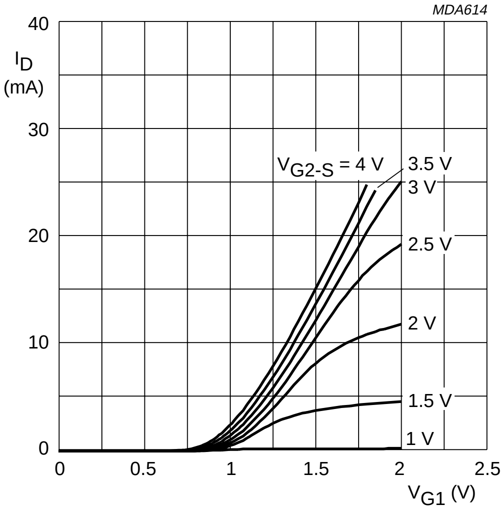
Common source; T_{amb} = 25 °C; $V_{G2\text{-}S}$ = 4 V; V_{DS} = 9 V; self-biasing current; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	24	30	–	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1	f = 1 MHz	–	2.2	2.7	pF
$C_{ig2\text{-}ss}$	input capacitance at gate 2	f = 1 MHz	–	1.5	–	pF
C_{oss}	output capacitance	f = 1 MHz	–	1.3	–	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	25	40	fF
F	noise figure	f = 800 MHz; $Y_S = Y_{S\ opt}$	–	1.5	2.5	dB
G_p	power gain	G_S = 2 mS; $B_S = B_{S\ opt}$; G_L = 0.5 mS; $B_L = B_{L\ opt}$; f = 200 MHz; see Fig.16	–	38	–	dB
		G_S = 3.3 mS; $B_S = B_{S\ opt}$; G_L = 1 mS; $B_L = B_{L\ opt}$; f = 800 MHz; see Fig.17	–	20	–	dB
X_{mod}	cross-modulation	input level for k = 1% at 0 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz; see Fig.18	85	–	–	dBμV
		input level for k = 1% at 40 dB AGC; f_w = 50 MHz; f_{unw} = 60 MHz; see Fig.18	100	–	–	dBμV



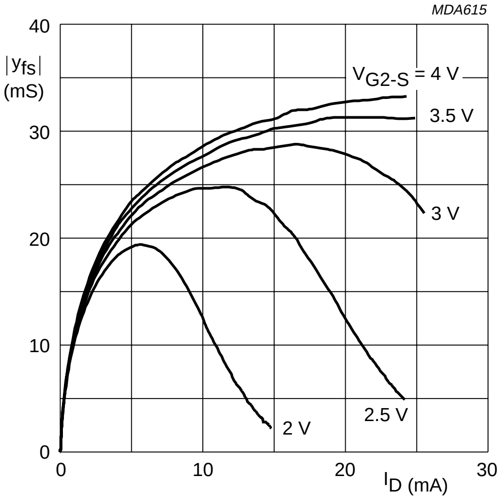
$V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



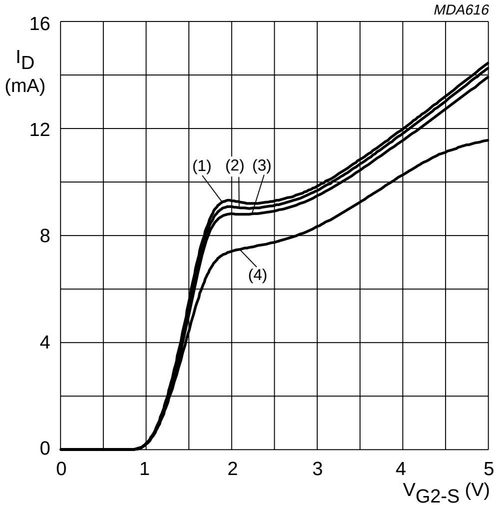
V_{DS} = 9 V.
T_j = 25 °C.

Fig.6 Transfer characteristics; typical values.



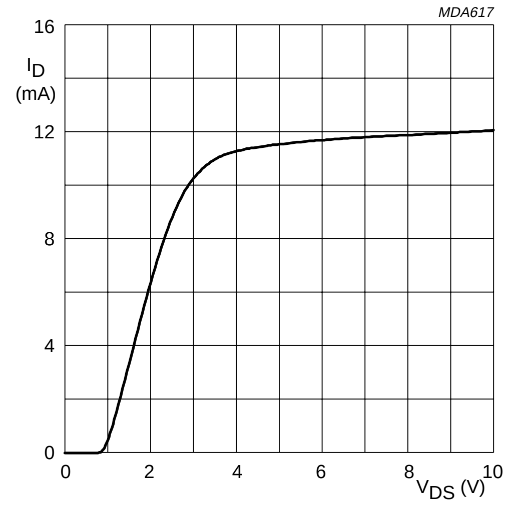
V_{DS} = 9 V.
T_j = 25 °C.

Fig.7 Forward transfer admittance as a function of drain current; typical values.



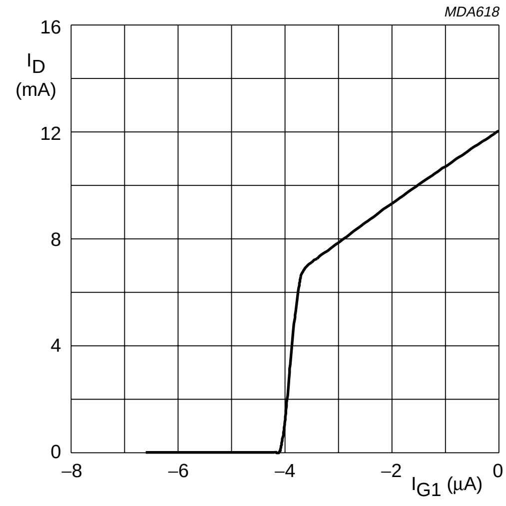
(1) V_{DS} = 9 V.
(2) V_{DS} = 7 V.
(3) V_{DS} = 5 V.
(4) V_{DS} = 3 V.

Fig.8 Drain current as a function of gate 2 voltage; typical values.



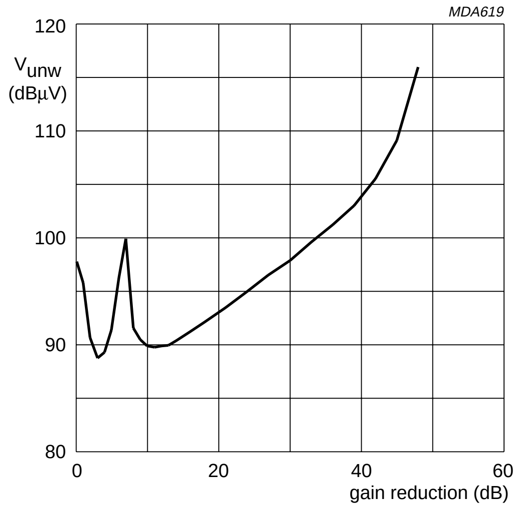
$V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.9 Drain current as a function of drain-source voltage; typical values.



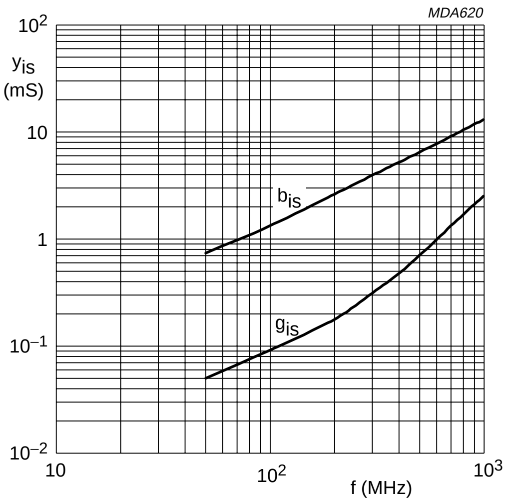
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 current; typical values.



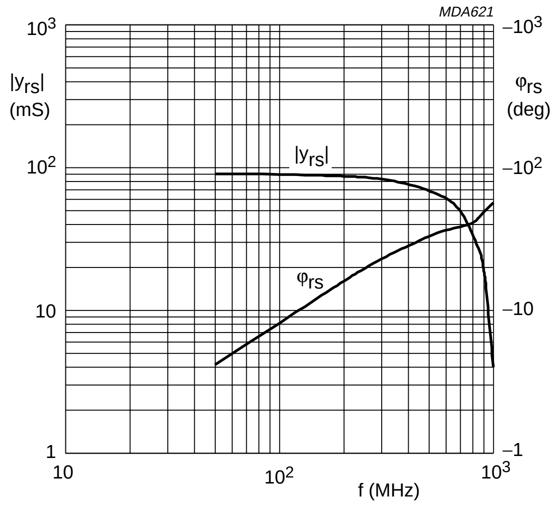
V_{DS} = 9 V; V_{G2nom} = 4 V; I_{Dnom} = 12 mA; f_w = 50 MHz;
f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.11 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values (see Fig.18).



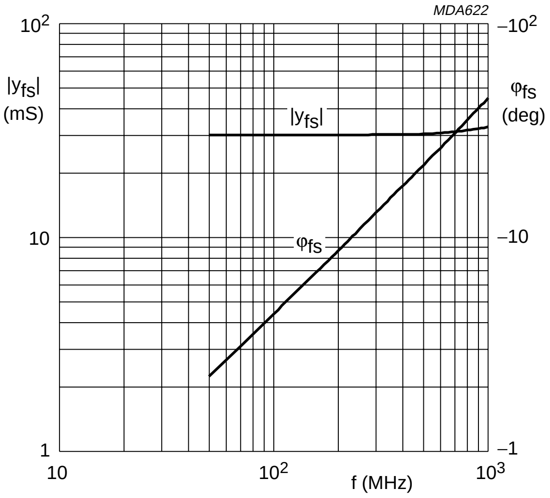
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.12 Input admittance as a function of frequency; typical values.



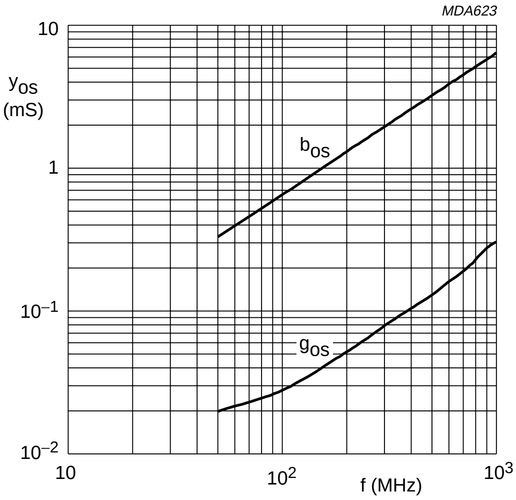
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.13 Reverse transfer admittance and phase as a function of frequency; typical values.



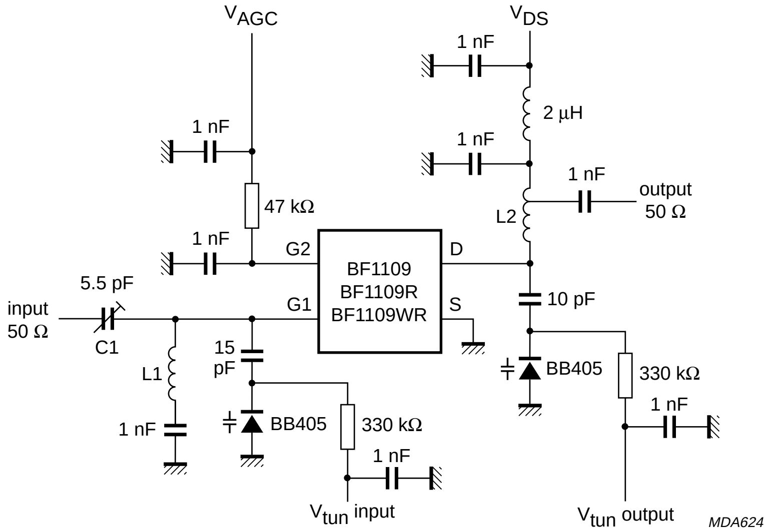
V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.14 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.15 Output admittance as a function of frequency; typical values.



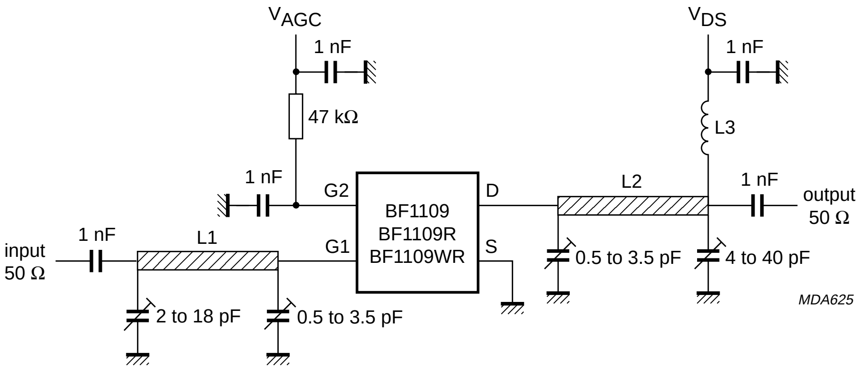
V_{DS} = 9 V, G_S = 2 mS, G_L = 0.5 mS, f = 200 MHz.

L1 = 45 nH, 4 turns, internal diameter = 4 mm, 0.8 mm copper wire.

L2 = 160 nH, 3 turns, internal diameter = 8 mm, 0.8 mm copper wire; tapped at approximately half a turn from the cold side, to set G_L = 0.5 mS.

C1 adjusted for G_S = 2 mS.

Fig.16 Gain test circuit.



V_{DS} = 9 V, G_S = 3.3 mS, G_L = 1 mS, f = 800 MHz.

L1 = 2 cm, silvered 0.8 mm copper wire 4 mm above ground plane.

L2 = 2 cm, silvered 0.8 mm copper wire 4 mm above ground plane.

L3 = 11 turns 0.5 mm copper wire without spacing, internal diameter = 3 mm, L = approx. 200 nH.

Fig.17 Gain test circuit.

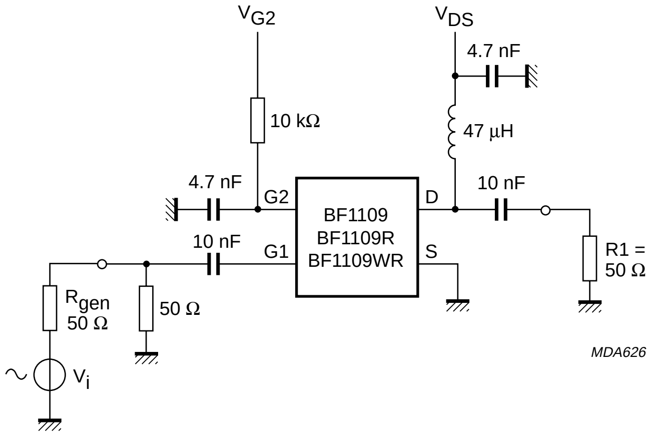


Fig.18 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 12 mA

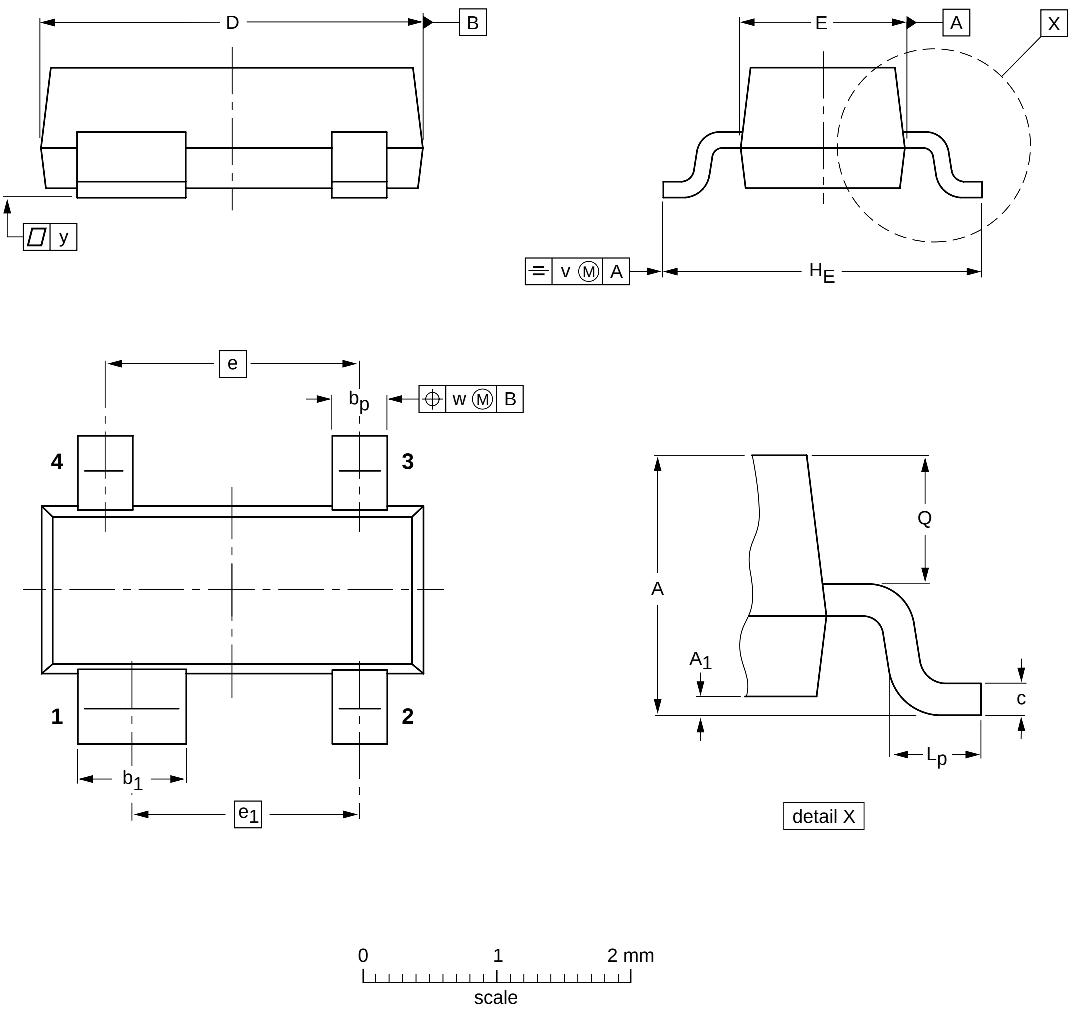
f (MHz)	**S_{11}**		**S_{21}**		**S_{12}**		**S_{22}**	
	MAGNITUDE (ratio)	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**	**MAGNITUDE (ratio)**	**ANGLE (deg)**
50	0.995	–3.71	3.013	175.0	0.000	88.2	0.998	–1.8
100	0.992	–7.29	3.002	170.2	0.001	83.7	0.997	–3.5
200	0.984	–14.3	2.967	160.7	0.002	86.2	0.995	–7.0
300	0.973	–21.2	2.922	151.3	0.002	83.2	0.992	–10.5
400	0.961	–27.9	2.869	142.0	0.003	84.1	0.990	–13.9
500	0.944	–34.4	2.793	132.9	0.003	85.7	0.987	–17.2
600	0.926	–40.8	2.730	124.1	0.003	88.4	0.985	–20.5
700	0.906	–46.9	2.660	1115.3	0.003	94.6	0.983	–23.7
800	0.887	–52.9	2.605	106.5	0.004	107.2	0.981	–26.8
900	0.868	–58.8	2.527	97.8	0.004	114.9	0.977	–30.0
1000	0.852	–64.3	2.457	89.6	0.004	129.7	0.9377	–33.1

Table 2 Noise data: V_{DS} = 9 V; $V_{G2\text{-}S}$ = 4 V; I_D = 12 mA

f (MHz)	**F_{min} (dB)**	**Γ_{opt}**		**R_n (Ω)**
		(ratio)	**(deg)**	
800	1.5	0.684	40.94	40.4

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads SOT143B

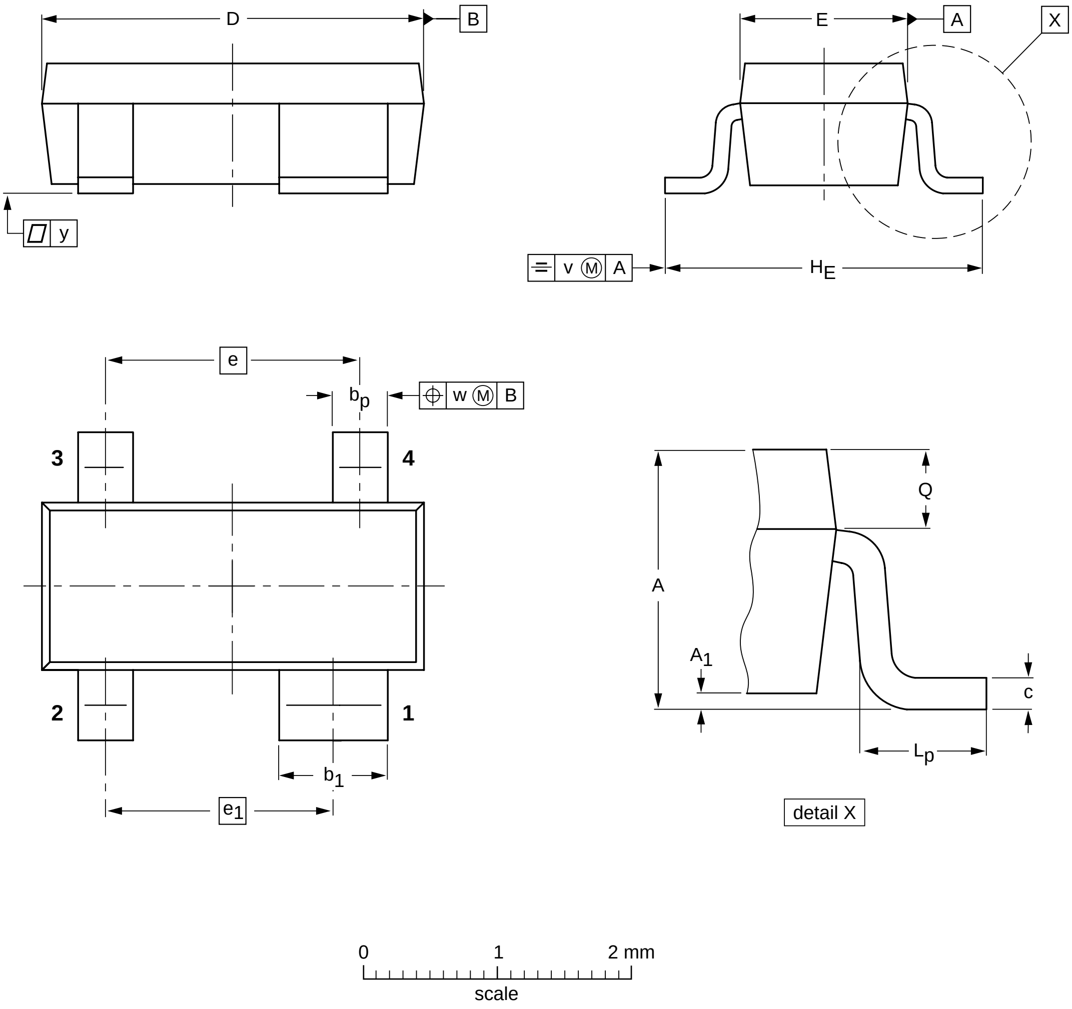


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

Plastic surface mounted package; reverse pinning; 4 leads **SOT143R**

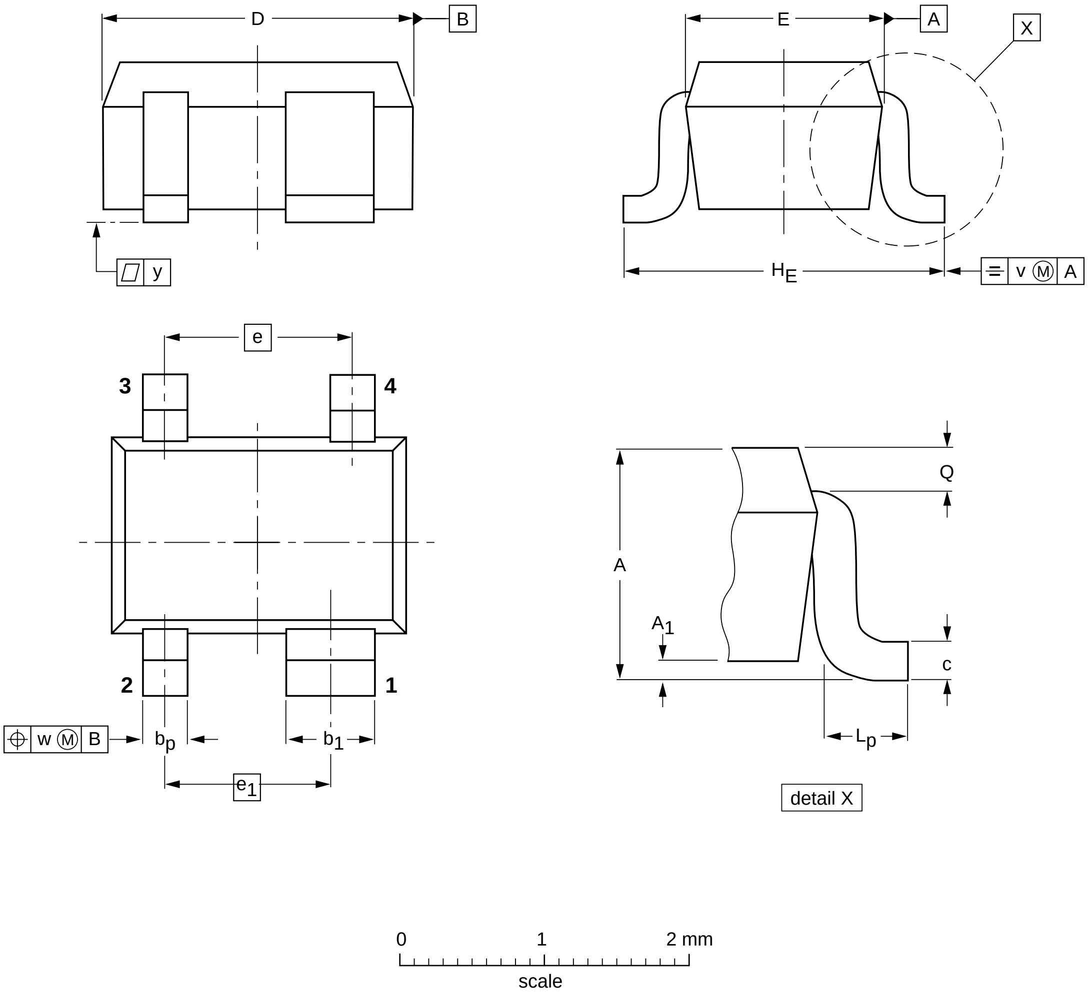


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143R						97-03-10

Plastic surface mounted package; reverse pinning; 4 leads **SOT343R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

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