General Description

BF1510 is a highly integrated summing mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in sub 30W range.

The PWM switch frequency is created by a VCO (voltage control oscillator) which consisted in BF1510. Simultaneously, the frequency is externally programmable and trimmed to tight range. In a typical condition (RI=100K), the switch frequency is 65 KHz.

At no load or light load condition, the IC operates in extended “burst mode” to minimize switching loss, lower standby power and higher conversion efficiency is thus achieved.

BF1510 offers complete protection coverage with auto self-recovery including cycle-by-cycle current limiting, over load protection and SENSE pin short protection, etc. The gate driver is clamped to maximum about 12V to protect the power MOSFET.

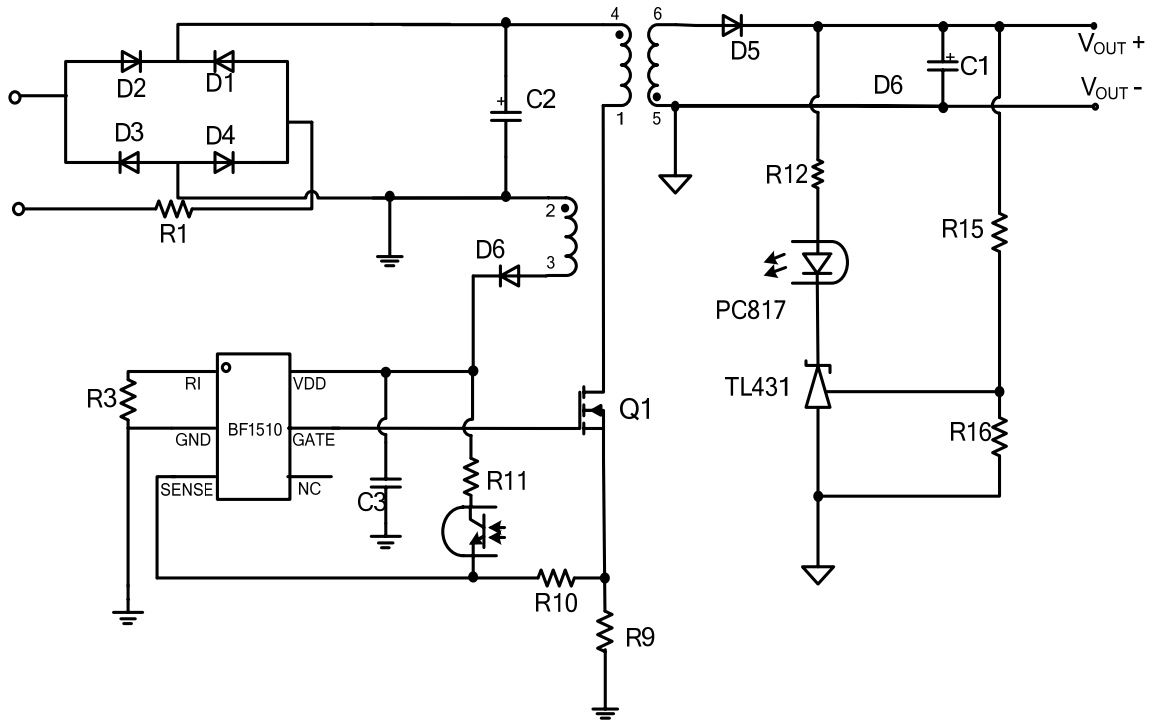
Features

- Summing-mode PWM
- Extended burst mode control to improve efficiency and standby power
- Programmable PWM switch frequency
- Built-in soft start
- Low start-up current and low operating current
- UVLO(under voltage lockout)
- Single fault protection
- LEB(leading edge blanking)
- Audio noise free operation
- Small SOT23-6 package

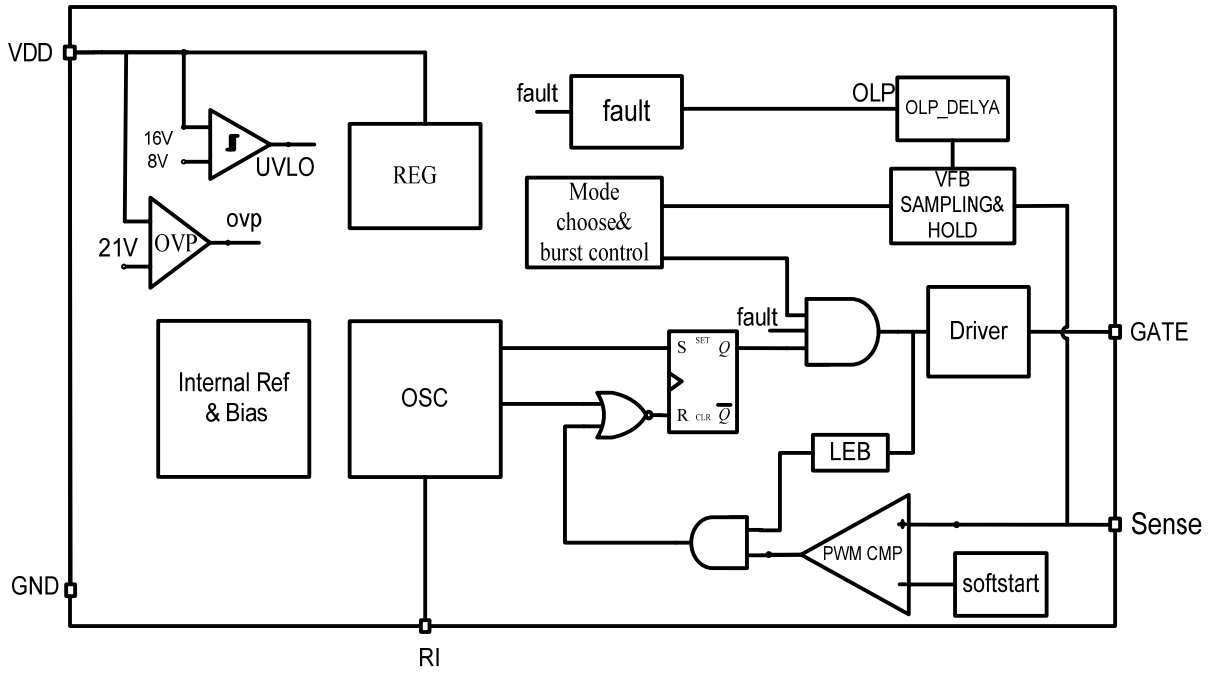
Applications

- Power adaptor
- Battery charger
- Open frame switching power supply

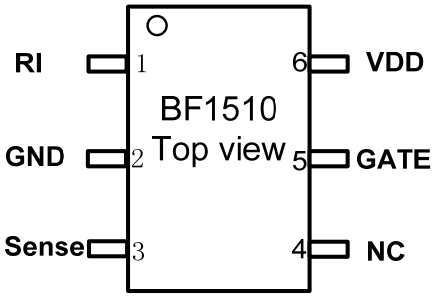
Typical Application



Block Diagram



Package Type



Pin Description

Pin Num	Pin Name	Description
1	RI	Internal Oscillator frequency set pin. A resistor connected between RI and GND sets the PWM frequency.
2	GND	Ground
3	SENSE	Current sense input pin, connected to MOSFET current sensing resistor node.
4	NC	Not connected
5	GATE	Gate drive output for the external power MOSFET switch
6	VDD	Power supply

Electrical Characteristic

(T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply voltage						
Start-up Current	I_VDD_startup			21	30	uA
Operation voltage	I_VDD_OPS			18		V
Turn-on Threshold Voltage	VDD_{ON}		14	16	18	V
Turn-off Threshold Voltage	VDD_{OFF}		7	8	9	V
Over-voltage Threshold	V_{OVP}		20	21	24	V
Oscillator						
Output Frequency	F_{OSC}	RI=100KΩ	60	65	70	KHz
Max Duty Cycle	D_MAX			75%		
RI Open Voltage	V_RI_OPEN			1		V
Operating RI_range	RI_range		50	100	150	KΩ
Sensing						
Leading Edge Blanking	T_LEB			300		ns
Current Sense Detection Voltage	V_OCP			1		V
Power limiting SENSE threshold voltage	V_PL			0.2		V
Burst mode off voltage	V_burst_off			0.8		V
Burst mode on voltage	V_burst_on			0.6		V
Power limiting delayed time	T_D_PL	F=65KHz		63		ms
Soft start time	T_SS	F=65KHz		4		ms
Gate driver output						
Output Delay Time	T_D_OC			150		ns
Output Rising time	Tr	VDD=18V,CL=1nF		170		ns
Output falling time	Tf	VDD=18V,CL=1nF		50		ns
Output Voltage Clamp	V_Clamp			12		V

Absolute Maximum Ratings

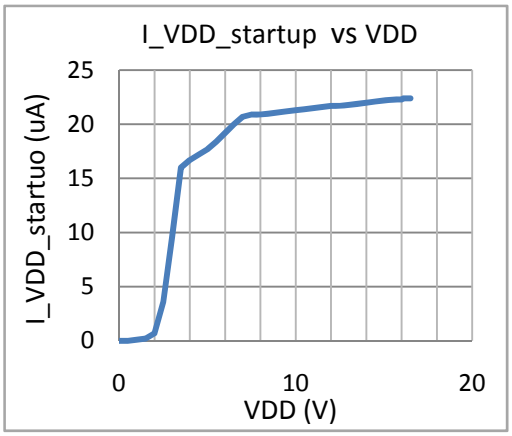
Parameter	Symbol	Value	Unit
VDD input voltage	V_{DD}	40	V
RI input voltage	VRI	7	V
SENSE pin input voltage	V_{SENSE}	7	V
Power Dissipation	P_D	400	mW
Operating Junction Temperature	T_J	-20 to +125	℃
Storage Temperature Range	T_{STJ}	-55 to +150	℃
Lead temperature	T_L	260	℃

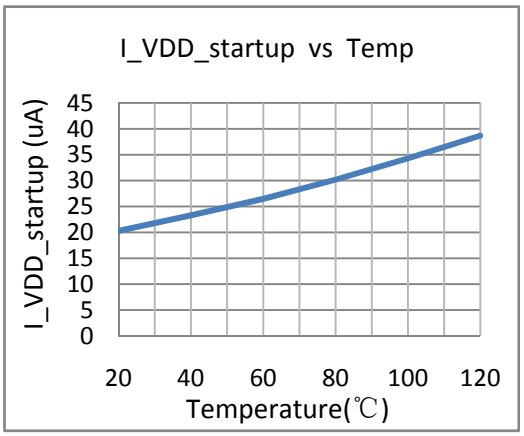
ESD Capability, Human Body Model	HBM	4000	V
ESD Capability, Machine Model	MM	500	V

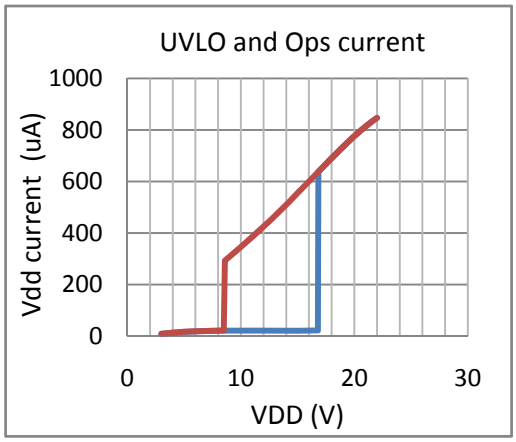
Attention: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

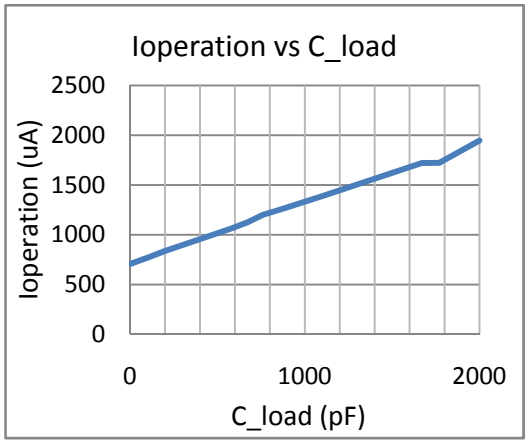
Characterization Plots

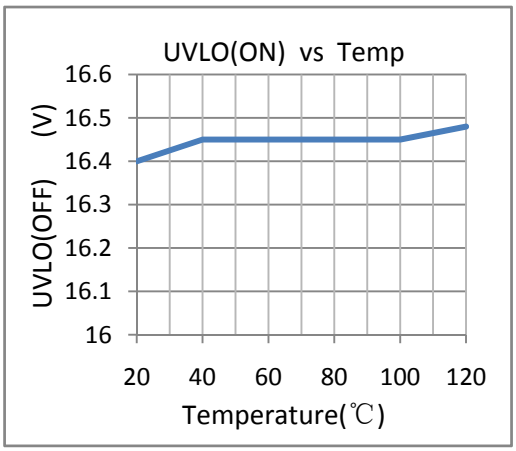
VDD=18V, RI=100KΩ, Ta=25℃ condition applies if not otherwise noted

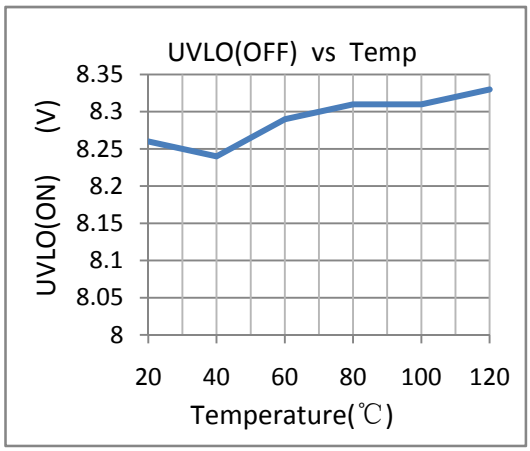


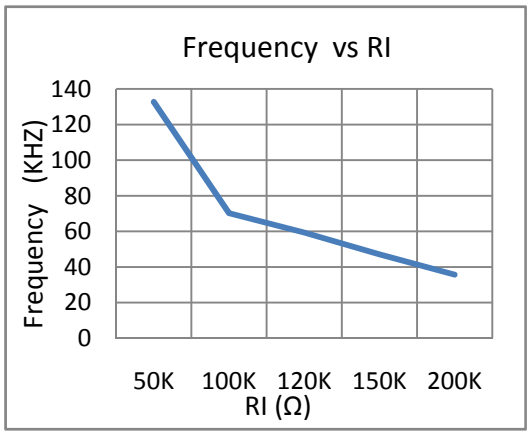


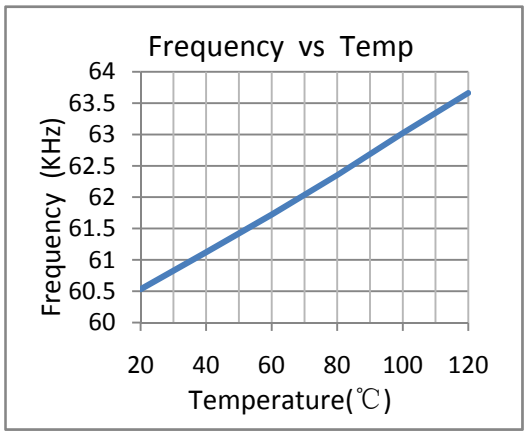


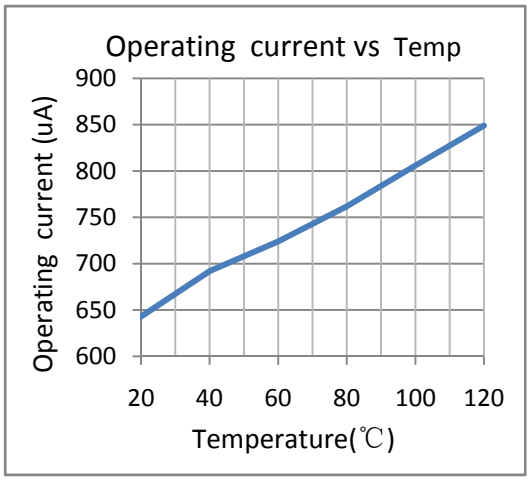







Frequency vs RI
Frequency (KHZ)
140
120
100
80
60
40
20
0
50K
100K
120K
150K
200K
RI (Ω)


Frequency vs Temp
Frequency (KHz)
64
63.5
63
62.5
62
61.5
61
60.5
60
20
40
60
80
100
120
Temperature(℃)


Operating current vs Temp
Operating current (uA)
900
850
800
750
700
650
600
20
40
60
80
100
120
Temperature(℃)

Operation Description

Start-up current and start-up control

Start-up current of BF1510 is designed to be low (typical 21uA) so that VDD could be charged up above UVLO threshold level (typical 16V) and IC starts up quickly. A large value start-up resistor can be used to minimize the power loss. For universal input range design, two 1.5MΩ,1/8W resistors could be used together with a VDD capacitor to a fast start up and low power dissipation solution.

Operating current

The operating current of BF1510 is very low. Good efficiency is achieved by the low operating current, and then a small VDD capacitor can be used in application.

Oscillator operation

A resistor connected between the RI pin and GND sets the constant current source to charge/discharge the internal cap which creates the oscillator frequency and thus the PWM frequency is determined. The frequency is in inverse proportion to the resistor RI. The exact relationship follows the below equation within the specified RI in KΩ range at normal load condition.

$$\text{Fosc} = \frac{6500}{\text{RI (K}\Omega\text{)}}\text{KHz}$$

Summing-mode control PWM

BF1510 is a highly integrated summing mode PWM controller. The difference between summing mode control and peak current control is show in the figure 1.

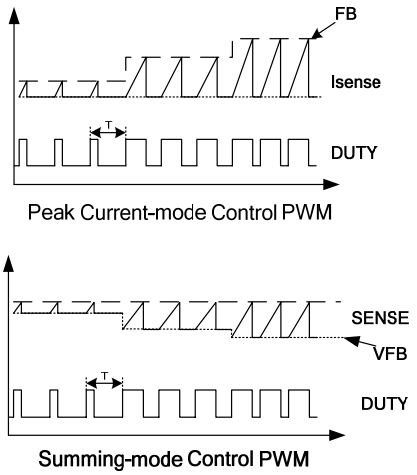


Figure1

In summing-mode, the voltage of SENSE pin contains the information of output voltage and primary current .It leads the system with BF1510 to be a single-loop control system, and has faster response at the same time.

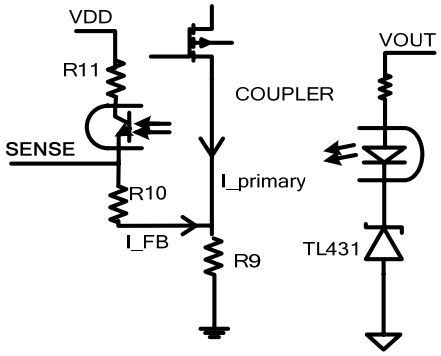


Figure2

As show in the figure 2, the current through the photocoupler I_FB is in proportion to the output voltage at normal operation condition. Refer to the figure 1, we have the below equations:

$$\text{VFB} = \text{I\_FB} \times (\text{R10} + \text{R9})$$
$$\approx \text{I\_FB} \times \text{R10}$$
$$\text{Vsense} = \text{I}_{\text{\_primary}} \times \text{R9} + \text{VFB}$$

Thus, BF1510 can determine the duty by SENSE only.

Burst model operation

At zero load or light load condition, majority of the power dissipation in a switching power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. At no load or light load, the VOUT is higher than at full load, that's means the larger VFB. When the VFB exceeds the threshold level, the output of BF1510 would be turned off until the VFB drops below another threshold level. By these, BF1510 can minimize the switching loss and reduce the standby power consumption.

Over load protection

At over load condition which means VFB (as show in the figure 1) drops below power limiting threshold value (typical 0.2V) for more than power limiting delayed time , BF1510 reacts to shut down the power MOSFET, and the IC restarts when VDD voltage drops below UVLO limit.

Soft start

During initial power on, the BF1510 provides the soft-start. It effectively suppresses the start current peak, especially at high line. The soft-start is activated when a new start-up sequence occurs, and it's over when the built-in 4mS delay is finished or the output voltage is built (the VFB exceeds 0.2V).

Current sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in BF1510 summing mode control. The switch current is sensed by the resistor series between the Source of power MOSFET and the ground. Each time the power MOSFET switches on, a turn-on spike occurs on the sense resistor. To avoid premature termination of the switching pulse, lead edge blanking time is built in. During the blanking time, the comparator output is blocked. This function can save an R-C network to cut down cost.

Over voltage protection on VDD

Once the voltage of the VDD pin rises above OVP threshold the power MOSFET will be shut down immediately. The VDD OVP function is an auto-recovery type protection, when OVP happens, the pulse will be stopped and recovered at the next UVLO on.

Fault protection

Under the conditions listed below, the gate output will turn off immediately.

- *SENSE pin floating*
- *SENSE pin short to GND*
- *RI pin floating*
- *RI pin short to GND*

Test Circuits

(1) Start-up current consumption

The test circuit is showed below:

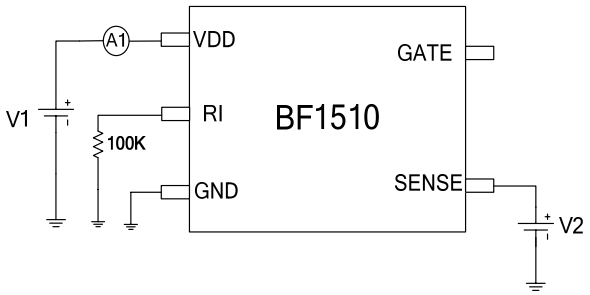


Figure3

① Set V1=0±0.01V, V2=0.5V±0.01V and make the GATE pin floating.

② Set V1=5±0.01V with 1ms delay time.

③ Keep V1 powered, increase V1 to 14±0.01V, the current A1 flowing into VDD is the startup current consumption.

(2) Hysteresis start-up

The test circuit is showed in the figure 3. When V1 increases over Von (the first threshold voltage) from 0V, the IC starts to work normally; and when V1 decreases under Voff (the second threshold voltage), the IC stops working and turns into standby mode.

① Set V1=5±0.01V, V2=0.5V±0.01V with 1ms delay time and make the GATE pin floating.

② Increase V1 until the output (the GATE pin) frequency changes from (0±1KHz) to (65±5KHz). At that time, Von is the V1.

③ Decrease V1 until the output (the GATE pin) frequency changes from (65±5KHz) to (0±1KHz).

At that time, Voff is the V1.

(3) VDD over voltage protection

The test circuit is showed in the figure3. When V1 increases to a certain value, IC will turn off the output.

① Set V1=0±0.01V, V2=0.5V±0.01V and make the GATE pin floating.

② Set V1=18±0.01V with 1ms delay time and make sure the output frequency is 65±5KHz.

③ Keep V1 powered, increase V1 until the output (the GATE pin) frequency changes from (65±5KHz) to (0±1KHz). At that time, V1 is just the VDD OVP voltage.

(4) Burst mode

The test circuit is showed in the figure3. When V2 increase over a certain voltage, the IC will turn into the burst mode and turn off the output immediately.

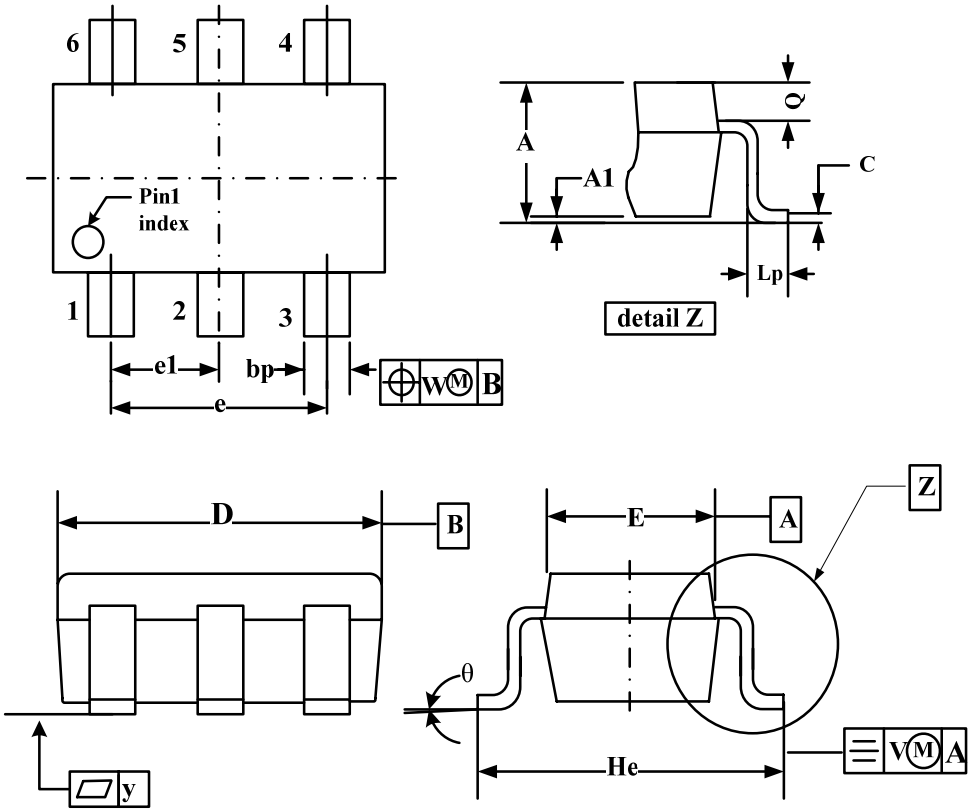
① Set V1=18±0.01V, V2=0.5V±0.01V with 1ms delay time and make the GATE pin floating.

② keep V1 ,V2 powered , increase V2 until the output (the GATE pin) frequency changes from (65±5KHz) to (0±1KHz).At that time, the V2 is the burst mode off voltage

③ keep V1 ,V2 powered , decrease V2 until the output (the GATE pin) frequency changes from (0±1KHz) to (65±5KHz). At that time, the V2 is the burst mode on voltage.

Package Outline

SOT23-6



Dimensions (mm)

A	A1	bp	c	D	E	e	e1	He	Lp	Q	v	w	y	θ
1.3	0.15	0.50	0.20	3.1	1.7	1.9	0.95	3.0	0.6	0.33	0.2	0.2	0.1	0°
1.0	0.03	0.35	0.10	2.7	1.3			2.5	0.2	0.23				10°

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