HD720P CMOS Image Sensor

BF3710

Datasheet

Contents

1. General Description

The BF3710 is a highly integrated HD 720P camera chip which includes CMOS image sensor (CIS) and image signal processing function (ISP). It is fabricated with the world's most advanced CMOS image sensor process to realize ultra-low dark noise, high sensitivity and very low power imaging system. The sensor consists of a 1297 x 817 effective pixel array which has an optical format of 1/6 inch. It has integrated noise canceling CDS (Correlated Double Sampling) circuits, analog global gain and separated R/G/B gain controller, auto black level compensation and on-chip 10-bit ADC. The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB (Auto White Balance) control. It provides various data formats, such as Bayer RGB, RGB444, RGB555, RGB565, YCbCr4:2:2, CCIR656.It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

The product is capable of operating at up to 30 fps @ 72MHz master clock in 720P (1280x720) mode, with complete user control over image quality and data formatting. All required image processing functions, including exposure control, white balance control, color saturation control and so on, are also programmable through the two-wire serial bus.

2. Features

- Standard optical format of 1/6 inch.
- Max 30 fps in 720P mode @ 72MHz master clock.
- Ultra-low dark noise at high temperature.
- Ultra-low Power consumption of typical 140mW@30fps, 45uA at power down.
- Various output formats: YCbCr4:2:2, RGB444, RGB555, RGB565, Raw Bayer，CCIR656-like.
- Power supply: 1.4~1.6V for Core，2.7~3.1V for Analog, 1.7~3.1V for I/O. Can work with single 2.8V power supply.
- Horizontal mirror and Vertical flip.
- 50/60Hz flicker cancellation.
- Programmable I/O drive capability.
- Automatic black level control.
- Image processing function: Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, False Color Suppression, Purple Fringe Correction, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto exposure, Auto White Balance, Color Saturation, Contrast, Skin tone detection, Scaling and Data Format Conversion.
- Maximum resolution: 1288*808.
- On-chip test pattern generation..
- Package: CSP, Bare Die.

3. Applications

- Notebook and desktop PC cameras
- Cellular phone cameras
- PDAs
- Toys
- MP4
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

4. Technical Specifications

- Active pixel array: 1297 x 817
- Pixel size: 1.9μm×1.9μm
- Sensitivity: 1.0V/lux.s
- Dark current: 3 mV/S at 40℃
- Power consumption: 140mW @ 30fps
- Standby current: 45uA
- S/N Ratio: 35dB
- Dynamic range: 57dB
- Operating temperature: -20~60℃
- Optimal lens chief ray angle: 25º

5. Functional Overview

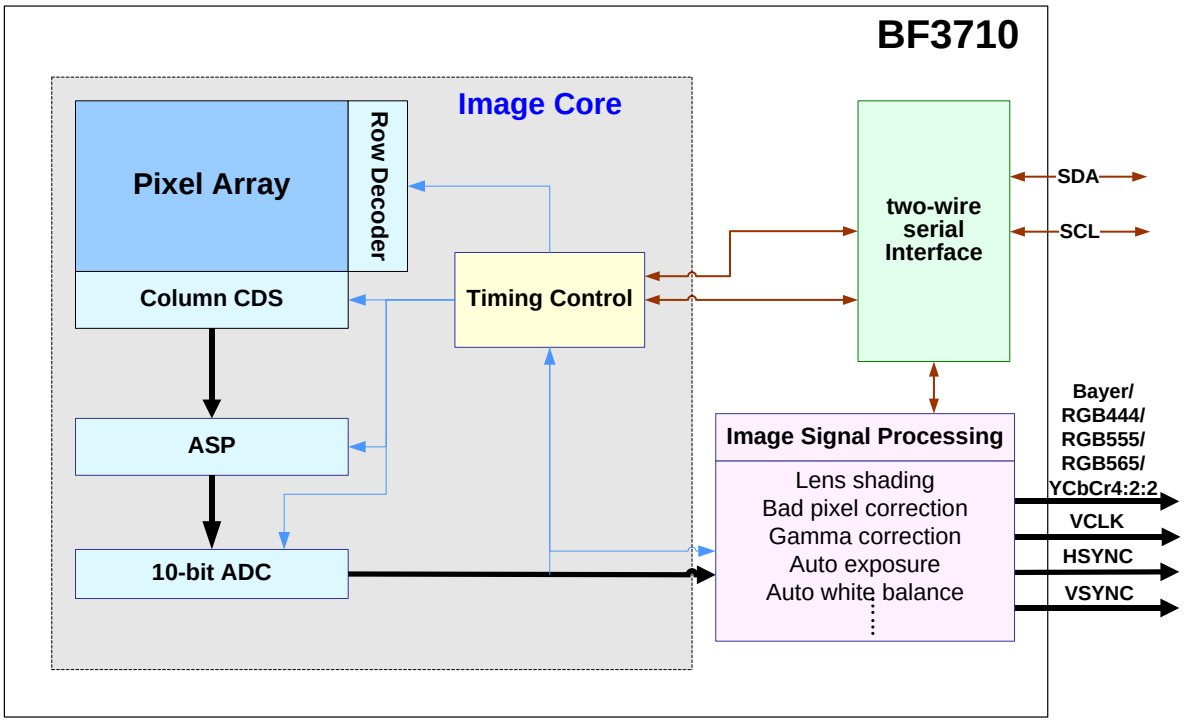


Figure 1. Block Diagram

BF3710 has an active image array of 1297x817 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The ASP block is mainly used to control global gain and color gains to get accurate exposure and white balance under different light condition and color temperature. The analog signal is transferred to digital signal by A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, low pass filter, color correction, gamma correction, skin detection, scaling and data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

5.1 Pixel Array

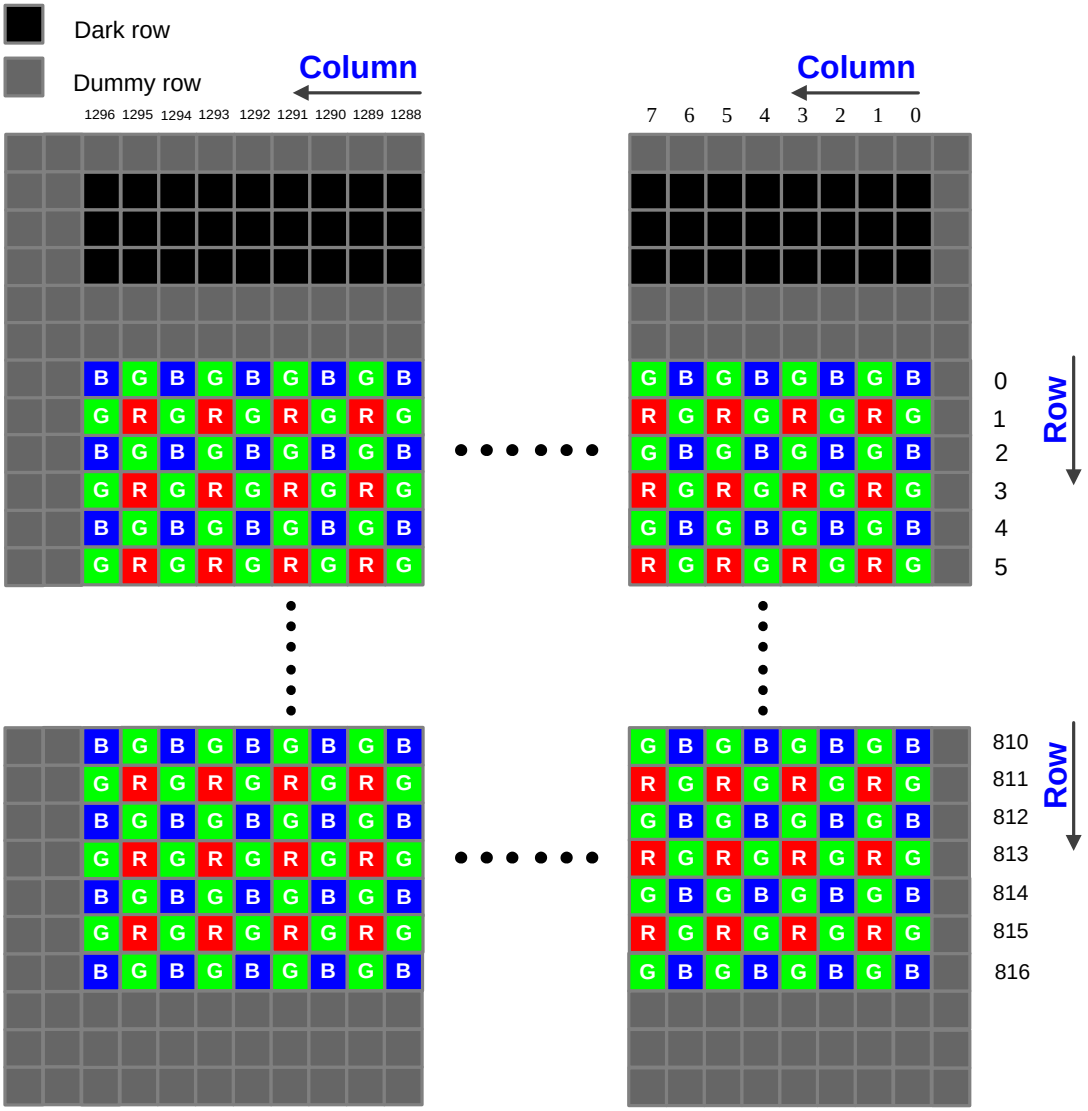


Figure 2. Sensor Array Region

The active pixel array is configured as 1297 columns by 817 rows. Dummy pixels and dark rows are added outside the active pixel array.

Pixel array is covered by Bayer color filters as can be seen in figure2. The primary color BG/GR array is arranged in line-alternating fashion. Since each pixel can have only one type of color filter on it, only one color component can be obtained by a pixel. BF3710 can provide the Raw Bayer data or YUV data through an 8-bit output data bus. For full resolution, if no mirror in column, column is read out from 4 to 1291. If mirror in column, column is read out from 1292 to 5. If no flip in row, row is read out from 4 to 811. If flip in row, row is read out from 812 to 5.

5.2 Column CDS

BF3710 has column/row driver circuits to read out the pixel data progressively. The CDS (Correlated Double Sampling) circuit reduces temporal noise and pixel level FPN (Fixed Pattern Noise). The unique patented column buffer amplifier and ASP (Analog Signal Processing) circuit remove column level FPN caused by various sources of manufacturing process variations.

5.3 Timing controller

The timing controller controls the following functions

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- External timing outputs (VSYNC, HSYNC and VCLK)

5.4 Analog Signal Processor

This block performs all analog image functions including Color gain/Global gain control and black level compensation. Each of the R, G, B color pixel signals can be multiplied by different gain factors to balance the color of the image at various light conditions.

5.5 A/D converter

The analog signals are converted to digital forms column by column and row by row, through out the whole array. BF3710 provides the 10-bit Raw Bayer data for ISP through an internal 10-bit data bus.

5.6 Automatic Black Control

The automatic black level controller calculates the data of the dark row and controls the lowest black level for output image data.

5.7 Image Signal Processor

This block performs all image processing functions including Lens Shading Correction, Gamma Correction, Bad pixel correction, Color Interpolation, False Color Suppression, Low Pass Filter, Color Space Conversion, Color Correction, Edge Enhancement, Auto Exposure, Auto White Balance, Color Saturation, Contrast, Skin detection, Scaling and Data Format Conversion.

6. Specifications

6.1 Electrical Characteristics

6.1.1. Absolute Maximum Ratings

- Supply voltage (VDDIO): 1.7 ~ 3.1 V
- Supply voltage (VDD3A): 2.7 ~ 3.1 V
- Supply voltage (VDDD): 1.4 ~ 1.6 V
- Supply voltage (VDDL): 1.7 ~ 3.1 V
- Operating temperature: -20~60 ℃
- Storage temperature: -30~80 ℃
- ESD Rating, Human Body mode: 2000 V

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

6.1.2. DC Parameters

Table 1. DC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
VDDIO	I/O power supply	V	1.7	2.8	3.1	--
VDDD	Digital power supply	V	1.4	1.5	1.6	--
VDDL	LDO power supply	V	1.7	1.8/2.8	3.1	--
VDD3A	Analog power supply	V	2.7	2.8	3.1	--
Vih	Input voltage logic “1”	V	0.7*VDDIO	--	--	--
Vil	Input voltage logic “0”	V	--	--	0.3*VDDIO	--
Voh	Output voltage logic “1”	V	0.9*VDDIO	--	--	--
Vol	Output voltage logic “0”	V	--	--	0.1*VDDIO	--
I_vddio	VDDIO supply current, normal operation mode	mA	--	--	13	1
I_vddd	VDDD supply current	mA	-- --	--	19	--
I_vddl	VDDL supply current	mA	-- --	--	19	--
I_vdd3a	VDD3A supply current	mA	--	--	31	2

Note：

1. Because power consumption of I/O depends on the output load and system environment, user should supply enough current to sensor for stable operation. It is measured when output load is

floated.

2. Because current of analog circuit depends on the registers' values, it is measured at specific register's value.

6.1.3. Clock Requirement

Table 2. AC Operation Conditions

Symbol	Parameter	Unit	Min.	Typ.	Max.	Notes
XCLK	External clock frequency	MHz	6	24	27	1
MCLK	Master clock	MHz	--	72	80	2
PCLK	Pixel clock	MHz	--	36	40	3
VCLK	Output Video clock	MHz	--	36	80	4
SCL	two-wire serial interface clock frequency	KHz	--	400	--	5

Note:

1. XCLK is the input clock and it is the input of PLL.
2. MCLK is the master clock of the system, and it is internally generated by PLL.
3. PCLK is the pixel clock and its frequency is half of MCLK.
4. VCLK is the output video clock of the system.
5. SCL is driven by host processor. For the detail serial bus timing, refer to two-wire serial Interface section.

6.2 Electro-Optical Characteristics

External input clock frequency: 24MHz.

Operating voltage: VDDIO=2.8V, VDD3A=2.8V,VDDD=1.5V.

Operating temperature: 25°C

Table 3. Electro-Optical Characteristics

Parameter	Unit	Min.	Typ.	Max.	Notes
Sensitivity	V/Lux·sec	--	1.0		1
Dark current	mV/sec	--	3	6	2
S/N ratio	dB	--	35	--	--
Dynamic Range	dB	--	57	--	--
Frame Rate	fps	--	--	30	3

Notes:

1. With color filter, measured at 50 lux green light condition at room temperature.
2. Measured at dark condition for exposure time of 1s (40 Celsius).
3. With 1288*728 window size @ MCLK 72MHz.

6.3 Input-Output AC Characteristics

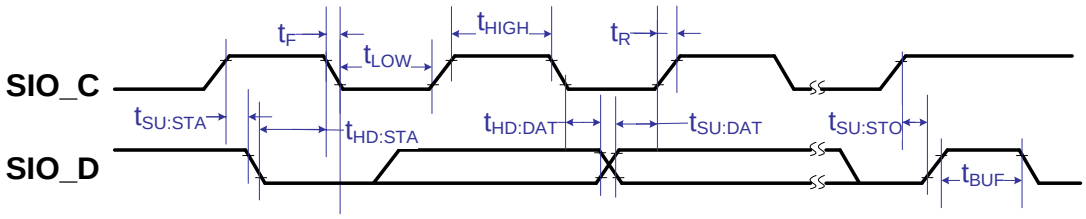


Figure 3. Two-Wire Serial Interface Timing

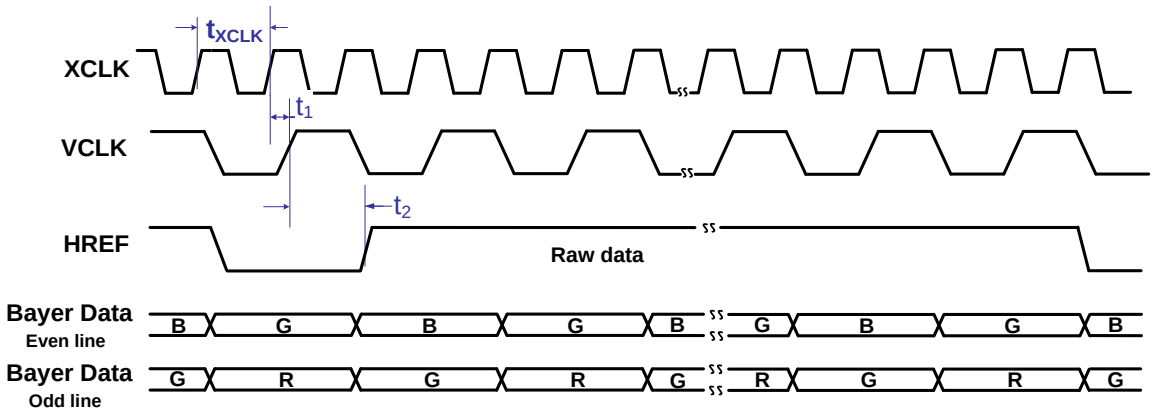


Figure 4. Horizontal Timing Raw Bayer Data

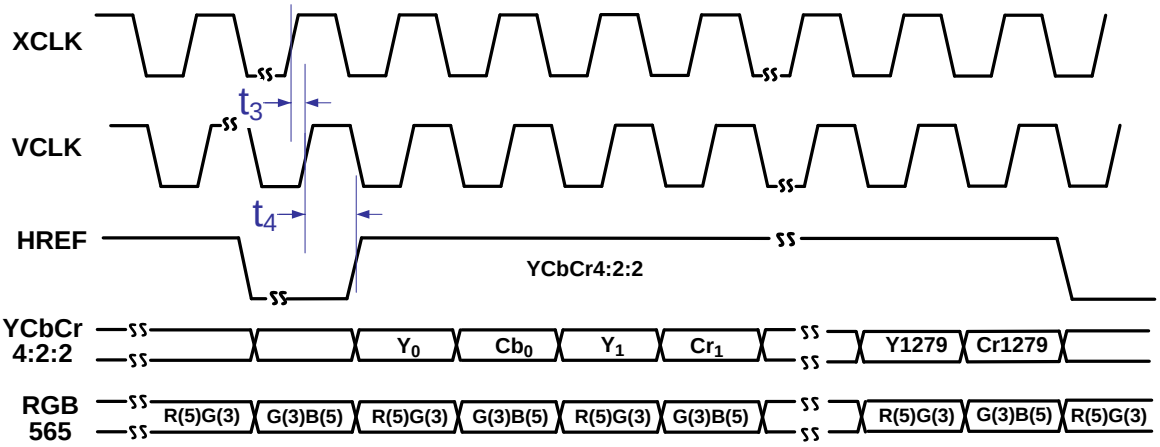


Figure 5. Horizontal Timing YUV4:2:2/ RGB565

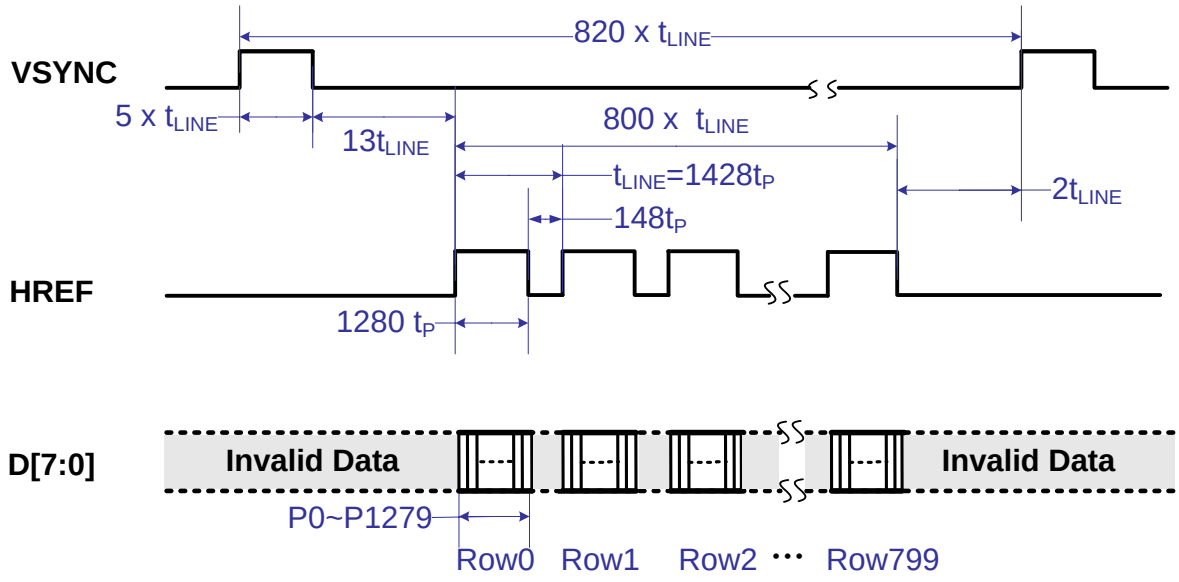


Figure 6(a). WXGA(1280x800) YUV Frame Timing

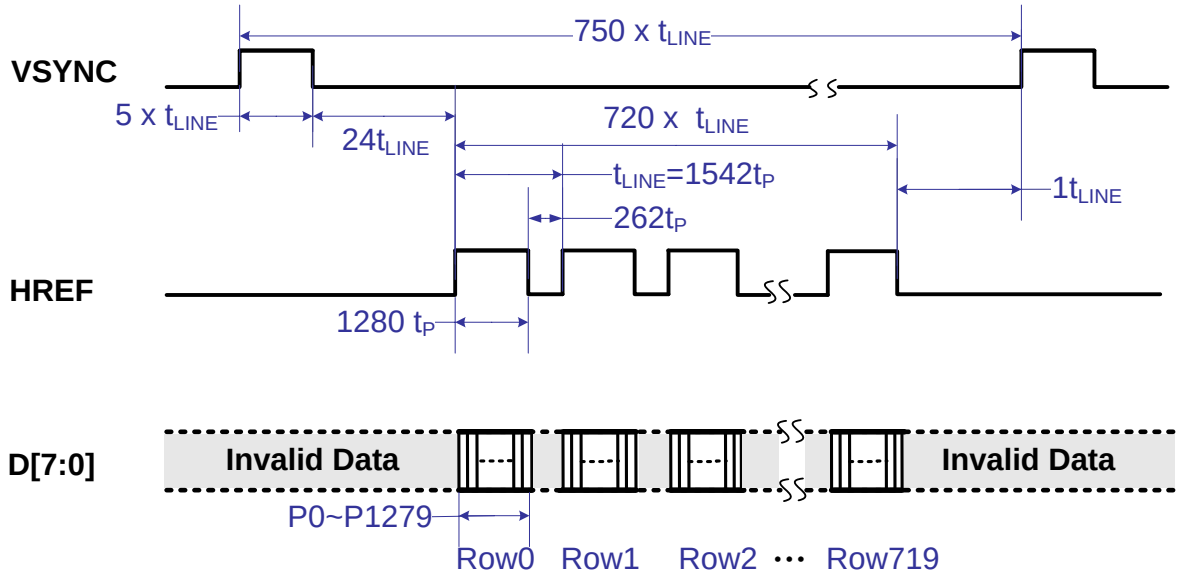


Figure 6(b). 720P(1280x720) YUV Frame Timing

Table 4. AC Characteristics

Symbol	Descriptions	Min.	Typ.	Max.	Unit
t_P	t_P=2 x t_{MCLK}	--	27.78	--	ns
f_{MCLK}	Master Clock Frequency	--	72	--	MHz
f_{VCLK}	Video Clock Frequency for Raw data , f_V= f_{MCLK} /2 for YUV, f_V= f_{MCLK}	--	36/72	--	MHz

t_{LINE}	Line length	--	WXGA: 1428xt_P 720P: 1542xt_P	--	ns
t_R, t_F	rise/fall times of both SCL and SDA	--	--	300	ns
t_{LOW}	Low Period of SCL	1.3	--	--	us
t_{HIGH}	High Period of SCL	600	--	--	ns
$t_{HD:STA}$	Start condition Hold Time	600	--	--	ns
$t_{SU:STA}$	Start condition Setup Time	600	--	--	ns
$t_{HD:DAT}$	Data-in Hold Time	0	--	--	ns
$t_{SU:DAT}$	Data-in Setup Time	100	--	--	ns
$t_{SU:STO}$	Stop condition Setup Time	600	--	--	ns
t1	XCLK rising to VCLK (RAW DATA)	--	28.8	--	ns
t2	VCLK rising to HREF (RAW DATA)	--	43.8	--	ns
t3	XCLK rising to VCLK (YUV)	--	19.2	--	ns
t4	VCLK rising to HREF (YUV)	--	21.6	--	ns

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below.

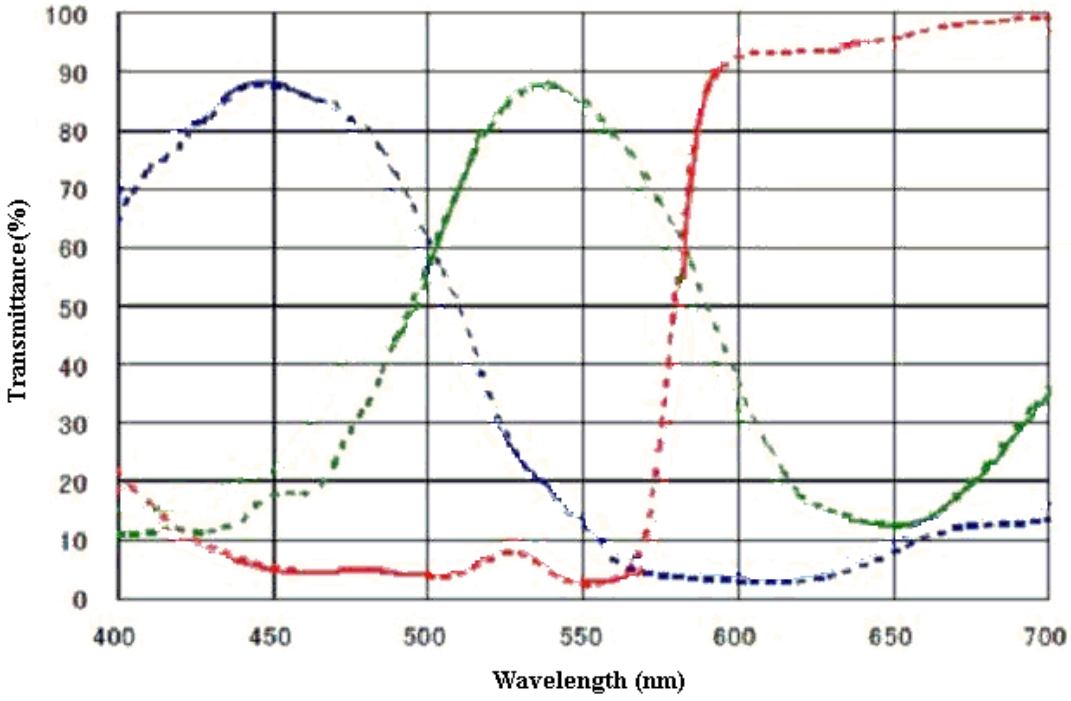


Figure 7. Spectral Characteristics

7. Two-wire serial interface & Register

7.1 Theory of Operation

The registers of BF3710 are written and read through the two-wire serial interface. BF3710 has two-wire serial interface slave. BF3710 is controlled by the two-wire serial interface clock (SCL), which is driven by the two-wire serial interface master. Data is transferred into and out of BF3710 through the two-wire serial interface data (SDA) line. The SCL and SDA lines are pulled up to VDDIO by a 2kΩ off-chip resistor. Either the slave or the master device can pull the lines down. The two-wire serial interface protocol determines which device is allowed to pull the two lines down at any given time.

Note: Two-wire serial interface device address of* BF3710 *is 7'h6e(7'b1101110).

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of 7 bits of address and 1 bit of direction. A "0" in the LSB of the address indicates write mode, and "1" indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The two-wire serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock: it can only change when the two-wire serial interface clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where "0" indicates write and "1" indicates read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The BF3710 uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

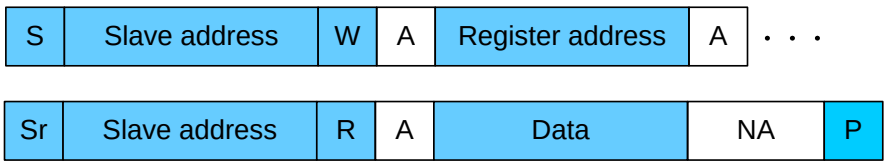
A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

7.2 Two-wire Serial Interface Functional Description

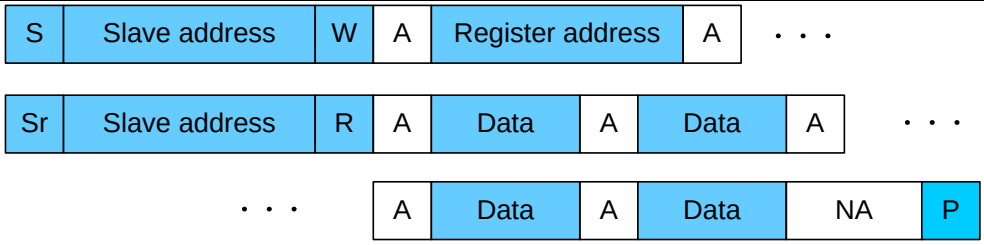
Single Write Mode Operation

Multiple Write Mode (Register address is increased automatically) [1] operation

Single Read Mode Operation



Multiple Read Mode (Register address is increased automatically) [1] Operation



S: Start condition. **Sr:** Repeated Start (Start without preceding stop.)

Slave Address: write address = DCh = 11011100b

read address = DDh = 11011101b

R/W: Read/Write selection. High = read, LOW = write.

A: Acknowledge bit. **NA:** No Acknowledge.

Data: 8-bit data **P:** Stop condition

Note1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

7.3 Register Summary (full list)

Table 5. BF3710 Register List

Address	Name	Width	Default value	Description
01h	***BLUE_GAIN***	6	19h	Blue gain register
02h	***RED_GAIN***	6	15h	Red gain register
03h	***HWIN***	8	50h	Bit[7]: Reserved Bit[6:4]: High 3 bits of *HSTOP* Bit[3]: Reserved Bit[2:0]: High 3 bits of *HSTART*
09h	***PDN_DR_CTR***	8	15h	Bit[7]: PDN_REG, (PDA=PDN_REG||PDN) Bit[5:4]: Driver capability control for DAT[9:0] pad: 00: 1x 01: 2x 10: 3x 11: 4x Bit[3:2]: Driver capability control for VSYNC/HREF pad: 00: 1x 01: 2x 10: 3x 11: 4x Bit[1:0]: Driver capability control for VCLK pad: 00: 1x 01: 2x 10: 3x 11: 4x
0ah	***CLK_DIV***	8	04h	Bit[7:3]: Reserved Bit[2]: PCLK_DIV2 Bit[1:0]: PCLK_DIV1[1:0]
0bh	***COM4***	8	00h	Bit[7:6]: Reserved Bit[5:4]: 00: Normal 01: 1/2 digital subsample 10: 1/3 digital subsample 11: 1/4 digital subsample Bit[3:0]: Reserved

0ch	***COM0***	8	00h	Bit[7:5]: Reserved Bit[4]: 0: No href when VSYNC DATA=0 1: Always has href, no matter VSYNC DATA=0 or not Bit[3]: 0: No swap, 1: Swap *DAT[9:0] (DAT[0:9]* output to pad[9:0]) Bit[2:0]: Reserved
10h	***VWIN***	8	30h	Bit[7:6]: Reserved Bit[5:4]: High 2 bits of *VSTOP* Bit[3:2]: Reserved Bit[1:0]: High 2 bits of *VSTART*
11h	***PLL_CTR1***	8	31h	Bit[7]: PD_PLL_REG, (PD_PLL=PD_PLL_REG||PDA) 0: PLL normal 1: Power down PLL Bit[5:4]: PLL input divider: Default=11 00: No divided 01: Divided by 2 10: Divided by 3 11: Divided by 4 Bit [3:2] : Reserved Bit[1:0]: PLL output divider: Default=01 00: No divided 01: Divided by 2 10: Divided by 4 11: Divided by 8
12h	***COM7***	8	00h	Bit[7]: SCCB Register Reset 0: Normal 1: Resets all registers to default values Bit[6:2]: Reserved Bit[1]: Process RAW selection {Bit[2],Bit[0]}: Raw RGB Selection. 00: YUV422 01: Bayer RAW 10: RGB565/RGB555/RGB444(use with 0x3a) 11: Process RAW(use with 0x12[1])
13h	***COM8***	8	17h	Bit[7]: Select Y 0: *Y_AVER* 1: Y Average modified value Bit[6]: Digital gain enable 0: Disable 1: Enable Bit[5]: The high bit of *INT_STEP_60* Bit[4]: The high bit of *INT_STEP_50* Bit[3]: Select when to use INTSTEPS 0: When *INT_TIM* lower than *INT_STEP_5060* 1: When *INT_TIM* lower than {*INT_STEP_5060*,1'B0} Bit[2]: AGC Enable. 0: OFF 1: ON Bit[1]: AWB Enable. 0: OFF 1: ON Bit[0]: AEC Enable. 0: OFF 1: ON

15h	***COM1***	8	02h	Bit[7]: Reserved Bit[6]: For output *DAT[9:0]* pad tri-state: 1: Tristate 0: No tri-state Bit[5]: For output VSYNC/HREF pad tri-state: 1: Tristate 0: No tri-state Bit[4]: For output VCLK pad tri-state: 1: Tristate 0: No tri-state Bit[3]: 0: VSYNC IMAGE 1: VSYNC DATA Bit[2]: 0: HREF 1: HSYNC Bit[1]: 0: Output VSYNC DATA/VSYNC IMAGE active low 1: Output VSYNC DATA/VSYNC IMAGE active high Bit[0]: 0: Output hsync/href active high 1: Output hsync/href active low
17h	***HSTART***	8	00h	Window Horizontal start low (high 3bits are in *0x03[2:0]*)
18h	***HSTOP***	8	00h	Window Horizontal stop low (high 3bits are in *0x03[6:4]*)
19h	***VSTART***	8	00h	Window Vertical start low (high 2bits are in *0x10[1:0]*)
1ah	***VSTOP***	8	20h	Window Vertical stop low (high 2bits are in *0x10[5:4]*)
1bh	***PLL_CTR2***	8	3ah	PLL feedback divider: Default=0011 1010 Bit[5:0]: 0xxx00: No divided 0xxx01: Divided by 2 0xxx10,0xxx11: Divided by 3 100000,100001,100010,100011,100100: Divided by 4 100101: Divided by 5 100110: Divided by 6 …… 111110: Divided by 30 111111: Divided by 31
1eh	***MVFP***	8	07h	Mirror/Vflip Enable Bit[7:6]: Reserved Bit[5]: Mirror 0: Normal image 1: Mirror image Bit[4]: Vflip enable 0: Normal image 1: Vertically flip Bit[3:0]: Reserved
21h	***VCLK_CTR***	8	e2h	Bit[7]: 1: VCLK free run 0: VCLK is gated by CKGATE_OUT Bit[6]: Reserved Bit[5]: Output VCLK polarity2 Bit[4]: Output VCLK polarity1 Bit[2:0]: Reserved

23h	***GLGAINREG***	7	33h	GreenGain[2:0]: Bit[6:4]: For even column (used as GreenEgain[2:0]) Bit[3]: Reserved. Bit[2:0]: For odd column (used as GreenOgain[2:0])
24h	***AE_TAR1***	8	82h	Y target value1
25h	***AE_LOC***	8	88h	Bit[7:4]: AE_LOCK_INT Bit[3:0]: AE_LOCK_GLB
27h	***DBLK_AUTO_LOCK***	8	04h	DBLK_AUTO_LOCK
2ah	***EXHCH***	8	0ch	Bit[7:4]: Dummy Pixel Insert MSB Bit[3:0]: Reserved
2bh	***EXHCL***	8	00h	Dummy Pixel Insert LSB, for dummy pixel insert in horizontal direction
33h	***OFFSET_MODE***	8	20h	Reserved
35h	***R_COEF***	8	64h	Lens shading gain of R
36h	***{OFFSET_MODE Y0H_B,X0H_B}***	8	12h	Bit[7]: OFFSET_MODE Bit[6]: Reserved Bit[5:4]: Center Y coordinate MSB for B(vertical center) Bit[3:2]: Reserved Bit[1:0]: Center X coordinate MSB for B(horizontal center)
37h	***Y0L_B***	8	98h	Center Y coordinate LSB for B(vertical center)
38h	***X0L_B***	8	88h	Center X coordinate LSB for B(horizontal center)
39h	***{MAN_OFFSET OFFSET_ME}***	8	a0h	Bit[7]: MAN_OFFSET Bit[6:0]: Manual OFFSET_ME value

3ah	***TSLB***	8	00h	Bit[7:6]: Reserved. Bit[5:0]: When 0x12[2]=1&0x12[0]=0, Bit[5:0] is used for RGB 565/RGB555/RGB444 Sequence: RGB565: 00h: R5G3H,G3LB5 01h: B5G3H,G3LR5 02h: B5R3H,R2LG6 03h: R5B3H,B2LG6 04h: G3HB5,R5G3L 05h: G3LB5,R5G3H 06h: G3HR5,B5G3L 07h: G3LR5,B5G3H 08h: G6B2H,B3LR5 09h: G6R2H,R3LB5 RGB555: 0ah: 1'b0R5G2H,G3LB5 0bh: G3LB5,1'b0R5G2H 0ch: R5G3H,G2LB51'b0 0dh: G2LB51'b0, R5G3H 0eh: B5G3H,G2L1'b0,R5 0rh: R5G3H,G2L1'b0,B5 10h: B51'b0G2H,G3LR5 11h: R51'b0G2H,G3LB5 RGB444: 12h: 4'b0R4,G4B4 13h: G4B4,4'b0R4 14h: 4'b0B4,G4R4 15h: G4R4,4'b0B4 16h: R4G4,B44'b0 17h: B44'b0,R4G4 18h: B4G4,R44'b0 19h: R44'b0,B4G4 1ah: B4G4,R4B4 1Bh: R4G4,B4R4 1ch: R4G2H2'b0,G2LB42'b0 1dh: B4G2H2'b0,G2LR42'b0 1eh: B41'b0G3H,G1L2'b0R41'b0 1fh: R41'b0G3H,G1L2'b0B41'b0 2xh: G1L2'b0B41'b0,R41'b0G3H When 0x12[2]=0&0x12[0]=0, Bit[1:0] is used for YUV422 Sequence: 00: YUYV, 01: YVYU 10: UYVY, 11: VYUY
3bh	***Y_AVER_TH***	7	60h	Y average threshold for auto offset adjust in low light scene
3ch	***OFFSET_TH2***	7	24h	Bit[6:0]: OFFSET_TH2
3eh	***COM5***	8	15h	Bit[7:4]: Reserved Bit[3]: PAD SDA driver capacity: 0: 1X 1: 2X Bit[2:0]: Reserved
3fh	***{OFF_SEL , OFFSET_MO}***	8	a0h	Bit[7]: OFF_SEL Bit[6:0]: Manual OFFSET_MO value
40h	***K0***	8	50h	Gamma Correction Slop Coefficients
41h	***K1***	8	50h	Gamma Correction Slop Coefficients
42h	***K2***	8	58h	Gamma Correction Slop Coefficients
43h	***K3***	8	55h	Gamma Correction Slop Coefficients
44h	***K4***	8	50h	Gamma Correction Slop Coefficients
45h	***K5***	8	4ah	Gamma Correction Slop Coefficients
46h	***K6***	8	44h	Gamma Correction Slop Coefficients
47h	***K7***	8	3eh	Gamma Correction Slop Coefficients
48h	***K8***	8	38h	Gamma Correction Slop Coefficients
49h	***K9***	8	34h	Gamma Correction Slop Coefficients

4ah	***WINDOW SUBSAMPLE***	8	80h	Bit[7:4]: Reserved Bit[3]: 0: Normal output, disable window 1: Enable window Bit[2:0]: Subsample mode 00x: Normal 010: 720P=1288x728 011: XGA=1032x776 100: 4/5 subsample 101: 2/3 subsample 110: 1/2 subsample 111: 1/3 subsample
4bh	***K10***	8	30h	Gamma Correction Slop Coefficients
4ch	***K11***	8	2dh	Gamma Correction Slop Coefficients
4dh	***EDGE_TH***	8	0fh	Bit[7:5]: Reserved Bit[4:0]: Edge threshold
4eh	***K12***	8	28h	Gamma Correction Slop Coefficients
4fh	***K13***	8	24h	Gamma Correction Slop Coefficients
50h	***K14***	8	20h	Gamma Correction Slop Coefficients
51h	***CCM1***	8	0dh	Low 8 bit of Color Correction Matrix Coefficients 1
52h	***CCM2***	8	0eh	Low 8 bit of Color Correction Matrix Coefficients 2
53h	***CCM3***	8	42h	Low 8 bit of Color Correction Matrix Coefficients 3
54h	***CCM4***	8	4ch	Low 8 bit of Color Correction Matrix Coefficients 4
55h	***BRIGHT***	8	00h	Brightness control: Bit[7]: 0: Positive 1: Negative Bit[6:0]: Brightness value
56h	***Y_COEF***	8	40h	Y Coefficient for Contrast
57h	***CCM5***	8	76h	Low 8 bit of Color Correction Matrix Coefficients 5
58h	***CCM6***	8	21h	Low 8 bit of Color Correction Matrix Coefficients 6
59h	***TARGET_H***	8	00h	Bit[7:6]: Reserved Bit[5]: High bit of Color Correction Matrix Coefficients 6 Bit[4]: High bit of Color Correction Matrix Coefficients 5 Bit[3]: High bit of Color Correction Matrix Coefficients 4 Bit[2]: High bit of Color Correction Matrix Coefficients 3 Bit[1]: High bit of Color Correction Matrix Coefficients 2 Bit[0]: High bit of Color Correction Matrix Coefficients 1
5ah	***TARGET_SIGN***	8	16h	Bit[7:6]: Reserved Bit[5]: Sign of Color Correction Matrix Coefficients 6 Bit[4]: Sign of Color Correction Matrix Coefficients 5 Bit[3]: Sign of Color Correction Matrix Coefficients 4 Bit[2]: Sign of Color Correction Matrix Coefficients 3 Bit[1]: Sign of Color Correction Matrix Coefficients 2 Bit[0]: Sign of Color Correction Matrix Coefficients 1
5bh	***FRM_CNT_TH***	8	0ah	F-light Coefficients number1
5ch	***TARGET_ADJ***	8	0eh	Bit[7:6]: Reserved Bit[5:4]: Color space select: 0: BT601 01: BT709 1x: YUV Bit[3:0]: Adjust Coefficients
5eh	***GLB_GAIN_TH***	8	20h	Bit[7]: Reserved; Bit[6:0]: Global gain threshold.
60h	***MA_TH_CTR1***	8	85h	Reserved
61h	***MA_TH_CTR2***	8	48h	Reserved

62h	***COLOR_TEM_TH***	8	07h	Reserved
63h	***TEMP_CNT_SPEED***	8	00h	Reserved
65h	***G_COEF***	8	64h	Lens shading gain of G
66h	***B_COEF***	8	64h	Lens shading gain of B
67h	***MANU***	8	80h	Manual U value
68h	***MANV***	8	80h	Manual V value
69h	***DICOM1***	8	00h	Bit[7]: YCBCR RANGE select 0: YCBCR 0~255 1: Y 16~235, CBCR 16~240 Bit[6]: Negative image enable 0: Normal image 1: Negative image Bit[5]: UV output value select. 0: Output normal value 1: Output fixed value set in MANU and MANV Bit[4:0]: Dither control1
6ah	***DE_GAIN_EN GNGAINREG***	8	01h	Bit[7:3]: Reserved Bit[2:0]:G channel Gain (0x6a[2:0] is used as GreenGain[5:3])
6bh	***CCIR656_COM0***	8	abh	ASAV
6dh	***CCIR656_COM1***	8	80h	AEAV
6eh	***CCIR656_COM2***	8	b6h	SAV
6fh	***DICOM2***	8	20h	Bit[7]: 0: Enable PRE DATFORMAT function 1: Bypass PRE DATFORMAT function Bit[6:0]: Dither control2.
70h	***INT_ED_CTR***	8	01h	Bit[7]: Select Denoise mode Bit[6]: Select Mean value: 0: Less smoothing 1: More smoothing Bit[5:1]: Reserved Bit[0]: Edge enhancement on/off 0: Off 1: On
71h	***EDG_TH_SET***	8	ffh	Reserved
72h	***EDG_TH_CTR***	8	62h	Bit[7:6]: Edge_Gain_P--positive edge enhancement gain 00: 0.5 01: 1.0 10: 1.5 11: 2.0 Bit[5:4]: Edge_Gain_N--negative edge enhancement gain 00: 0.5 01: 1.0 10: 1.5 11: 2.0 Bit[3:0]: Reserved
73h	***ED_OFF_CTR***	8	24h	Reserved

75h	***COL_EF_CTR***	8	00h	Bit[7]: Spe_Eff_En--special effect output on/off 0: Off 1: On Bit[6:4]: Spe_Eff_Sel--special effect choice 011: Sketch 100: Cuprum relievo 101: Blue relievo 110: Black relievo 111: White relievo Default: Normal relievo Bit[3:0]: Reserved
76h	***SOBCTR***	8	90h	Reserved
77h	***SOBMAX***	8	55h	Reserved
78h	***INTCTR***	8	37h	Bit[7:2]: Reserved Bit[1]: Reserved Bit[0]: Low pass filter Switch 0: Off 1: On
79h	***BPCCTR***	8	a6h	Reserved
7ah	***DENCTR***	8	47h	Reserved
7bh	***DAKCTR***	8	0eh	Reserved
7ch	***MACCTR***	8	86h	Reserved
7dh	***BLACTR***	8	80h	Reserved
7eh	***GAICTR***	8	36h	Reserved
80h	***AE_MODE***	8	82h	Bit[7:6]: Reserved Bit[5:4]: G_MIN_SLOPE When *INT_TIM > INT_MAX_MID[2:0]*, gain Coefficients. 00: 0 01: 1 10: 2 11: 3 Bit[3]: RAW_AE 1: Select RawData generate the Y average value 0: Select Ygenerate the Y average value Bit[2]: 1: Digital gain decrease to 3/4 0: Digital gain decrease to 1/2 Bit[1]: 0: Choose 60HZ step 1: Choose 50HZ step. Bit[0]: STEPS_EN when STEPS_EN changes If 0x80[7]=0, AE is adjusted manual
81h	***AE_SPEED***	8	e0h	Bit[7:4]: The speed of adjusting from light to dark Bit[3:0]: The speed of adjusting from dark to light
82h	***GLB_MIND1***	8	23h	GLB_MIN1 low 8 bits, bit[8] is in 0x96[0]
83h	***GLB_MAXD1***	8	4ch	GLB_MAX1 low 8 bits, bit[8] is in 0x96[1]
84h	***GLB_MIND2***	8	34h	GLB_MIN2 low 8 bits, bit[8] is in 0x96[2]
85h	***GLB_MAXD2***	8	62h	GLB_MAX2 low 8 bits, bit[8] is in 0x96[3]
86h	***GLB_MAXD3***	8	99h	GLB_MAX3 low 8 bits, bit[8] is in 0x96[4]
87h	***GLB_GAIN***	8	37h	Global gain register low 8 bits, bit[8] is in 0x96[7]
88h	***Y_AVER***	8	80h	The Y average value of the current frame. **Read Only**
89h	***INT_MAX_MID***	8	07d	Bit[7:3]: Integration time Maximum Bit[2:0]: Integration time mean value.

8ah	***INT_STEP_50***	8	0ah	50HZ Banding Filter STEP low 8 bits, bit[8] is in 0x13[4]
8bh	***INT_STEP_60***	8	deh	60HZ Banding Filter STEP low 8 bits, bit[8] is in 0x13[5]
8ch	***INT_TIM[15:8]***	8	03h	Integration time MSB
8dh	***INT_TIM[7:0]***	8	1eh	Integration time LSB.
8fh	***INT_MIN***	8	82h	Bit[7]: Integration time minimum 0: INT_MIN is 1*step 1: INT_MIN is 0x8f[6:0] Bit[6:0]: INT_MIN Value.
91h	***OFFSET_TH1***	7	1ch	Reserved.
92h	***DM_LNL***	8	02h	Dummy line insert after active line low 8 bits
93h	***DM_LNH***	8	00h	Dummy line insert after active line high 8 bits
94h	***TAR_BASE***	8	02h	TAR_BASE[7:4] is used to adjust the speed of AE TAR_BASE[3:0] is used to control the start of AE
95h	***TAR_BASE1***	8	66h	TAR_BASE1 is used to modify the Y_AVER
96h	***GLB_SEL***	8	00h	Bit[7]: For write/read *GLB_GAIN*[8] Bit[6]: For read *GLB_GAIN*[8] Bit[4]: Use as *GLB_MAX3*[8] Bit[3]: Use as *GLB_MAX2*[8] Bit[2]: Use as *GLB_MIN2*[8] Bit[1]: Use as *GLB_MAX1*[8] Bit[0]: Use as *GLB_MIN1*[8]
97h	***AE_TAR2***	8	78h	Y target value2
98h	***COM1***	8	02h	Bit[7]: Outdoor select Bit[5:4]: WINDOW_SEL 00: 960*600(full) ,256*192(1/2sub) 01: 800*500(full) ,192*144(1/2sub) 10: 640*400(full) ,144*108(1/2sub) 11: 480*300(full) ,108*80 (1/2sub) Bit[2:0]: WEIGHT_SEL 000: 4/8*center+4/8*border 001: 5/8*center+3/8*border 010: 6/8*center+2/8*border 011: 7/8*center+1/8*border 100: Center 100%
99h	***DIG_GAIN***	8	10h	Read or write digital gain (can be written only when *0x13[2]=0*)
9ah	***GLB_GAIN0***	7	1ch,ro	Global gain read value, read only
9bh	***Y0L_G***	8	98h	Center Y coordinate LSB for G(vertical center)
9ch	***X0L_G***	8	88h	Center X coordinate LSB for G(horizontal center)
9dh	***DIG_GAIN_MAX***	8	40h	DIG gain limit
a0h	***AWB_CTR_SET***	8	d0h	Bit[7:2]: Reserved Bit[1:0]: Address ***RGB_AVER*** (0xaf) read select: 00: Read out R average value 01: Read out G average value 10: Read out B average value 11: Read out G average value
a1h	***AWB_TH1_SET***	8	31h	Bit[7:4]: Auto White Balance Lock Boundary Bit[3:0]: AWB Update Speed
a2h	***BLU_GAIN_TH1***	6	0bh	Bit[5:0]: The threshold of blue gain1
a3h	***BLU_GAIN_TH2***	6	20h	Bit[5:0]: The threshold of blue gain2
a4h	***RED_GAIN_TH1***	6	09h	Bit[5:0]: The threshold of red gain1
a5h	***RED_GAIN_TH2***	6	26h	Bit[5:0]: The threshold of red gain2
a6h	***COUNT_EN***	8	04h	AWB criterion: White pixels count threshold, '1' equal to 1024 pixels.

a7h	***BASE_B_GAIN***	8	96h	Bit[7]: Open pure function: 0: Disable 1: Enable Bit[6:5]: Reserved Bit[4:0]: Base B gain
a8h	***BASE_R_GAIN***	8	13h	Bit[7]: Change pure judgement condition: 1: Use cb absolute value and cr absolute value 0: Use cb absolute value, cr absolute value， cb difference value, and cr difference value. Bit[6:5]: Reserved Bit[4:0]: Base R gain
a9h	***AWB_CB_LIM***	8	57h	CB limited
aah	***AWB_CR_LIM***	8	56h	CR limited
abh	***AWB_BR_LIM***	8	16h	CBCR limited
ach	***AWB_Y_LOW***	8	3ch	Y limited1
adh	***AWB_Y_HIG***	8	f0h	Y limited2
aeh	***SKIN_TH_SET***	8	57h	Bit[7:4]: B limit to estimate F light Bit[3:0]: R limit to estimate F light
afh	***RGB_AVER***	8	80h,ro	Read out r/g/b aver value ,use with 0xa0[1:0] ,read only
b0h	***SAT_CTR1***	8	c0h	Saturation control: Bit[7]: Saturation mode 0: Normal 1: Auto. Bit[6:0]: Used as Y pixel threshold for auto saturation.
b1h	***CB_COEF***	8	c6h	Cb Coefficient for Color Saturation
b2h	***CR_COEF***	8	cch	Cr Coefficient for Color Saturation
b3h	***SAT_CTR2***	8	8ch	Bit[7:4]: Used as Y average value threshold for auto saturation. Bit[3:0]: Reserved
b6h	***MAN_R***	8	80h	Define R value
b7h	***MAN_G***	8	80h	Define G value
b8h	***MAN_B***	8	80h	Define B value
bch	***READ_CE Y0H_R,X0H_R***	8	12h	Bit[7:6]: Reserved Bit[5:4]: Center Y coordinate MSB for R(vertical center) Bit[3:2]: Reserved Bit[1:0]: Center X coordinate MSB for R(vertical center)
bdh	***Y0L_R***	8	98h	Center Y coordinate LSB for R(vertical center)
beh	***X0L_R***	8	88h	Center X coordinate LSB for R(horizontal center)
bfh	***RD_OE Y0H_G,X0H_G***	8	12h	Bit[7:6]: Reserved Bit[5:4]: Center Y coordinate MSB for G(vertical center) Bit[3:2]: Reserved Bit[1:0]: Center X coordinate MSB for G(horizontal center)
c0h	***XY_HCTR***	8	00h	Bit[7]: Scaling Mode--scaling on/off 0: Off 1: On Bit[6:4]: High bits of image's width after scaling Bit[3:2]: Reseverd Bit[1:0]: High bits of image's length after scaling
c1h	***XL_CTR***	8	00h	Bit[7:0]: Low bits of image's width after scaling
c2h	***YL_CTR***	8	00h	Bit[7:0]: Low bits of image's length after scaling
c3h	***S_MCTR***	8	00h	Bit[7:0]: Minification of image's width
c4h	***S_NCTR***	8	00h	Bit[7:0]: Minification of image's length
c8h	***BLUE_GAIN_LOW_OUT***	6	0dh	Bit[5:0]: The threshold1 of blue gain
c9h	***BLUE_GAIN_HIG_OUT***	6	20h	Bit[5:0]: The threshold2 of blue gain

cah	***H_START_L***	8	00h	When SUBSAMPLE[3]=1(in window mode), X WINDOW START COORDINATE[7:0]
cbh	***H_END_L***	8	10h	When SUBSAMPLE[3]=1(in window mode), X WINDOW END COORDINATE[7:0]
cch	***H_ADD_H***	8	50h	In window mode: Bit[7]: Reserved Bit[6:4]: X WINDOW END COORDINATE[10:8] Bit[2:0]: X WINDOW START COORDINATE[10:8]
cdh	***V_START_L***	8	00h	In window mode, Y WINDOW START COORDINATE[7:0]
ceh	***V_END_L***	8	30h	In window mode, Y WINDOW END COORDINATE[7:0]
cfh	***V_ADD_H***	6	30h	In window mode: Bit[5:4]: Y WINDOW END COORDINATE[9:8] Bit[3:2]: Reserved Bit[1:0]: Y WINDOW START COORDINATE[9:8]
d0h	***F_OFFSET***	8	00h	Reserved
d1h	***NF_OFFSET***	8	00h	Reserved
d3h	***RED_GAIN_LOW_OUT***	6	09h	Bit[5:0]: The threshold1 of red gain
d4h	***RED_GAIN_HIG_OUT***	6	20h	Bit[5:0]: The threshold2 of red gain
ddh	***Y_LS0***	8	00h	Bit[7]: Reserved Bit[6:4]: Bottom left LS1,**Read Only** Bit[3]: Reserved Bit[2:0]: Bottom left LS0,**Read Only**
deh	***Y_LS1***	8	00h	Bit[7]: Reserved Bit[6:4]: Bottom right LS3, **Read Only** Bit[3]: Reserved Bit[2:0]: Bottom center LS2,**Read Only**
dfh	***LS_REG,Y_LS2***	8	00h	Bit[7:3]: Reserved Bit[2:0]: Bottom right LS4, **Read Only**
e3h	***DM_ROWL***	8	05h	Dummy line insert before active line low 8 bits
e4h	***DM_ROWH***	8	00h	Dummy line insert before active line high 8 bits
eeh	***P_TH***	8	4ch	Skin probability threshold
f1h	***ISPBYPASS***	8	00h	Bit[7]: Contrast enable 0: Enable 1: Disable Bit[6]: Saturation enable 0: Enable 1: Disable Bit[5]: Color Correction and Color Space conversion enable 0: Enable 1: Disable Bit[4]: Color Correction enable 0: Enable 1: Disable Bit[3]: Color Interpolation and Edge enhancement enable 0: Enable 1: Disable Bit[2]: Bad pixel and Denoise enable 0: Enable 1: Disable Bit[1]: Gamma Correction enable 0: Enable 1: Disable Bit[0]: Lens Correction enable 0: Enable 1: Disable
f2h	***HUE_COS***	8	7fh	Hue cosine coefficient, range -1~0.99(0x80~0x7f) Bit[7]: 0, positive, 1: negative. Bit[6:0]: Value.
f3h	***HUE_SIN***	8	00h	Hue sine coefficient range -1~0.99(0x80~0x7f) Bit[7]: 0, positive, 1: negative. Bit[6:0]: Value.
f8h	***CCIR656_COM3***	8	9dh	EAV

f9h	***CCIR656_COM4***	8	00h	Bit[7]: 0: Normal 1: CCIR656 enable Bit[6]: 0: Normal 1: Odd data change with even data in blank Bit[5]: 0: Data in blank is 8010 1: Data in blank is 0000 Bit[4]: CCIR mode1 Bit[3]: CCIR mode2 Bit[1]: 0: No data when blank 1: Has data when blank Bit[0]: 0: No data when Hblank/Vblank 1: No data when Hblank
fch	***PID_BME***	8	37h	Product ID MSB. **Read Only**
fdh	***VER_BME***	8	10h	Product ID LSB. **Read Only**

8. Package Specifications

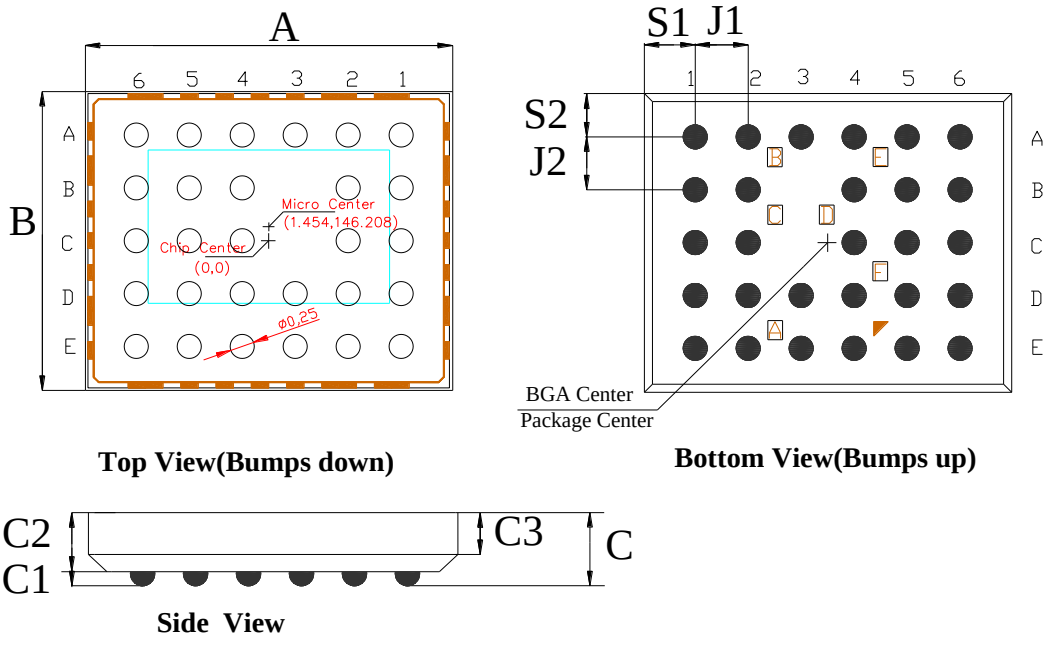


Figure 8. CSP dimension description

Table 6. CSP Dimensions

	Symbol	Nominal	Min	Max
		μm		
Package Body Dimension X	**A**	3769	3744	3794
Package Body Dimension Y	**B**	3079	3054	3104
Package Height	**C**	745	685	805
Ball Height	**C1**	130	100	160
Package Body Thickness	**C2**	615	580	650
Thickness from top glass surface to wafer	**C3**	435	415	455
Ball Diameter	**D**	250	220	280
Total Ball Count	**N**	28		
Ball Count X axis	**N1**	6		
Ball Count Y axis	**N2**	5		
Pins Pitch X axis	**J1**	550		
Pins Pitch Y axis	**J2**	550		
Edge to Pin Center Distance along X	**S1**	510	480	540
Edge to Pin Center Distance along Y	**S2**	440	410	470

Table 7. Ball Matrix Table

	1	2	3	4	5	6
A	VSSA	VSSIO	D9	D8	D7	VDDIO
B	VDD3A	VSYNC	/	D6	D5	VSSD
C	SCL	SDA	/	D2	D3	D4
D	VDD3A	D0	D1	RSTB	HSYNC	VDDD
E	VSSA	VSSD	VCLK	PDN	XCLK	VDDL

Table 8. Pin Descriptions

PIN Num.	PIN Name	PIN Type	Function/Description
A1	VSSA	PWR/GND	Analog ground
A2	VSSIO	PWR/GND	I/O ground
A3	D9	Output	YUV image data output port [7]/RGB image data output port [9]
A4	D8	Output	YUV image data output port [6]/RGB image data output port [8]
A5	D7	Output	YUV image data output port [5]/RGB image data output port [7]
A6	VDDIO	PWR/GND	I/O Power supply (1.7~3.1V)
B1	VDD3A	PWR/GND	Analog power supply（2.7V~3.1V）
B2	VSYNC	Output	Vsync output
B4	D6	Output	YUV image data output port [4]/RGB image data output port [6]
B5	D5	Output	YUV image data output port [3]/RGB image data output port [5]
B6	VSSD	PWR/GND	Digital ground
C1	SCL	Input	Two wire serial interface clock input
C2	SDA	Input	Two wire serial interface data I/O

C4	D2	Output	YUV image data output port [0]/RGB image data output port [2]
C5	D3	Output	YUV image data output port [1]/RGB image data output port [3]
C6	D4	Output	YUV image data output port [2]/RGB image data output port [4]
D1	VDD3A	PWR/GND	Analog power supply（2.7V~3.1V）
D2	D0	Output	RGB image data output port [0]
D3	D1	Output	RGB image data output port [1]
D4	RSTB(1)*	Input	Reset Input: 0:Reset; 1:Normal
D5	HSYNC	Output	Hsync output
D6	VDDD(2)*	PWR/GND	Digital Power supply(1.4V~1.6V)
E1	VSSA	PWR/GND	Analog ground
E2	VSSD	PWR/GND	Digital ground
E3	VCLK	Output	Video clock output
E4	PDN(3)*	Input	Power Down Control: 0: Normal 1: Power down
E5	XCLK	Input	System clock input
E6	VDDL(4)*	PWR/GND	LDO power supply(1.7~3.1V)

Note:
(1)* Represents an internal pull-up resistor.
(2)* Sholud be floating when VDDL is used.
(3)* Represents an internal pull-down resistor.
(4)* Sholud be floating when VDDD is used.

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