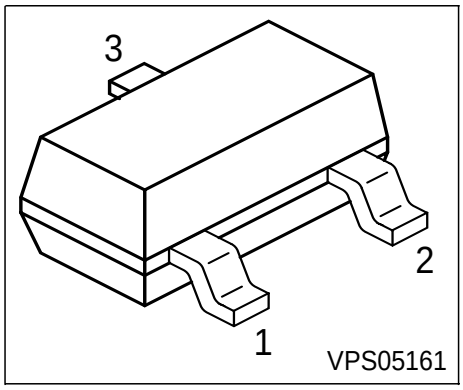
Silicon N-Channel MOSFET Triode

- For high-frequency stages up to 300 MHz preferably in FM applications
- I_{DSS} = 4mA, g_{fs} = 12mS



ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precaution!

Type	Marking	Pin Configuration			Package
BF543	LDs	1 = G	2 = D	3 = S	SOT23

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	20	V
Drain current	I_D	30	mA
Gate-source peak current	$\pm I_{GSM}$	10	
Total power dissipation, $T_S \leq 76$ °C	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	°C
Ambient temperature range	T_A	-55 ... 150	
Channel temperature	T_{ch}	150	

Thermal Resistance

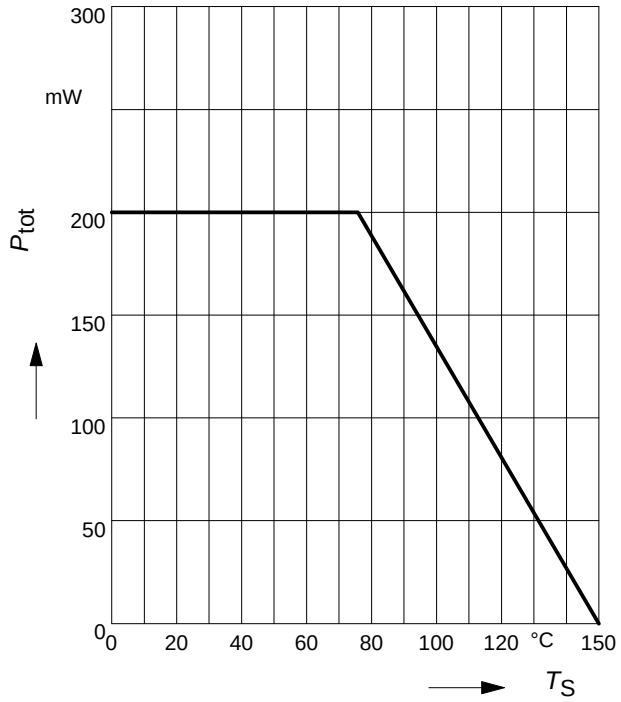
Channel - soldering point[1)]	R_{thchs}	≤370	K/W

[1)]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

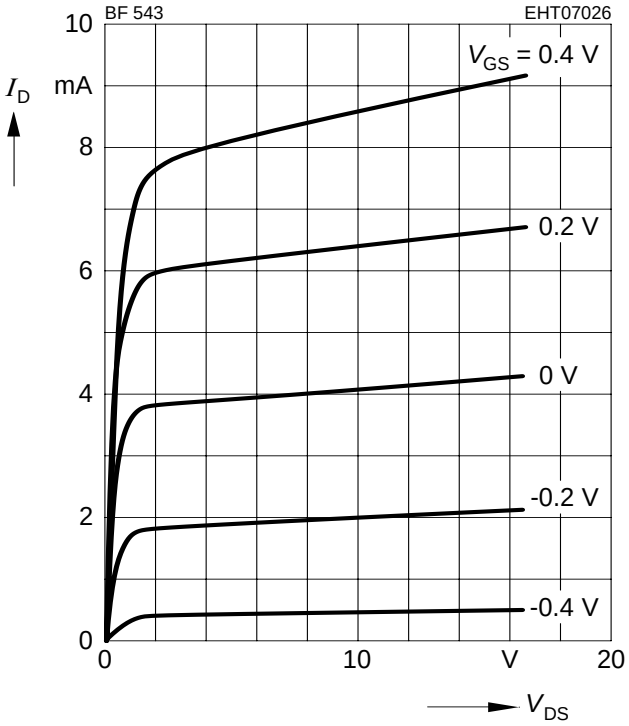
Electrical Characteristics at T_A = 25 °C, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC characteristics					
Drain-source breakdown voltage I_D = 10 µA, - V_{GS} = 4 V	$V_{(BR)DS}$	20	-	-	V
Gate-source breakdown voltage ± I_{GS} = 10 mA, V_{DS} = 0	± $V_{(BR)GSS}$	7	-	12	
Gate-source leakage current ± V_{GS} = 6 V, V_{DS} = 0	± I_{GSS}	-	-	50	nA
Drain current V_{DS} = 10 V, V_{GS} = 0	I_{DSS}	2	4	6	mA
Gate-source pinch-off voltage V_{DS} = 10 V, I_D = 20 µA	- $V_{GS\ (p)}$	-	0.7	1.5	V
AC characteristics					
Forward tranconductance V_{DS} = 10 V, I_D = 4 mA	g_{fs}	9.5	12	-	mS
Gate input capacitance V_{DS} = 10 V, I_D = 4 mA, f = 1 MHz	C_{gss}	-	2.7	-	pF
Reverse tranfer capacitance V_{DS} = 10 V, I_D = 4 mA, f = 1 MHz	C_{dg}	-	18	-	fF
Output capacitance V_{DS} = 10 V, I_D = 4 mA, f = 1 MHz	C_{dss}	-	0.9	-	pF
Power gain (test circuit) G_G = 2mS, G_L = 0,5 mS V_{DS} = 10 V, I_D = 4 mA, f = 200 MHz	G_p	-	22	-	dB
Noise figure (test circuit) G_G = 2mS, G_L = 0,5 mS V_{DS} = 10 V, I_D = 4 mA, f = 200 MHz	F	-	1	-	

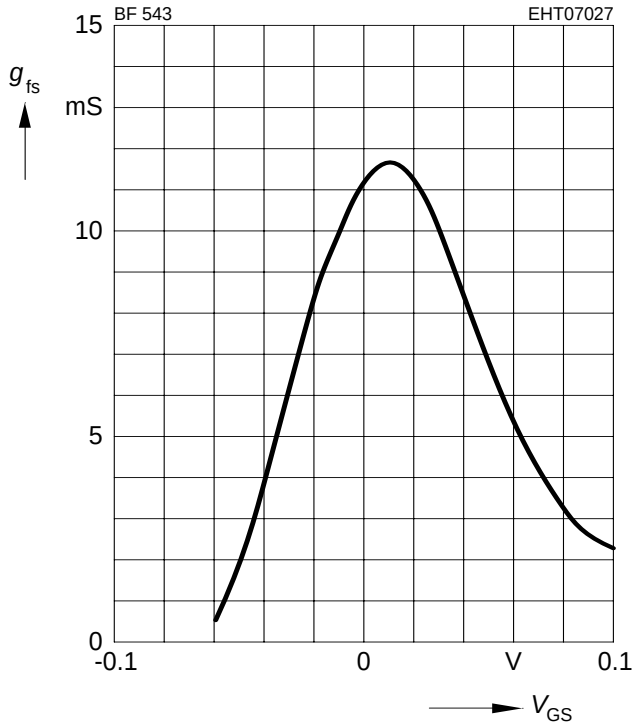
Total power dissipation $P_{tot} = f(T_S)$



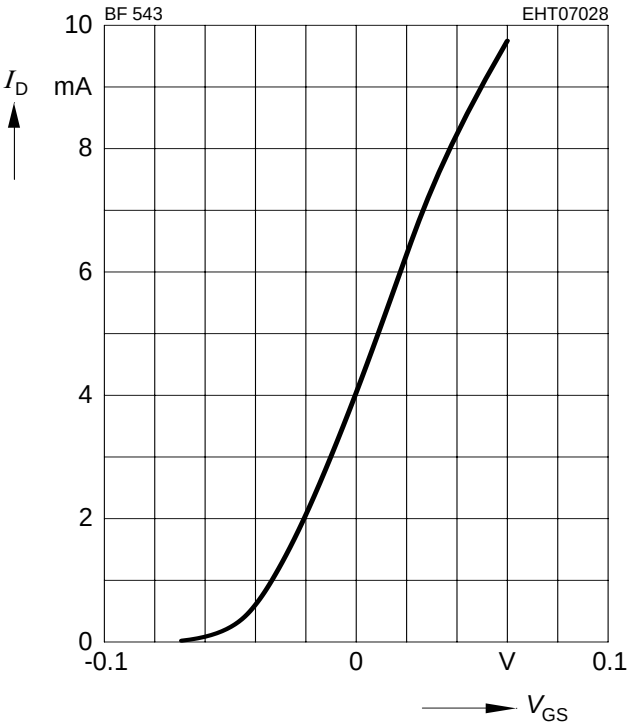
Output characteristics $I_D = f(V_{DS})$



Gate transconductance $g_{fs} = f(V_{GS})$
V_{DS} = 10, I_{DSS} = 4mA, f = 1kHz

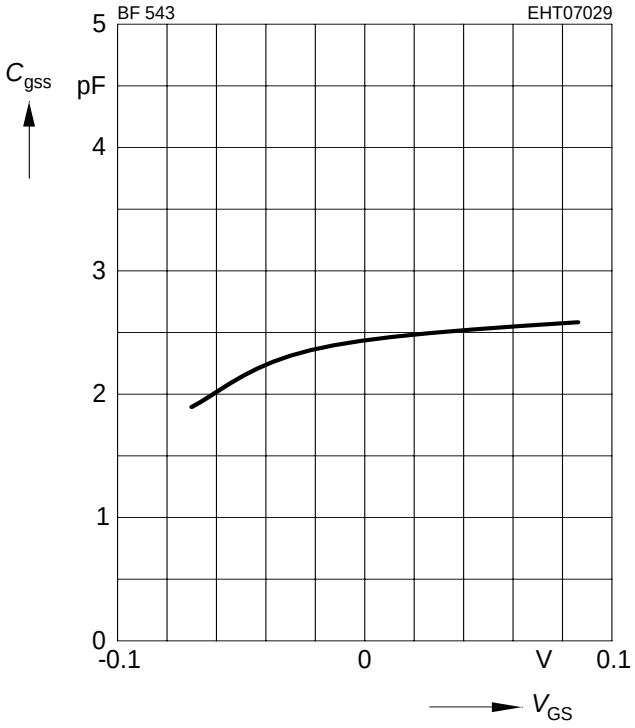


Drain current $I_D = f(V_{GS})$
V_{DS} = 10V



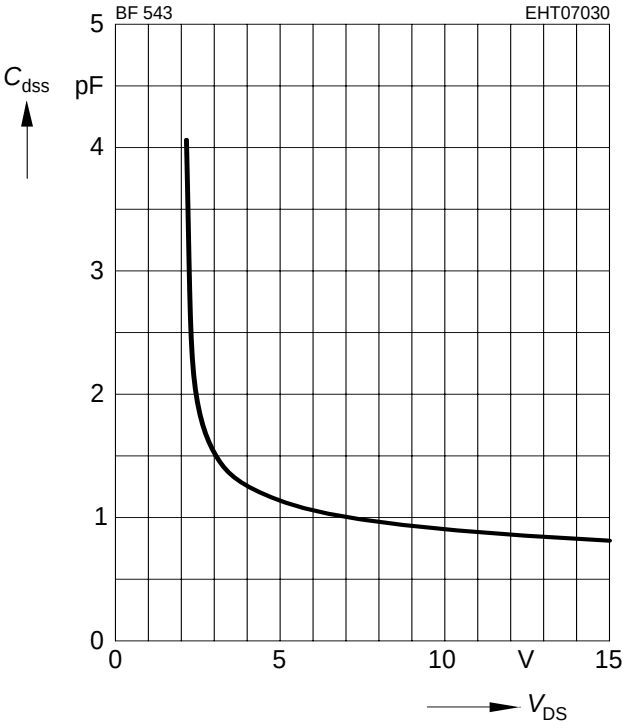
Gate input capacitance $C_{gss} = f(V_{GS})$

V_{DS} = 10, I_{DSS} = 4mA, f = 1MHz



Output capacitance $C_{dss} = f(V_{DS})$

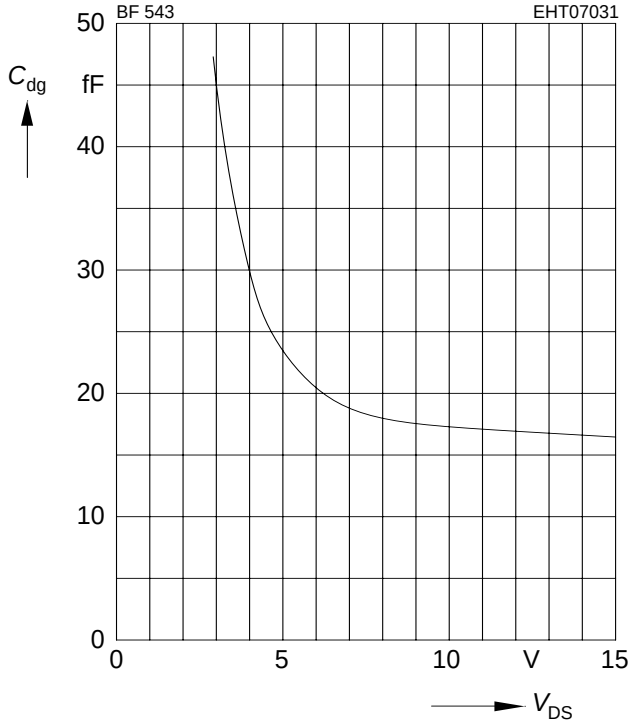
V_{GS} = 0, I_{DSS} = 4mA, f = 1MHz



Reverse transfer capacitance

$C_{dg} = f(V_{DS})$

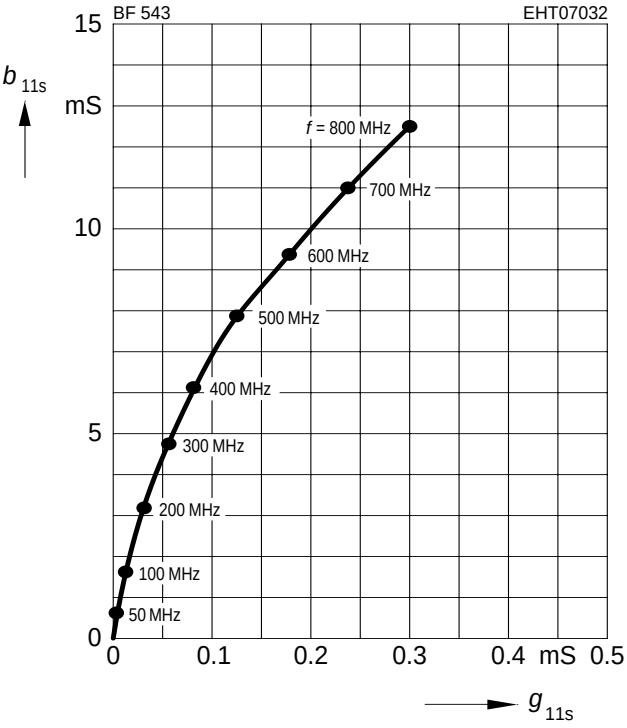
V_{GS} = 0, I_{DSS} = 4mA, f = 1MHz



Gate input admittance y_{11s}

V_{DS} = 10, I_{DSS} = 4mA, V_{GS} = 0

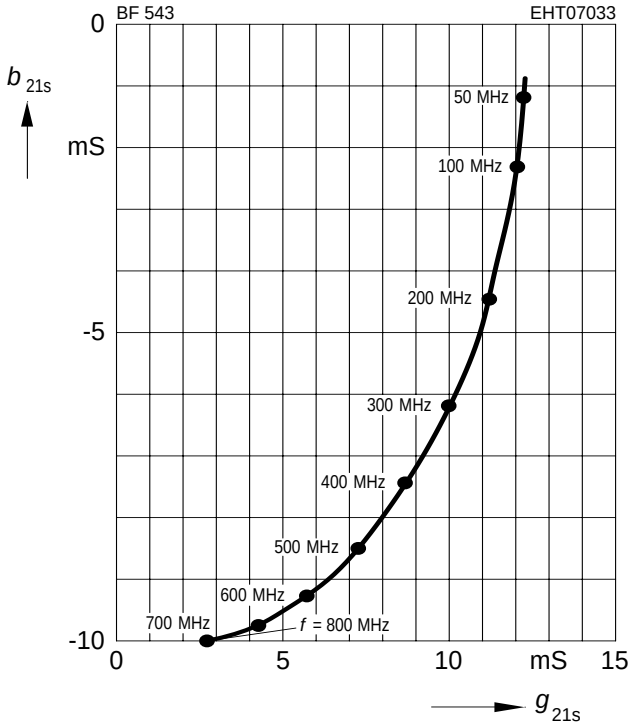
(source circuit)



Gate forward transfer admittance y_{21s}

V_{DS} = 10V, I_{DSS} = 4mA, V_{GS} = 0

(source circuit)



Output admittance y_{22s}

V_{DS} = 10V, I_{DSS} = 10mA, V_{GS} = 0

(source circuit)