BF6921A Datasheet

8/16-Channel Capacitive TouchKey Controller

Product Preview

Reversion 1.0

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1. SPECIFICATION

1.1 Features

- Number of Keys
  —From 1 to 8/16 keys
- LP(low power) Mode
  — Variable low power mode: Idle Mode or Sleep Mode
- Versatile Interfaces Available
  - SPI
  - I^2C:（standard mode or fast mode）
  - UART
- Selectable Key Mode
  — Each key can operate in a mode individually
- Supply Voltage: 2.7~5.5V
- Wide IO Voltage Range: 1.65~5.5V
- Insensitive to Environment Variations
- Operation Mode
  —Interrupt mode or query mode
- Key Sensitivity
  — Individual sensitivity can be set by interface
- On-chip Automatic Calibration Logic
  — Optional speed for self-calibration
- HBM ESD : ±2000V
- Package type: QFN24/QFN40/SOP30

1.2 Applications

- White Home Application
- Mobile/Portable Device
- Smart Phone
- Control Device
- Game Controller
- Remote Controller
- Computer & Peripheral

2. INTRODUCTION

The BF6921A is a digital controller which is capable of detecting near-proximity or touch based on capacitive touch electrodes up to eight/sixteen. It offers designers a cost-efficient alternative to mechanical keys anywhere a mechanical switch, slider or wheel could be found. It could also support to realize the function of LED driver.

Each of the eight/sixteen keys operates independently, and each can be tuned for a different sensitivity simply by giving commands to the corresponding specified registers.

The device uses a SPI and I^2C selectable interface to communicate with the host and a DAV signal is used to indicate the host of status changes.

The BF6921A contains MCU core whose frequency is up to 32MHz and other several peripherals are also include; its block diagram is shown as follows:

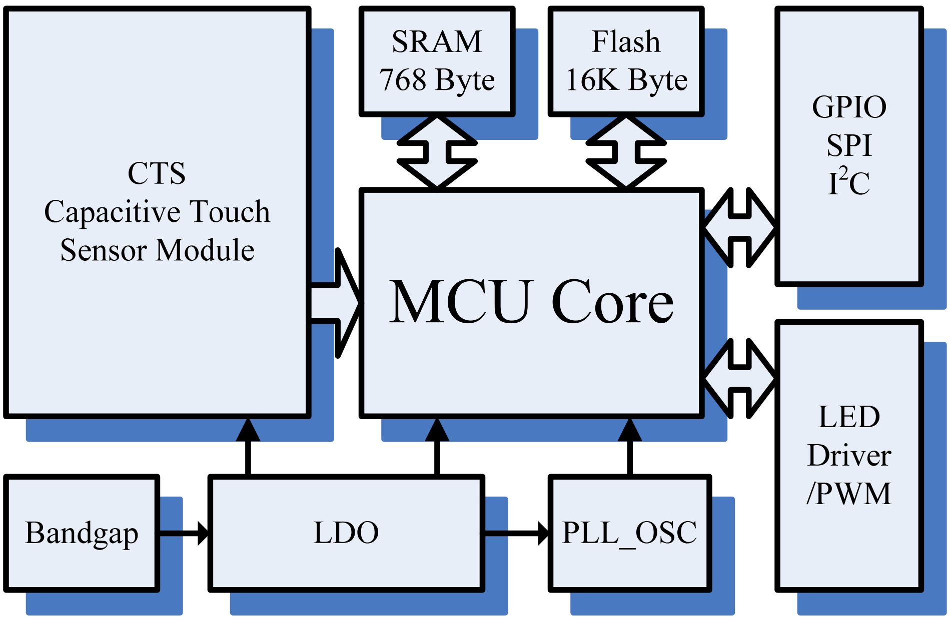


Figure 1 BF6921A Block Diagram

3. HARDWARE INTERFACE

This chapter provides descriptions for capacitive sensor Standard Interface. Interface protocol is intended to be used for data transfer between a touch sensor device and a host device. The protocol is designed for fast and easy communication, giving minimal overhead to the host device by adopting interrupt signaling scheme as default.

While protocol is designed to be operating over I^2C and SPI interface.

3.1 I^2C Timing Specification

As a human interface device (HID), the TS (short for Touch Sensor) device is required to support the following actions of the host device:

- Read data from TS device

• Send configure command to TS device

In the application of I²C interface implementation, the host device can be a single MCU that act as an I²C bus master. As the following figure depicts, the host CPU, as a master, together with a TS device consist of an I²C system.

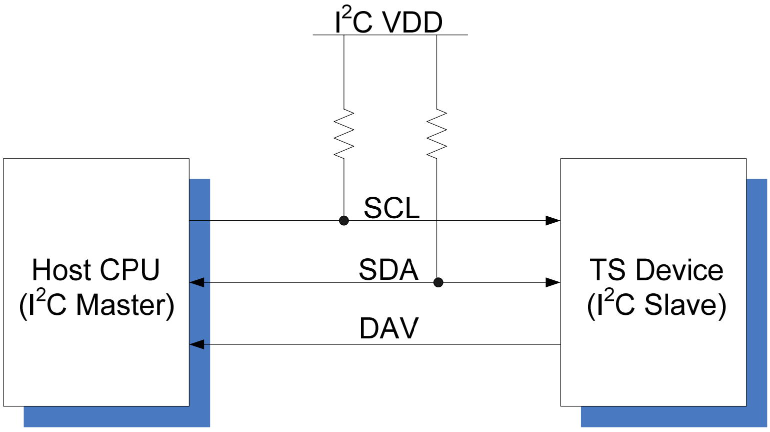


Figure 2 I²C Application

The bus between the host device and the TS device is composed of by a serial clock (SCL) line and a serial data (SDA) line, and also a DAV (interrupt) line. The DAV line is used to giving an interrupt signal to the host device. It functions as an indication for Master device that there is touch-related information available in TS device, such as touch-on or leave-off states and the coordinate of the touch-point.

As soon as receiving a DAV signal, the host device identifies the TS device by its I²C slave address. If a TS device connecting to the I²C bus, there would be a 7-bits I²C slave address, whose format is 11000xx. Also, under the situation that multiple TS devices are connected to the I²C bus, they could be accessed separately by different I²C slave addresses.

SS_ADD1	SDO_ADD0	I²C Address
0	0	1100 000
0	1	1100 001
1	0	1100 010
1	1	1100 011

Table 1 BF6921 Device Address

The lower two bits are set or cleared by tying the SS_ADD1 and SDO_ADD0 pins high or low.

3.1.1 Register Write Packet

In order to write a register of the TS device, the host device should send a packet with a corresponding register address. The basic format of a register write packet transmitted over I²C bus is illustrated as Figure 3. The I²C Header shown in the figure consists of an I²C slave address for the TS device and an R/W bit = 0.

Start	Device Address (W)	ACK	Register Address	ACK	Register Value	ACK	Stop

Figure 3 I²C Single Register Write Packet

As an extension to a single register access with a single register write packet, consequence register write can also be supported. Consequence register write is used for writing a series of registers with consecutive addresses. In this consequence register write mode, as shown in Figure 4, host only need to write the first address of the series registers, and then to write each value to each register corresponding to register sequence. After the start address is written, the register address counter is automatically added in the TS device every access to the register.

Start	Device Address (W)	ACK	Register Address(n)	ACK	Register Value to Reg(n)	ACK	Register Value to Reg(n+1)	ACK	…	Register Value to Reg(m)	ACK	Stop

Figure 4 I²C Multiple Register Write Packet

From Master to Slave   From Slave to Master

3.1.2 Register Read Packet

Reading register values is similar to writing register. Host writes a specific register address and extracts the corresponding register value from the TS device. The basic register read packet format over I²C bus is as shown as Figure 5.

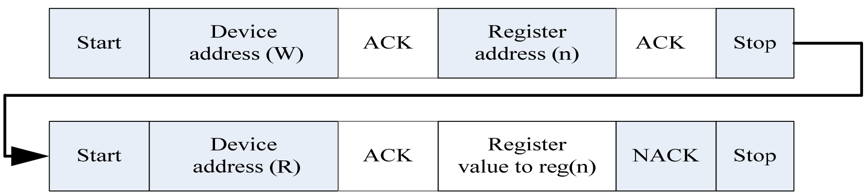


Figure 5 I²C Single Register Read Packet

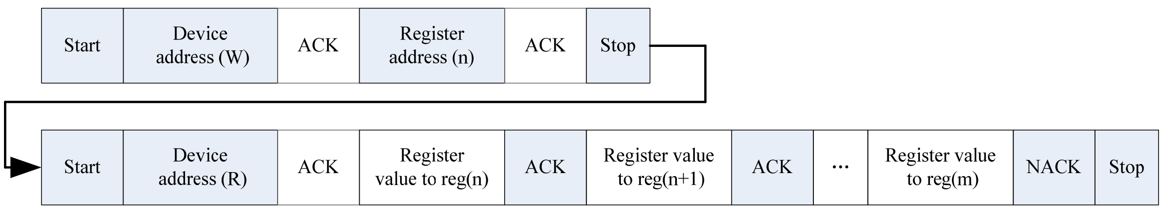


Figure 6 I²C Multiple Register Read Packet

For the situation of reading multiple register values from a series of registers having consequent register addresses at once, host can use consequence register read mode to access. (See Figure 6) In this mode, host first write a start register address and then repeats register reading without additional address adding. This feature is implemented by automatic register address increasing logic in the TS device.

3.2 SPI Timing Specifications

The BF6921A can also communicate via a standard SPI bus. The BF6921A SPI supports full-duplex, synchronous, serial communication with a master processor (the master). The SPI master generates the synchronized clock and establishes a transmission. The SPI slave devices will not start and synchronize transmissions until the Master starts a transmission.

The transmission starts once initiated by a master SPI. The byte from the master SPI begins to shift in on the slave SDI (MOSI—master out, slave in) pin under the control of the master serial clock. As the byte shifts in on the SDI (MOSI) pin, a byte will be shifted out on the SDO (MISO—master in, slave out) pin to the master.

When idle, the clock stays at high level. The falling edge of SCK is used to transmit output (MISO) data and the rising edge of SCK is used to latch input (MOSI) data. Eight clocks are needed for one byte communication and the SS (slave select) signal must stay low during the whole communication process.

Standard SPI Signal Names	BF6921A SPI Signal Names
SS (Slave Select)	SS_ADD1 (Slaver Select)
SCK (Serial Clock)	SCK_SCL (Serial Clock)
MISO (Master In Slave Out)	SDO_ADD0 (Serial Data Out)
MOSI (Master Out Slave In)	SDI_SDA (Serial Data In)

Table 2　Standard SPI Signal Names VS BF6921A SPI Signal Names

Start(7bits) 1010110	R/W (1 bit)	Register Address (8bits)	Register value (8bits)

Table 3　SPI Interface Timing Format

Bit D [23:17]: The bit must be set to 1010110 to successfully begin a bus transaction.

Bit D [16]: R/W bit. The “1” is for reading from register, and “0” for writing to register.

Bit D [15:8]: Register Address.

Bit D [7:0]: Register Value will be written to register.

Bit d [7:0]: Register value read from register.

3.2.1 Register Write Packet

The Command Byte with Write Bit is used to access the internal registers. It uses the D6 and D1 (Register Address) to control the flow of data. After the Command Byte with Write Bit, it is followed by 8-bits Configuration Register. Byte 3, Byte 4, Byte 5 will also be sent though in write mode(R/W=0), and these three bytes are insignificant. Please See Figure 7.

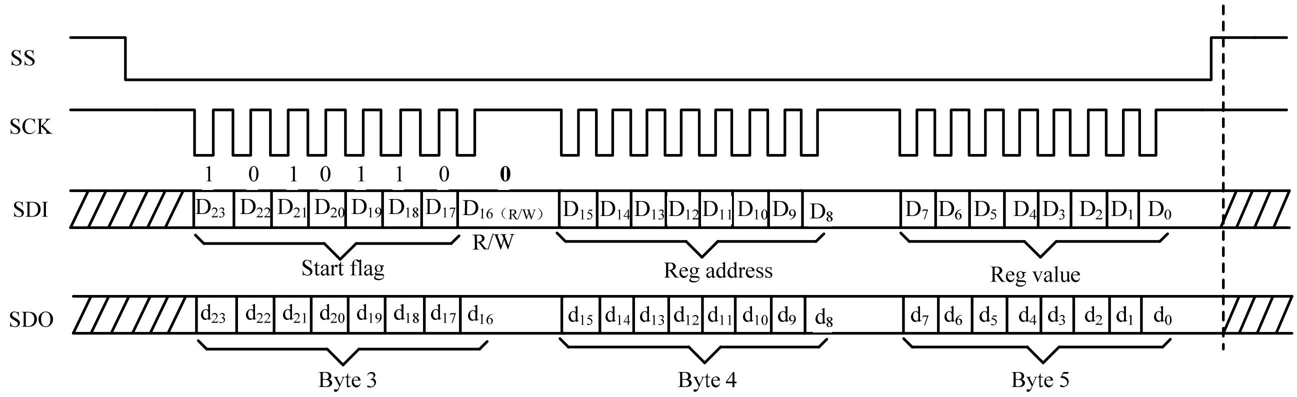


Figure 7　SPI Write Internal Register

So, the data coming from SDI (MOSI) will be written to the register corresponding address bits in the Configuration Register.

3.2.2 Register Read Packet

Register read packet is shown in Figure 8. First, the SPI master sends Start flag (1010110) and R/W (1) bit followed with a Reg address, and then BF6921A will send Reg value corresponding to specified Reg address on the SDO line. Byte 2, Byte 3, Byte 4, will also be sent in read mode (R/W=1), but they are insignificant.

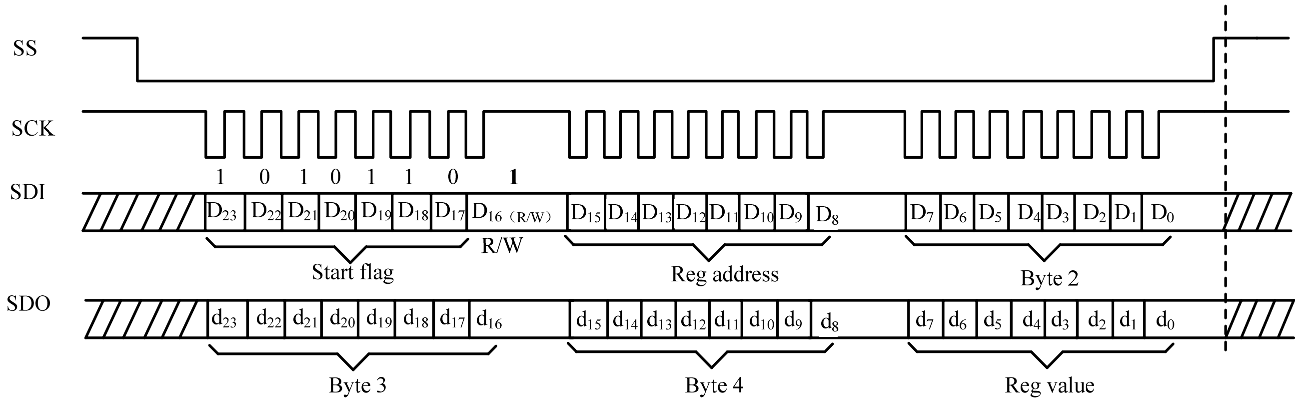


Figure 8　SPI Read Internal Register

4. WORK MODES TRANSITION

BF6921A is composed of three work modes, which could be chosen for different situations.

Active Mode: BF6921A operates normally;

Idle Mode: A timer will be made to work in this mode, which could be called the name WDT module. The interval time countered by WDT can be set by idle time register, once WDT start to work; and most modules in BF6921A will not work at this interval time. Capacitance detect module will start to work to detect whether touch happens when the interval time finished. After some frames' scanning, capacitance detect module will stop working if any touch don't happen. The process will loop in this operation mode.

Sleep Mode: SLEEP_MODE≠0 will make BF6921A enter the sleep mode. Any external interrupt signal will wake it up.

The following figure shows the transition relationship of the three modes.

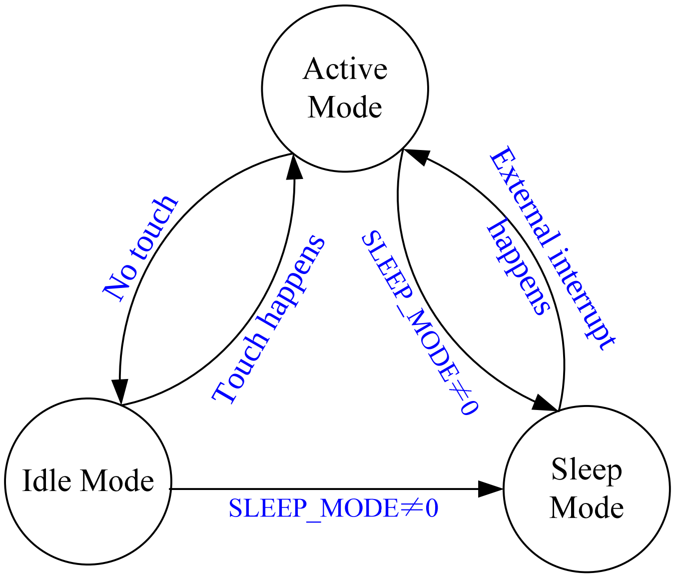


Figure 9 Work Modes Transition

5. INTERRUPT AND QUERY MODE

The TS device supports both interrupt mode and query mode. As explained above, DAV line is used to generate interrupt signal, and every time DAV signal received, the host device may initiate data extraction via I^2C bus. When operated in the query mode, however, the TS device transmits most updated data whenever the host device accesses TS device via I^2C to extract data. In this query mode, the host could request for touch-related information to the TS device at any time. The TS device can be configured as interrupt modes or query mode by programming corresponding Register.

5.1 Interrupt Mode

In the interrupt mode, the TS device indicates the host device by sending DAV signal whenever there is updated information to transmit. DAV line works as a interrupt signal. When an input event occurs, e.g., touch-on/leave-off state changing, the DAV line is pull down by the TS device to give out interrupt signal, which implies that there is information to be transmitted in corresponding the input event. Once touch-on is detected, the TS device continually asserts INTR signal at a regular interval until leave-off is detected. By extracting data from the TS device at every instance the DAV line pull-down is detected, the host device can always obtain the most updated information corresponding to user input.
In the default setting, DAV line is used as an active-low manner. This means that the INTR line remains 'high' until user input is applied to the TS device. But when the user input is detected and the TS device is prepared to transmit more updated data to the host, it starts pulling down DAV signal. The DAV will not pull high until no touch is ever detected.

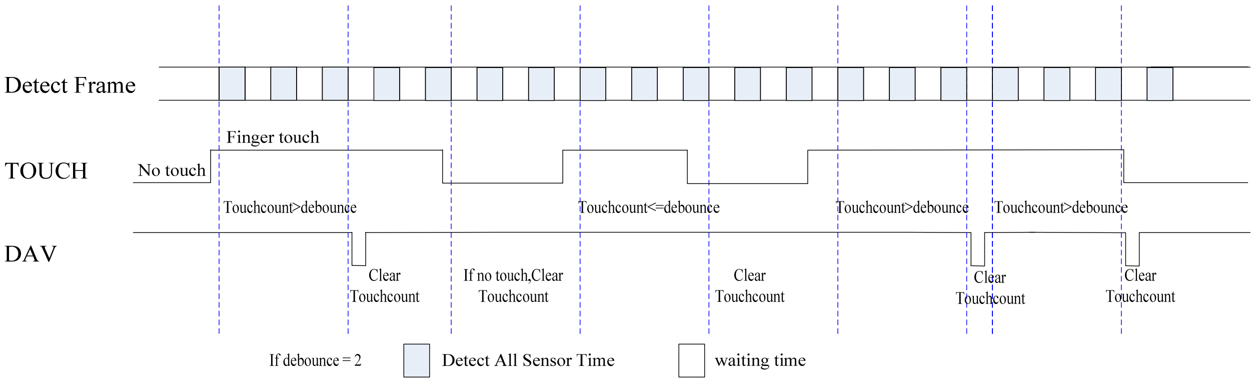


Figure 10 Interrupt Mode Finger Status and DAV

It should be noted in Figure 10 that DAV line is pull down once touch count>debounce. This is to make sure that the touch count of finger touch must exceed the value of debounce which implies the least times of available touch. Otherwise, DAV will not be pull down even if touch happens, when touch count<debounce.
The DAV signal is also generated when the gesture recognition features is turned on and any supported type of gesture input is recognized by monitoring a series of touch events. Supported types of gesture movements will be outputted according to each gesture model in TS device after getting the touch number and complexity of the requested gesture inputs.

5.2 Query Mode

In the query mode, host can freely access the TS device's registers at any moment for input information. While operating in the query mode, DAV line of the TS device is maintained 'high'. Included in the input information being transmitted in the query mode is touch state information indicating whether or not the user's touch is being applied to the TS device and the type of input, such as a single touch input, a multi-touch input, or various kinds of gesture inputs.

6. REGISTERS MAP

6.1 Overview

The BF6921A has the capability to implement a lot of applications by providing a series of registers. The values of these registers are written to the device over the SPI or I^2C serial interfaces.
This usual register access method simplifies the implementation of communication interface to the host, thus greatly reducing communication time, efforts and other resources needed for development.

Register Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value	Type
00h	MID	manufacture ID code								00h	R
01h	Module Revision	Module Revision								00h	R
02h	Firmware Version	Firmware Version								00h	R

03h	Reserved										
04h	Reserved										
05h	Reserved										
06h	Reserved										
07h	Reserved										
08h	Reserved										
09h	Reserved										
0Ah	Reserved										
0Bh	Operating Mode	Interrupt Mode/query mode								00h	R/W
0Ch	Idle Time	Reserved				IDIT				00h	R/W
0Dh	Sleep Mode	SLEEP_MODE								00h	R/W
0Eh	Resolution	Reserved				RESO				00h	R/W
0Fh	Touch debounce	Reserved				TD				00h	R/W
10h	Reference calibration speed	Reserved				RCS				00h	R/W
11h	Voltage reference	CSD_RV								00h	R/W
12h	Shield Enable	SHIELD_EN								00h	R/W
13h	Reserved									00h	
14h	Reserved									00h	
15h	Reserved									00h	
16h	Reserved									00h	
17h	Reserved									00h	
18h	Reserved									00h	
19h	Reference Always Calibration	RAC								00h	R/W
1Ah	Detect Speed	Reserved						CSD_DS		00h	R/W
1Bh	Key Mode	KEY 3	KEY 3	KEY 2	KEY 2	KEY 1	KEY 1	KEY 0	KEY 0	00h	R/W
1Ch		KEY 7	KEY 7	KEY 6	KEY 6	KEY 5	KEY 5	KEY 4	KEY 4	00h	R/W
1Dh		KEY 11	KEY 11	KEY 10	KEY 10	KEY 9	KEY 9	KEY 8	KEY 8	00h	R/W
1Eh		KEY 15	KEY 15	KEY 14	KEY 14	KEY 13	KEY 13	KEY 12	KEY 12	00h	R/W
1Fh	Key Enable	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0	FFh	R/W
20h		KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	FFh	R/W
21h-30h	Noise Threshold1~16	NTHRD								00h	R/W
31h	DAV Mask	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0	00h	R/W
32h		KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	00h	R/W
33h-42h	Touch Threshold1~16	TTHRD								00h	R/W
43h	Register Key1 Raw Data	MSB OF KEY DATA								00h	R
44h		LSB OF KEY DATA								00h	R

45h	Register Key2 Raw Data	MSB OF KEY DATA	00h	R
46h		LSB OF KEY DATA	00h	R
47h	Register Key3Raw Data	MSB OF KEY DATA	00h	R
48h		LSB OF KEY DATA	00h	R
49h	Register Key4 Raw Data	MSB OF KEY DATA	00h	R
4Ah		LSB OF KEY DATA	00h	R
4Bh	Register Key5 Raw Data	MSB OF KEY DATA	00h	R
4Ch		LSB OF KEY DATA	00h	R
4Dh	Register Key6 Raw Data	MSB OF KEY DATA	00h	R
4Eh		LSB OF KEY DATA	00h	R
4Fh	Register Key7Raw Data	MSB OF KEY DATA	00h	R
50h		LSB OF KEY DATA	00h	R
51h	Register Key8 Raw Data	MSB OF KEY DATA	00h	R
52h		LSB OF KEY DATA	00h	R
53h	Register Key9 Raw Data	MSB OF KEY DATA	00h	R
54h		LSB OF KEY DATA	00h	R
55h	Register Key10 Raw Data	MSB OF KEY DATA	00h	R
56h		LSB OF KEY DATA	00h	R
57h	Register Key11 Raw Data	MSB OF KEY DATA	00h	R
58h		LSB OF KEY DATA	00h	R
59h	Register Key12 Raw Data	MSB OF KEY DATA	00h	R
5Ah		LSB OF KEY DATA	00h	R
5Bh	Register Key13 Raw Data	MSB OF KEY DATA	00h	R
5Ch		LSB OF KEY DATA	00h	R
5Dh	Register Key14 Raw Data	MSB OF KEY DATA	00h	R
5Eh		LSB OF KEY DATA	00h	R
5Fh	Register Key15 Raw Data	MSB OF KEY DATA	00h	R
60h		LSB OF KEY DATA	00h	R
61h	Register Key16 Raw Data	MSB OF KEY DATA	00h	R
62h		LSB OF KEY DATA	00h	R
63h	Error status	Error ID	60h	R
64h	Position	Position	00h	R
65h	Channel Status	Channel 7~0	00h	R
66h		Channel 15~8	00h	R

Table 4　Summarizes Registers

6.2 Register Description

MID Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	MID							

8 bits manufacture ID code

Module Revision Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	Module Revision							

The Module Revision Register provides the hardware revision information of TS device module, which is often used while in the test or development period. The value of this register is updated at every hardware revision.

Firmware Version Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	Firmware Version							

The Firmware Version Register provides version information of the firmware that is embedded in the current TS device module. This register may be referred to during the test or development period, as well as when downloading firmware to the sensor IC.

Firmware Version [bit7~bit0]
N: Firmware Version Number

Operation Mode Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	Interrupt Mode/query mode							

Writing a nonzero value to this address leads the device into query mode.

Idle Time Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	Reserved					IDIT		

The IDIT defines the interval between key measurements. A longer value yields longer intervals that result in lower power consumption at the expense of slower response time.

IDIT	Interval
000	16ms
001	32ms
010	64ms
011	128ms
100	256ms
101	512ms
110	1024ms
111	2048ms
…	Reserved

SLEEP Mode Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Dh	SLEEP_MODE							

Writing a nonzero value to this address leads the device into sleep mode.

Resolution Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Eh	Reserved					RESO		

The RESO indicates the resolution of key data and reference data. Using a larger value of RESO can enhance the sensitivity of detection at the expense of lower sample rate.

RESO	Content
000	7bits
001	8bits
010	9bits
011	10bits
100	11 bits
101	12 bits
110	13 bits
111	14 bits

Touch Debounce Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	Reserved					TD		

TD defines the number of consecutive times a key must be confirmed as having passed the touch threshold before the key is registered as being touched. This mechanism can effectively suppress noisy signals (ESD, supply spikes), and provide reliable touch detection under various conditions. A value of 0 means no debouncing.

TD	Content
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Reference Calibration Speed Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	Reserved					RCS		

The RCS defines the reference data calibration speed for accommodating the environment. The smaller the value set, the faster the calibration speed.
000: Highest Calibration Speed Level
111: Lowest Calibration Speed Level

Voltage Reference Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11h	Reserved					CSD_RV		

The register set the reference voltage, when reference voltage increases the sensitivity is decreased.
000: Lowest Voltage Reference Level
111: Highest Voltage Reference Level

Shield Enable Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
12h	SHIELD_EN							

Writing a nonzero value to this address leads the device to Enable shield function. With this register, the host can enable or disable anti-water function.

Reference Always Calibration Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19h	RAC							

Writing a nonzero value to this address leads the device into reference always calibration mode.

Detect Speed Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Ah	Reserved						CSD_DS	

The DS is used to improve SNR. Using a higher value helps improve SNR at the expense of lower sample rate when situated in a noisy environment.
Default: 0.

Key Mode Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Bh	KEY3	KEY 3	KEY 2	KEY 2	KEY 1	KEY 1	KEY 0	KEY 0
1Ch	KEY7	KEY 7	KEY 6	KEY 6	KEY 5	KEY 5	KEY 4	KEY 4
1Dh	KEY11	KEY11	KEY10	KEY10	KEY9	KEY9	KEY8	KEY8
1Eh	KEY15	KEY15	KEY14	KEY14	KEY13	KEY13	KEY12	KEY12

The two registers are used to set the mode information of each key. See Section 5.4 on page for more information of each group.
Default: 0x00, 0x00

Value	Content
00	Group 0
01	Group 1
10	Group 2
11	Group 3

BF6921A allows each key to be set to an individual group from group 0 to group 3. Each group has its own function independent of another group:
Group 0: If a key is set to group 0, each key can be reported as being touched whenever it is touched.
Group 1: If a key is set to group 1, only one key of group 1 can be reported as being touched at any one time.
Group 2: If a key is set to group 2, only one key of group 2 can be reported as being touched at any one time.
Group 3: If a key is set to group 3, each key can be reported as being touched whenever it is touched. In addition, the keys of group 3 compose a slider/wheel and the position of the slider/wheel will be reported if it is touched.

Key Enable Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Fh	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
20h	KEY15	KEY14	KEY13	KEY12	KEY11	KEY10	KEY9	KEY8

These bits control the availability of each key. A 1 allows the corresponding key to be detected, a 0 prevents

the corresponding key from being detected. Though floating some keys also can disable them, setting their corresponding bits to 0 can increase sample rate.
Default: 0xFF

Noise Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
21h~30h	NTHRD							

Register orderly define the noise threshold from key 0 to key 15.
BF6921A figures the influence of noise effectively by the value of NTHRD.
Default: 0x20

DAV Mask Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
31h	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
32h	KEY15	KEY14	KEY13	KEY12	KEY11	KEY10	KEY9	KEY8

These bits control whether a change in corresponding key of each bit causes the DAV request. A 1 means the change causes the RDYN request, a 0 means the change doesn't cause the DAV request.
Default: 0xFF

Touch Threshold Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
33h-42h	TTHRD							

Register 24 – 31 orderly define the Touch Threshold from key 0 to key 15.
TTHRD set the threshold value for each key to register a touch.
Default: 0x30

Register Key Raw Data

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43h-62h	MSB OF KEY DATA							
	LSB OF KEY DATA							

Register allow key data to be orderly read for each key from key 0 to key 15. There are two registers for each key, the first register stores the MSB of key data and the second register stores the LSB of key data.

Error ID Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
63h	Reserved				ERID			

The Error ID Register provides a property value of each type of device error state. The host can refer to this register to check the device state. The Error ID Register is set by BF6921A and clears by host.
Here lists Error ID and its corresponding meaning.

Error ID	Content
0x02	Power on reset/Brown out reset
0x01	MCLR Occurred/ Watchdog Occurred
0x00	No error (default)

Position Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
64h	Position							

The Position Register provides the slider or wheel coordinate information of current input.

Channel State Register

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
65h	Ch15	Ch 14	Ch13	Ch12	Ch11	Ch10	Ch9	Ch8
66h	Ch7	Ch 6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

Each bit indicates the information of its corresponding channel. Bit ‘1’ means that the channel has been touched, otherwise, bit ‘0’ means the channel has not been touched.

7. DEVICE DESCRIPTION

Three packages could be chose for different applications, such as QFN24 for 8key, QFN40 or SOP30 for 16key.

7.1 BF6921A8

7.1.1 BF6921A8 QFN24 Package

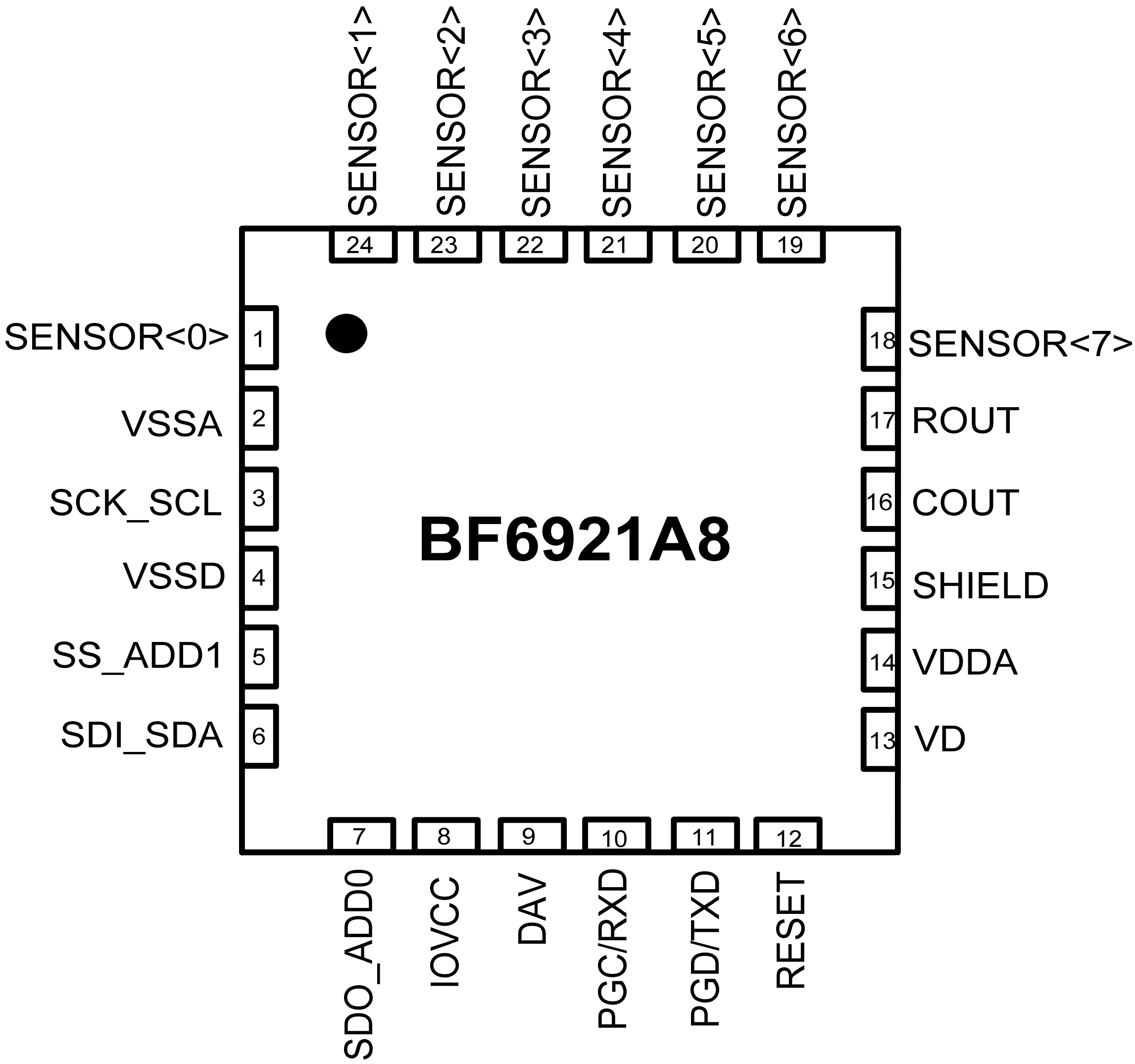


Figure 11 BF6921A 8KEY QFN24 Package

7.1.2 BF6921A8 QFN24 Pin Description

Pin No.	Symbol	Function Description	If Unused
1	SENSOR<0>	Capacitive touch sensor channel.	Open
2	VSSA	Analog ground	
3	SCK_SCL	GPIO The Clock in/output of SPI/I^{2}C	
4	VSSD	Digital ground	
5	SS_ADD1	GPIO The Slave select signal of SPI ADD1 in I^{2}C mode	Open
6	SDI_SDA	GPIO The SPI Data Out or I^{2}C Data I/O	
7	SDO_ADD0	GPIO The SPI Data Out ADD0 in I^{2}C mode	Open
8	IOVCC	Power IO supply:1.65~5.5V	
9	DAV	GPIO Signal of data ready to be available Interrupt Input (INT)	
10	PGC/RXD	Serial Programming Clock (PGC) Uart port data input (RXD)	Open
11	PGD/TXD	Serial Programming Data (PGD) Uart port data output (TXD)	Open
12	RESET	Reset signal. Default: high. When reset=0, BF6921A is reset.	
13	VD	Internal LDO output. Core voltage 2.5V	
14	VDDA	Power supply:2.7~5.5V	
15	SHIELD	Connected to the shield electrode.	Open
16	COUT	Connected to Capacitance.	
17	ROUT	Connected to Resistance.	
18	SENSOR<7>	Capacitive touch sensor channel.	Open
19	SENSOR<6>	Capacitive touch sensor channel.	Open
20	SENSOR<5>	Capacitive touch sensor channel.	Open
21	SENSOR<4>	Capacitive touch sensor channel.	Open
22	SENSOR<3>	Capacitive touch sensor channel.	Open
23	SENSOR<2>	Capacitive touch sensor channel.	Open
24	SENSOR<1>	Capacitive touch sensor channel.	Open

Note: “-” indicates the pin must be used for operation.

Table 5 BF6921A8 QFN24 Pin Description

7.2 BF6921A16

7.2.1 BF6921A16 QFN40 Package

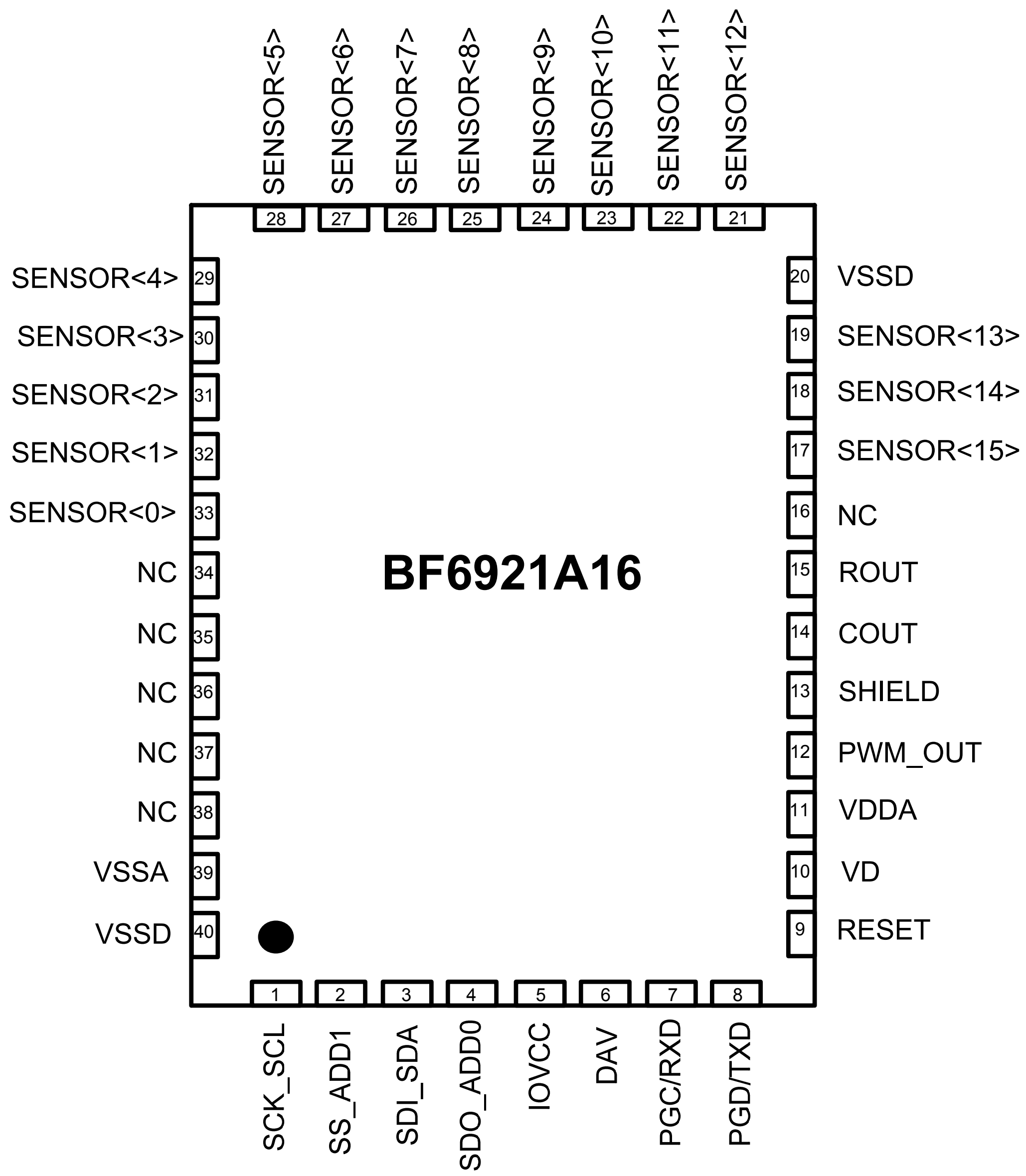


Figure 12 BF6921A 16KEY QFN40 Package

7.2.2 BF6921A16 QFN40 Pin Description

Pin No.	Symbol	Function Description		If Unused
1	SCK_SCL	GPIO	The Clock in/output of SPI/I^{2}C	
2	SS_ADD1	GPIO	The Slave select signal of SPI ADD1 in I^{2}C mode	Open
3	SDI_SDA	GPIO	The SPI Data Out or I^{2}C Data I/O	
4	SDO_ADD0	GPIO	The SPI Data Out ADD0 in I^{2}C mode	Open

5	IOVCC	Power IO supply:1.65~5.5V	
6	DAV	GPIO Signal of data ready to be available Interrupt Input (INT)	
7	PGC/RXD	Serial Programming Clock (PGC) Uart port data input (RXD)	Open
8	PGD/TXD	Serial Programming Data (PGD) Uart port data output (TXD)	Open
9	RESET	Reset signal. Default: high. When reset=0, BF6921A is reset.	
10	VD	Internal LDO output. Core voltage 2.5V	
11	VDDA	Power supply:2.7~5.5V	
12	PWM_OUT	PWM output.	Open
13	SHIELD	Connected to the shield electrode.	Open
14	COUT	Connected to Capacitance.	
15	ROUT	Connected to Resistance.	
16	NC	NOT CONNECTED.	Open
17	SENSOR<15>	Capacitive touch sensor channel.	Open
18	SENSOR<14>	Capacitive touch sensor channel.	Open
19	SENSOR<13>	Capacitive touch sensor channel.	Open
20	SENSOR<12>	Capacitive touch sensor channel.	Open
21	VSSD	Digital ground.	
22	SENSOR<11>	Capacitive touch sensor channel.	Open
23	SENSOR<10>	Capacitive touch sensor channel.	Open
24	SENSOR<9>	Capacitive touch sensor channel.	Open
25	SENSOR<8>	Capacitive touch sensor channel.	Open
26	SENSOR<7>	Capacitive touch sensor channel.	Open
27	SENSOR<6>	Capacitive touch sensor channel.	Open
28	SENSOR<5>	Capacitive touch sensor channel.	Open
29	SENSOR<4>	Capacitive touch sensor channel.	Open
30	SENSOR<3>	Capacitive touch sensor channel.	Open
31	SENSOR<2>	Capacitive touch sensor channel.	Open
32	SENSOR<1>	Capacitive touch sensor channel.	Open
33	SENSOR<0>	Capacitive touch sensor channel.	Open
34	NC	NOT CONNECTED.	Open
35	NC	NOT CONNECTED.	Open
36	NC	NOT CONNECTED.	Open
37	NC	NOT CONNECTED.	Open
38	NC	NOT CONNECTED.	Open
39	VSSA	Analog ground.	
40	VSSD	Digital ground.	

Note: “-” indicates the pin must be used for operation.

Table 6 BF6921A16 QNF40 Pin Description

7.2.3 BF6921A16 SOP30 Package

Figure 13 BF6921A 16KEY SOP30 Package

7.2.4 BF6921A16 SOP30 Pin Description

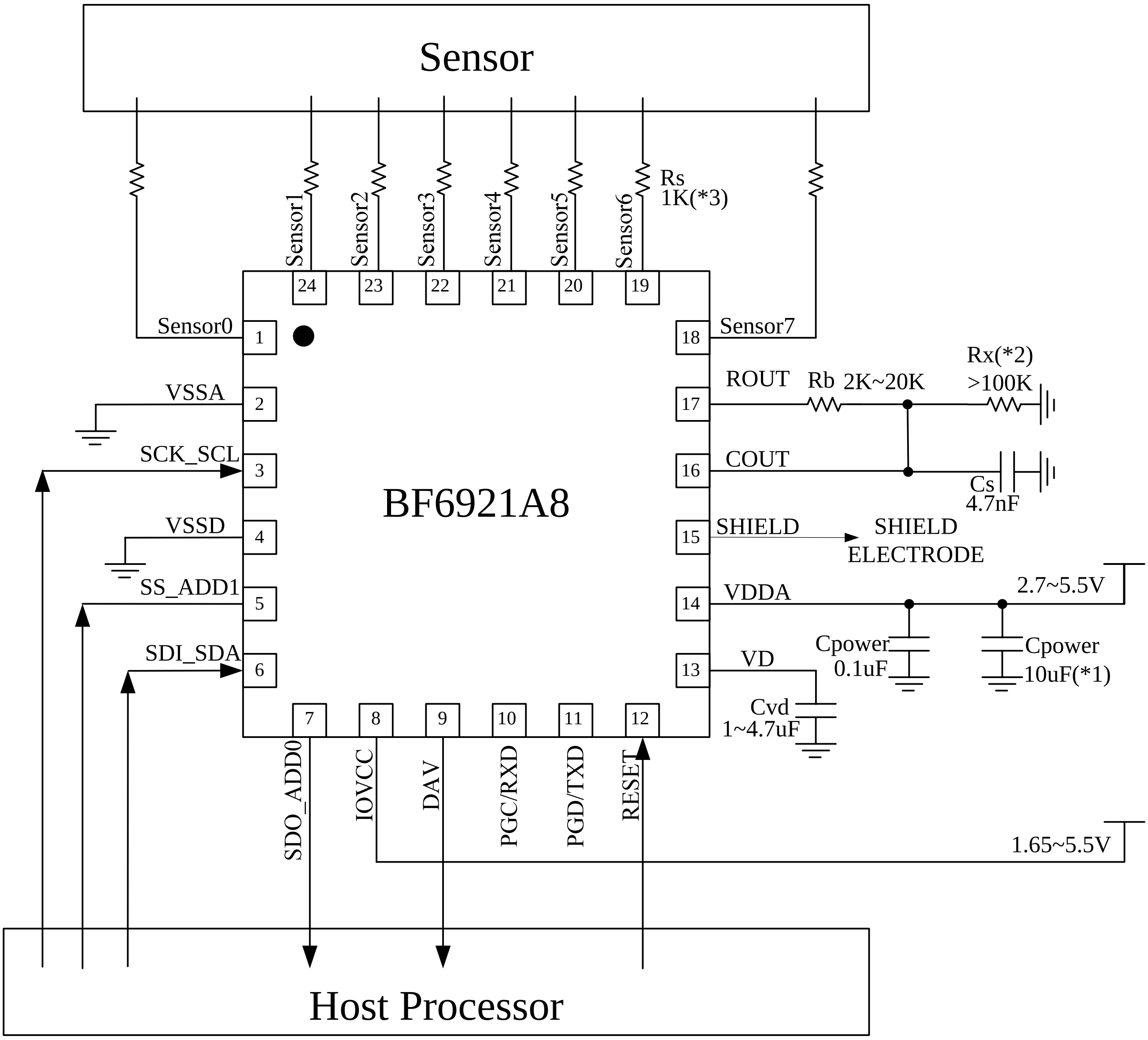
Pin No.	Symbol	Function Description	If Unused
1	PGC/RXD	Serial Programming Clock (PGC) Uart port data input (RXD)	Open
2	PGD/TXD	Serial Programming Data (PGD) Uart port data output (TXD)	Open
3	GPIO<0>	General purpose IO	Open
4	DAV	GPIO Signal of data ready to be available Interrupt Input (INT)	
5	RESET	Reset signal. Default: high. When reset=0, BF6921A is reset.	
6	VD	Internal LDO output. Core voltage 2.5V	
7	VDDA	Power supply:2.7~5.5V	
8	PWM_OUT	PWM output.	Open
9	COUT	Connected to Capacitance.	
10	ROUT	Connected to Resistance.	
11	SENSOR<15>	Capacitive touch sensor channel.	Open
12	SENSOR<14>	Capacitive touch sensor channel.	Open
13	SENSOR<13>	Capacitive touch sensor channel.	Open
14	SENSOR<12>	Capacitive touch sensor channel.	Open
15	SENSOR<11>	Capacitive touch sensor channel.	Open
16	SENSOR<10>	Capacitive touch sensor channel.	Open
17	SENSOR<9>	Capacitive touch sensor channel.	Open
18	SENSOR<8>	Capacitive touch sensor channel.	Open
19	SENSOR<7>	Capacitive touch sensor channel.	Open
20	SENSOR<6>	Capacitive touch sensor channel.	Open
21	SENSOR<5>	Capacitive touch sensor channel.	Open
22	SENSOR<4>	Capacitive touch sensor channel.	Open
23	SENSOR<3>	Capacitive touch sensor channel.	Open
24	SENSOR<2>	Capacitive touch sensor channel.	Open
25	SENSOR<1>	Capacitive touch sensor channel.	Open
26	SENSOR<0>	Capacitive touch sensor channel.	Open
27	VSS	Ground.	
28	SCK_SCL	Clock port of I^2C	
29	SDI_SDA	Data port of I^2C	
30	IOVCC	Power IO supply:1.65~5.5V	

Note: “-” indicates the pin must be used for operation.

Table 7 BF6921A16 SOP30 Pin Description

7.3 Application Circuit

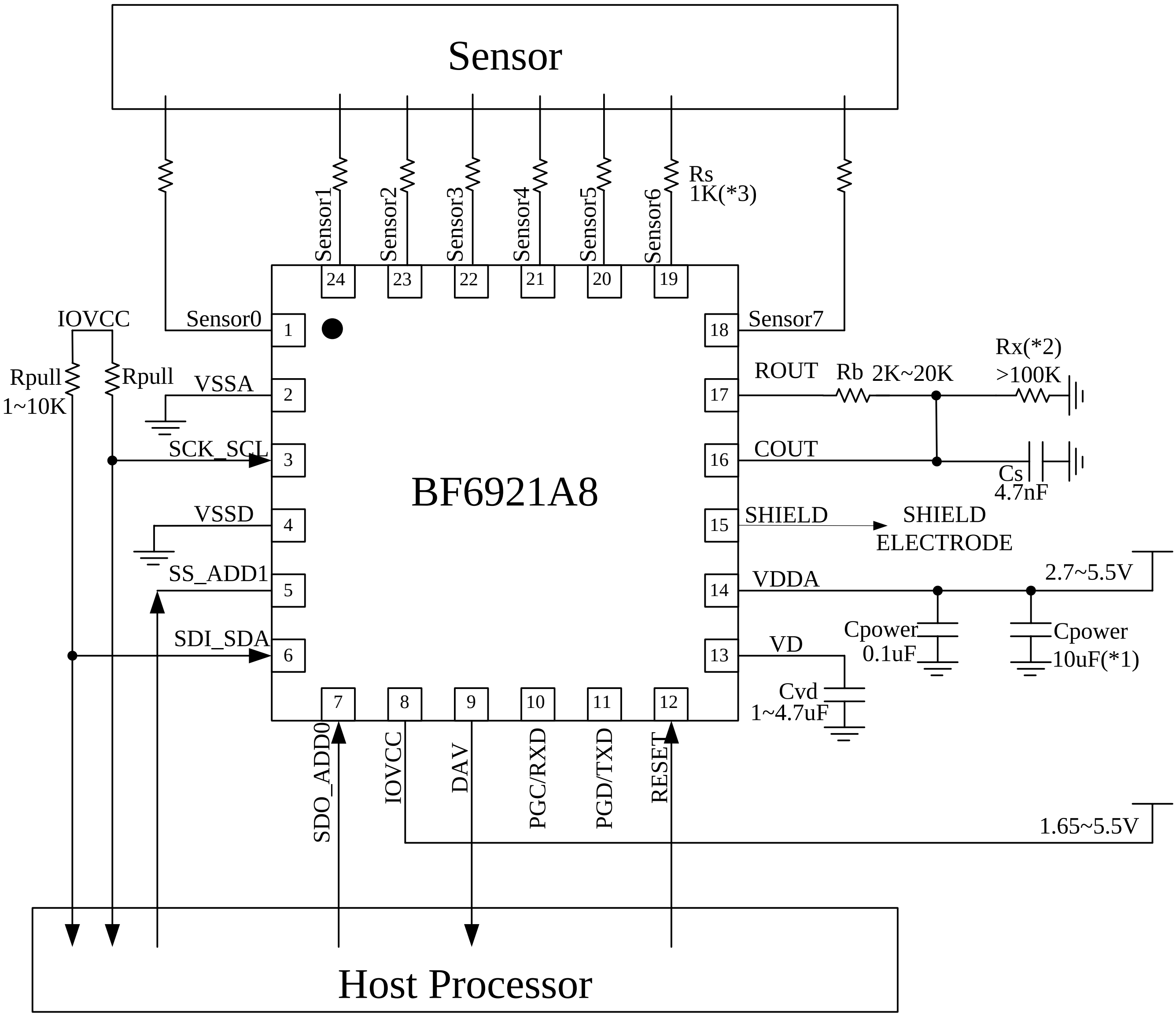
7.3.1 BF6921A8 SPI Application



Note: *1、Value of Cap determined by current situation
*2、Rx could be chosen in some situations to eliminate noise
*3、Rs could be used to decrease some noise brought by EMI
*4、IOVCC could be connected with VDDA together under 2.7~5.5V

Figure 14 8KEY Application Circuit with SPI

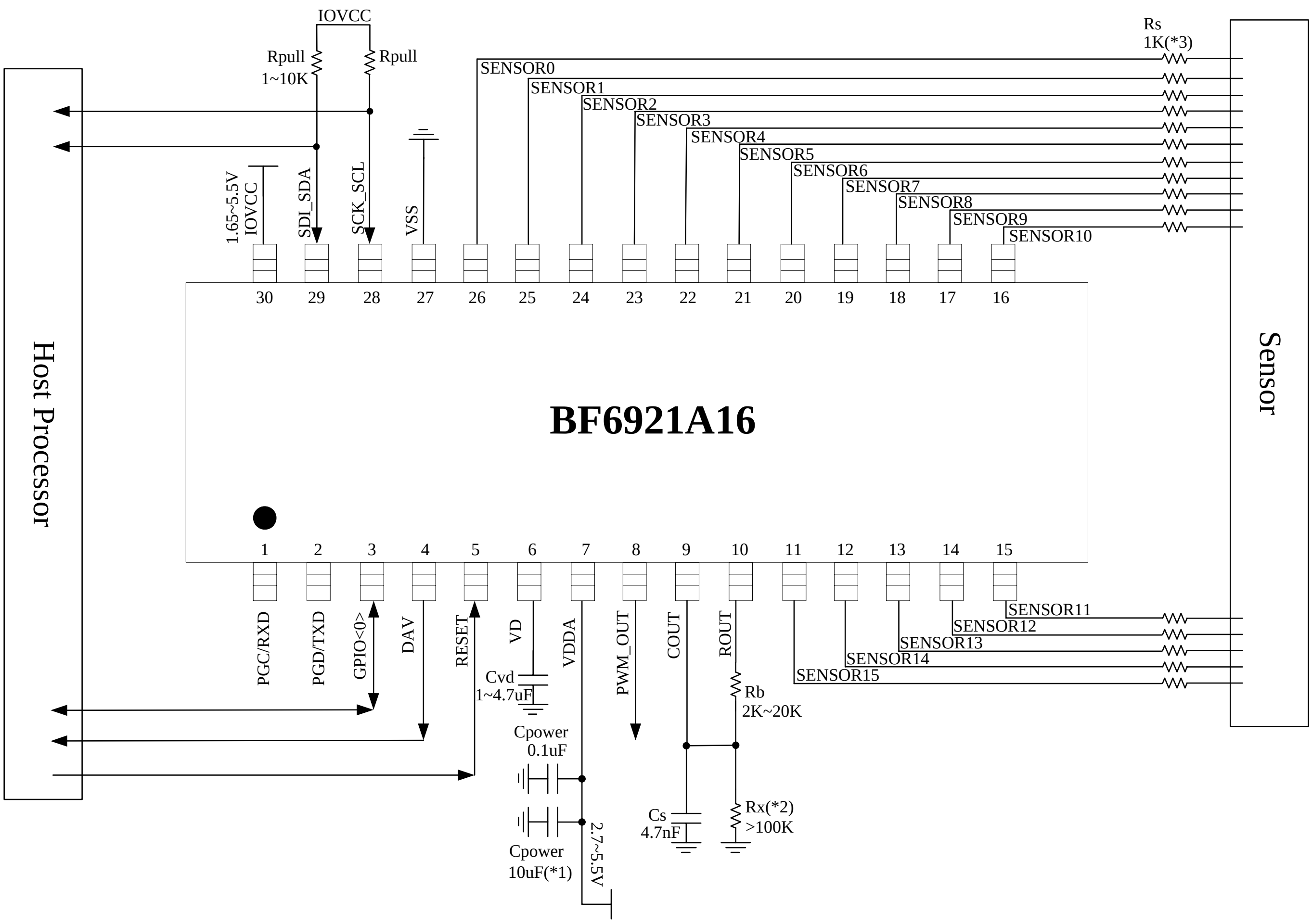
7.3.2 BF6921A8 I²C Application



Note: *1、Value of Cap determined by current situation
*2、Rx could be chosen in some situations to eliminate noise
*3、Rs could be used to decrease some noise brought by EMI
*4、IOVCC could be connected with VDDA together under 2.7~5.5V

Figure 15 8KEY Application Circuit with I²C

7.3.3 BF6921A16 I^{2}C Application



Note: *1、Value of Cap determined by current situation

*2、Rx could be chosen in some situations to eliminate noise

*3、Rs could be used to decrease some noise brought by EMI

*4、IOVCC could be connected with VDDA together under 2.7~5.5V

Figure 16 16KEY Application Circuit with I^{2}C

8. ELECTRICAL CHARACTERISTIC

8.1 AC Specification

8.1.1 I²C Timing

Parameter	symbol	Standard mode		Fast mode		Units	Notes
		Min	Max	Min	Max		
Fscl	SCL	0	100	0	400	kbps	
Start condition hold time	t_{HDSTA}	4.0		0.6		us	
Clock low period	t_{LOW}	4.7		1.3		us	
Clock high period	t_{HIGH}	4.0		0.6		us	
Re-start condition setup time	t_{SUSTA}	4.7		0.6		us	
Data hold time	t_{HDDAT}	0	3.45	0	0.9	us	
Data setup time	t_{SUDAT}	250		100		ns	
Stop condition setup time	t_{SUSTO}	4.0		0.6		us	
BUS free time	t_{BUF}	4.7		1.3		us	
Clock/data rise time	t_R		1000	$20+0.1C_b$	300	ns	
Clock/data fall time	t_F		300	$20+0.1C_b$	300	ns	
Low voltage noise level	VnL	0.1VDDA		0.1VDDA		V	
High voltage noise level	VnH	0.2VDDA		0.2VDDA		V	

I²C timing spec

TA=-40℃ to +85℃ , IOVCC=1.65V to 5.5 V , VDDA=2.7V to 5.5 V.

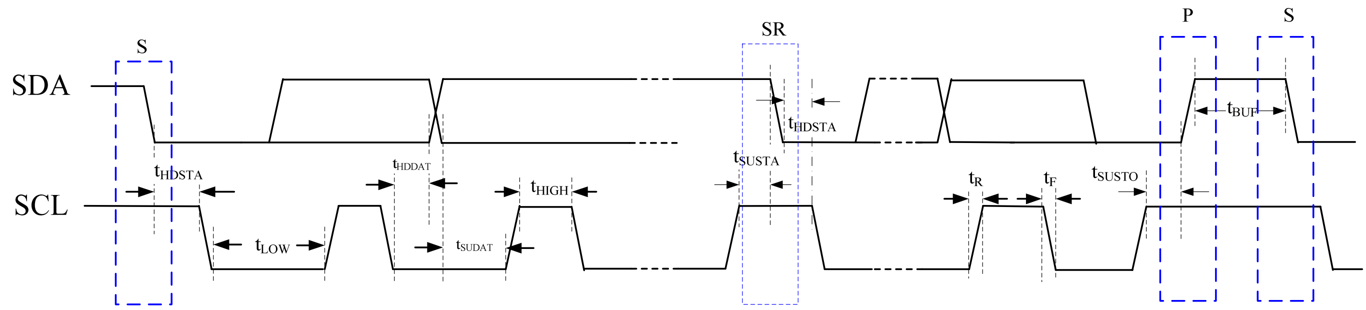


Figure 17 I²C Timing Diagram

8.1.2 SPI Timing

Parameter	Symbol	Min	Max	Unit
SCLK pulse with	Ckwid	250		ns
SCLK duty cycle	CKdut	40	60	%
SDO data output changes on	Falling edge of clock from host			
SDI data input is read on	Rising edge of clock from host			
SCLK high pulse width	T1	100		ns
SCLK low pulse width	T2	100		ns
SDI setup time	T3	20		ns
SDI hold time	T4	20		ns
CS falling edge to first SCLK falling edge	T5	10		ns
SCLK rising edge to CS high	T6	15		ns

TA=-40℃ to +85℃ ,IOVCC=1.65 Vto 5.5V, VDDA= 2.7V to 5.5 V .

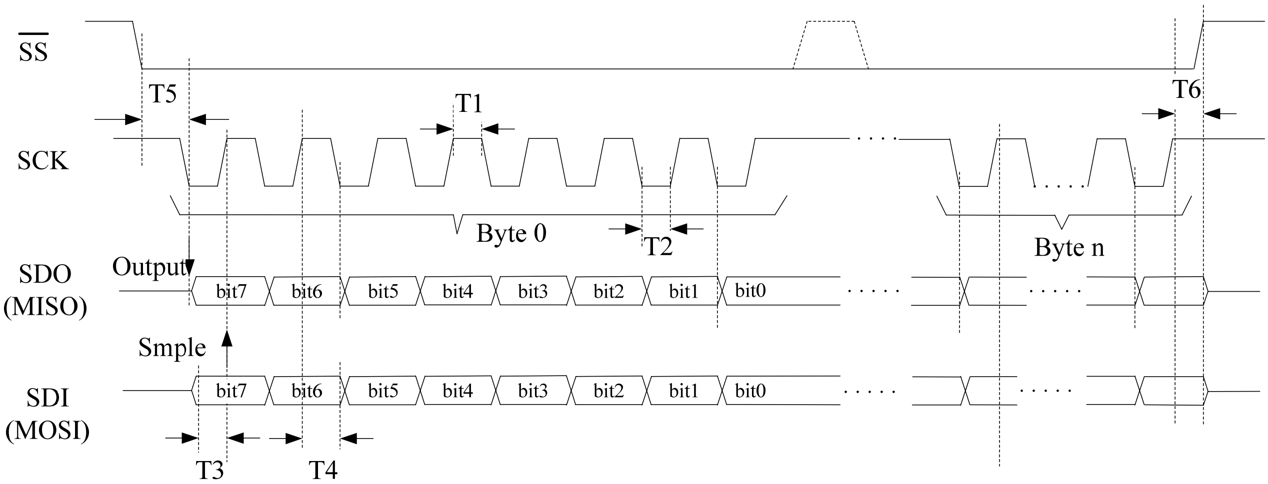


Figure 18 SPI Timing Diagram

8.1.3 General Purpose IO Specification

Parameter	Description	Min	Max	unit	Note
T_{rise}	Rise time C_{load}=20pf	10		ns	VDDA=3.10V to 3.6V 10%-90%
T_{fall}	Fall time C_{load}=20pf	10		ns	VDDA=3.10V to 3.6V 10%-90%

3.3V AC General Purpose Specification

Parameter	Description	Min	Max	unit	Note
T_{rise}	Rise time C_{load}=20pf	10		ns	VDDA=1.65V to 1.9V 10%-90%
T_{fall}	Fall time C_{load}=20pf	10		ns	VDDA=1.65V to 1.9V 10%-90%

1.8V AC General Purpose Specification

8.2 DC Characteristics

The table list guaranteed maximum and minimum specification for the voltage and temperate range: 2.7V to 5.5V and -20℃<TA<85℃, typical parameters apply to 3.3V at 25℃ are for design guidance only.

Parameter	symbol	Condition	Min	TYP	Max	Unit
Supply voltage	VDDA		2.7		5.5	V
IDD		ACTIVE MODE		5		mA
		SLEEP MODE		30	50	uA
Input low voltage	V_{IL}	IOVCC=3.3V			0.2*IOVCC	V
Input high voltage	V_{IH}	IOVCC=3.3V	0.7*IOVCC			V
Output low voltage	V_{OL}	IOL=4mA@IOVCC=3.3V			0.2*IOVCC	V
Output high voltage	V_{OH}	IOH=-4mA@IOVCC=3.3V	0.8*IOVCC			V
Input leakage	I_{IH}			1	5	uA
	I_{IL}					

Table 8　DC Characteristics

8.3 Absolute Maximum Rating

parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Storage temperature	Tstg	-55		125	℃
Operating temperature	Totg	-40		85	℃
Ambient temperate	T_A	-40		85	℃
Input voltage	Vin	VSS-0.5		VCC+0.5	V
Latch up current	LU	150			mA
Static discharge voltage	ESD(HBM)	±2000			V
Power Supply voltage	VCC	-0.5		5.5	V

Table 9　Absolute Maximum Rating

9. PACKAGE

	Package Type	Dimension (Body Size)	Description
I	QFN 24	4mm*4mm*0.9mm	8Key
II	QFN 40	4.5mm*6mm*0.75mm	16key
III	SOP 30	19mm*7.6mm*2.3mm	16Key

I—QFN24

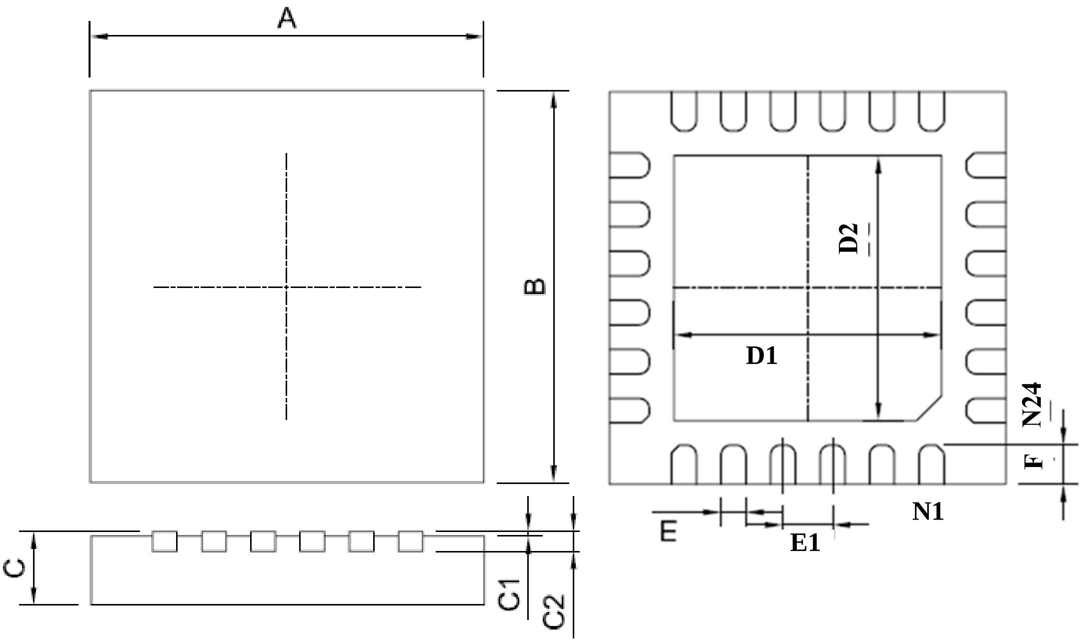


Figure 19 QFN-24 Package

Package Information

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	3.900	4.000	4.100
B	3.900	4.000	4.1.00
C	0.850	0.900	0.950
C1	0		0.050
C2		0.203	
D1		2.700	
D2		2.700	
E		0.250	
E1		0.500	
F		0.400	

Table 10 QFN-24 Package

II—QFN 40

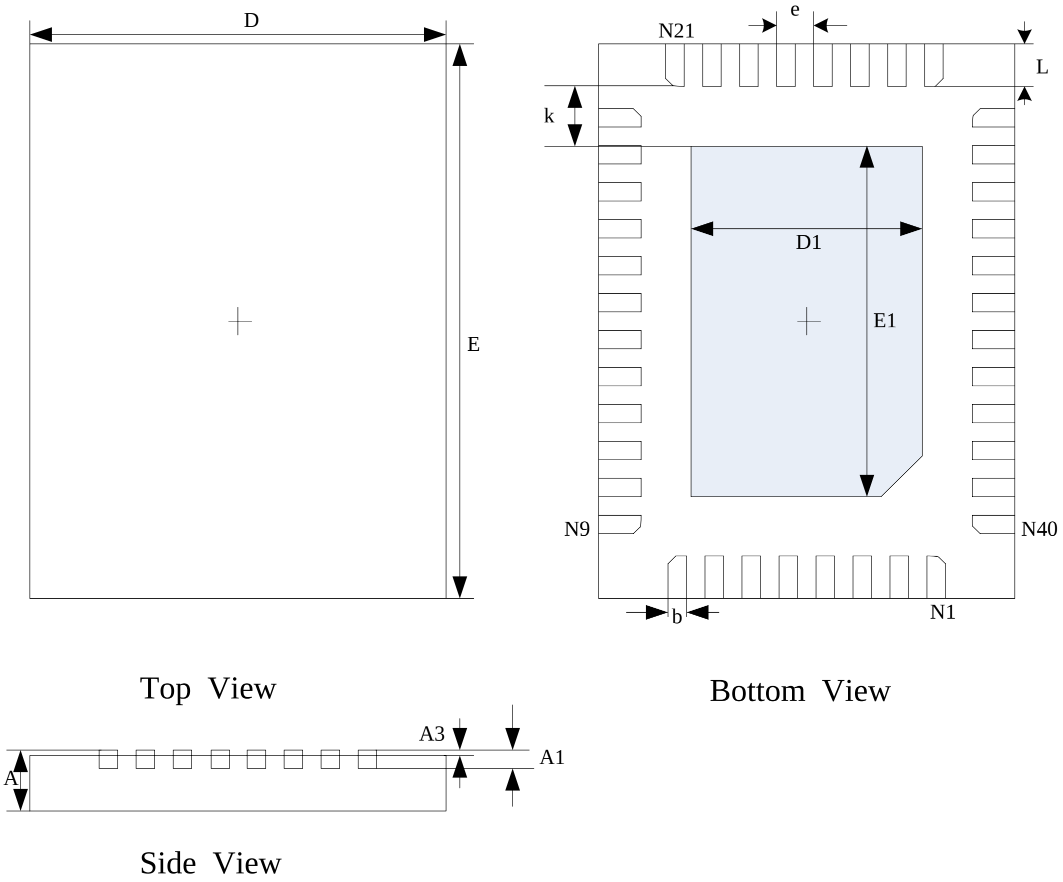


Figure 20 QFN-40 Package

Package Information

Symbol	Dimensions In Millimeters		
	MIN	REF	MAX
A	0.7	0.75	0.8
A3	0	0.025	0.05
A1	0.153	0.203	0.253
D	4.4	4.5	4.6
E	5.9	6	6.1
D1	2.4	2.5	2.6
E1	3.7	3.8	3.9
k		0.64	
b	0.15	0.2	0.25
e	0.35	0.4	0.45
L	0.36	0.46	0.56

Table 11 QFN-40 Package

III—SOP30

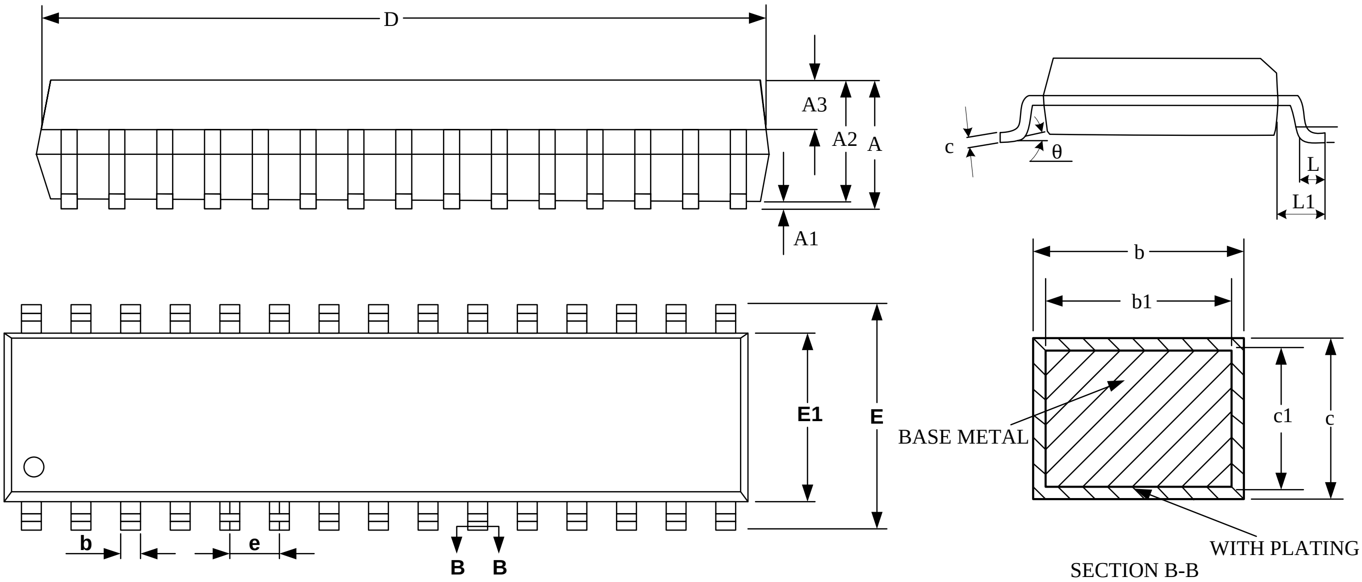


Figure 21 SOP-30 Package

Package Information

DIM	MILLIMETERS		
	MIN	NOM	MAX
A			2.70
A1	0.10	0.20	0.30
A2	2.10	2.30	2.50
A3	0.92	1.02	1.12
b	0.39		0.48
b1	0.38	0.41	0.43
c	0.25		0.31
c1	0.24	0.25	0.26
D	18.80	19.00	19.20
E	10.10	10.30	10.50
E1	7.40	7.60	7.80
e	1.27BSC		
L	0.70	0.85	1.00
L1	1.35BSC		
θ	0		8°

Table 12 SOP-30 Package

RESTRICTIONS ON PRODUCT USE

- The information contained herein is subject to change without notice.

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