



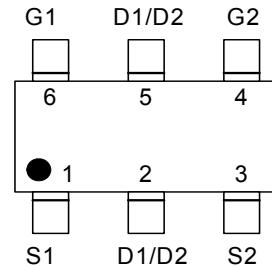
BYD Microelectronics Co., Ltd.

**BF8205E**

## Dual N-Channel MOSFET

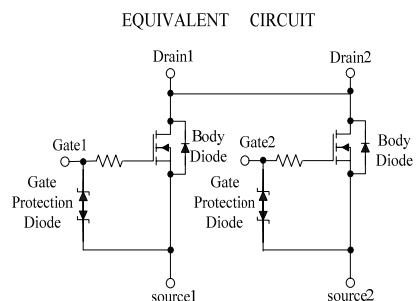
### General Description

The BF8205E is a dual N-channel MOS Field Effect Transistor, which uses advanced trench technology to provide excellent  $R_{DS(on)}$ , low gate charge and operation with low gate voltages. This device is suitable for use as a load switch. This device has ESD protection.



### Features

- $V_{DS} = 20\text{ V}$
- $I_D = 6\text{ A}$
- Low on-state resistance Fast switching
  - $R_{DS(on)} \leq 22\text{m}\Omega$  ( $V_{GS} = 4.5\text{V}$ ,  $I_D = 3.0\text{A}$ )
  - $R_{DS(on)} \leq 24\text{m}\Omega$  ( $V_{GS} = 3.8\text{V}$ ,  $I_D = 3.0\text{A}$ )
  - $R_{DS(on)} \leq 32\text{m}\Omega$  ( $V_{GS} = 2.5\text{V}$ ,  $I_D = 3.0\text{A}$ )
- Built-in G-S protection diode against ESD.
- Lead Pb-free and Halogen-free



### Absolute Maximum Ratings ( $T_c = 25^\circ\text{C}$ )

Symbol	Parameter	Value	Unit	
$V_{DS}$	Drain-source Voltage	20	V	
$I_D$	Drain Current(continuous)at $T_c=25^\circ\text{C}$	(Note1)	6	A
$I_{DM}$	Drain Current (pulsed)	(Note2)	24	A
$V_{GS}$	Gate-source Voltage	$\pm 12$	V	
$P_D$	Power Dissipation ( $T_c = 25^\circ\text{C}$ )	(Note1)	1.25	W
$T_J, T_{Stg}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$	

### Ordering Information

Part Number	Package	Packaging
BF8205E	SOT23-6	3000pcs Tape& Reel



## Thermal Data

Symbol	Parameter	Max.	Unit
R <sub>thj-amb</sub>	Thermal Resistance Junction- ambient	100	°C/W

## Electrical Characteristics ( $T_C = 25^\circ\text{C}$ )

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	20			V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}, V_{GS}=0\text{V}$			1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate Leakage Current	$V_{GS}=\pm 12\text{V}, V_{DS}=0\text{V}$			$\pm 15$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D= 250\mu\text{A}$	0.5	0.7	1.0	V
$R_{DS(\text{on})}$	Drain to Source On-state Resistance	$V_{GS}=4.5\text{V}, I_D=3\text{A}$		17	22	$\text{m}\Omega$
		$V_{GS}=3.8\text{V}, I_D=3\text{A}$		18	24	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_D=3\text{A}$		23	30	$\text{m}\Omega$
$C_{iss}$	Input Capacitance	$V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$		370		$\text{pF}$
$C_{oss}$	Output Capacitance			89		$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance			9.7		$\text{pF}$
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=10\text{V}, I_D=3\text{A}, V_{GS}=4.5\text{V}, R_G=4.7\Omega$ (Note2,3)		200		ns
$t_r$	Rise Time			236		ns
$t_{d(off)}$	Turn-off Delay Time			36		ns
$t_f$	Fall Time			165		ns
$Q_g$	Total Gate Charge	$V_{DD}=16\text{V}, V_{GS}=4.5\text{V}, I_D=6\text{A}$ (Note2,3)		7.5		nC
$Q_{gs}$	Gate to Source Charge			2.5		nC
$Q_{gd}$	Gate to Drain Charge			1.3		nC
$V_{SD(*)}$	Body Diode Forward Voltage	$I_F=6\text{A}, V_{GS}=0\text{V}$		0.74	1.2	V
$T_{rr}$	Reverse Recovery Time	$V_{DD}=10\text{V}, I_F=6\text{A}, di/dt=100\text{A/us}$ (Note2)		80		ns

### Notes:

1. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$
  2. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
  3. Essentially independent of operating temperature
- (\*Pulsed: Pulse duration

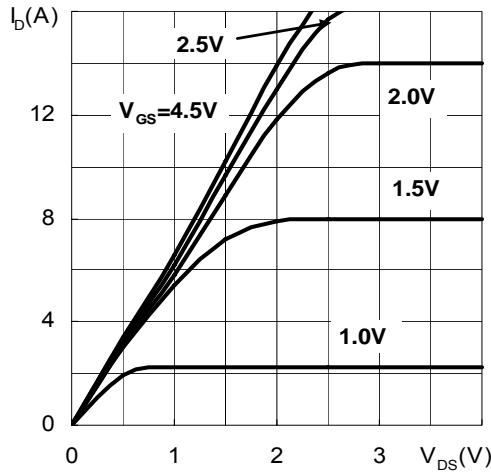
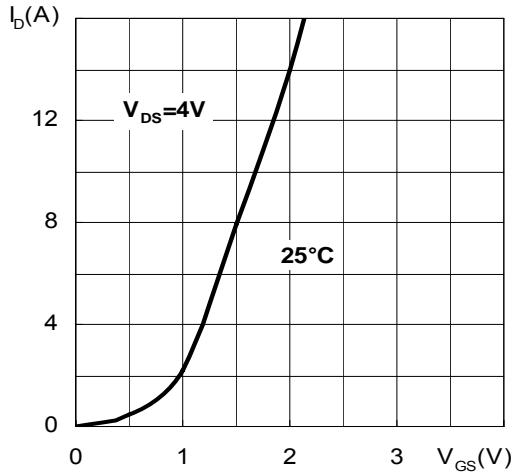
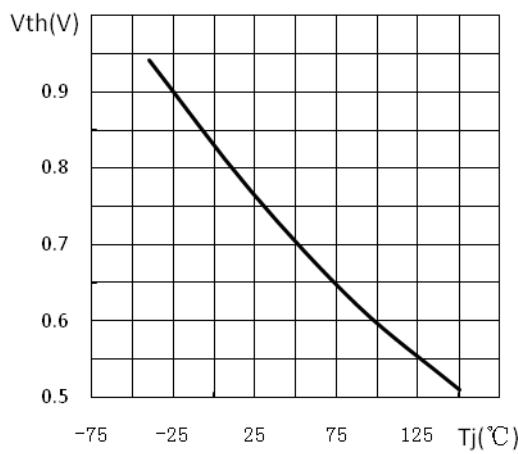
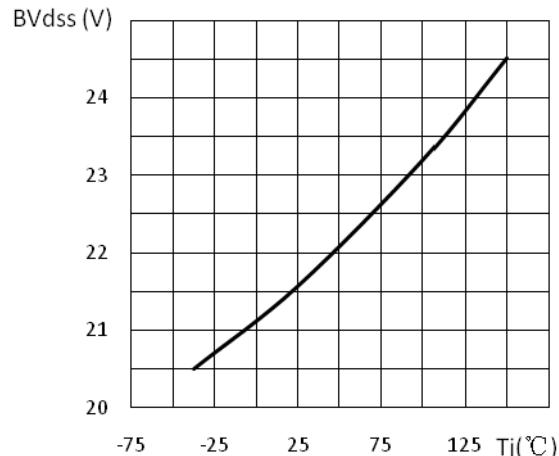
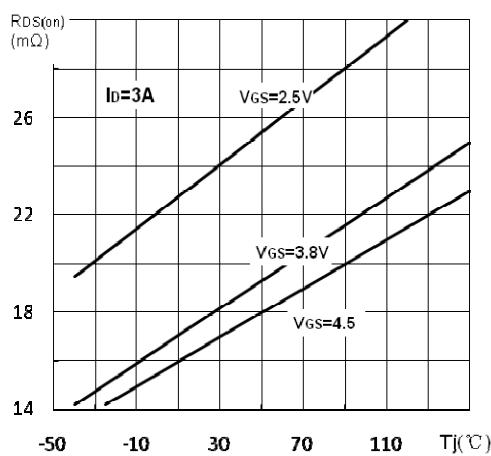
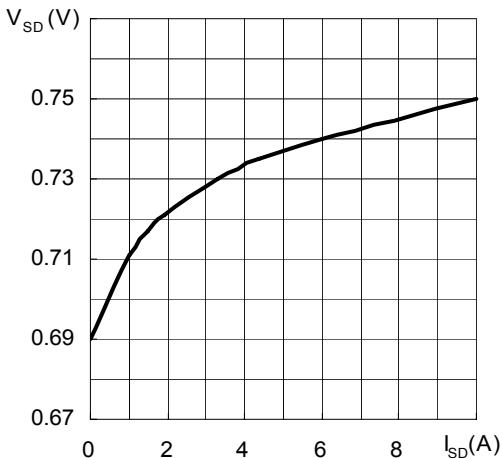
**Typical characteristics (25°C unless noted)****Figure 1 Output Characteristics****Figure 2 Transfer Characteristics****Figure 3 Normalized Threshold Voltage vs. Temperature****Figure 4 Normalized  $BV_{DSS}$  vs. Temperature****Figure 5 Normalized on Resistance vs Temperature****Figure 6 Source-drain diode forward characteristics**



Figure 7 Capacitance

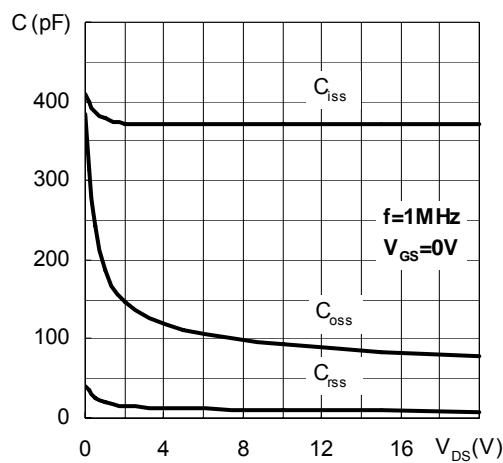


Figure 8 Gate Charge

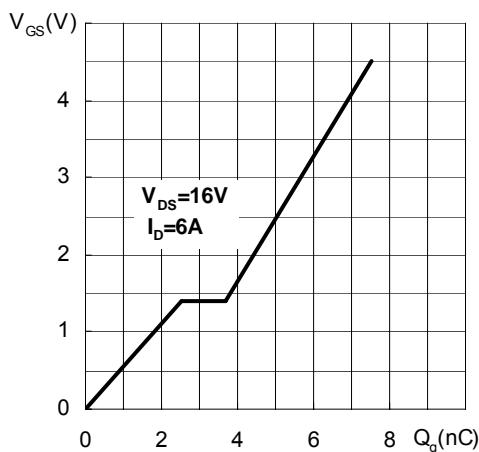


Figure 9 Safe Operating Area Temperature

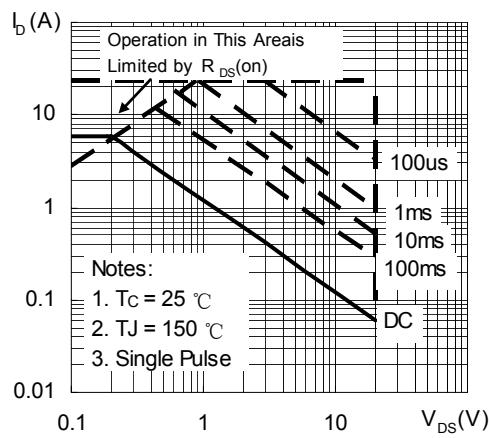


Figure 10 Maximum Drain Current vs Case Temperature

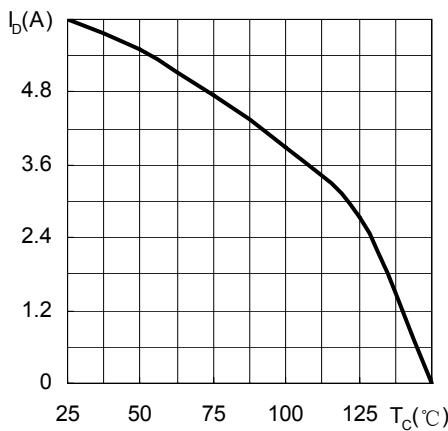


Figure 11 On-Resistance vs. Gate-to-Source Voltage

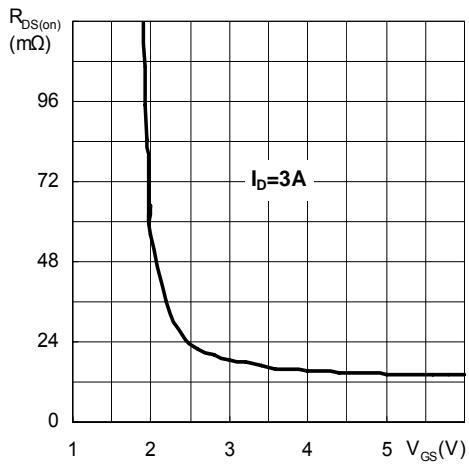
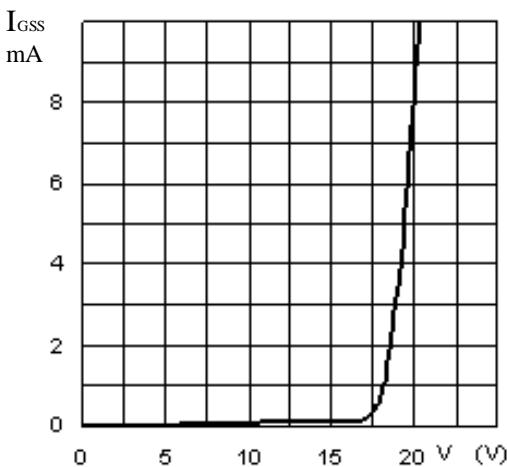
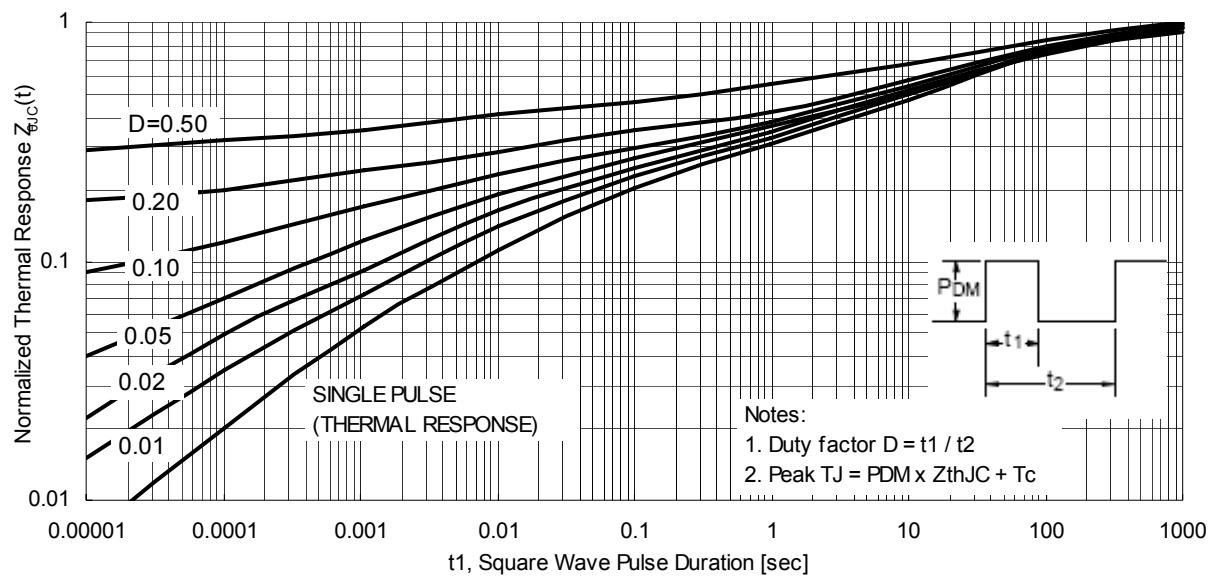
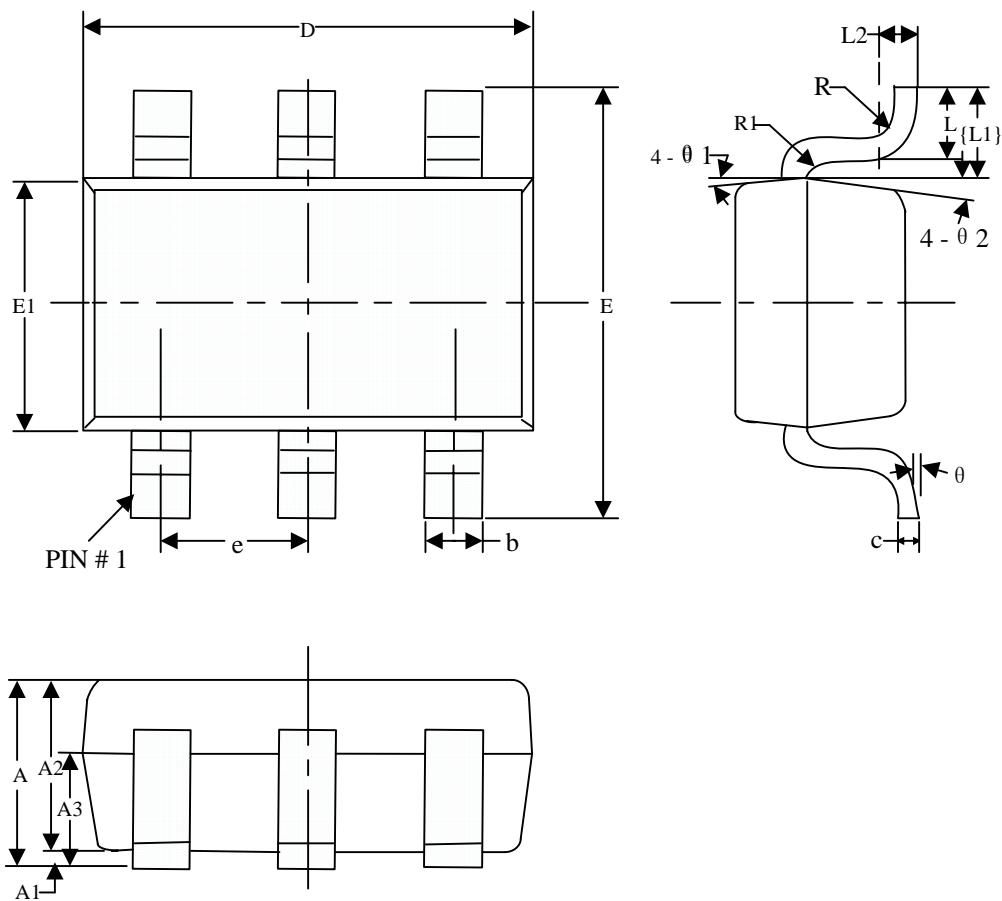


Figure 12 Gate-Current vs. Gate-Source Voltage



**Figure 13 Maximum Transient Thermal impedance**


### Package Drawing

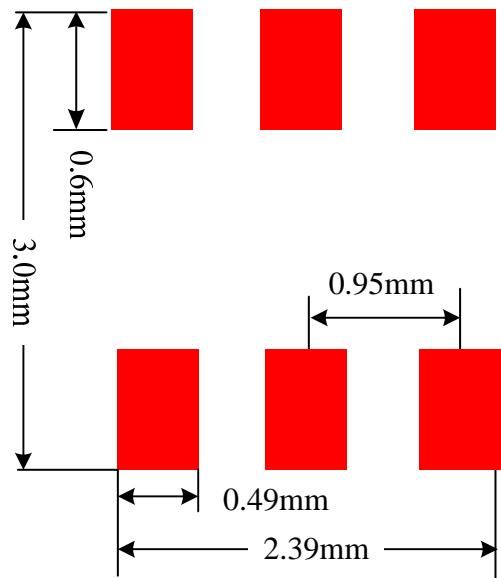




## Dimensions (unit: mm)

SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	-	-	1.30	e	0.85	0.95	1.05
A1	0	-	0.15	L	0.35	0.45	0.60
A2	0.90	1.10	1.30	L1	0.59REF		
A3	0.60	0.65	0.70	L2	0.25BSC		
b	0.39	-	0.49	R	0.05	-	-
c	0.12	-	0.19	R1	0.05	-	0.02
D	2.85	2.95	3.15	$\theta$	$0^\circ$	-	$8^\circ$
E	2.60	2.80	3.00	$\theta_1$	$3^\circ$	$5^\circ$	$7^\circ$
E1	1.55	1.65	1.75	$\theta_2$	$6^\circ$	$8^\circ$	$10^\circ$

## PCB Layout Guide





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