

BFP620

Surface mount high linearity silicon NPN RF bipolar transistor



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Technical
documents



Simulation



Support

Product description

The BFP620 is a RF bipolar transistor based on SiGe:C technology that is part of Infineon's established sixth generation transistor family. Its high linearity characteristics and collector design make the device suitable for a wide range of wireless applications. It remains cost competitive without compromising on ease of use.



Feature list

- Minimum noise figure $NF_{min} = 0.7$ dB at 1.8 GHz, 1.5 V, 5 mA
- High gain $G_{ms} = 21.5$ dB at 1.8 GHz, 1.5 V, 50 mA
- $OIP_3 = 25.5$ dBm at 1.8 GHz, 2 V, 50 mA

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22, and J-STD-020.

Qualified for industrial applications according to the relevant tests of AEC-Q 101.

Potential applications

- Low noise amplifiers (LNAs) in SDARS receivers
- LNAs for wireless communications
- LNAs for ISM band applications

Device information

Table 1 Part information

Product name / Ordering code	Package	Pin configuration				Marking	Pieces / Reel
BFP620 / BFP620H7764XTSA1	SOT343	1 = B	2 = E	3 = C	4 = E	R2s	3000

Attention: *ESD (Electrostatic discharge) sensitive device, observe handling precautions*

Table of contents**Table of contents**

Product description	1
Feature list	1
Product validation	1
Potential applications	1
Device information	1
Table of contents	2
1 Absolute maximum ratings	3
2 Thermal characteristics	4
3 Electrical characteristics	6
3.1 DC characteristics	6
3.2 General AC characteristics	6
3.3 Frequency dependent AC characteristics	7
3.4 Characteristic AC diagrams	8
4 Package information SOT343	13
Revision history	14
Disclaimer	15

Absolute maximum ratings**1 Absolute maximum ratings****Table 2 Absolute maximum ratings at $T_A = 25^\circ\text{C}$ (unless otherwise specified)**

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Collector emitter voltage	V_{CEO}	-	2.3	V	Open base
			2.1		$T_A = -55^\circ\text{C}$, open base
Collector emitter voltage			7.5		E-B short circuited
Collector base voltage			7.5		Open emitter
Emitter base voltage	V_{EBO}		1.2		Open collector
Base current	I_B	3	mA		-
Collector current	I_C	80			
Total power dissipation ¹⁾	P_{tot}	185	mW	$T_S \leq 95^\circ\text{C}$	
Junction temperature	T_J	150	°C		-
Storage temperature	T_{Stg}				
		-55			

Attention: *Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding only one of these values may cause irreversible damage to the integrated circuit.*

¹⁾ T_S is the soldering point temperature. T_S is measured on the emitter lead at the soldering point of the PCB.

Thermal characteristics

2 Thermal characteristics

Table 3 Thermal resistance

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Junction - soldering point	R_{thJS}	–	300	–	K/W	–

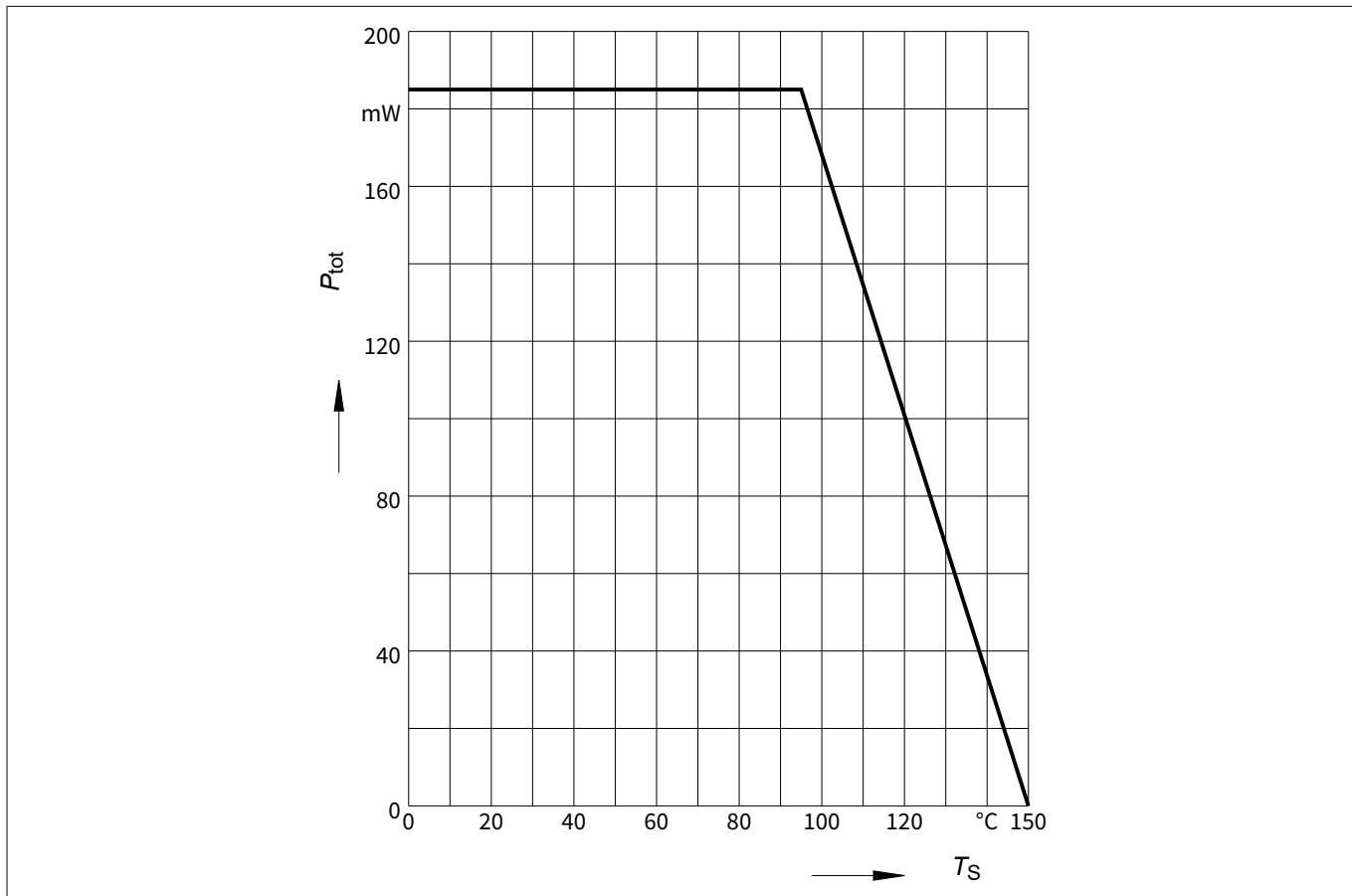


Figure 1

Total power dissipation $P_{\text{tot}} = f(T_S)$

Thermal characteristics

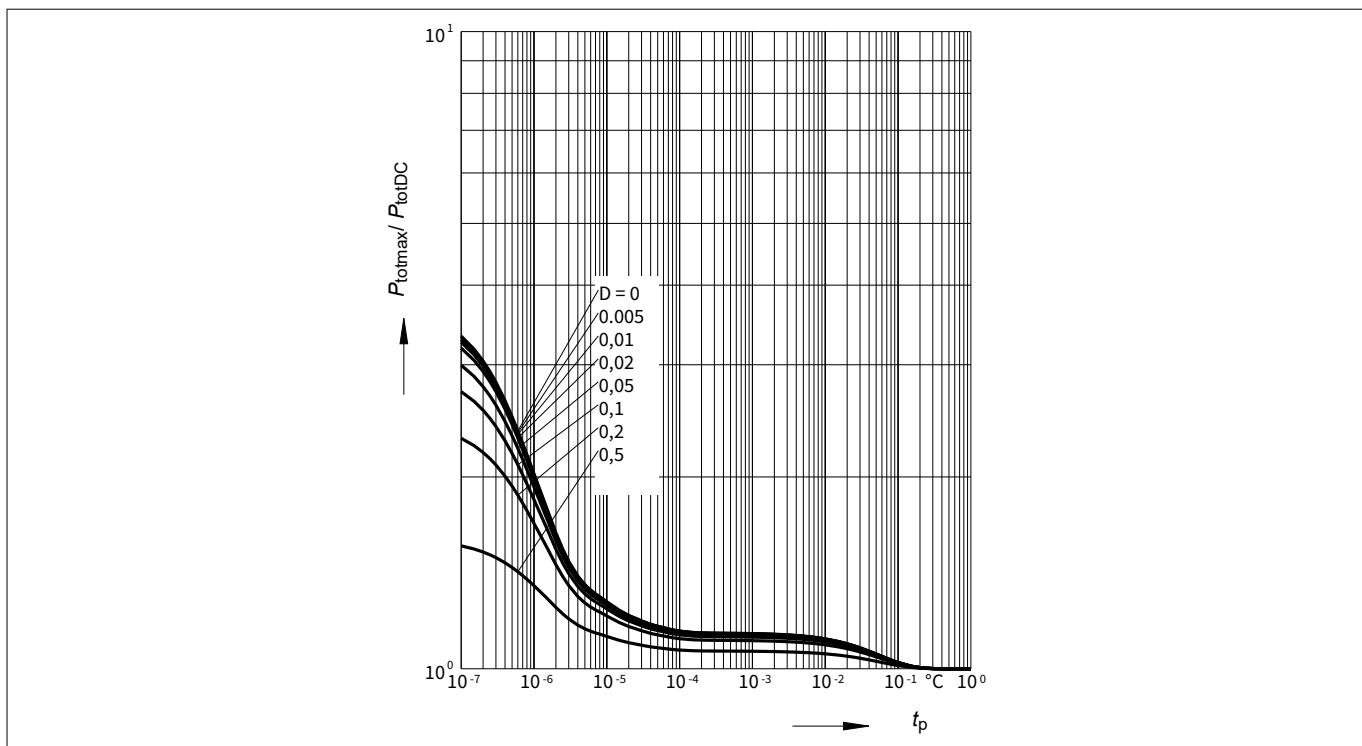


Figure 2 Permissible pulse load $P_{\text{tot},\text{max}} / P_{\text{tot},\text{DC}} = f(t_p)$

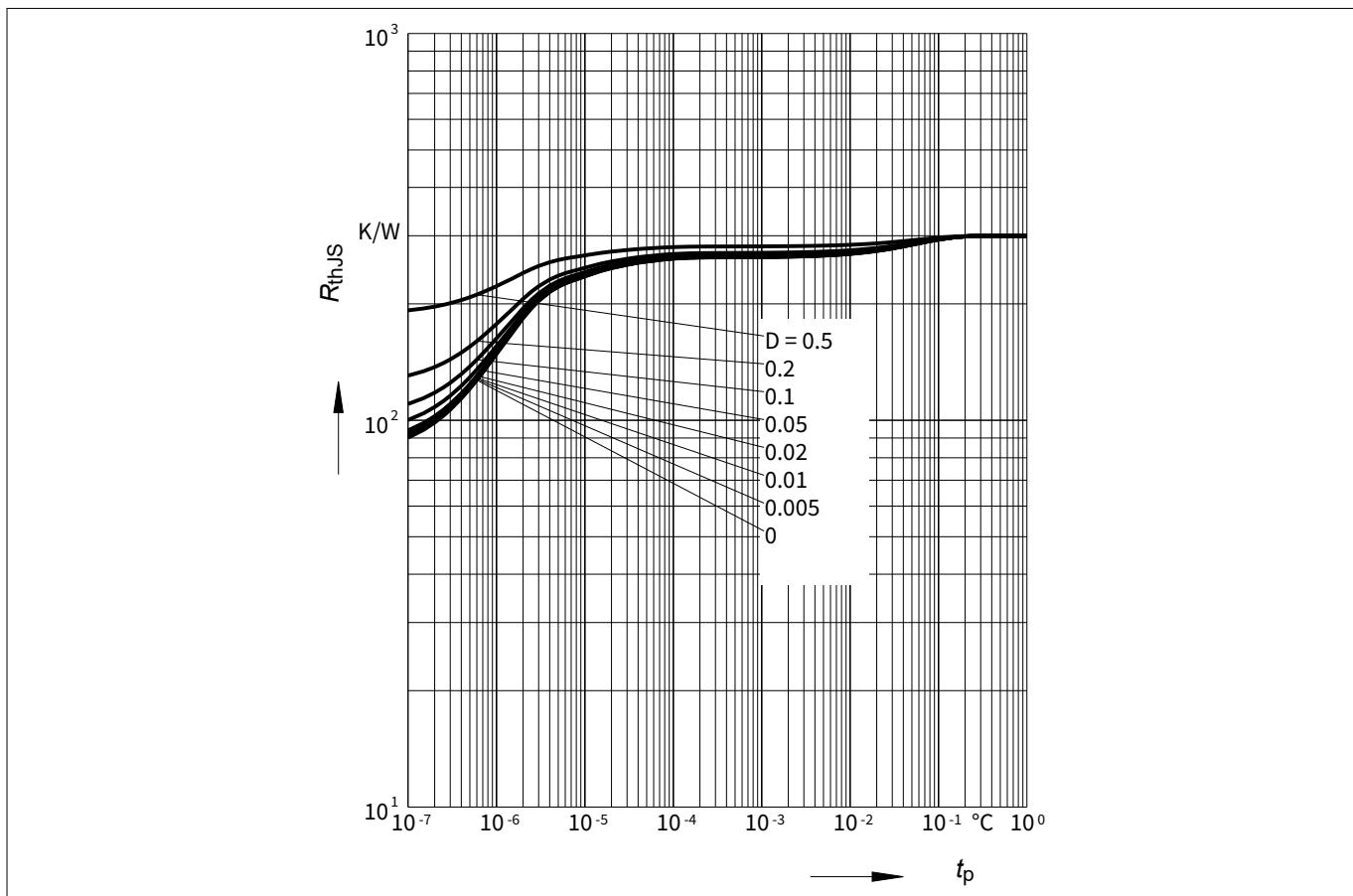


Figure 3 Permissible pulse load $R_{\text{thJS}} = f(t_p)$

Electrical characteristics

3 Electrical characteristics

3.1 DC characteristics

Table 4 DC characteristics at $T_A = 25^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Collector emitter breakdown voltage	$V_{(\text{BR})\text{CEO}}$	2.3	2.8	-	V	$I_C = 1 \text{ mA}, I_B = 0,$ open base
Collector emitter leakage current	I_{CES}	-	-	$10^{2)} \text{ } \mu\text{A}$	μA	$V_{\text{CE}} = 7.5 \text{ V}, V_{\text{BE}} = 0,$ E-B short circuited
		0.001	0.04 ²⁾	$10^{2)} \text{ } \mu\text{A}$		$V_{\text{CE}} = 5 \text{ V}, V_{\text{BE}} = 0,$ EB short circuited
Collector base leakage current	I_{CBO}	1	40 ²⁾	nA	nA	$V_{\text{CB}} = 5 \text{ V}, I_E = 0,$ open emitter
Emitter base leakage current	I_{EBO}	10	900 ²⁾	$10^{2)} \text{ nA}$		$V_{\text{EB}} = 0.5 \text{ V}, I_C = 0,$ open collector
DC current gain	h_{FE}	110	180	270		$V_{\text{CE}} = 1.5 \text{ V}, I_C = 50 \text{ mA},$ pulse measured

3.2 General AC characteristics

Table 5 General AC characteristics at $T_A = 25^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Transition frequency	f_T	-	65	-	GHz	$V_{\text{CE}} = 1.5 \text{ V}, I_C = 50 \text{ mA},$ $f = 1 \text{ GHz}$
Collector base capacitance	C_{CB}	0.12	0.2	pF	pF	$V_{\text{CB}} = 2 \text{ V}, V_{\text{BE}} = 0,$ $f = 1 \text{ MHz},$ emitter grounded
		0.22	-	$10^{2)} \text{ pF}$		$V_{\text{CE}} = 2 \text{ V}, V_{\text{BE}} = 0,$ $f = 1 \text{ MHz},$ base grounded
Emitter base capacitance	C_{EB}	0.46				$V_{\text{EB}} = 0.5 \text{ V}, V_{\text{CB}} = 0,$ $f = 1 \text{ MHz},$ collector grounded

² Maximum values not limited by the device but by the short cycle time of the 100% test.

Electrical characteristics

3.3 Frequency dependent AC characteristics

Measurement setup is a test fixture with Bias-T's in a 50Ω system, $T_A = 25^\circ\text{C}$.

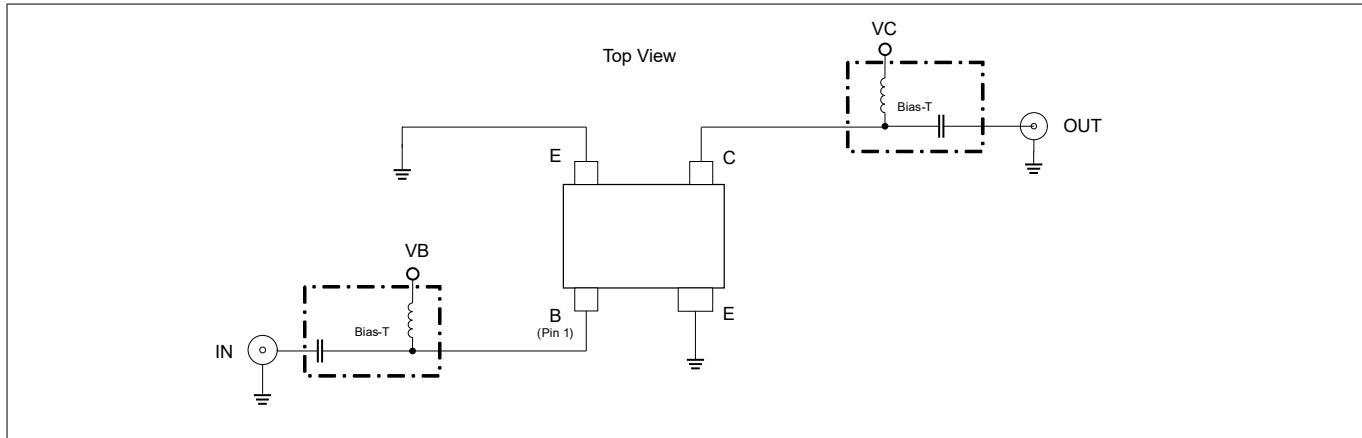


Figure 4 Testing circuit

Table 6 AC characteristics, $V_{CE} = 1.5 \text{ V}$, $f = 1.8 \text{ GHz}$

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Power gain		-		-	dB	
• Maximum power gain	G_{ms}	21.5				$I_C = 50 \text{ mA}$
• Transducer gain	$ S_{21} ^2$	20				
Noise figure			0.7			$I_C = 5 \text{ mA}$
• Minimum noise figure	NF_{min}					
Linearity					dBm	
• 3rd order intercept point at output	OIP_3	25.5				$I_C = 50 \text{ mA}, V_{CE} = 2 \text{ V}, Z_S = Z_L = 50 \Omega$
• 1 dB gain compression point at output	$OP_{1\text{dB}}$	14.5				

Table 7 AC characteristics, $V_{CE} = 1.5 \text{ V}$, $f = 6 \text{ GHz}$

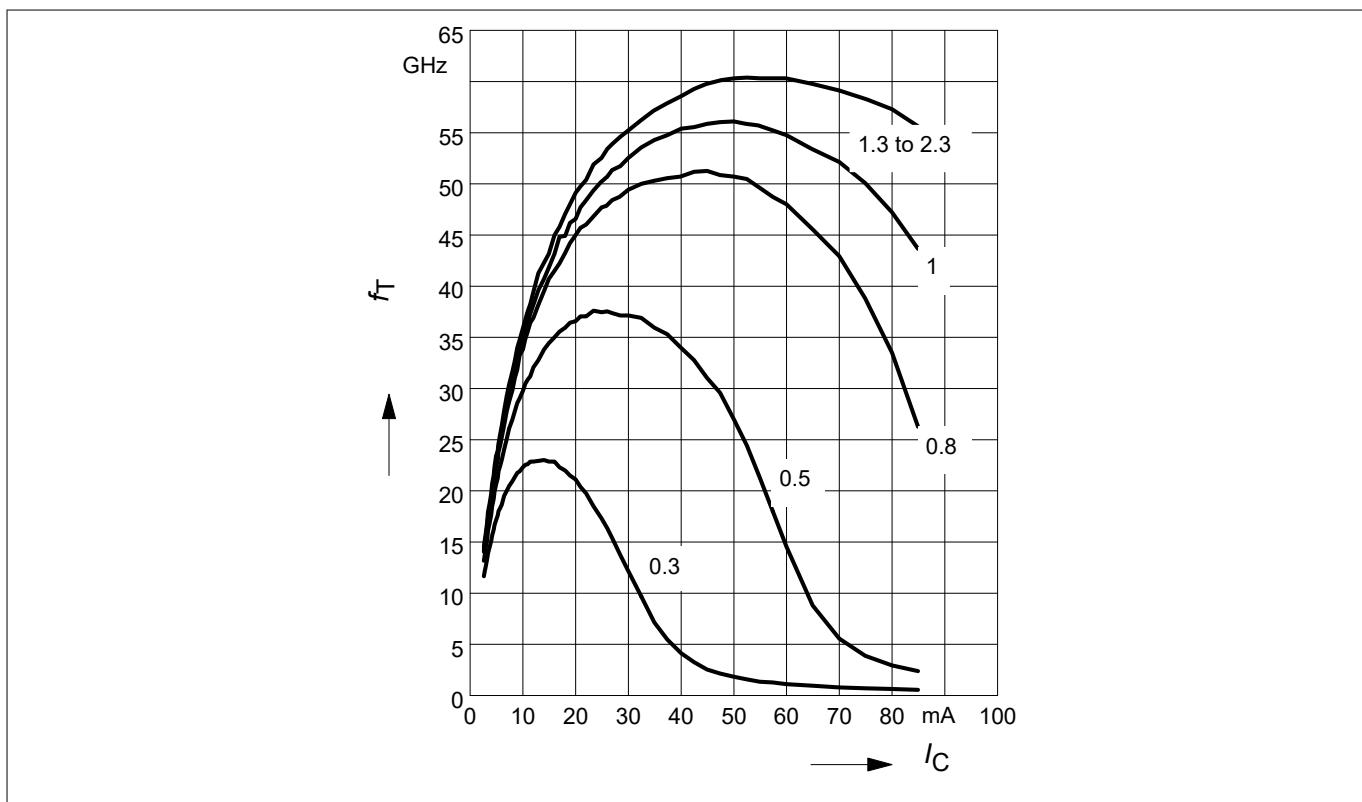
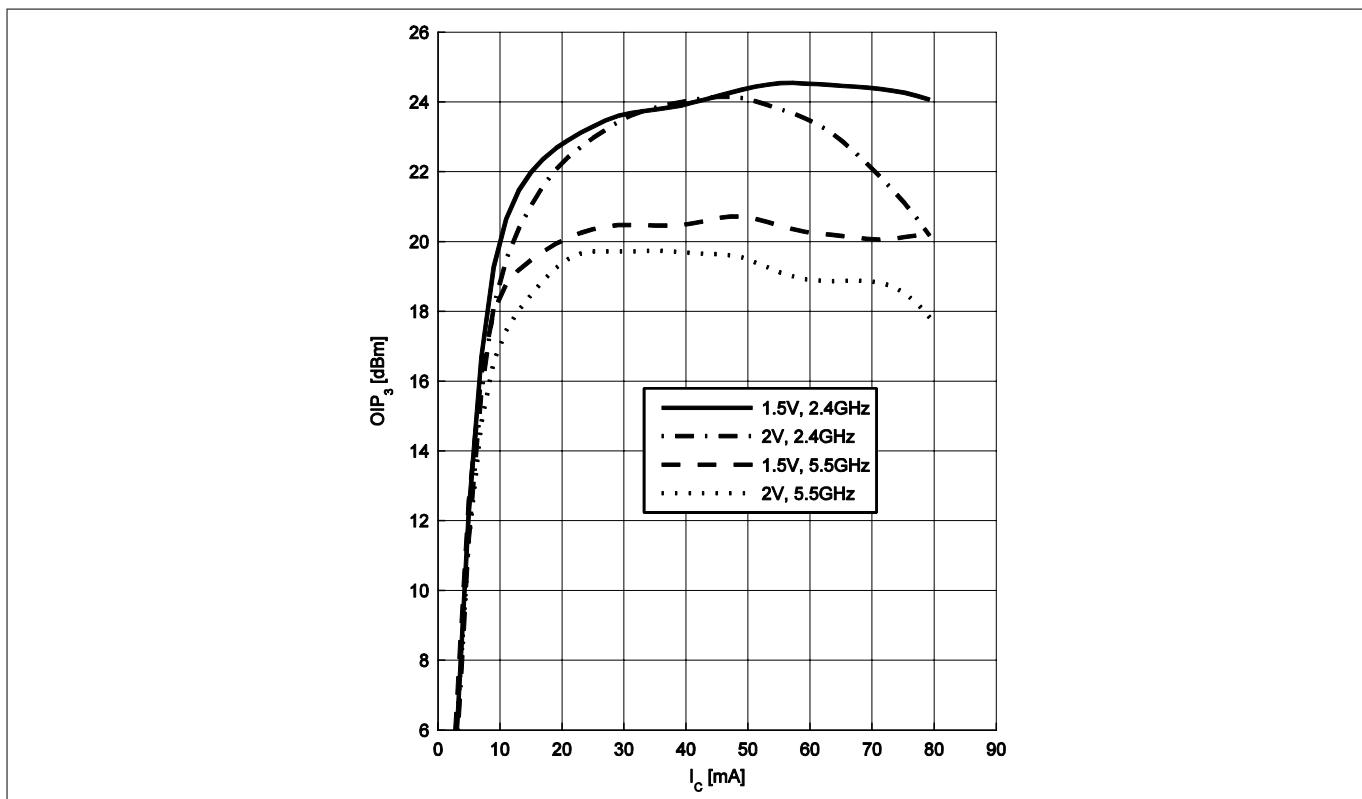
Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Power gain		-		-	dB	
• Maximum power gain	G_{ms}	11				$I_C = 50 \text{ mA}$
• Transducer gain	$ S_{21} ^2$	9.5				
Noise figure			1.3			$I_C = 5 \text{ mA}$
• Minimum noise figure	NF_{min}					

Note: $G_{ms} = IS_{21}/S_{12}I$ for $k < 1$; $G_{ma} = IS_{21}/S_{12}I(k-(k^2-1)^{1/2})$ for $k > 1$. In order to get the NF_{min} values stated in this chapter, the test fixture losses have been subtracted from all measured results. OIP_3 value depends on termination of all intermodulation frequency components. Termination used for this measurement is 50Ω from 0.1 MHz to 6 GHz .

Electrical characteristics

3.4

Characteristic AC diagrams

Figure 5 Transition frequency $f_T = f(I_C)$, $f = 1$ GHz, V_{CE} = parameterFigure 6 3rd order intercept point $O/I_P_3 = f(I_C)$, $Z_S = Z_L = 50 \Omega$, V_{CE} , f = parameters

Electrical characteristics

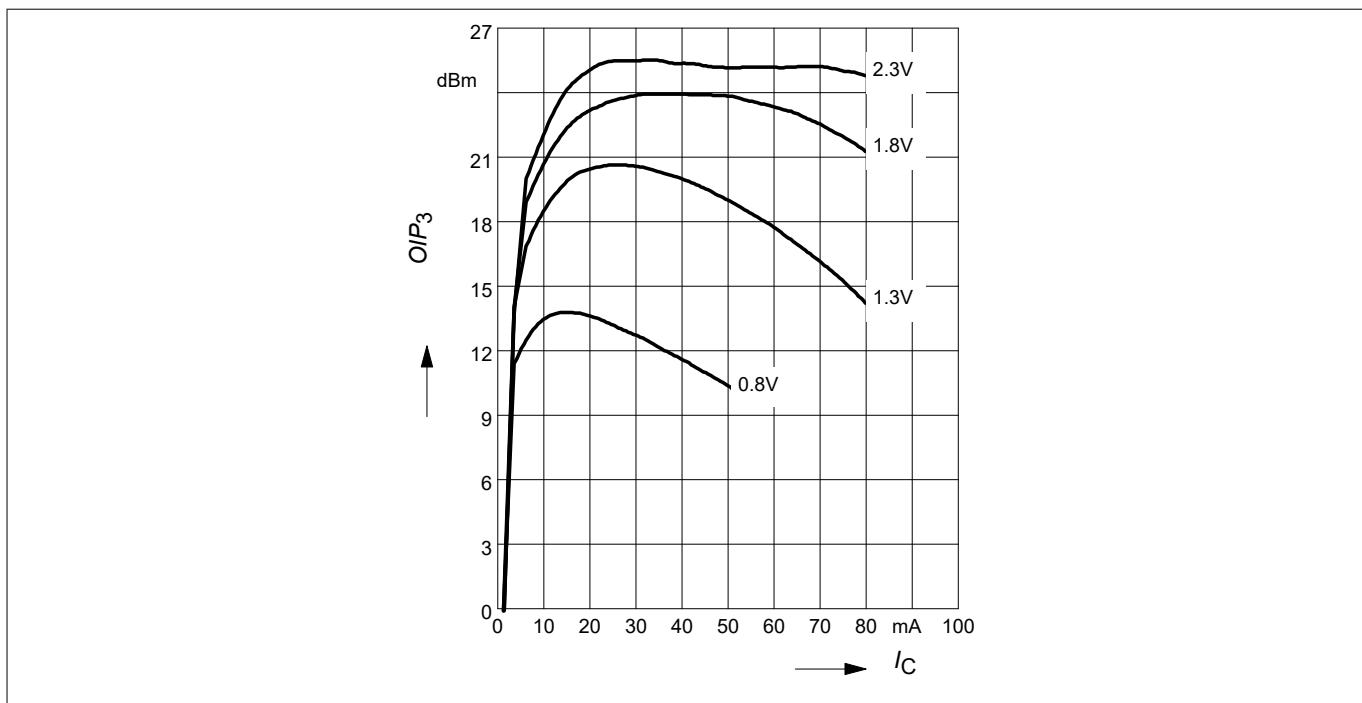


Figure 7 3rd order intercept point at output $O/I_P3 = f(I_C, V_{CE})$, $Z_S = Z_L = 50 \Omega$, $f = 900 \text{ MHz}$

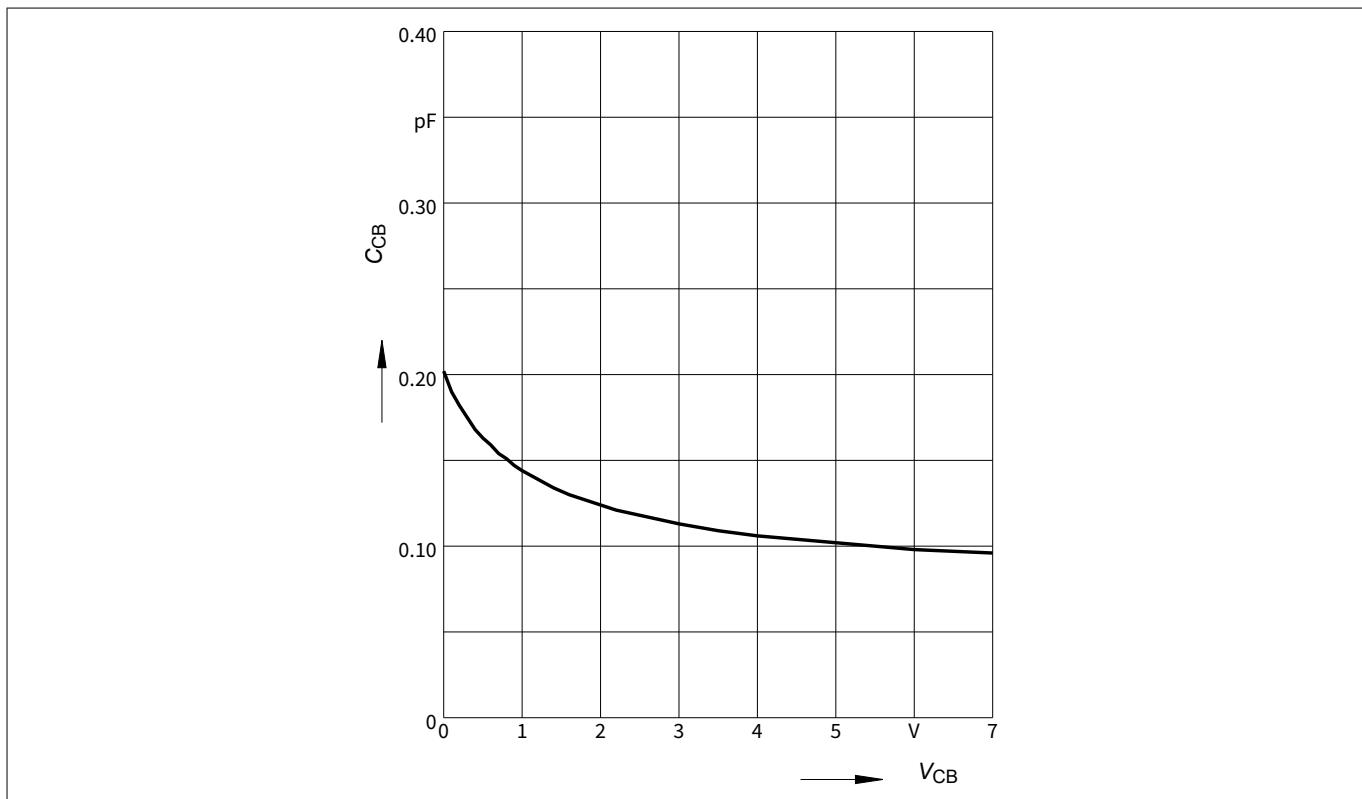


Figure 8 Collector base capacitance $C_{CB} = f(V_{CB})$, $f = 1 \text{ MHz}$

Electrical characteristics

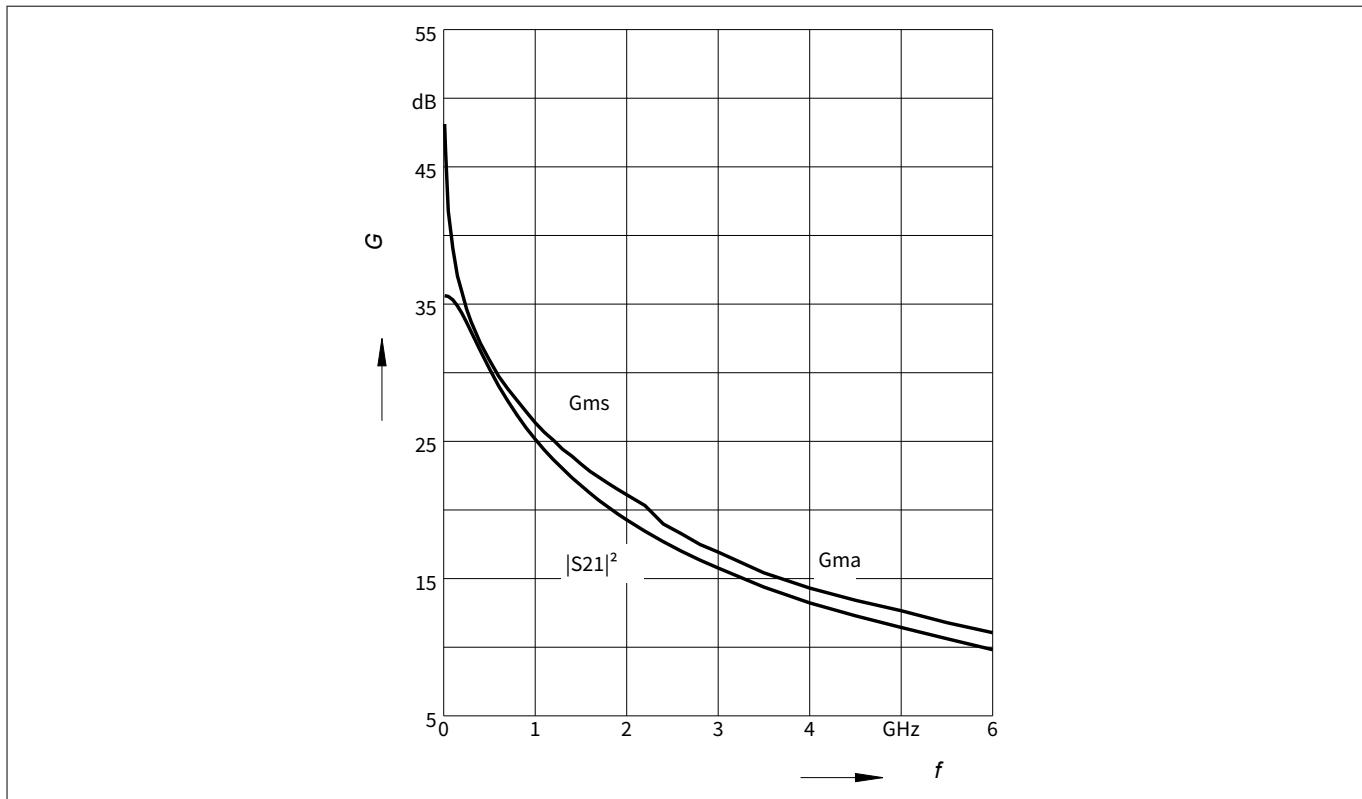


Figure 9 Gain G_{ms} , G_{ma} , $|S_{21}|^2 = f(f)$, $V_{CE} = 1.5$ V, $I_C = 50$ mA

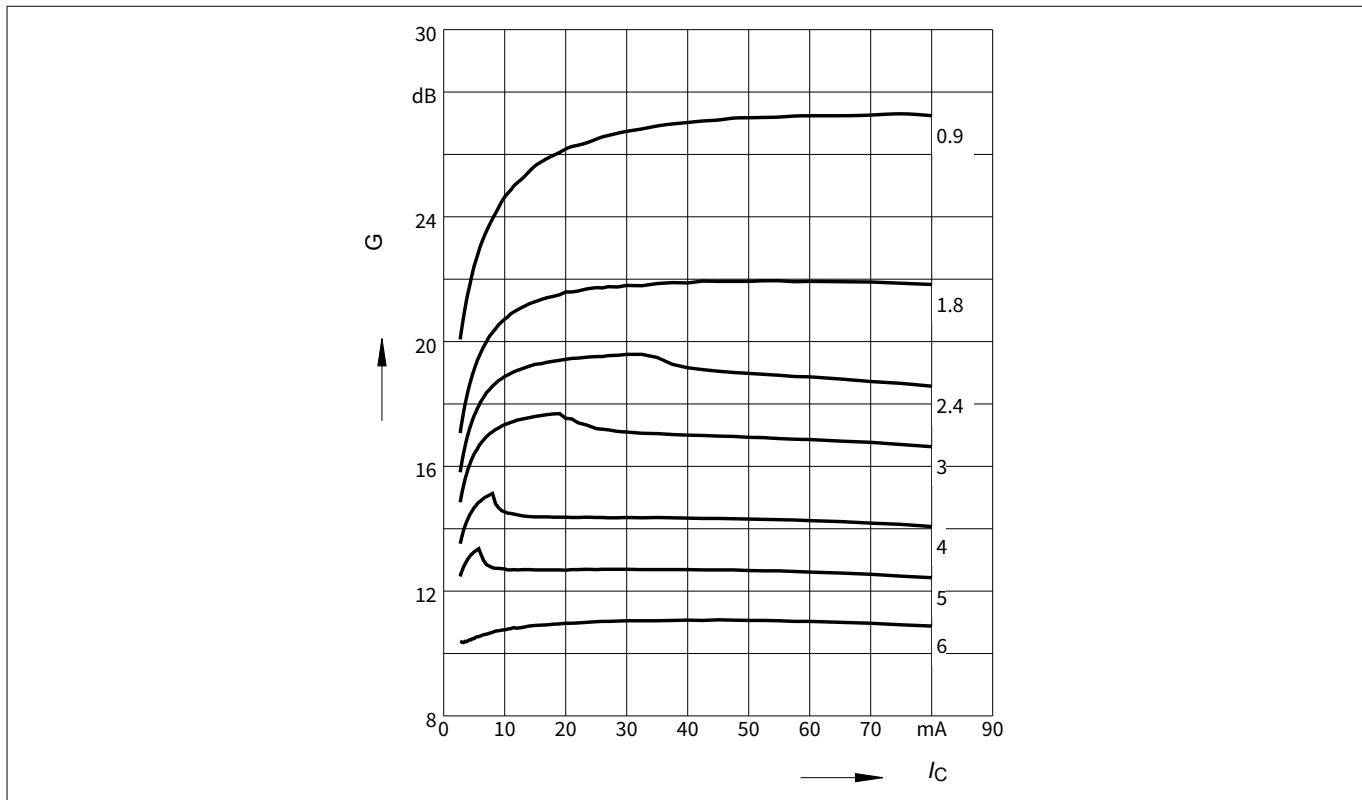


Figure 10 Maximum power gain $G_{max} = f(I_C)$, $V_{CE} = 1.5$ V, f = parameter in GHz

Electrical characteristics

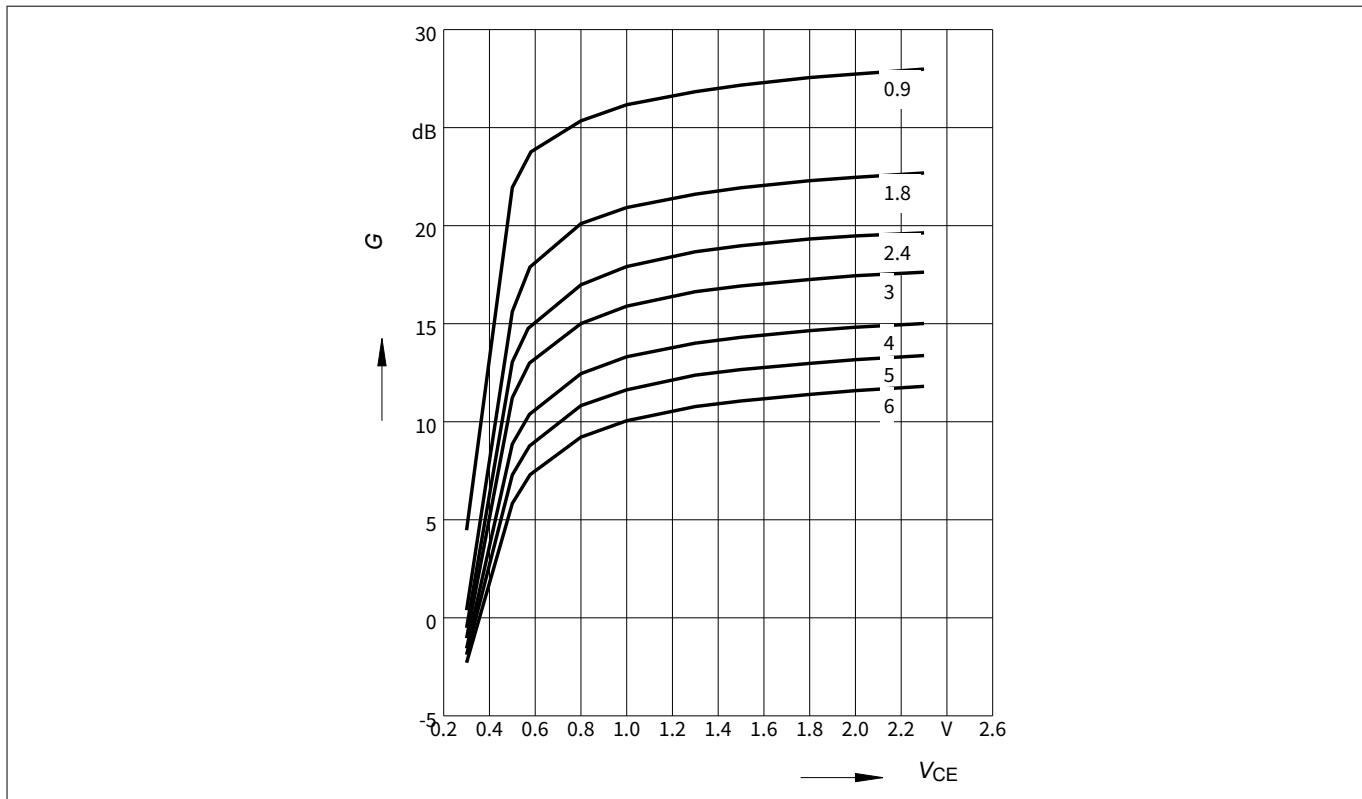


Figure 11 Maximum power gain $G_{\max} = f(V_{CE})$, $I_C = 50 \text{ mA}$, $f = \text{parameter in GHz}$

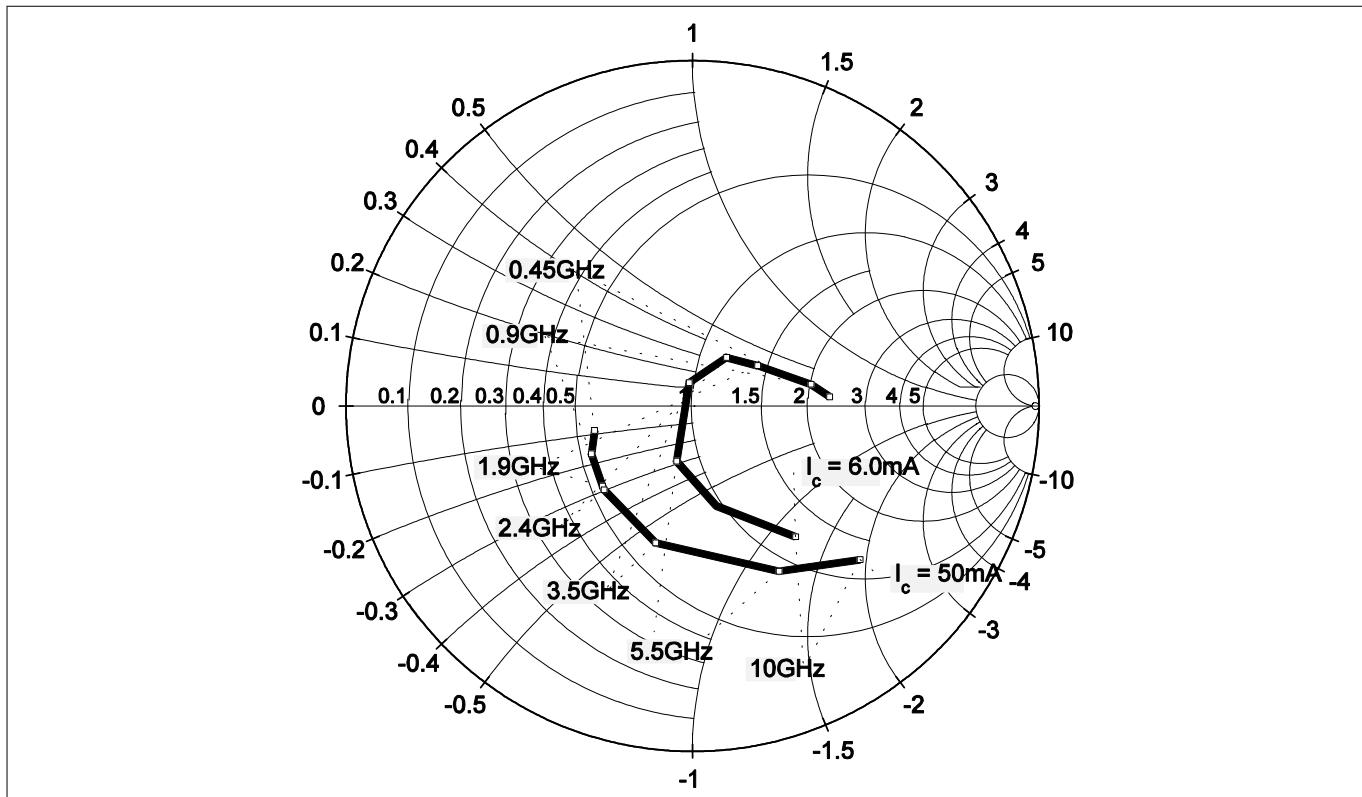


Figure 12 Source impedance for minimum noise figure $Z_{S,\text{opt}} = f(f)$, $V_{CE} = 3 \text{ V}$, $I_C = 6 / 50 \text{ mA}$

Electrical characteristics

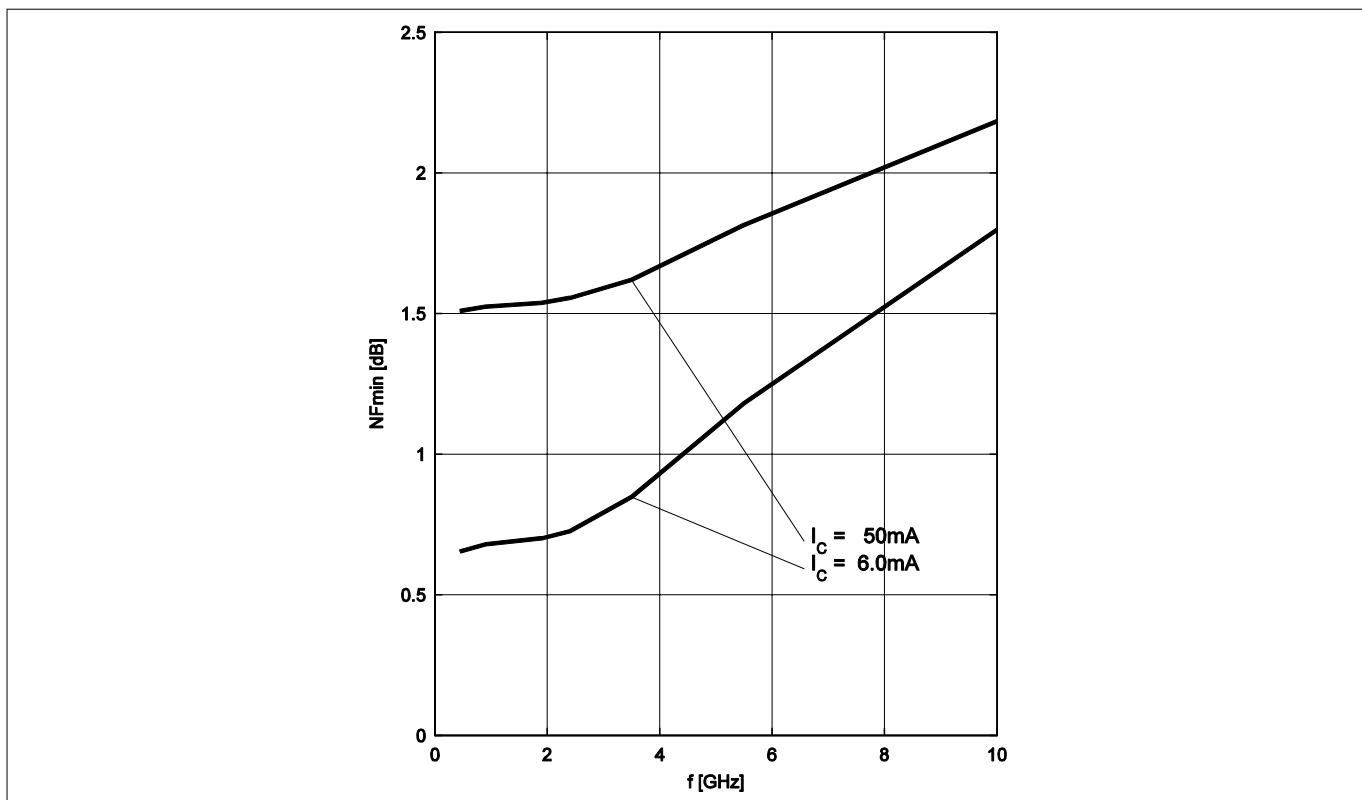


Figure 13

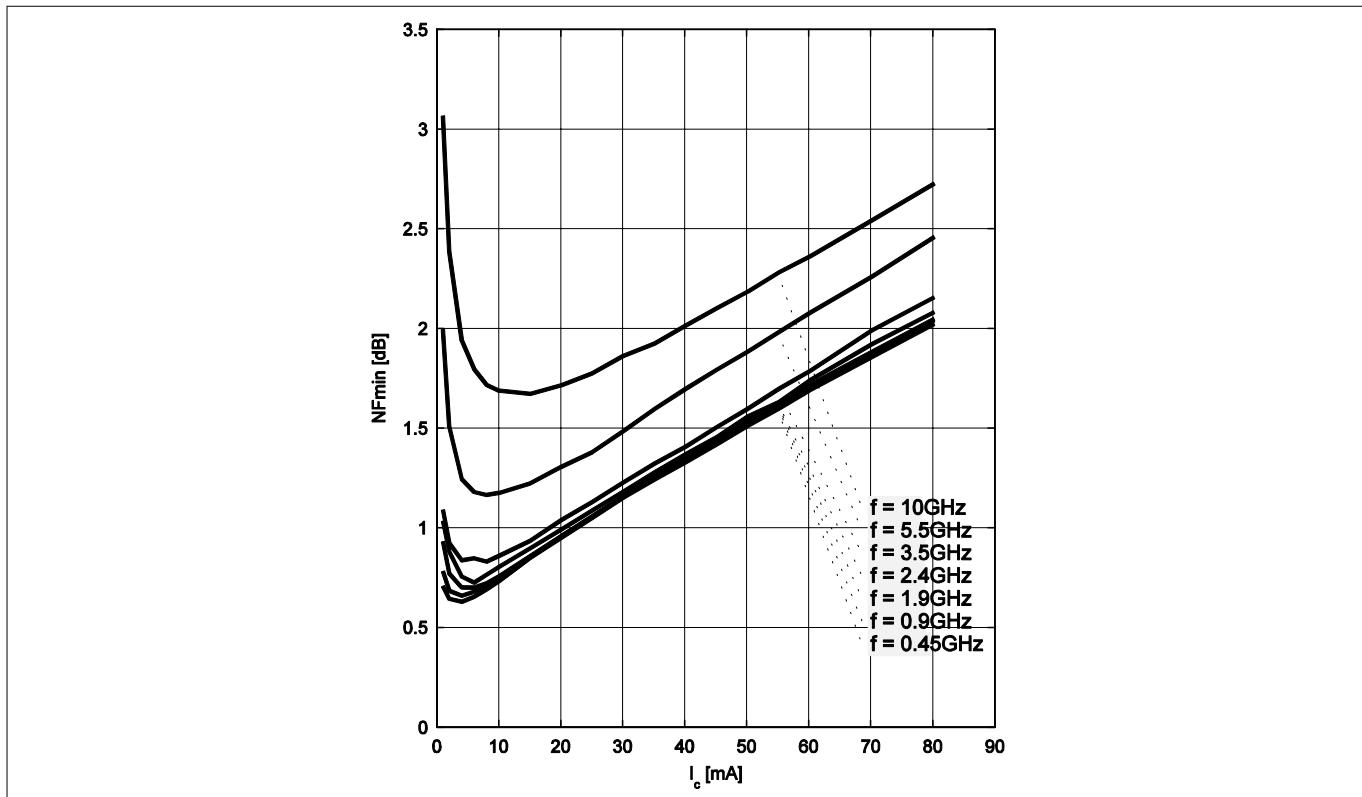
Noise figure $NF_{min} = f(f)$, $V_{CE} = 2\text{ V}$, $Z_S = Z_{S,opt}$, $I_C = 6 / 50\text{ mA}$ 

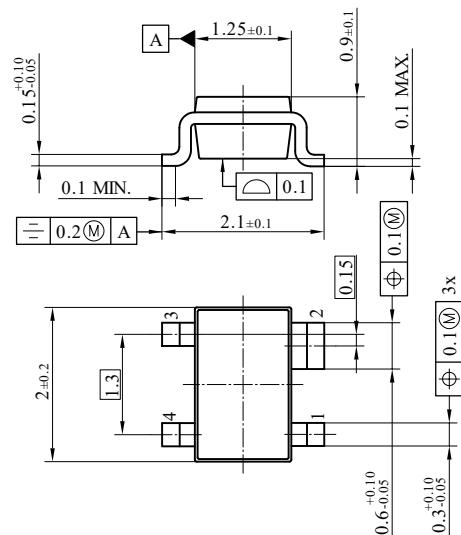
Figure 14

Noise figure $NF_{min} = f(I_c)$, $V_{CE} = 2\text{ V}$, $Z_S = Z_{S,opt}$, f = parameter in GHz

Note: The curves shown in this chapter have been generated using typical devices but shall not be considered as a guarantee that all devices have identical characteristic curves. $T_A = 25^\circ\text{C}$.

4

Package information SOT343



MOLD FLASH, PROTRUSION OR GATE BURRS OF 0.2 MM MAXIMUM PER SIDE ARE NOT INCLUDED
ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 []

Figure 15 **SOT343 package**

Note: For package information including footprint, packing and assembly recommendation refer to:

<https://www.infineon.com/cms/en/product/packages/PG-SOT343/PG-SOT343-4-1>

Revision history**Revision history**

Document version	Date of release	Description of changes
Revision 2.0	2019-01-25	New datasheet layout.
Revision 3.0	2024-07-01	Updated product validation

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